VHDL

ELEC 311

Digital Logic and Circuits

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Images Courtesy of Cengage Learning

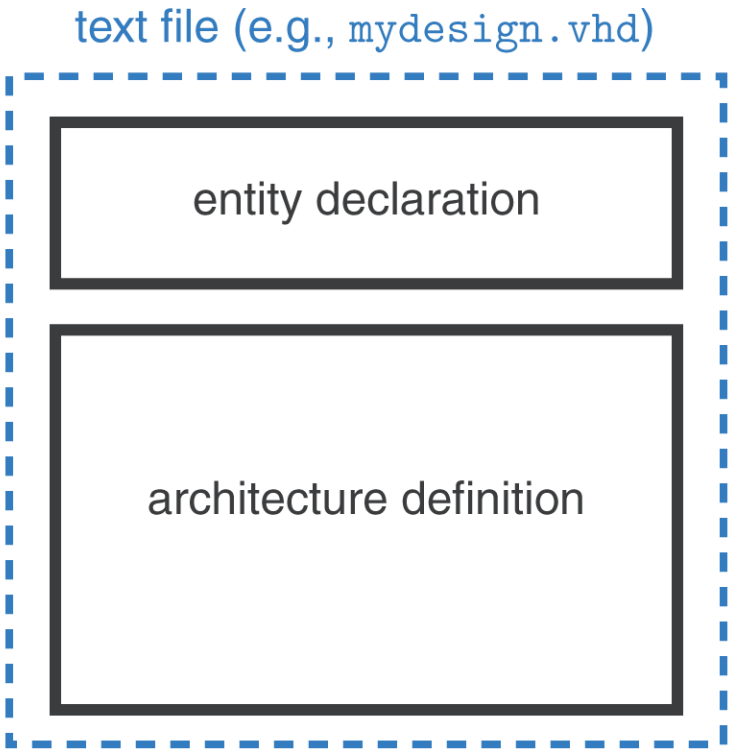
THE CITADEL
DEPARTMENT OF ELECTRICAL & COMPUTER ENGINEERING

VHDL Tools

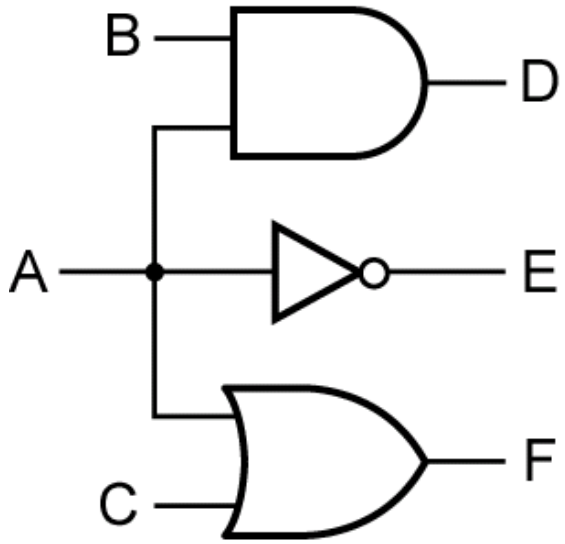
- Hardware Description Language Tools
  - Text Editor
    - Design Entry
  - Compiler
    - Syntax
  - Simulator
    - Test Bench
    - Functional Verification
  - Synthesis tool
    - Libraries
    - Target Technology

VHDL Model

- Entity
  - Component interface
    - Inputs
    - Outputs
- Architecture
  - Structural
  - Dataflow
  - Behavioral

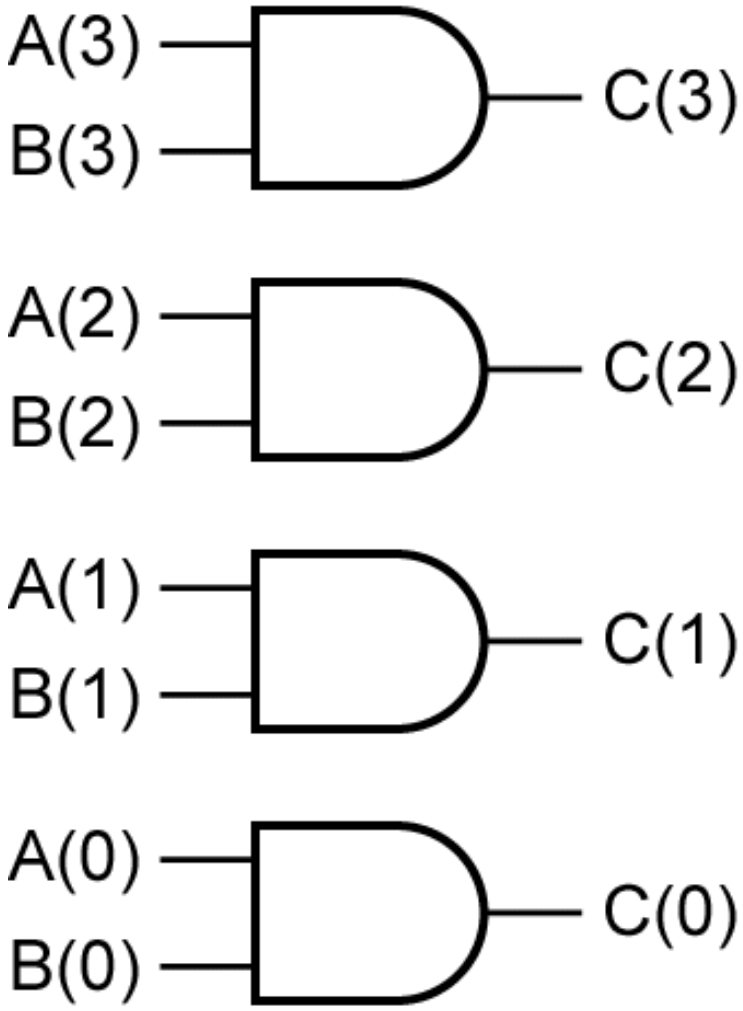


Propagation Delays



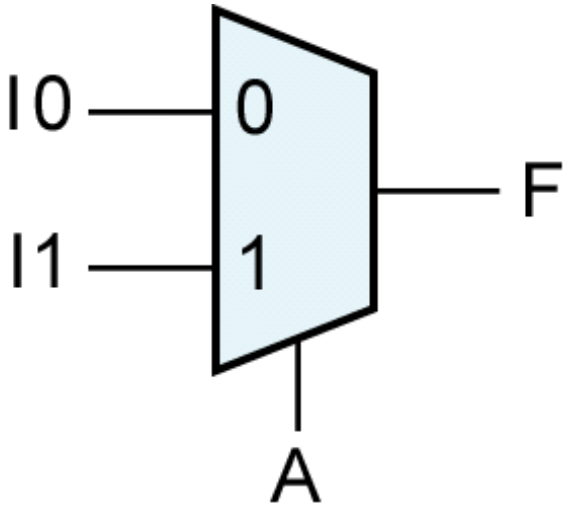

```
-- when A changes, these concurrent
-- statements all execute at the same time

D <= A and B after 2 ns;

E <= not A after 1 ns;

F <= A or C after 3 ns;
```

Bit_Vectors



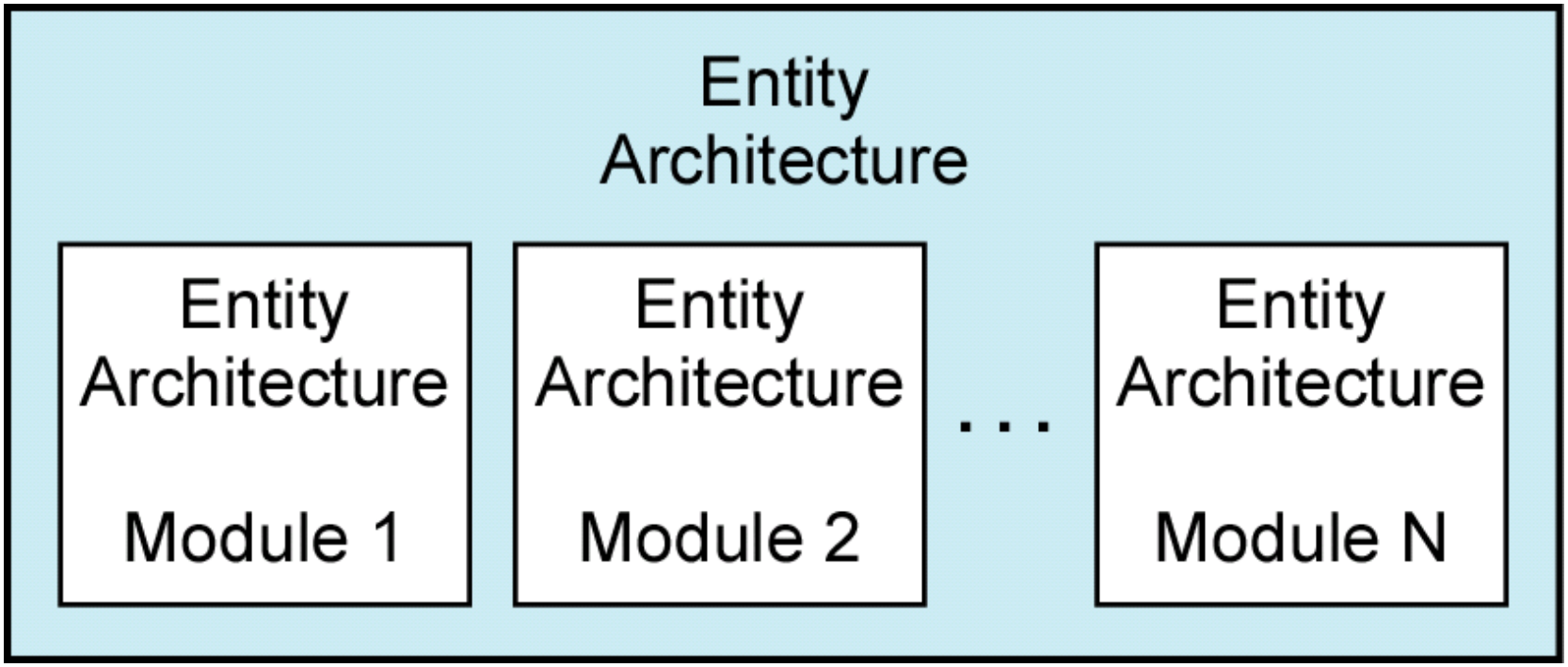

```
-- the hard way
C(3) <= A(3) and B(3);
C(2) <= A(2) and B(2);
C(1) <= A(1) and B(1);
C(0) <= A(0) and B(0);
```

Multiplexers

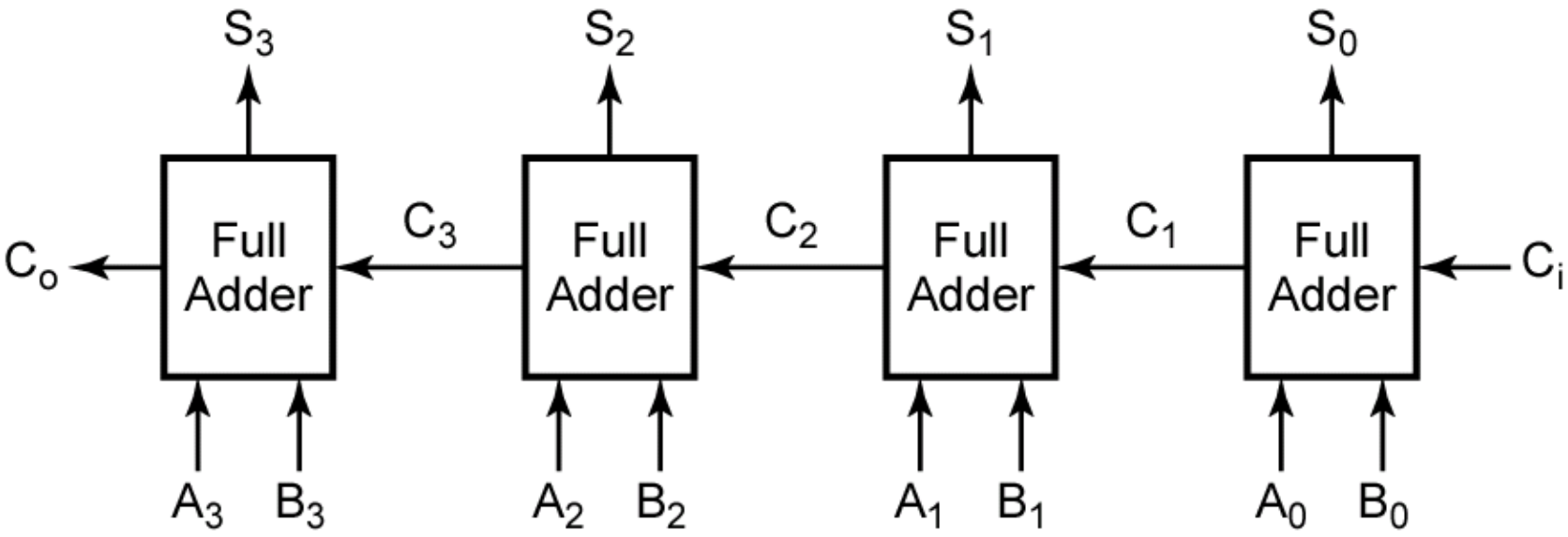



```
-- conditional signal assignment statement
F <= I0 when A = '0' else I1;
```

Design Hierarchy



4-bit Adder Example



VHDL Types

- Predefined Types

```
bit                 character         severity_level
bit_vector          integer           string
boolean             real              time
```

- IEEE Standard Logic

```
type STD_ULOGIC is ( 'U',   -- Uninitialized
                     'X',   -- Forcing  Unknown
                     '0',   -- Forcing  0
                     '1',   -- Forcing  1
                     'Z',   -- High Impedance
                     'W',   -- Weak     Unknown
                     'L',   -- Weak     0
                     'H',   -- Weak     1
                     '-'    -- Don't care
                   );
subtype STD_LOGIC is resolved STD_ULOGIC;
```

VHDL Operators

integer Operators		*boolean* Operators	
+	addition	and	AND
-	subtraction	or	OR
*	multiplication	nand	NAND
/	division	nor	NOR
mod	modulo division	xor	Exclusive OR
rem	modulo remainder	xnor	Exclusive NOR
abs	absolute value	not	complementation
**	exponentiation	&	concatenation

VHDL Libraries and Packages

- library IEEE;
- use IEEE.numeric_bit.all;

- library IEEE;
- use IEEE.std_logic_1164.all;
- use IEEE.numeric_std.all;

- use work.project3_gates.all;

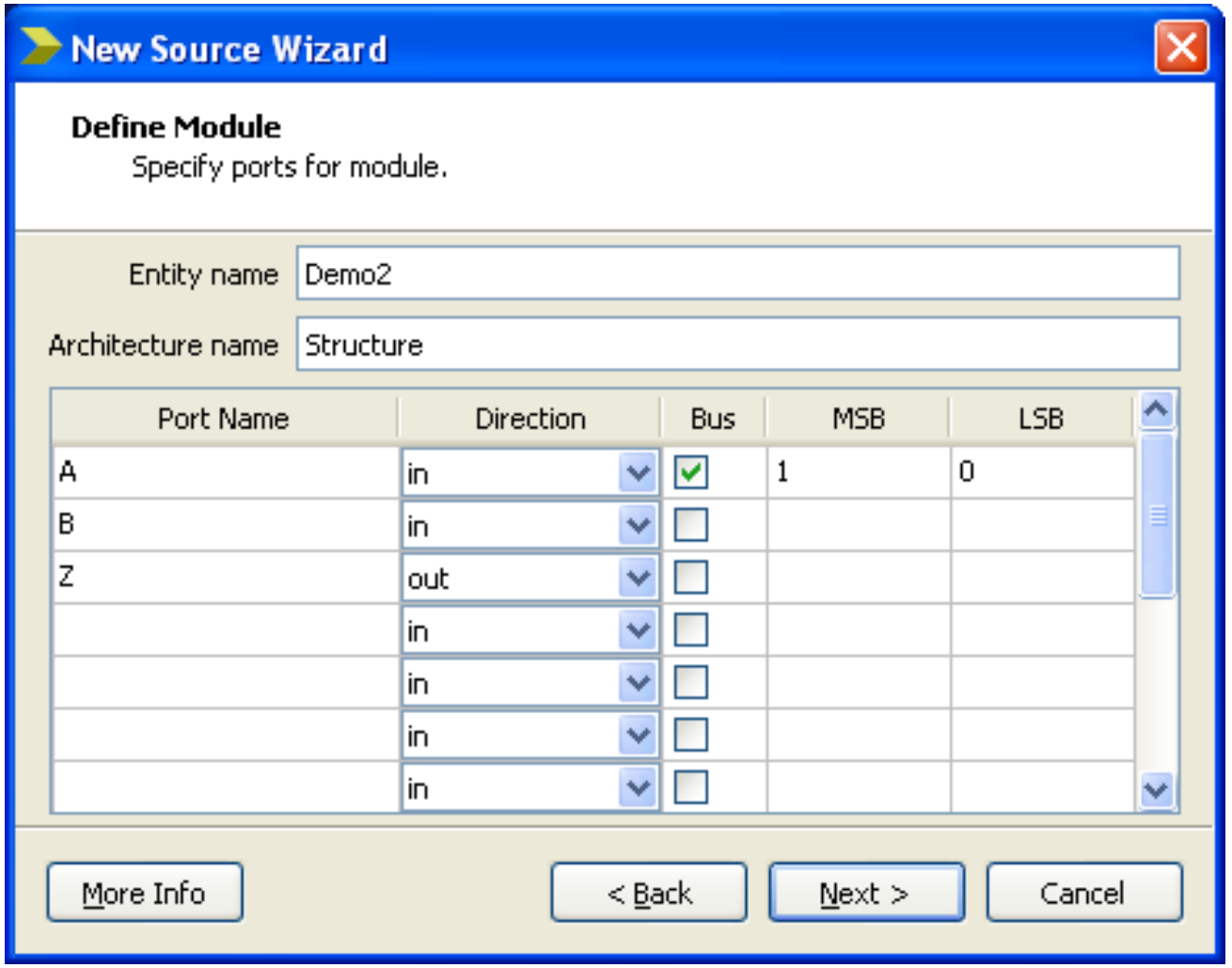
Project 3 VHDL

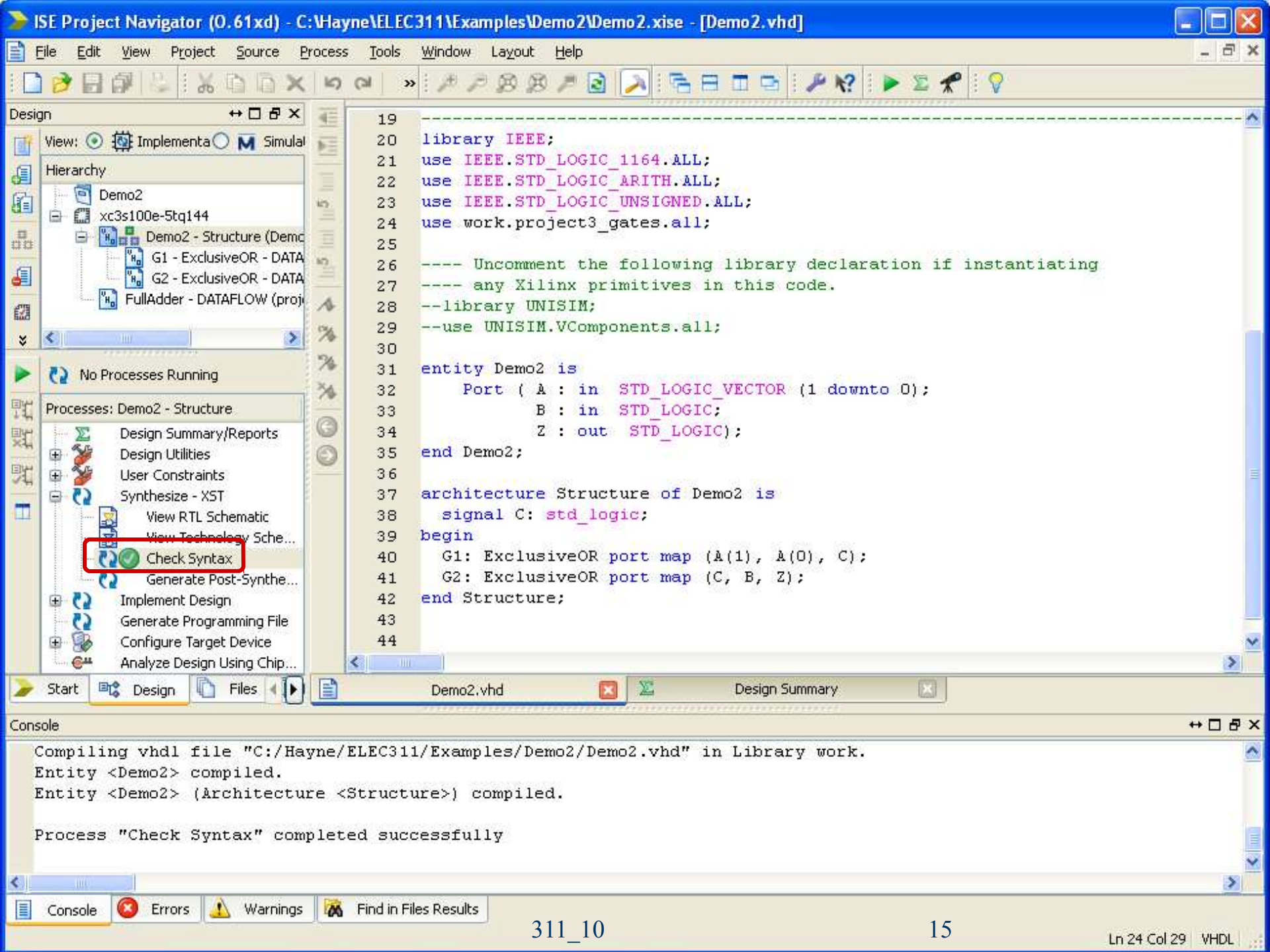
- Structural Description
  - Entity
  - Structural Architecture
- Package
  - Component declarations
  - Dataflow descriptions

Project 3 Xilinx

- New Project
  - Top-Level Source Type → HDL
- Project → New Source
  - VHDL Module
- Project → Add Copy of Source
  - project3_gates.vhd

New Source


New Source Wizard
Define Module
Specify ports for module.
Entity name
Demo2
Architecture name
Structure
Port Name
Direction
Bus
MSB
LSB
A
in
1
0
B
in
Z
out
in
in
in
in
More Info
< Back
Next >
Cancel


ISE Project Navigator (O.61xd) - C:\Hayne\ELEC311\Examples\Demo2\Demo2.xise - [Demo2.vhd]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementa Simulat
Hierarchy
Demo2
xc3s100e-5tq144
Demo2 - Structure (Demc
G1 - ExclusiveOR - DATA
G2 - ExclusiveOR - DATA
FullAdder - DATAFLOW (proj
No Processes Running
Processes: Demo2 - Structure
Design Summary/Reports
Design Utilities
User Constraints
Synthesize - XST
View RTL Schematic
View Technology Sche...
Check Syntax
Generate Post-Synthe...
Implement Design
Generate Programming File
Configure Target Device
Analyze Design Using Chip...
19 ----------
20 library IEEE;
21 use IEEE.STD_LOGIC_1164.ALL;
22 use IEEE.STD_LOGIC_ARITH.ALL;
23 use IEEE.STD_LOGIC_UNSIGNED.ALL;
24 use work.project3_gates.all;
25
26 ---- Uncomment the following library declaration if instantiating
27 ---- any Xilinx primitives in this code.
28 --library UNISIM;
29 --use UNISIM.VComponents.all;
30
31 entity Demo2 is
32 Port (A : in STD_LOGIC_VECTOR (1 downto 0);
33 B : in STD_LOGIC;
34 Z : out STD_LOGIC);
35 end Demo2;
36
37 architecture Structure of Demo2 is
38 signal C: std_logic;
39 begin
40 G1: ExclusiveOR port map (A(1), A(0), C);
41 G2: ExclusiveOR port map (C, B, Z);
42 end Structure;
43
44
Start Design Files
Demo2.vhd
Design Summary
Console
Compiling vhdl file "C:/Hayne/ELEC311/Examples/Demo2/Demo2.vhd" in Library work.
Entity <Demo2> compiled.
Entity <Demo2> (Architecture <Structure>) compiled.
Process "Check Syntax" completed successfully
Console Errors Warnings Find in Files Results
Ln 24 Col 29 VHDL

Summary

- Entity
- Architecture
  - Structural
  - Dataflow
  - Behavioral
- Types
- Operators
- Libraries and Packages