ELEC 311 Final Exam Review

TOPICS

Number Systems
- Base conversion (2, 10, 16)
- Negative numbers: sign and magnitude, 2's complement
- Arithmetic: addition (subtraction), overflow, multiplication

Codes
- BCD, Gray, ASCII

Boolean Algebra
- Logic gates: AND, OR, NOT, XOR
- Circuit analysis: logic equations, truth tables
- Laws and theorems: identity, complements, simplification (adjacency)
- Sum-of-products (SOP), product-of-sums (POS)

Combinational Design
- Word problem -> truth table
- Minterms and Maxterms
- Incompletely specified functions (don't cares)
- Propagation delay, timing diagrams, and hazards

Minimizing Switching Functions
- Adjacency theorem, essential prime implicants
- Karnaugh maps
- Quine McCluskey

NAND and NOR Gates
- DeMorgan's Laws
- SOP -> NAND-NAND, POS -> NOR-NOR
- CMOS logic gates
- Noise Margin

Combinational Logic Circuits
- Multiplexer
- Tri-State Buffer
- Decoder, (Priority) Encoder
- Read Only Memory (ROM)
- Programmable Logic Devices (CPLD, FPGA)

VHDL
- Entity, Architecture
- Types, Operators
- Libraries and Packages
- Structural Model
  - Component, Port Map
- Dataflow Model
  - Concurrent Signal Assignment Statements
- Behavioral Model
  - Process, Sequential Statements

Latches and Flip-Flops
- Set-Reset Latch, D Latch
- D Flip-Flop, J-K Flip-Flop, T Flip-Flop
- Timing Diagrams

Registers and Counters
- Register, Shift Register
- Tri-State Bus
- Counters
- Sequential Design

Sequential Analysis
- State Tables
- State Graphs
- Timing Diagrams
- Next State (FF) Equations
- Transition Tables

Sequential Design
- State Graphs
- State Tables
- Transition Tables
- Next State (FF) Equations

Sequential Arithmetic
- Serial Addition
- Parallel Multiplication

Practice Questions

1. Perform the following subtraction using 12-bit 2's complement arithmetic and verify your answer in base 10:

$$1D.4_{16} - 2B.6_{16} = \_\_\_\_\_{}_{16}$$

2. Determine the ROM size and contents to implement the function which converts a two's complement number from -4 to +3 to sign and magnitude format.

3. Minimize the following function using Quine-McCluskey:

$$F(A,B,C) = \Sigma m(1,3,4,7) + \Sigma d(2,5)$$

4. Given the following VHDL model, draw the schematic diagram (label completely).

```
entity SR is
  port (SR_IN, CK : in std_logic;
        SR_OUT    : out std_logic);
end SR;
architecture STRUCTURE of SR is
  signal X : std_logic_vector(1 to 2);
  component DFF
    port (D, C : in  std_logic;
          Q    : out std_logic);
  end component;
begin
  FF1 : DFF port map (SR_IN, CK, X(1));
  FF2 : DFF port map (X(1),  CK, X(2));
  FF3 : DFF port map (X(2),  CK, SR_OUT);
end STRUCTURE;
```

5. Given the truth table below for a 2-bit shift register:
   a. Draw the circuit diagram using D flip-flops and 2-to-1 multiplexers.
   b. Determine the next-state equations for the flip-flops.
   c. Fill in an transition table.

	Input	Next State	
Function	S	$Q1^+$	$Q2^+$
Hold	0	Q1	Q2
Swap	1	Q2	Q1