Programmable Logic Devices

ELEC 418 Advanced Digital Systems Dr. Ron Hayne

Images Courtesy of Thomson Engineering



Programmable Logic Devices

	SPLD	CPLD	FPGA
Density	Low Few hundred gates	Low to Medium 500 to 12,000 gates	Medium to High 3,000 to 5,000,000 gates
Timing	Predictable	Predictable	Unpredictable
Cost	Low	Low to Medium	Medium to High
Major Vendors	Lattice Semiconductor Cypress AMD	Xilinx Altera	Xilinx Altera Lattice Semiconductor Actel
Example Device Families	Lattice Semiconductor GAL16LV8 GAL22V10 Cypress	Xilinx CoolRunner XC9500 Altera	Xilinx Virtex Spartan Altera
	PALCE16V8	MAX	Stratix
	AMD 22V10		Lattice Mach ECP
			Actel Accelerator

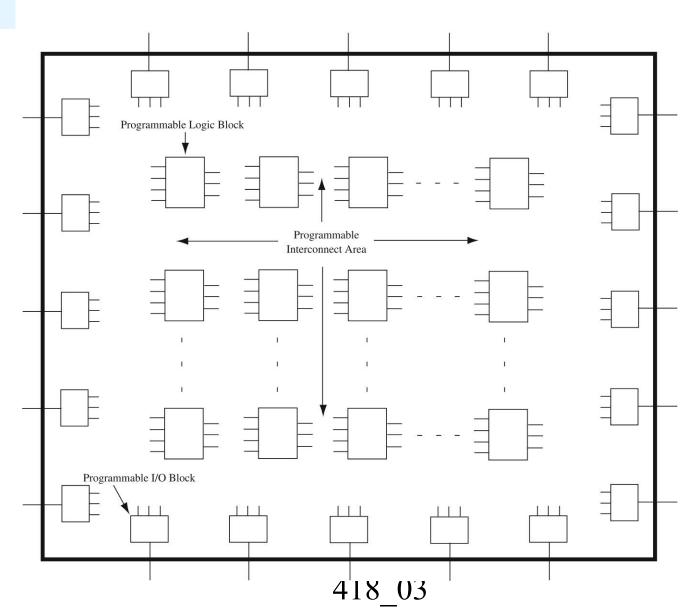
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FPGAs

Field Programmable Gate Arrays

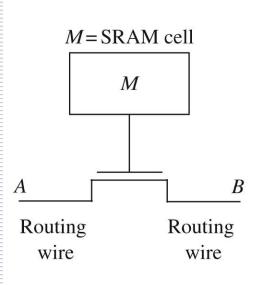
Vendor	FPGA Product	Capacity (Approx) in Gates/LUTs
Xilinx	Spartan-II	15K to 200K
	Spartan-IIE	50K to 600K
	Spartan-3	50K to 5M
	Virtex-5	19,200 to 207,360 LUTs
	Virtex	57,906 to 1,124,022
	Virtex-E	71,693 to 4,074,387
	Virtex-II	40K to 8M
Altera	ACEX 1K	56K to 257K
	APEX II	1.9M to 5.25M
	FLEX 10K	10K to 50K
	Stratix/Stratix II	10,570 to 132,540 logic elements

Organization of FPGAs

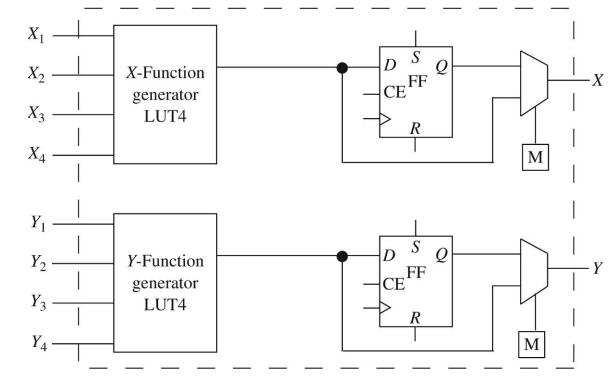


FPGA Programming

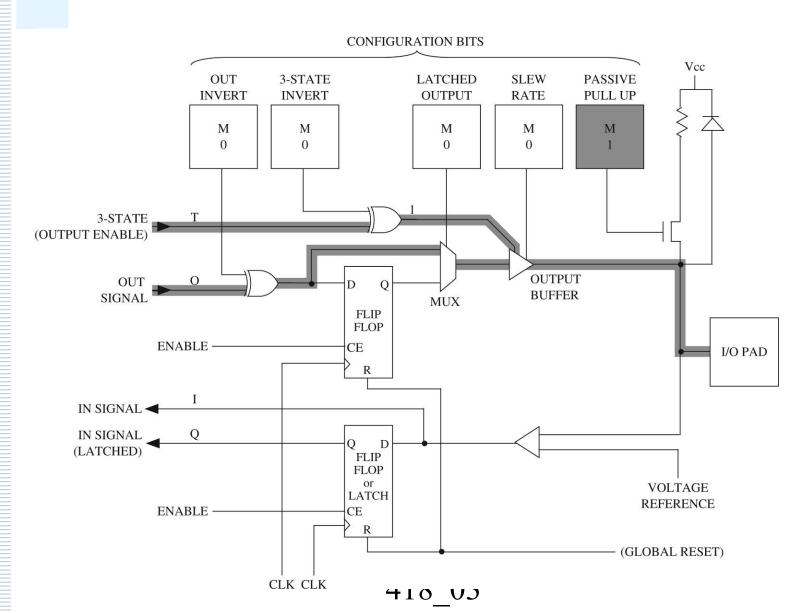
ProgrammableInterconnect



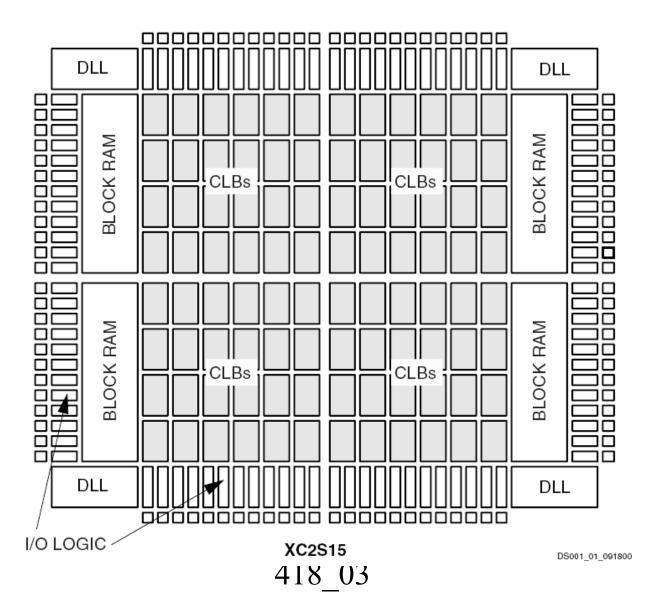
Programmable Logic Block



Programmable I/O Block



Spartan-II FPGA



Specialized Components

- Dedicated Memory
 - Block RAM
- Dedicated Arithmetic Units
 - Fast-Carry Logic
 - Dedicated Multipliers
- Embedded Processors
- Digital Signal Processing Blocks

FPGA Applications

- Rapid Prototyping
- Medium-Speed Final Product
- Reconfigurable Systems
- Glue Logic
- Hardware Accelerators

FPGA Design Flow

- VHDL Model
- VHDL Simulation
- Synthesis
- Mapping
- Place and Route
- Programming File
- Configure and Test

Summary

- FPGAs
 - Programmable Interconnect
 - Programmable Logic Block
 - Programmable I/O Block
 - Specialized Components
 - Applications
 - Design Flow