ELEC 418 Final Exam Review

Practice Questions:

1. Perform the following addition using the IEEE floating-point format. Normalize the result and verify your answer in base 10.

		S (1 bit)	E (8 bits)	F (23 bits)	Hex
N1	14.5_{10}				
N2	5.25_{10}				
N1 + N2					

2. Draw the datapath generated by the following VHDL. Completely label all signals.

```
  component Adder
    port(A, B: in unsigned(3 downto 0);
         S: out unsigned(3 downto 0));
  end component;
  signal Data_In, Data_Out, Data_Bus, Add_Out: unsigned(3 downto 0);
  signal CK, BUSorADD: std_logic;
begin
  A1: Adder port map(Data_Bus, Data_Out, Add_Out);
  Data_In <= Data_Bus when BUSorADD = '0' else Add_Out;
  process(CK)
  begin
    if CK'event and CK = '1' then
      Data_Out <= Data_In;
    end if;
  end process;
end;
```

3. Design a Moore state diagram for a traffic light controller for the intersection of streets A and B. Each street has a sensor to detect the presence of vehicles (Sa = 1 means a vehicle is approaching or stopped on street A). Each street will have a green light for a minimum of 30 seconds and only turn red if there is a vehicle on the other street. The state machine is controlled by a clock with a 10 second period and the outputs are Ga Ya Ra Gb Yb Rb.

4. Design an N-bit serial-in, serial-out shift register with inputs SI (serial input), EN (enable), CK (clock), and a single output SO (serial output). Assume that the following component for a D flip-flop with enable is available in the package Review_Components.

```
  component DFF
    port(D, CK, EN: in bit;
         Q: out bit);
  end component;
```

5. Given the Instructional Processor from lesson 9:

a. Determine the RTN sequence to execute the following instructions. Write the VHDL to implement the RTN.

```
AND  #Value,Rd
ROTL Rs,Addr
```

b. Encode the following assembly language instructions in binary machine code.

```
ADD  #-5,R2
INV  R1,0x6B
```