Programmable Logic Devices

ELEC 418

Advanced Digital Systems

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Images Courtesy of Thomson Engineering

THE CITADEL

DEPARTMENT OF ELECTRICAL & COMPUTER ENGINEERING

Programmable Logic Devices

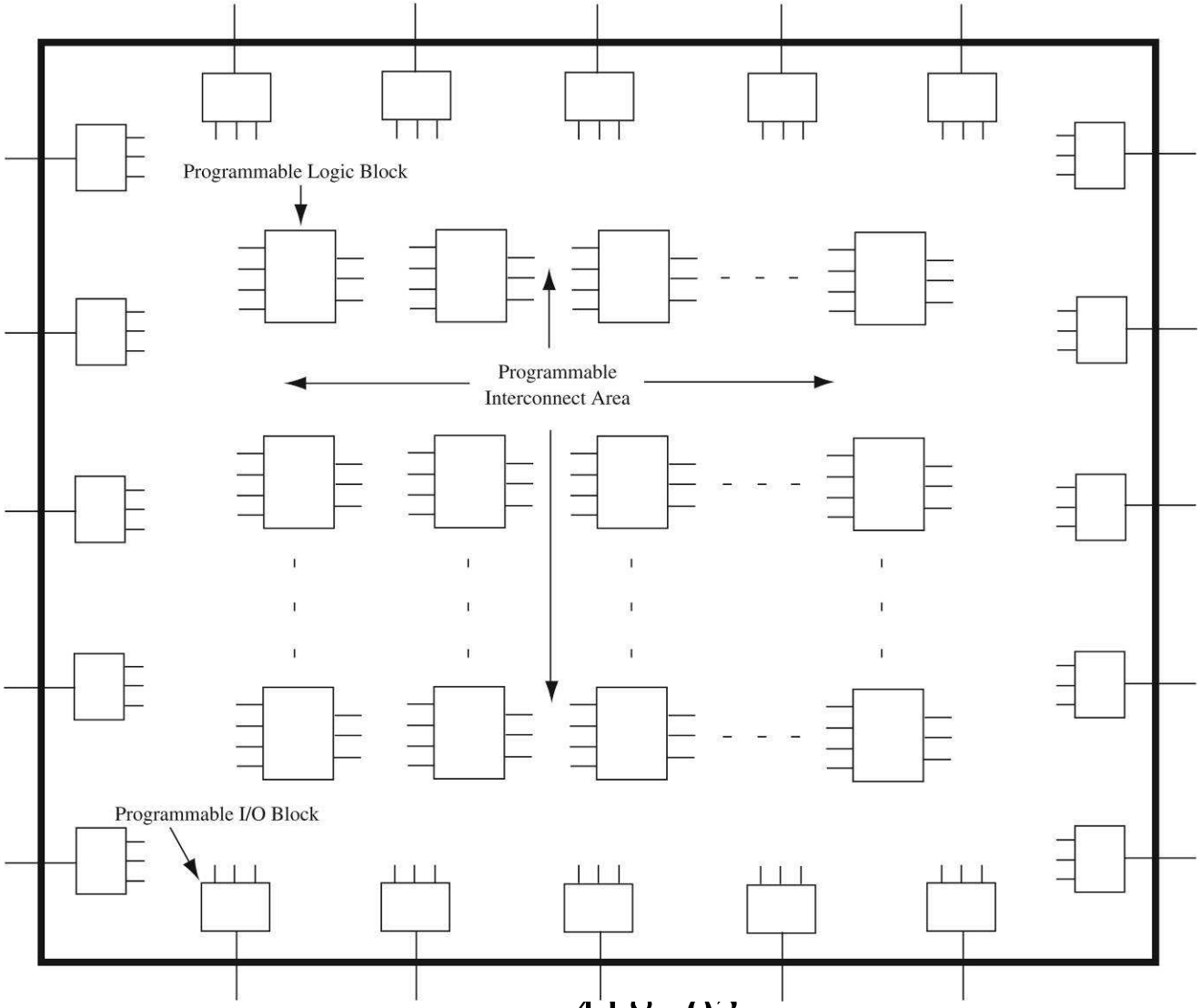
	SPLD	CPLD	FPGA
Density	Low Few hundred gates	Low to Medium 500 to 12,000 gates	Medium to High 3,000 to 5,000,000 gates
Timing	Predictable	Predictable	Unpredictable
Cost	Low	Low to Medium	Medium to High
Major Vendors	Lattice Semiconductor Cypress AMD	Xilinx Altera	Xilinx Altera Lattice Semiconductor Actel
Example Device Families	**Lattice Semiconductor** GAL16LV8 GAL22V10 **Cypress** PALCE16V8 **AMD** 22V10	**Xilinx** CoolRunner XC9500 **Altera** MAX	**Xilinx** Virtex Spartan **Altera** Stratix **Lattice** Mach ECP **Actel** Accelerator

FPGAs

- Field Programmable Gate Arrays

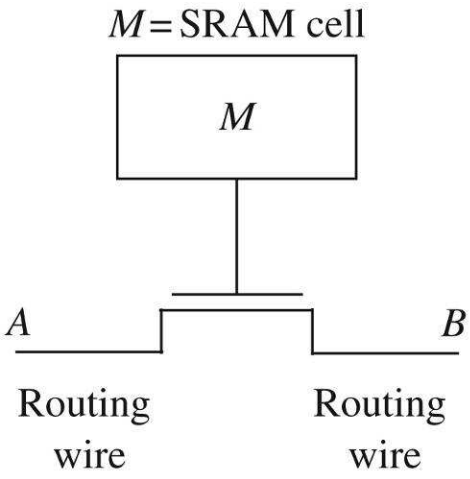
Vendor	FPGA Product	Capacity (Approx) in Gates/LUTs
Xilinx	Spartan-II Spartan-IIE Spartan-3 Virtex-5 Virtex Virtex-E Virtex-II	15K to 200K 50K to 600K 50K to 5M 19,200 to 207,360 LUTs 57,906 to 1,124,022 71,693 to 4,074,387 40K to 8M
Altera	ACEX 1K APEX II FLEX 10K Stratix/Stratix II	56K to 257K 1.9M to 5.25M 10K to 50K 10,570 to 132,540 logic elements

Organization of FPGAs

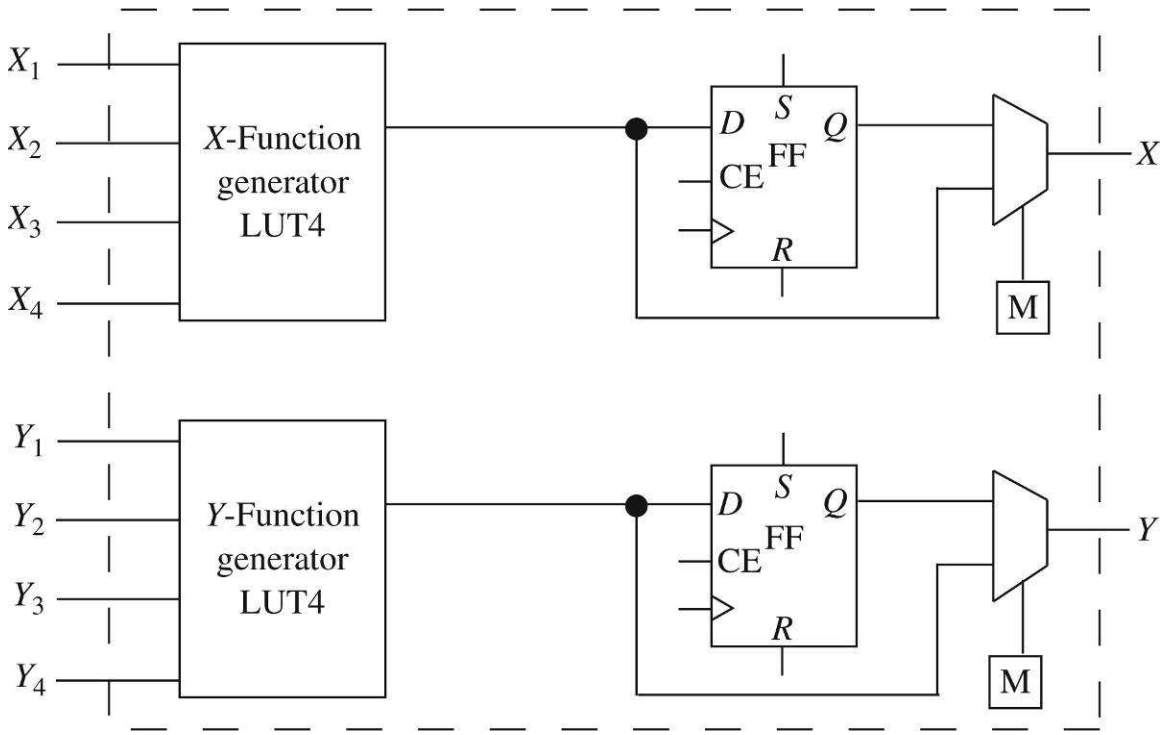


FPGA Programming

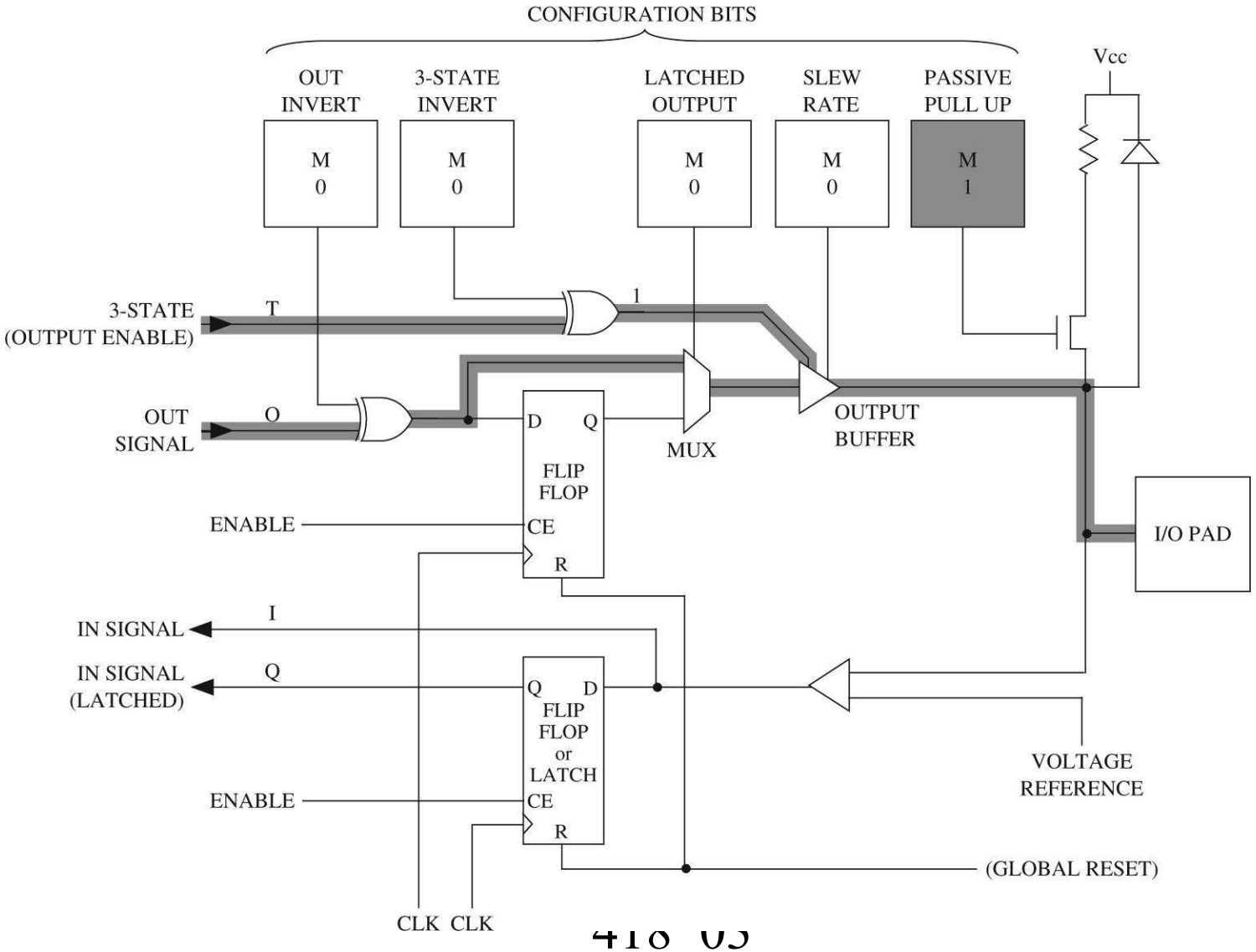
- Programmable Interconnect



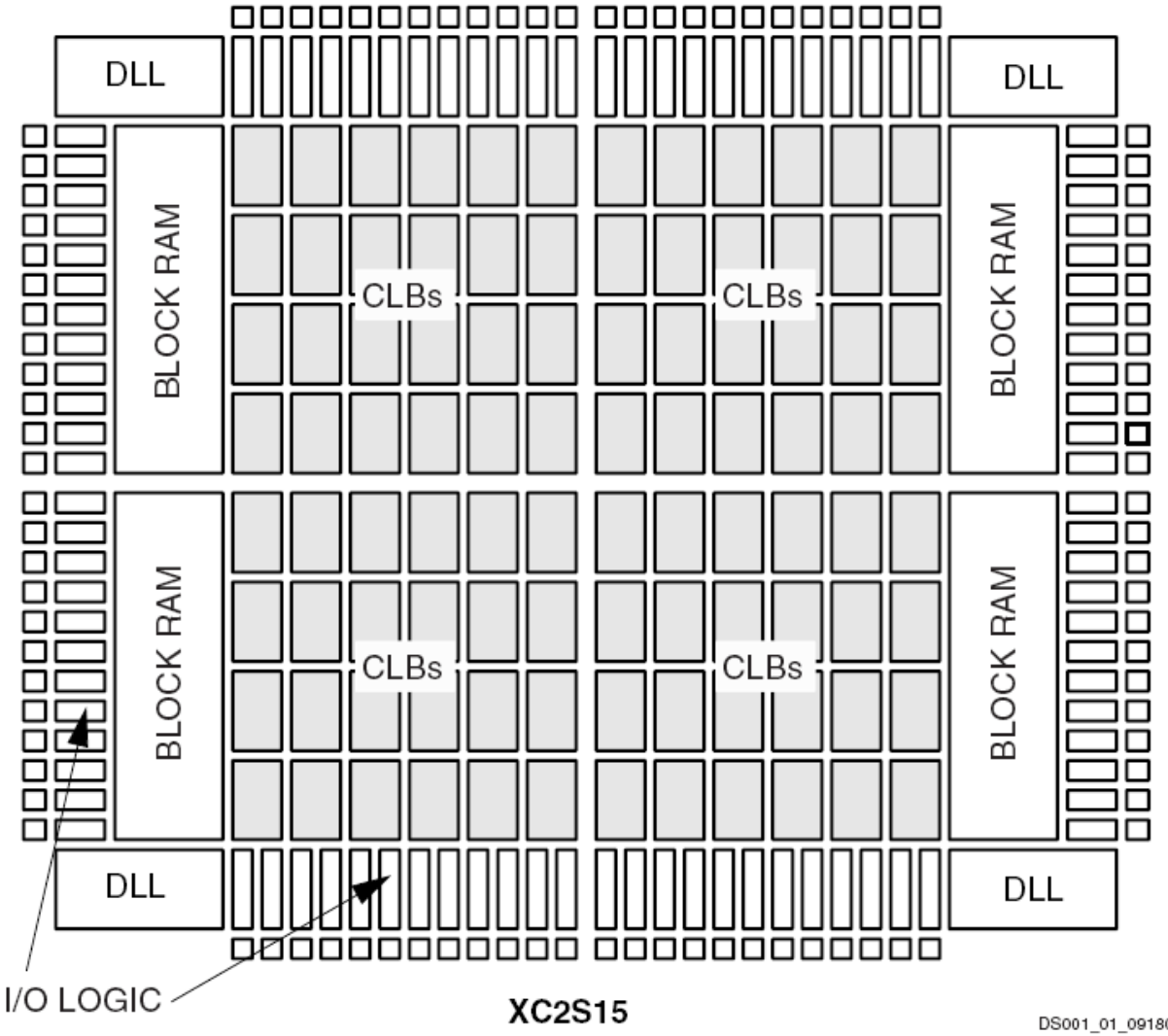
- Programmable Logic Block



Programmable I/O Block



Spartan-II FPGA



Specialized Components

- Dedicated Memory
  - Block RAM
- Dedicated Arithmetic Units
  - Fast-Carry Logic
  - Dedicated Multipliers
- Embedded Processors
- Digital Signal Processing Blocks

FPGA Applications

- Rapid Prototyping
- Medium-Speed Final Product
- Reconfigurable Systems
- Glue Logic
- Hardware Accelerators

FPGA Design Flow

- VHDL Model
- VHDL Simulation
- Synthesis
- Mapping
- Place and Route
- Programming File
- Configure and Test

Summary

- FPGAs
  - Programmable Interconnect
  - Programmable Logic Block
  - Programmable I/O Block
  - Specialized Components
  - Applications
  - Design Flow