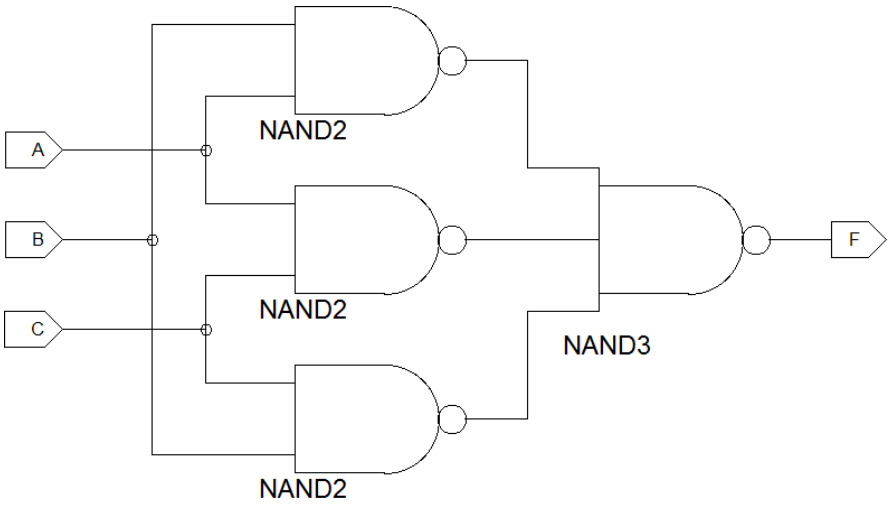
1. Given the following logic circuit:



a. Write a VHDL entity for the circuit.
b. Write a Boolean algebra expression for F and a VHDL dataflow architecture.
c. Write separate VHDL entities and dataflow architectures for the NAND2 and NAND3 components.
d. Write a VHDL structural architecture for the circuit using the components from Part c.