1. Design a falling-edge triggered J-K flip-flop with an active-high asynchronous clear.

a) Draw the logic symbol and a truth table.
b) Write a complete VHDL model (entity and behavioral architecture).

2. Draw the circuit generated by the following VHDL model. Completely label all components and signals.

```
entity SR2 is
  port(S, CLK: in bit;
       D : in bit_vector(1 downto 0);
       Q: out bit_vector(1 downto 0));
end SR2;

architecture DATAFLOW of SR2 is
  signal M, R: bit_vector(1 downto 0);
begin
  M <= D when S = '1' else (R(0)&R(1));
  process(CLK)
  begin
    if rising_edge(CLK) then
      R <= M;
    end if;
  end process;
  Q <= R;
end DATAFLOW;
```