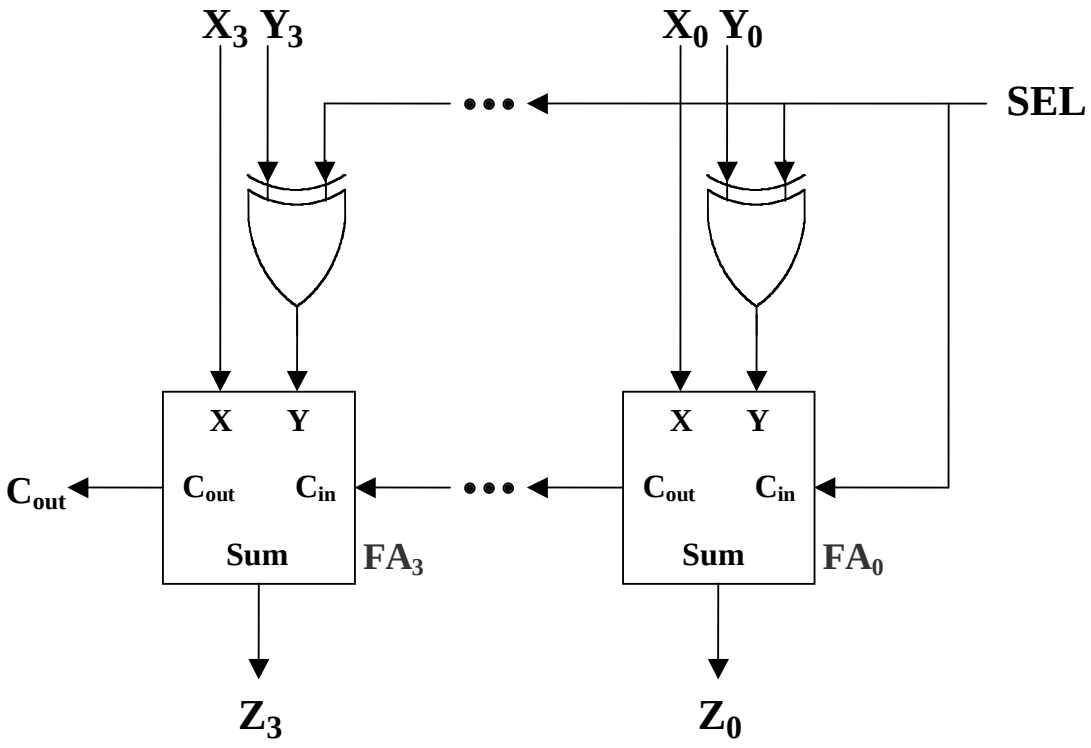
Project 3: Adder-Subtractor

Objectives

Design and test a combinational logic circuit which adds or subtracts two 4-bit 2's complement numbers. Describe the logic circuit using VHDL.

Specific Instructions



The circuit diagram above implements a 4-bit adder-subtractor:

$$\text{SEL} = 0 \Rightarrow Z = X \text{ plus } Y$$
$$\text{SEL} = 1 \Rightarrow Z = X \text{ plus } Y' \text{ plus } 1 = X \text{ minus } Y$$

1. Write a VHDL model to implement the design, including the following:
   a. Entity declaration.
   b. Structural architecture.
2. Use the given VHDL package (project3_gates.vhd) containing component declarations and dataflow descriptions of an *ExclusiveOR* gate and a *FullAdder*.
3. Implement the circuit in hardware, using the Xilinx design tools and the Spartan3E FPGA on the BASYS Board.

a. Constrain the design with the following pin assignments.

Name	Loc	BASYS	BASYS 2
X(3)	SW7	P6	N3
X(2)	SW6	P10	E2
X(1)	SW5	P12	F3
X(0)	SW4	P18	G3
Y(3)	SW3	P24	B4
Y(2)	SW2	P29	K3
Y(1)	SW1	P36	L3
Y(0)	SW0	P38	P11
SEL	BTN3	P41	A7

Name	Loc	BASYS	BASYS 2
COUT	LD4	P5	N5
Z(3)	LD3	P7	P6
Z(2)	LD2	P8	P7
Z(1)	LD1	P14	M11
Z(0)	LD0	P15	M5

b. Generate a programming file (.bit) for the FPGA.
c. Download the design onto the BASYS Board.

4. Test the circuit on the BASYS Board using the following test vectors:

X	Y	X	Y	X + Y	X - Y
3	1				
1	5				
-2	3				
-2	-4				
4	6				

5. Demonstrate the correct operation of your circuit to your professor and obtain his initials on your cover sheet.
6. Write a project report containing the following:
   a. Cover sheet with project name/number, date, and authors names.
   b. Objective section describing what was to be accomplished.
   c. Discussion section with your circuit diagram and VHDL description.
   d. Results and Conclusions.