Registers and Counters

ELEC 311

Digital Logic and Circuits

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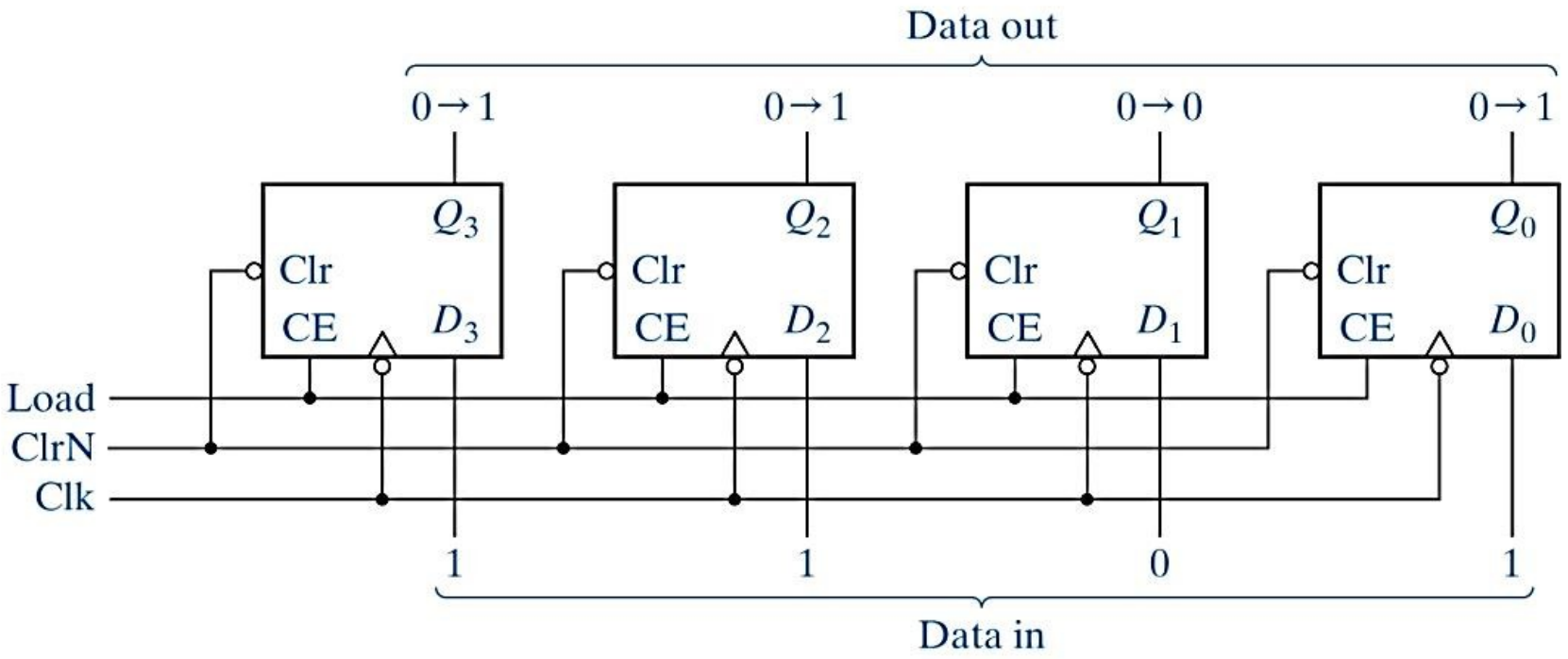
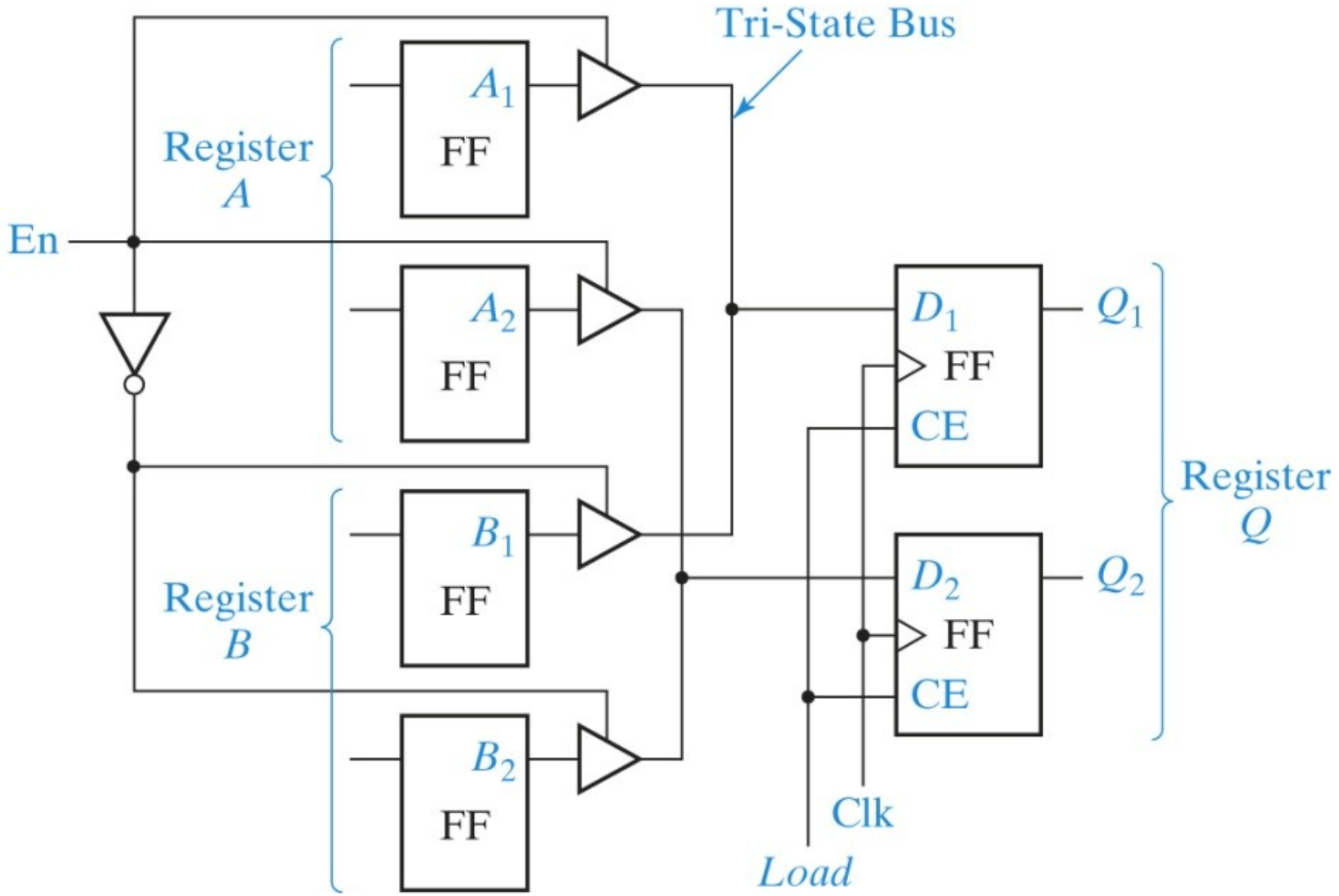
Images Courtesy of Cengage Learning

THE CITADEL
DEPARTMENT OF ELECTRICAL & COMPUTER ENGINEERING

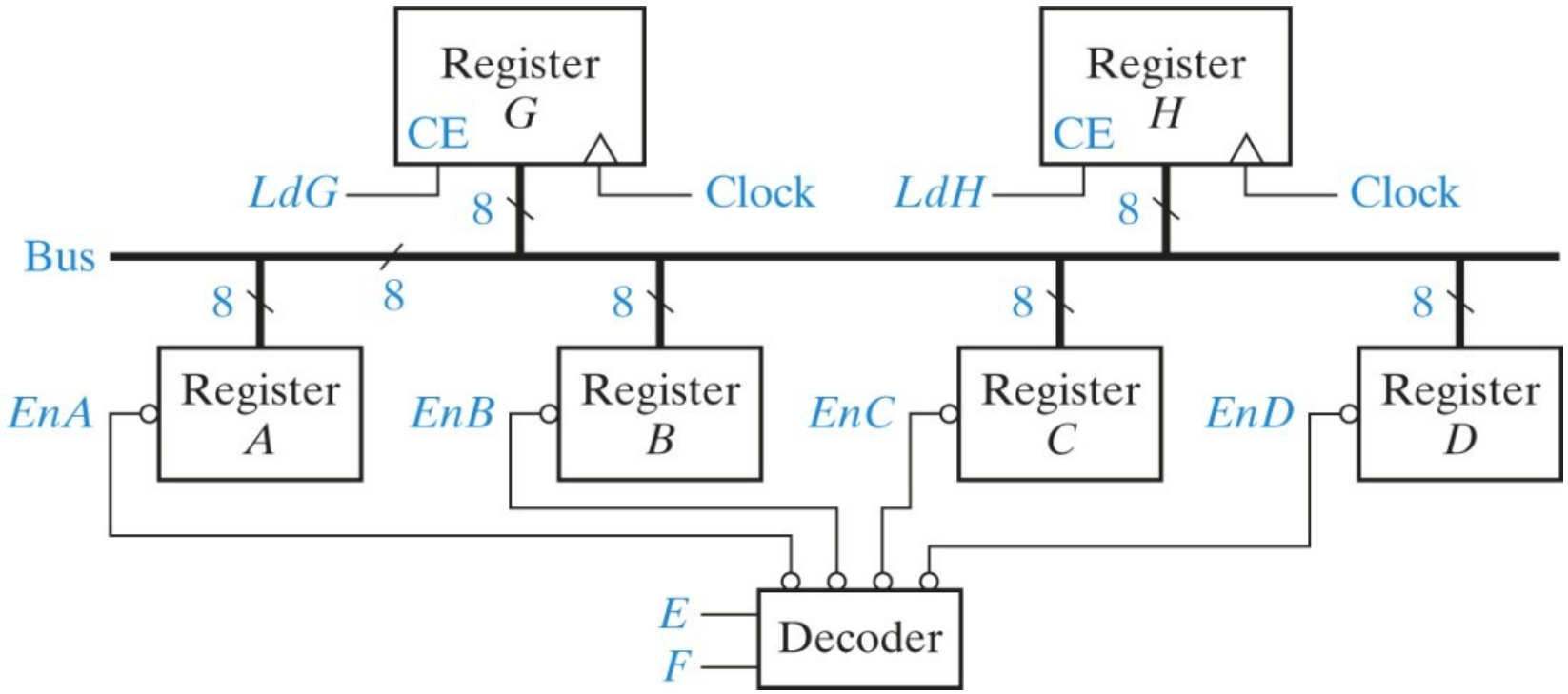
4-Bit Register



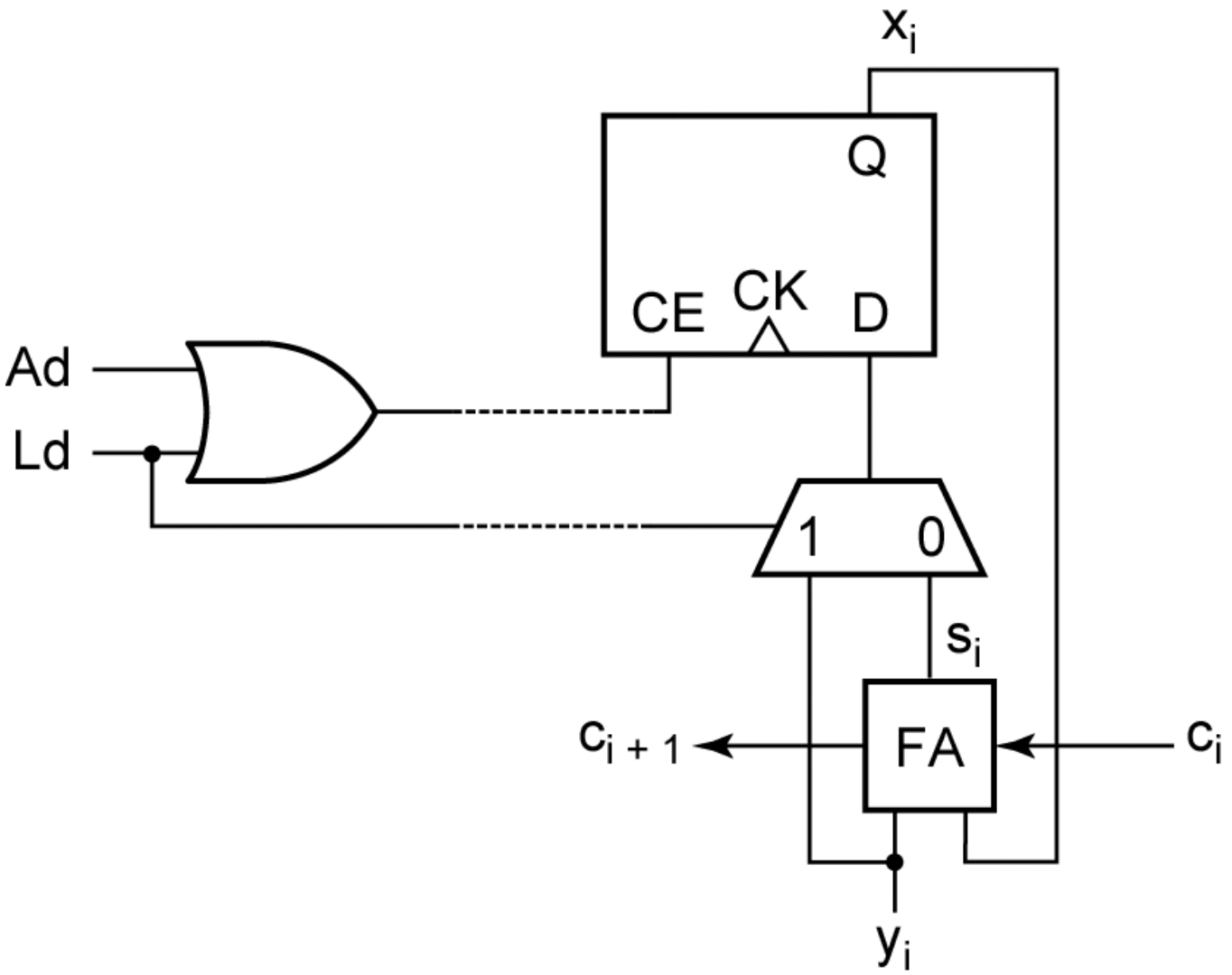
Data Transfer Between Registers



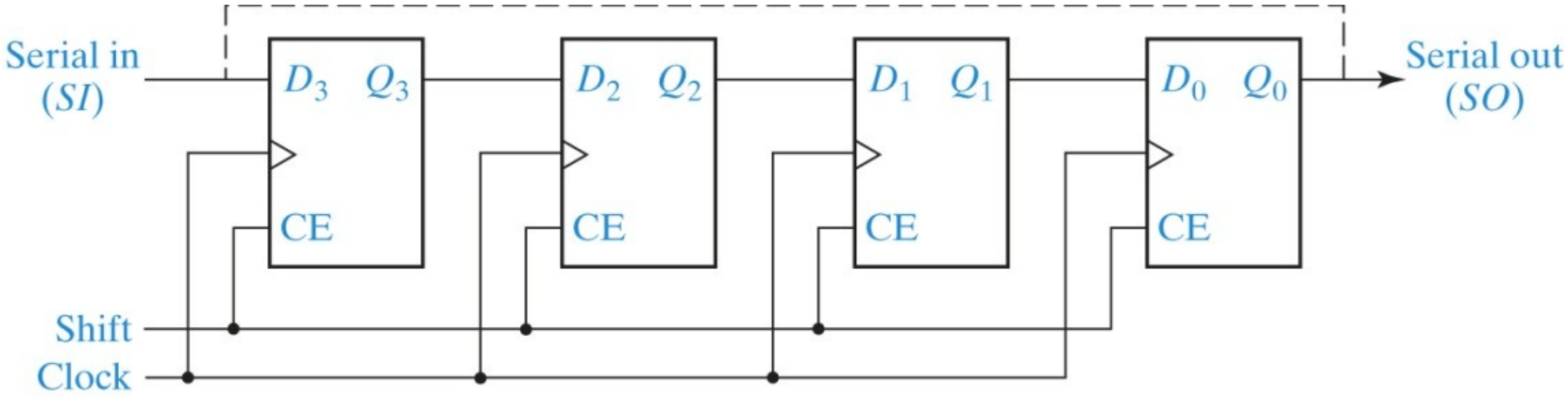
Tri-State Bus



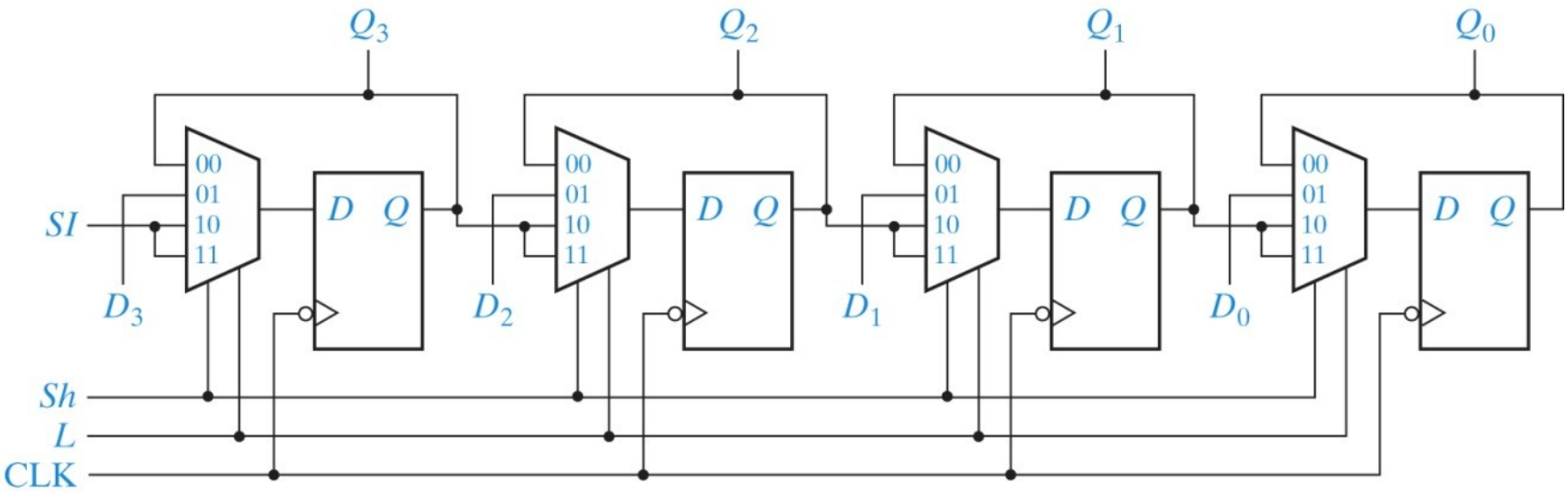
Adder with Accumulator



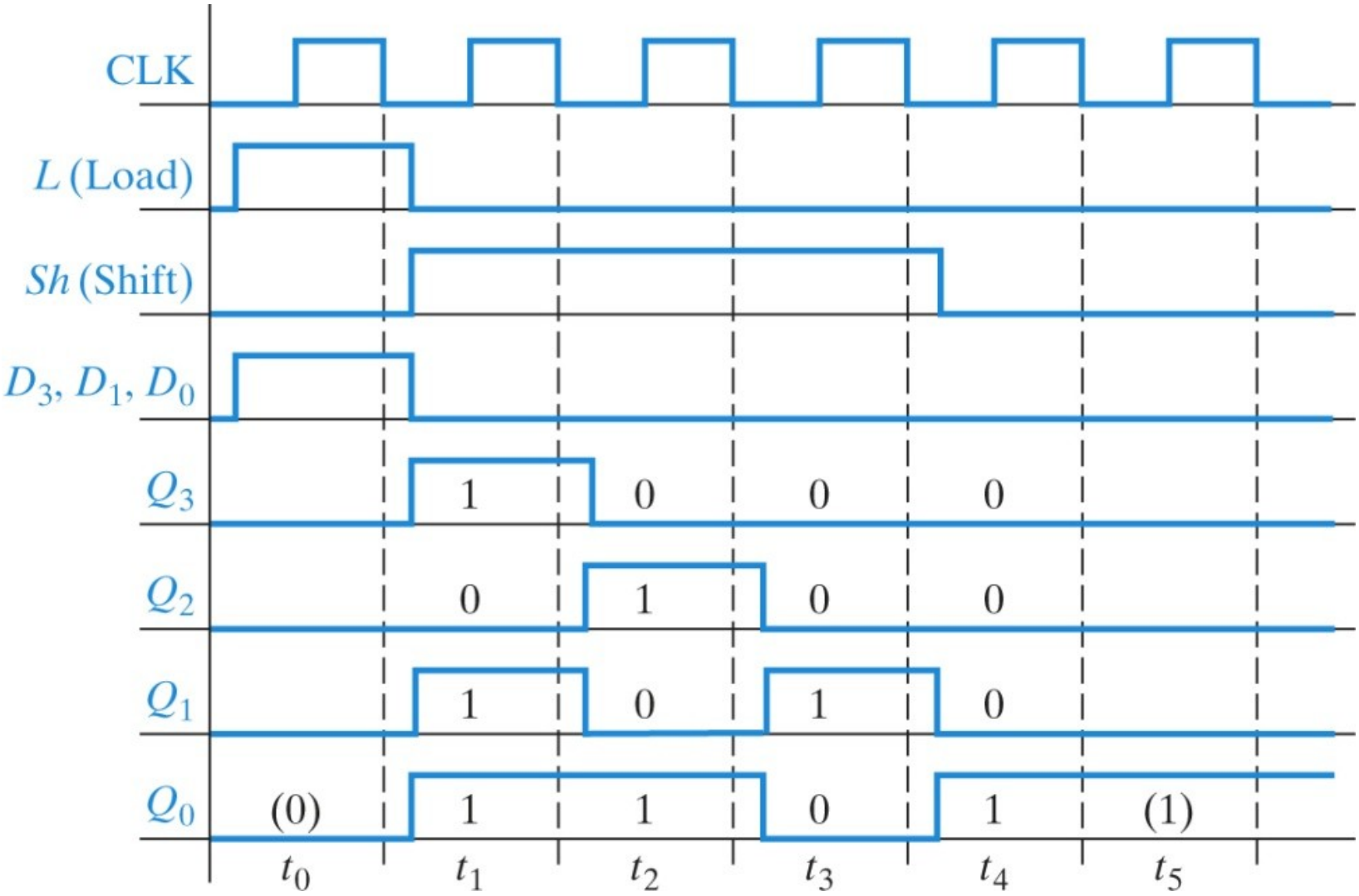
Basic Shift Register



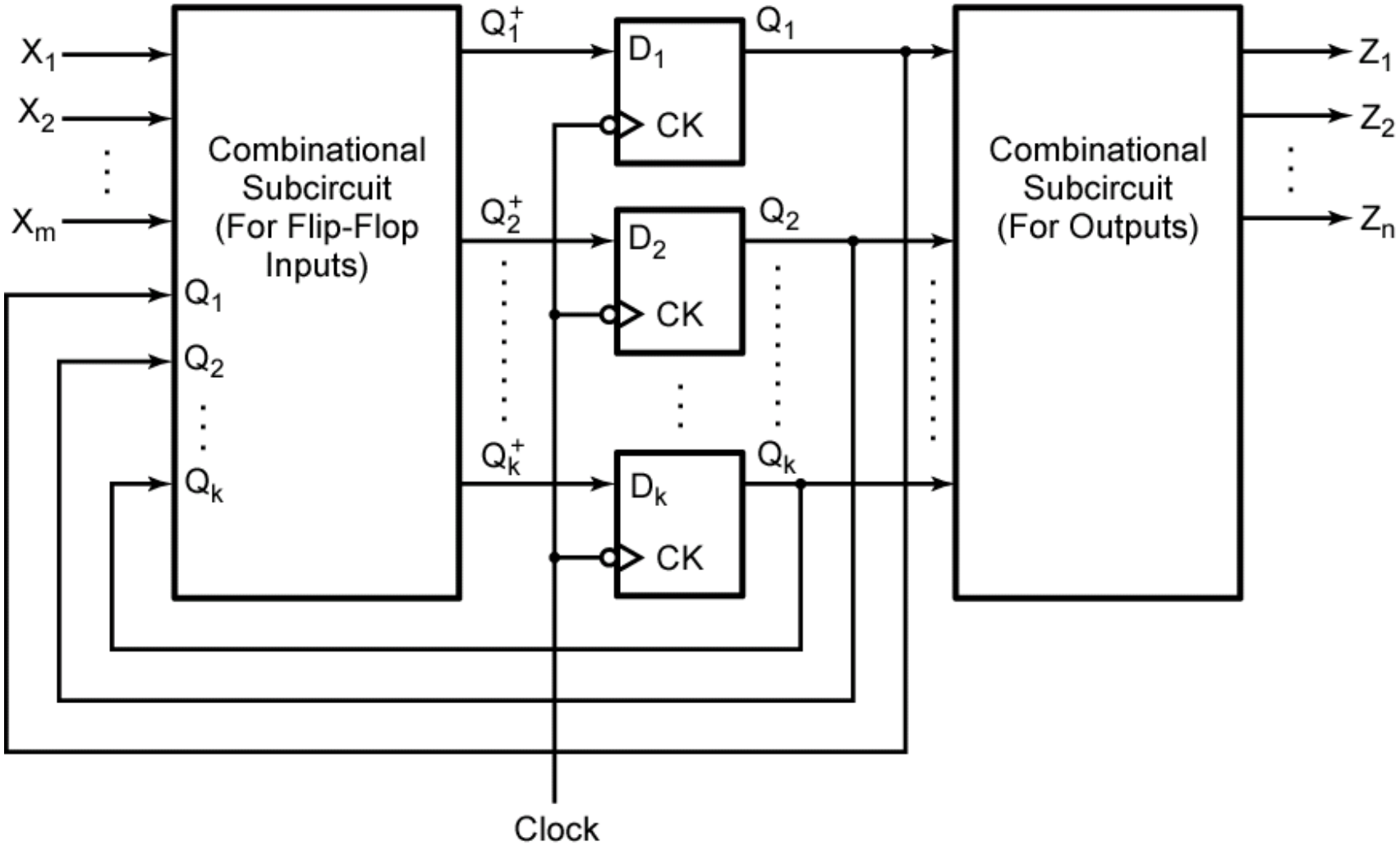
Multi-Function Shift Register



Timing Diagram



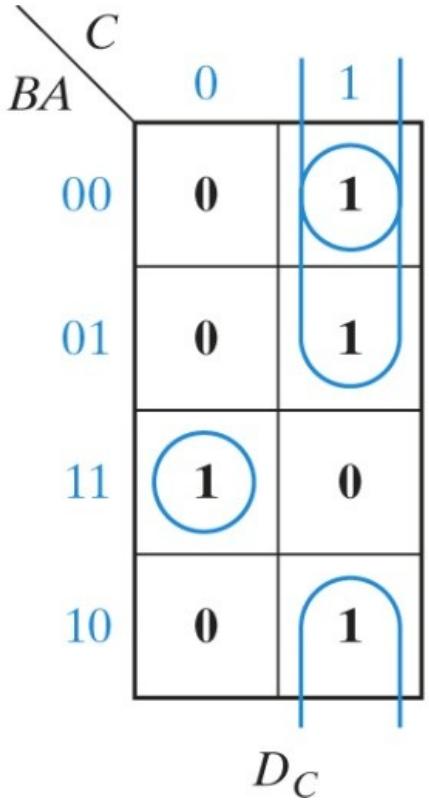
Sequential Circuits

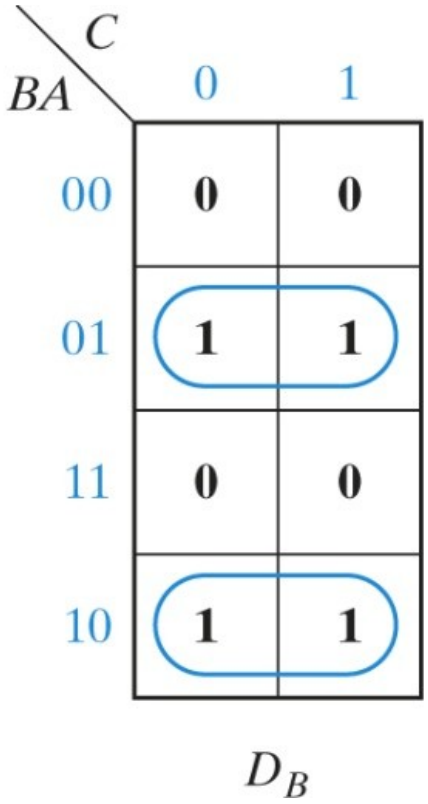


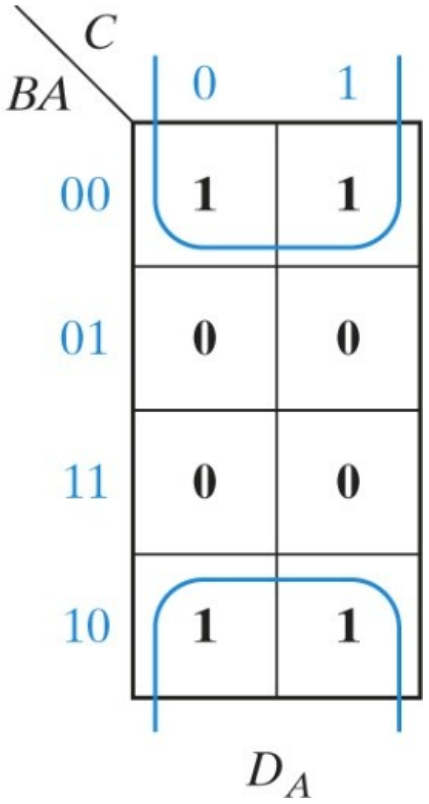
Binary Counter

Present State			Next State		
C	B	A	C^+	B^+	A^+
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	1	0	1
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	0	0

D FF Karnaugh Maps



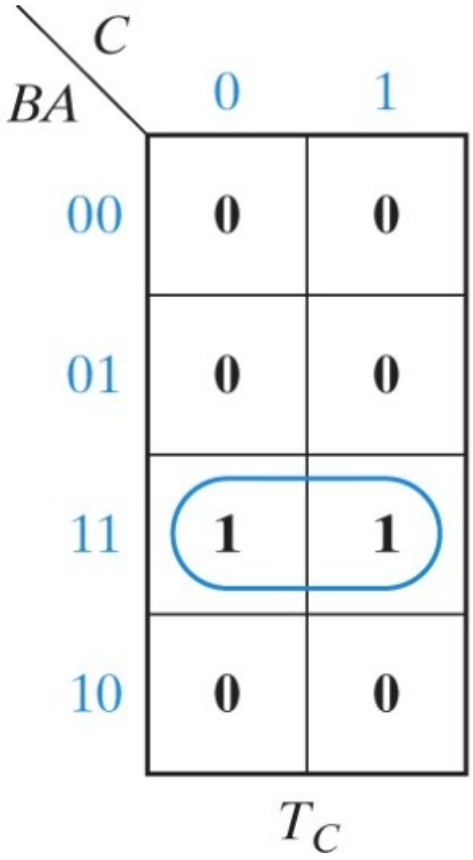


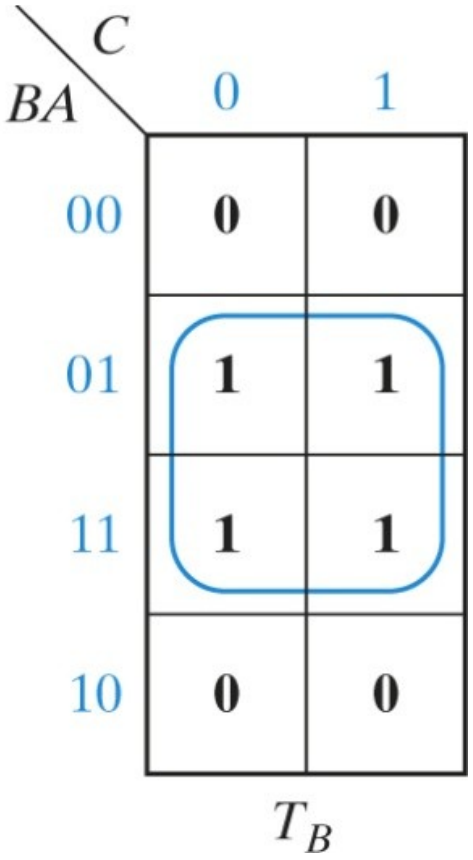


Binary Counter

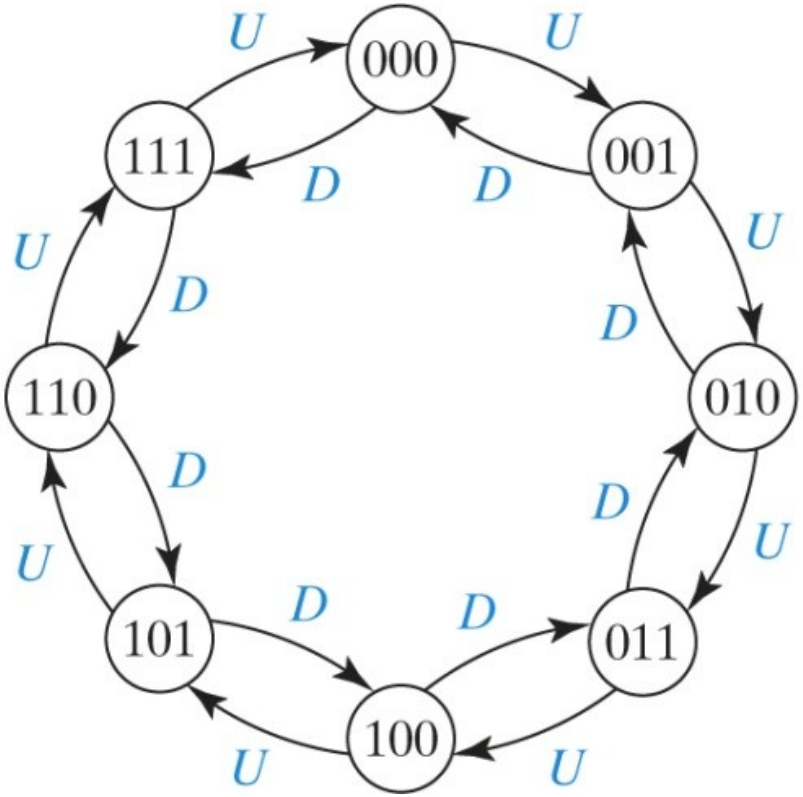
Present State			Next State			Flip-Flop Inputs		
C	B	A	C^+	B^+	A^+	T_C	T_B	T_A
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	0	1	1	1	0	0	1
1	1	1	0	0	0	1	1	1

T FF Karnaugh Maps





Up-Down Counter

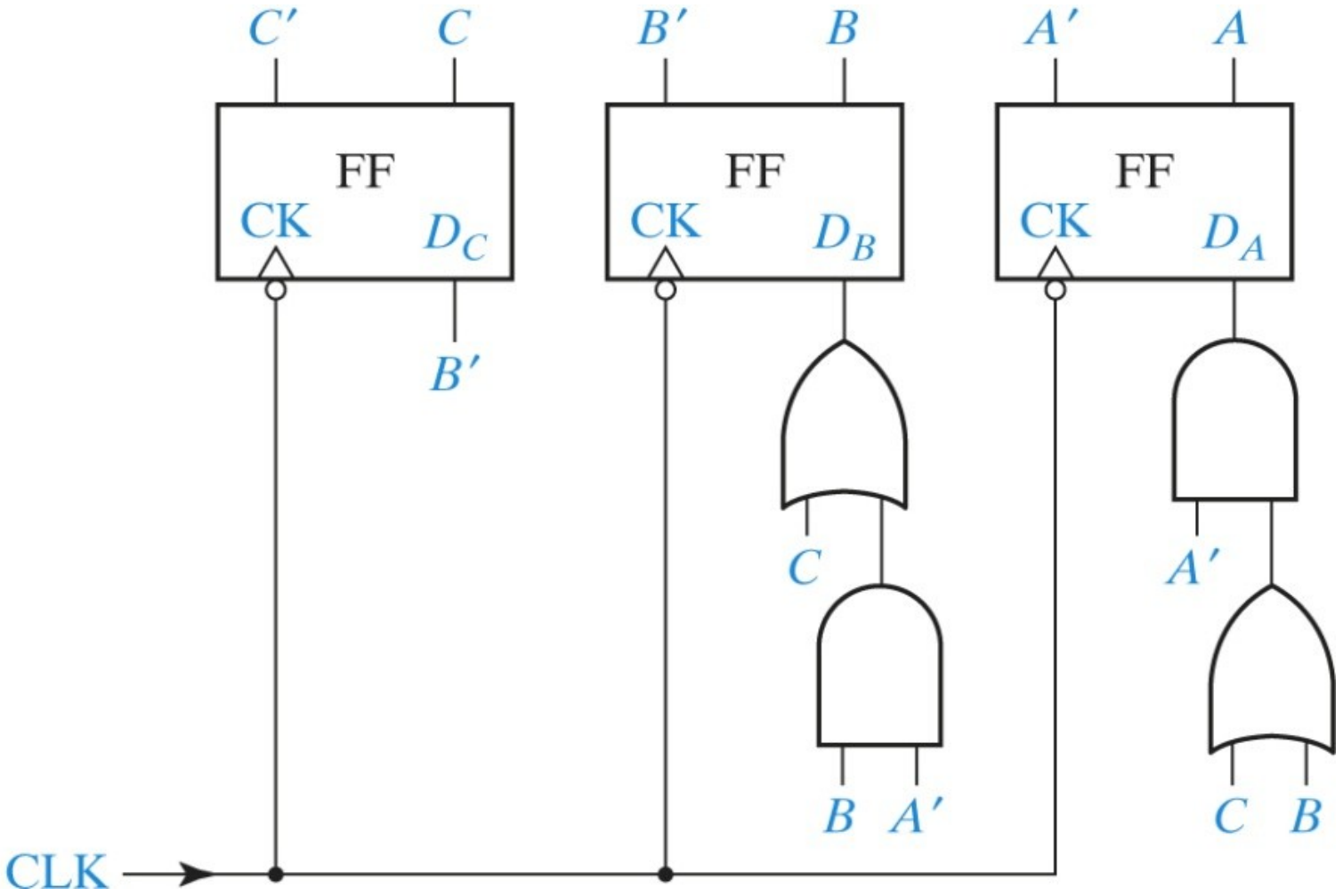


	$C^+B^+A^+$	
CBA	U	D
000	001	111
001	010	000
010	011	001
011	100	010
100	101	011
101	110	100
110	111	101
111	000	110

Modulo-5 Counter

C	B	A	C^+	B^+	A^+
0	0	0	1	0	0
0	0	1	.	.	.
0	1	0	0	1	1
0	1	1	0	0	0
1	0	0	1	1	1
1	0	1	.	.	.
1	1	0	.	.	.
1	1	1	0	1	0

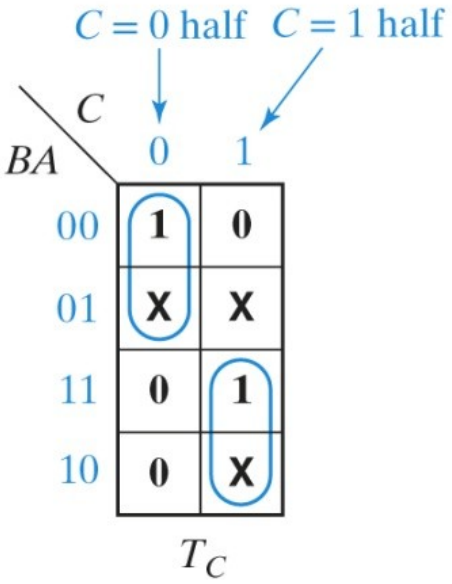
D FF Counter



Modulo-5 Counter

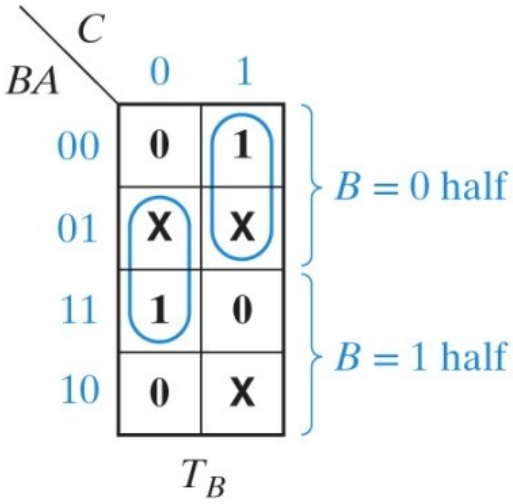
C	B	A	C+	B+	A+	TC	TB	TA
0	0	0	1	0	0	1	0	0
0	0	1	-	-	-	-	-	-
0	1	0	0	1	1	0	0	1
0	1	1	0	0	0	0	1	1
1	0	0	1	1	1	0	1	1
1	0	1	-	-	-	-	-	-
1	1	0	-	-	-	-	-	-
1	1	1	0	1	0	1	0	1

T FF Karnaugh Maps



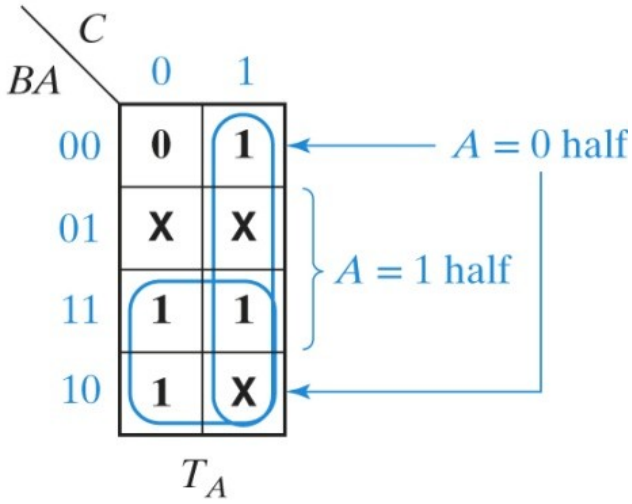
T_C

$T_C = C'B' + CB$



T_B

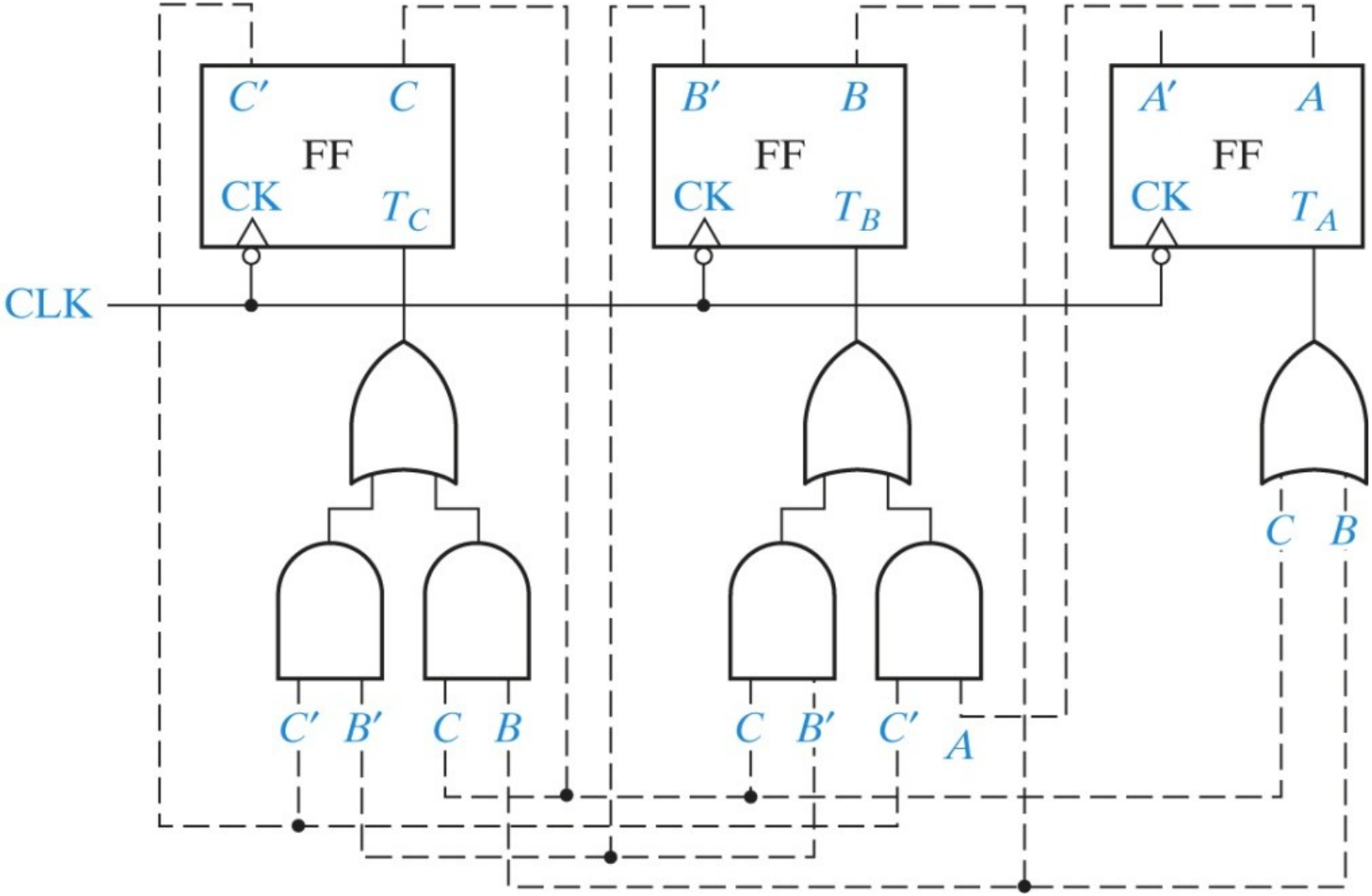
$T_B = C'A + CB'$



T_A

$T_A = C + B$

T FF Counter



Summary

- Registers
  - Data Transfer
  - Accumulators
  - Shift Registers
- Counters
  - State Tables
  - State Graphs
  - D Flip-Flops
  - T Flip-Flops