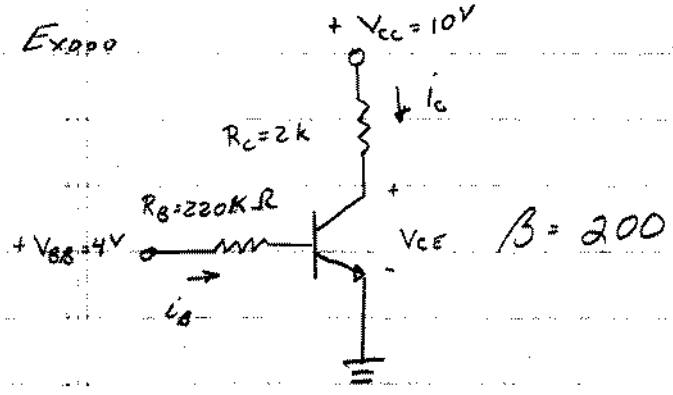


IV D.C. Analysis ; Load Lines

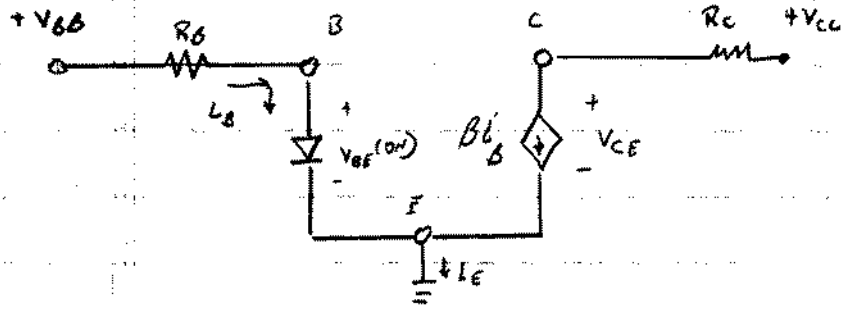
A. The Common Emitter Circuit

Example



Find I_B, I_C, I_E ; V_{CE} $\beta = 200$

DC Piecewise Linear Model



① $V_{BE} = 0.7^V$

② $I_B = \frac{4 - 0.7}{220k\Omega} = 15\mu A$

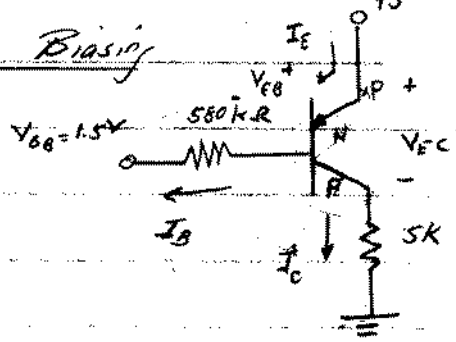
③ $I_C = \beta I_B = (200)(15\mu A) = 3mA$

④ $I_E = (1+\beta) I_B = 3.02^{mA}$

⑤ $V_{CE} = V_{CC} - I_C R_C = 10 - (3)(2) = 4V$

Note: Since $V_{BB} > V_{BE(ON)}$; $V_{CE} > V_{BE(ON)} \Rightarrow$ Fwd Active Mode

Example PNP Biasing



FIND I_B, I_C, I_E, V_{EC}

$V_{EB} = 0.6$

$\beta = 100$

① KVL: $-5 + V_{EB} - I_B(580k) + 1.5 = 0$

$$I_B = \frac{5 - 0.6 - 1.5}{580k} = 5\mu A$$

② $I_C = \beta I_B = 0.5mA$

③ $I_E = (\beta+1) I_B = 0.505mA$

④ KVL: $-5^V + V_{EC} + I_C 5K = 0 \Rightarrow V_{EC} = 5 - (.5)(5) = 2.5^V$

Note: ① The E-B junction is fwd biased since $\underbrace{V_{CC} - V_{BB}}_{V_{EB}\text{ (open)}} > 0.6^V$

② The C-B junction is reverse biased since

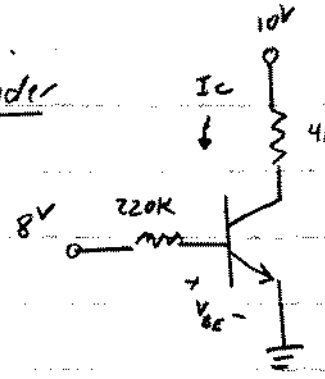
$V_{BC} = (5 - 0.7) - (.5 \times 5) = 4.3 - 2.5 = 2.8$

(V_B, V_C)

Thus transistor is in Linear Active mode

chk: $V_{EC} = 2.5^V > V_{EB(ON)}$ ✓

Consider



$\beta = 100$

① $I_B = \frac{8 - 0.7}{220k} = 33.2\ \mu A$

② $I_C = \beta I_B = 3.32\ mA$

③ $V_{CE} = V_{CC} - I_C R_C = 10 - 3.32(4)$

$= -3.28\ V$

↑ CAN'T BE

Can't have neg V_{CE} in Common Emitter NPN. (See characteristic curve)

∴ Transistor is not in Active Region

∴ $I_C \neq \beta I_B$

So: Set $V_{CE} = V_{CE(SAT)} = 0.2\ V$ ← typical

then: $I_C = I_{C(SAT)} = \frac{V_{CC} - V_{CE(SAT)}}{R_C} = \frac{10 - 0.2}{4k} = 2.45\ mA$

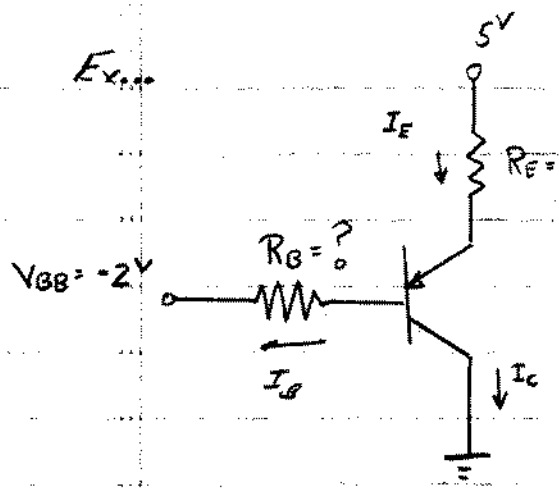
and $I_E = I_B + I_C = 33.2\ \mu A + 2.45\ mA = 2.48\ mA$

Notes: ① Typically $V_{CE(SAT)}$ = constant and is given, this is another piecewise linear approx of the transistor characteristic

② $I_C/I_B = \frac{2.45}{0.0332} = 74 < \beta$ which is typical of saturation.

So If $I_C < \beta I_B$ the transistor is in saturation.

Ex...



Given: $V_{EB(ON)} = 0.6V$

$\beta = 60$

Find: R_B so $V_{ECQ} = 2.5V$

1. EC Loop KVL: $-5^V + I_E\,2k + V_{EC} = 0$

$$I_E = \frac{5 - 2.5}{2k} = \underline{1.25\ mA}$$

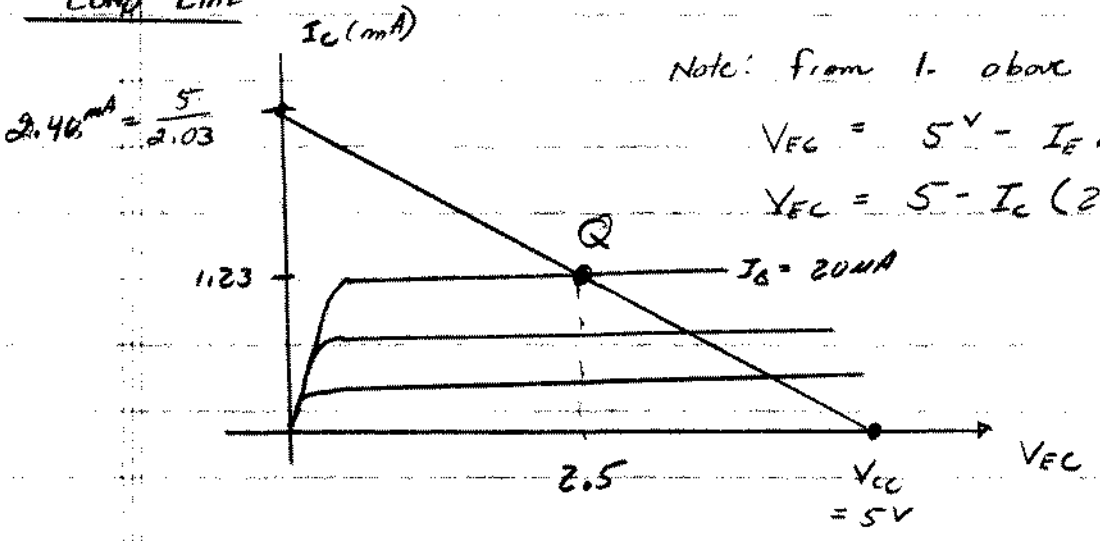
2. $I_C = \frac{\beta}{1+\beta} I_E = \left(\frac{60}{61}\right) 1.25 = \underline{1.23\ mA}$

3. $I_B = I_E/(1+\beta) = \underline{0.02\ mA}$

4. EB Loop KVL: $-5 + I_E\,2k + V_{EB(ON)} + I_B R_B - 2 = 0$

$$R_B = \frac{7 - 0.6 - 1.25(2)}{.02\ mA} = \boxed{190K\,R}$$

Load Line



Note: from 1. above

$V_{EC} = 5^V - I_E\,2k = 5^V - \left(\frac{61}{60}\right) I_C\,2k$

$V_{EC} = 5 - I_C\,(2.03k)$

Ex...

Given: $R_B = 240\Omega$ Find: currents, V_o, power dissapated

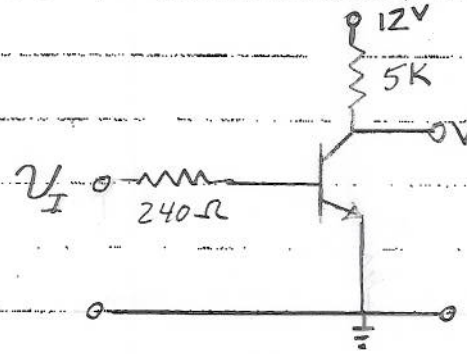
$V_{cc} = 12^V$

$V_{BE(on)} = 0.7^V$

$V_{CE(sat)} = 0.1$

$\beta = 75$

$R_C = 5\Omega$



① $V_I = 0$: transistor is C-O, $i_B = i_C = 0$, $v_o = V_{cc} = 12^V$

② $V_I = 12^V$: $I_B = \frac{V_I - V_{BE(on)}}{R_B} = \frac{12 - 0.7}{240} = 47.1\ mA$

Assuming Saturation:

$$I_C = \frac{V_{cc} - V_{CE(SAT)}}{R_C} = \frac{12 - 0.1}{5} = 2.38^A$$

Large for most transistors. Would need a power transistor

ck: $\frac{I_C}{I_B} \overset{?}{<} \beta$

$2.38 / 0.0471 = 50.6 < \beta$ ✓

$v_o = V_{CE(SAT)} = 0.1^V$

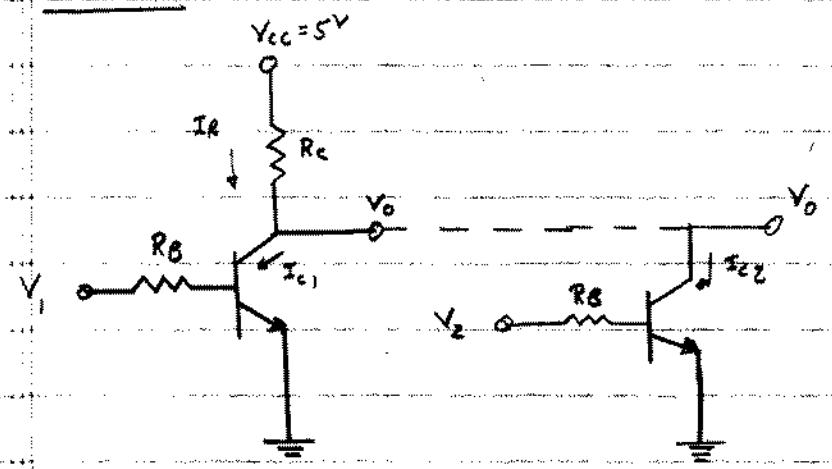
③ power dissapated in transistor = $P = i_C v_{CE} + i_B v_{BE}$

$= (2.38)(0.1) + (0.0471)(0.7)$

$= \underline{0.271^W}$

B. Digital Logic

Consider



For $V_1 = 0$, Q1 is cutoff, $I_B = 0$, $I_C = 0$, $V_o = V_{CC} = 5^V$

For $V_1 = 5^V$, Q1 is SATURATED, $V_o = V_{CE} \cong 0.2^V$

Now add a second transistor: 2 INPUT NOR GATE

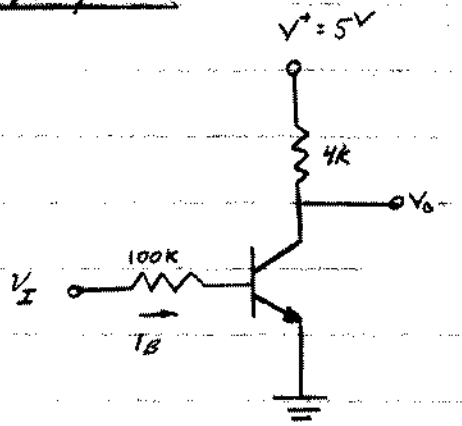
V_1	V_2	V_o
0	0	5^V
5	0	0.2^V
0	5	0.2
5	5	0.2

Ex 9.9 $\beta = 50$, $V_{BE(ON)} = 0.7V$, $V_{CE(SAT)} = 0.2V$

$R_C = 1K$, $R_B = 20K$

V_1	V_2	V_o	I_R	Q_1	Q_2
0	0	5	0	$I_{B1} = I_{C1} = 0$	$I_{B2} = I_{C2} = 0$
5	0	0.2	$\frac{5-0.2}{1K} = 4.8mA$	$I_{B1} = \frac{5-0.7}{20K} = 0.215mA$	$I_{B2} = I_{C2} = 0$
				$I_{C1} = I_R = 4.8mA$	
0	5	0.2	4.8 mA	$I_{B1} = I_{C1} = 0$	$I_{B2} = 0.215mA$
					$I_{C2} = 4.8mA$
5	5	0.2	4.8 mA	$I_{B1} = 0.215mA$	$I_{B2} = 0.215mA$
				$I_{C1} = I_R/2 = 2.4mA$	$I_{C2} = I_R/2 = 2.4mA$

C. Amplifier



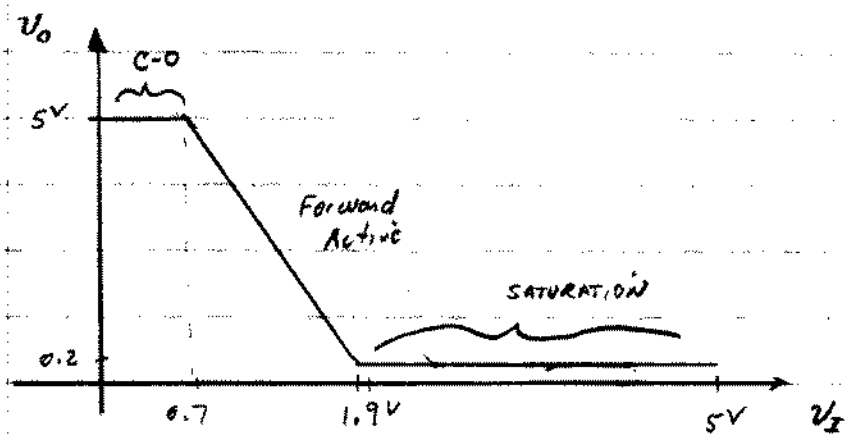
$\beta_F = 100$

$V_A = \infty$

$V_{BE(on)} = 0.7$

$V_{CE(SAT)} = 0.2$

SKETCH TRANSFER CHARACTERISTIC (V_o vs. V_I)



For $V_I < 0.7^V$, Q is C-O & $V_o = 5^V$

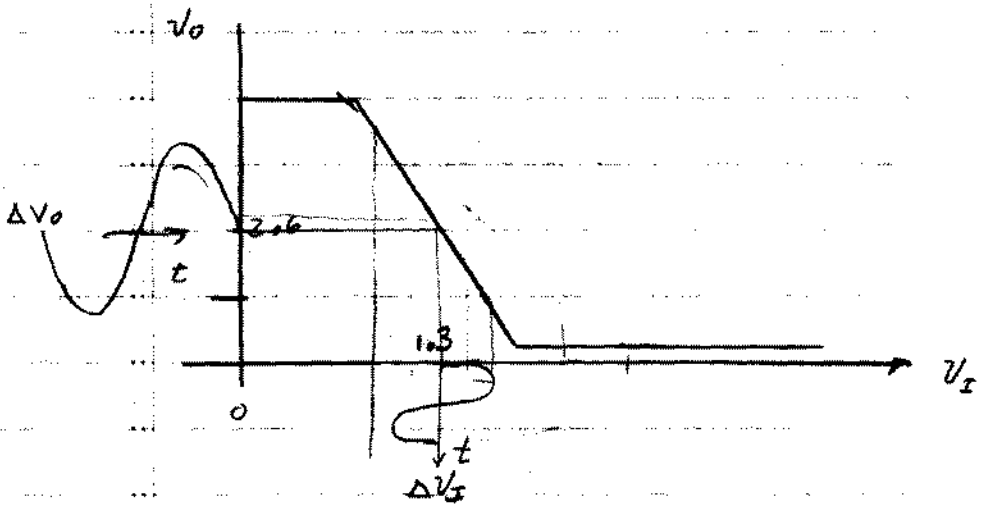
For $V_I > 0.7$, Q is ON $\quad I_B = \dfrac{V_I - V_{BE(ON)}}{R_E} = \dfrac{V_I - 0.7}{100k}$

$$V_o = V^+ - \beta I_B R_C = 5 - 100\left[\frac{V_I - 0.7}{100k}\right]4k = 7.8 - 4V_I$$

at $V_I > 1.9$ $\quad V_o = 0.2$ in SAT

AC Analysis

- Set $V_I = 1.3^V = V_{BB}$ and input an AC source ΔV_I.



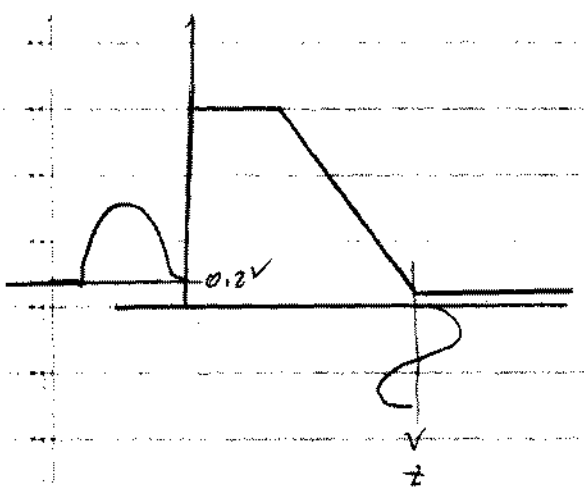
Note: $I_B = \dfrac{V_{BB} + \Delta V_I - V_{BE(ON)}}{R_B} = \dfrac{(1.3-0.7) + \Delta V_I}{100k\Omega}$

$$V_O = V^+ - \beta I_B R_C = 5 - (100)\left[\frac{0.6 + \Delta V_I}{100k}\right] 4k$$

$$\boxed{V_O = 2.6 - 4\Delta V_I}$$

$$\text{Gain} = A_V = \frac{\Delta V_O}{\Delta V_I} = \boxed{-4}$$

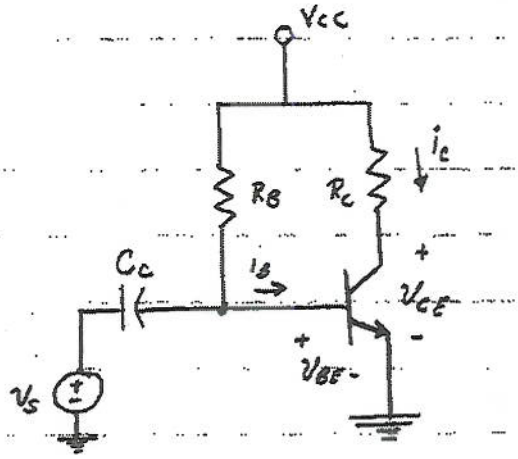
Suppose $V_I = 1.9V$



B. Single Base Resistor Biasing

DC ANALYSIS

1.



INPUT CIRCUIT

KVL: $I_{BQ} = \dfrac{V_{CC} - V_{BE}}{R_B}$

OUTPUT CIRCUIT

KVL: $I_{CQ} = \dfrac{V_{CC} - V_{CEQ}}{R_C}$

Ex 1a Consider $V_{CC} = 12^V$, $V_{BE(ON)} = 0.7^V$, $R_C = 6k\Omega$, $R_B = 1.13M\Omega$

then for $\beta_F = 100$:

$$I_{BQ} = \frac{V_{CC} - V_{BE(ON)}}{R_B} = \frac{12 - 0.7}{1.13M} = 10\mu A$$

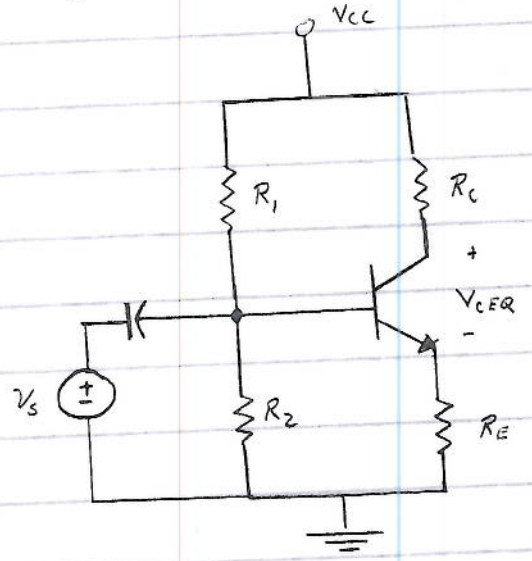
$$V_{CEQ} = V_{CC} - \beta_F I_B R_C = 12 - (100)(10\mu A)(6k) = \underline{6^V}$$

for $\beta_F = 50$,

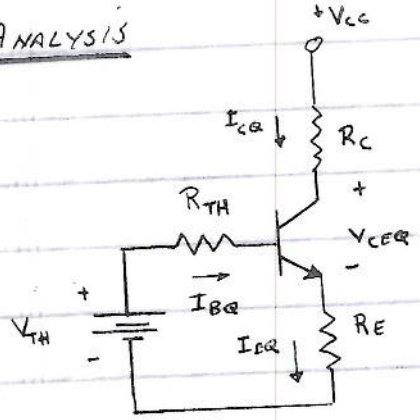
$$V_{CEQ} = 12 - (50)(10\mu A)(6k) = \underline{9^V}$$

50% ↓ β_F, 50% ↑ V_{CEQ}

C. Voltage Divider Biasing ; the Emitter Resistor



ANALYSIS



WHERE: $V_{TH} = \frac{R_2}{R_1 + R_2} V_{CC}$

$R_{TH} = R_1 // R_2 = \frac{R_1 R_2}{R_1 + R_2}$

Now: $V_{CEQ} = V_{CC} - \beta_F I_{BQ} R_C - (\beta_F + 1) I_{BQ} R_E$

However: KVL: $-V_{TH} + I_{BQ} R_{TH} + V_{BE} + (\beta_F + 1) I_{BQ} R_E = 0$

So $I_{BQ} = \frac{V_{TH} - V_{BE}}{R_{TH} + (\beta_F + 1) R_E}$

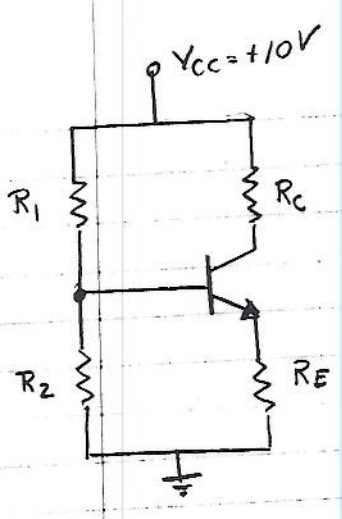
$\therefore V_{CE} = V_{CC} - \left[\frac{V_{TH} - V_{BE}}{R_{TH} + (\beta_F + 1) R_E}\right] \left[\beta_F R_C + (\beta_F + 1) R_E\right]$

NEARLY INDEPENDENT OF β

If by design $R_{TH} \ll (\beta_F + 1) R_E$;

Then $V_{CEQ} \cong V_{CC} - \left[V_{TH} - V_{BE}\right] \left[\frac{\beta_F R_C}{(\beta_F + 1) R_E} + 1\right]$

Ex..



Given: $\beta = 100$, $V_{BE,ON} = 0.7^V$

$R_1 = 56k\,\Omega$

$R_2 = 12.2k\,\Omega$

$R_C = 2K\,\Omega$

$R_E = 0.4K\,\Omega$

Find the Qpt: I_{CQ} & V_{CEQ}

① $R_{TH} = R_1 \| R_2 = 56k \| 12.2k = \underline{10K\Omega}$

$V_{TH} = \left(\frac{R_2}{R_1 + R_2}\right) 10^V = \frac{12.2}{12.2+56}(10) = \underline{1.79^V}$

② $-V_{TH} + I_B R_{TH} + V_{BE,ON} + I_E R_E = 0$

$I_B = \frac{V_{TH} - V_{BE,ON}}{R_{TH} + (\beta+1) R_E} = \frac{1.79 - 0.7}{10K + (101)(0.4K)} = \underline{21.6\mu A}$

③ $I_{CQ} = \beta I_B = \boxed{2.16\,mA}$

④ $V_{CEQ} = V_{CC} - I_{CQ} R_C - I_{EQ} R_E$

$= 10 - (2.16k)2^{mA} - (101)(21.6\,\mu A)(0.4K)$

$= \boxed{4.81^V}$

b) $\beta = 50$.

$I_B = \frac{1.79 - 0.7}{10K + (51)(0.4k)} = \underline{36\mu A}$

$I_{CQ} = (50)(36\mu A) = \boxed{1.80\,mA}$

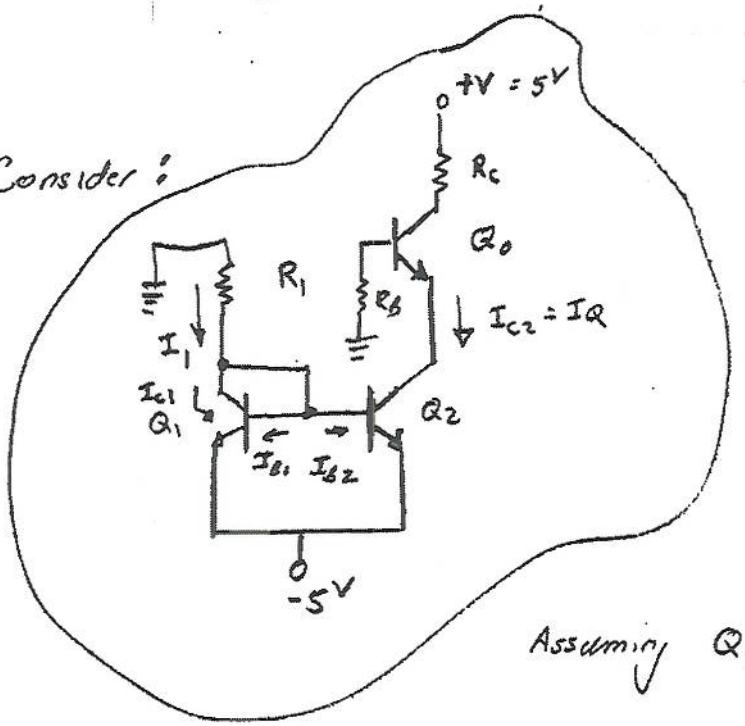
$V_{CEQ} = V_{CC} - I_{CQ} R_C - I_{EQ} R_E$

$= 10 - 1.8(2) - (51)(36\mu A)(0.4k)$

$= \boxed{5.67\,V}$

D. Integrated Circuit Biasing

Consider:



R_1 - Q_1 Loop

$$0 = I_1 R_1 + V_{BE(ON)} + V^-$$

$$I_1 = \frac{-(V^- + V_{BE(ON)})}{R_1}$$

ALSO

$$I_1 = I_{C1} + I_{B1} + I_{B2}$$

Assuming Q_1 & Q_2 are identical:

$$I_1 = I_{C1} + 2I_{B2} = I_{C2}\left(1 + \frac{2}{\beta}\right)$$

$$\boxed{I_{C2} = I_Q = \frac{I_1}{1 + 2/\beta}}$$

Ex. Let $R_1 = 10k\Omega$, $\beta = 50$, $V_{BE(ON)} = 0.7V$

Then

$$I_1 = \frac{-(V^- + V_{BE(ON)})}{R_1} = \frac{-(-5 + 0.7)}{10k} = 0.43\,mA$$

$$I_{C2} = \left(\frac{I_1}{1 + 2/\beta}\right) = \frac{0.43\,mA}{(1 + 2/50)} = 0.413\,mA$$

$$I_{B1} = I_{B2} = I_{C2}/\beta = \frac{0.413}{\beta} = 8.26\,\mu A$$