ELEC-313
Lab 6: MOSFET Characterization

November 5, 2013

Date Performed:	October 30, 2013
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1 Objective

The objective is to construct and observe the operation of a CMOS inverter and NAND gate.

2 Equipment

Transistor: 1N4007	Power supply: HP E3631A
Resistors: 330 Ω (x3), 2.2 kΩ, 33 kΩ	Multimeters: Fluke 8010A (x2)

3 Schematics

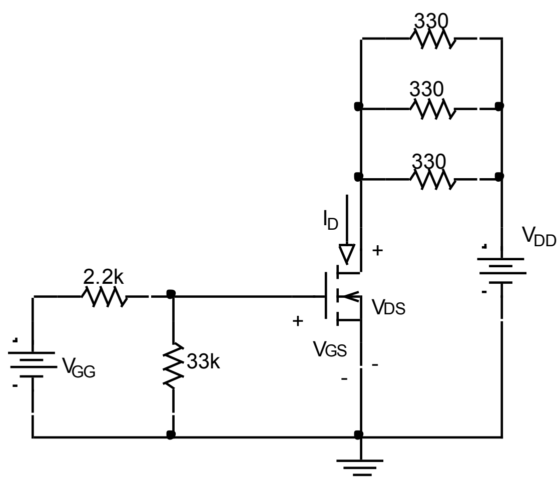

Figure 1: Circuit used in this lab.

4 Procedure

4.1 DC Characteristics

1. Obtain the 2N7000 MOSFET transistor and resistors needed to build the circuit shown.
2. Construct the circuit of figure 2. Use the HP multi-meter to measure the drain current, I_D , and the Fluke multi-meters to measure V_{DS} and V_{GS}. Use the +6 V power supply for V_{GG} and the +25 V supply for V_{DD}.
3. Set V_{GG} to 0 V and V_{DD} to 5 V and measure V_{DS} and I_D.

4. Slowly increase V_{GG} until the transistor just begins to conduct current as evidenced by a small drop in V_{DS}. Record the value of V_{GS} as the Gate Threshold Voltage, V_{TN}.

5. Adjust V_{GG} to increase V_{GS} by 0.2 V above the threshold. Readjust V_{DD} to return V_{DS} to 5 V, and then measure the drain current (I_D). Record the value of V_{GS} in the first column of table1, and record the value of I_D in the second column (the $V_{DS} = 5$ V column).

6. Continue to increase V_{GS} in steps of 0.2 V while maintaining V_{DS} at 5 V. Measure the drain current at each step. Record the values of V_{GS} and I_D in table 1. Stop this process when the drain current reaches approximately 80mA.

7. Complete the entries in table 1 by adjusting V_{DD} and V_{GG} to obtain the various required V_{DS} and V_{GS} values, then measuring I_D at each value. Do not exceed 80mA drain current.

4.2 Small-Signal Transconductance

1. Adjust V_{GG} and V_{DD} to obtain $V_{DS} = 5$ V and $I_D = 10$ mA.

2. Record the value of V_{GS} as V_{G1}.

3. Record the exact measured value of I_D and assign it to I_{D1}. Use the full resolution of the HP multimeter.

4. Increase V_{GS} by 10 mV and record it value as V_{G2}.

5. Measure I_D , recording it as I_{D2}.

6. Compute the small signal transconductance (Eq 1).

5 Results

The following table shows several V_{GS} values that are just slightly over the overdrive voltage V_{OV} and gives an idea of the amount of variation for values resulting from Equation 2.

$V_{TN} = 2.11\,\mathrm{V}$	$V_{DS} = 0.5\,\mathrm{V}$	$V_{DS} = 1\,\mathrm{V}$	$V_{DS} = 1.5\,\mathrm{V}$
$V_{GS} = 2.91\,\mathrm{V}$			0.1078
$V_{GS} = 2.71\,\mathrm{V}$		0.0931	
$V_{GS} = 2.51\,\mathrm{V}$	0.07688		

Table 1: k'_n

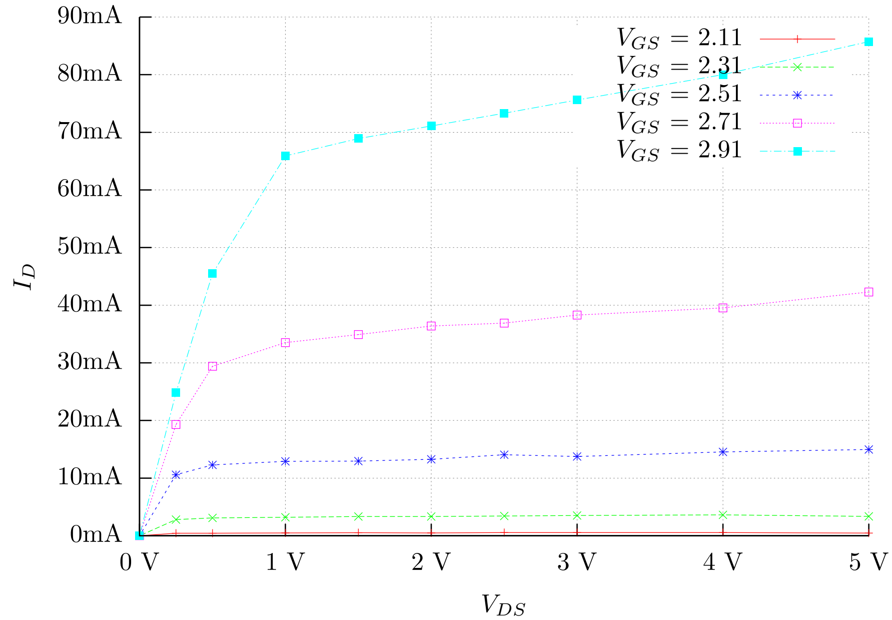

Figure 2: Graph

6 Conclusion

Its hard to compare the Figure 2 plot with the 2N7000 data sheet because the data sheets lowest V_{GS} curve is 3 V, which is still higher than the highest V_{GS} curve in Figure 2. However, it is still apparent that the V_{GS} curve of 2.91 V in Figure 2 is similar to the 3 V curve because the V_{OV} points are roughly the same with a V_{DS} value of 1 1.5 V. After the V_{OV} point, both curves taper off and have a very slight positive slope.

Its easier to compare Figure 2 plot with the PSpice simulation because the V_{GS} are closer to the values seen in Figure 2. Again the V_{OV} values are similar in both the plot and the simulation. But, the PSpice simulation curves are flat at points beyond the V_{OV} instead of sloped like it is in Figure 2.

The second PSpice simulation was more representative of the Figure 2 plots because the value of λ was changed from 0 (in the first simulation) to .06, which made the V_{GS} curves slope beyond the V_{OV}. Adding the λ also raised the I_D current for the individual V_{OV} points. This is because the λ value represents the slight resistance that is inherent to the transistor a low λ value is a higher resistance and a high λ is a lower resistance because the resistance is the inverse of the λ.

7 Equations

$$g_m = \frac{I_{D2} - I_{D1}}{V_{GS2} - V_{GS1}} \tag{1}$$

$$\frac{k'_n}{2} \cdot \frac{W}{L} = \frac{I_{D1}}{(V_{GS1} - V_{TN})^2} \tag{2}$$