

ELEC-311
Project 3
Adder-Subtractor

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1 Objective

- Design a combinational logic circuit that adds, or subtracts, two 4-bit 2's complement numbers
- Describe the circuit using VHDL

2 Discussion

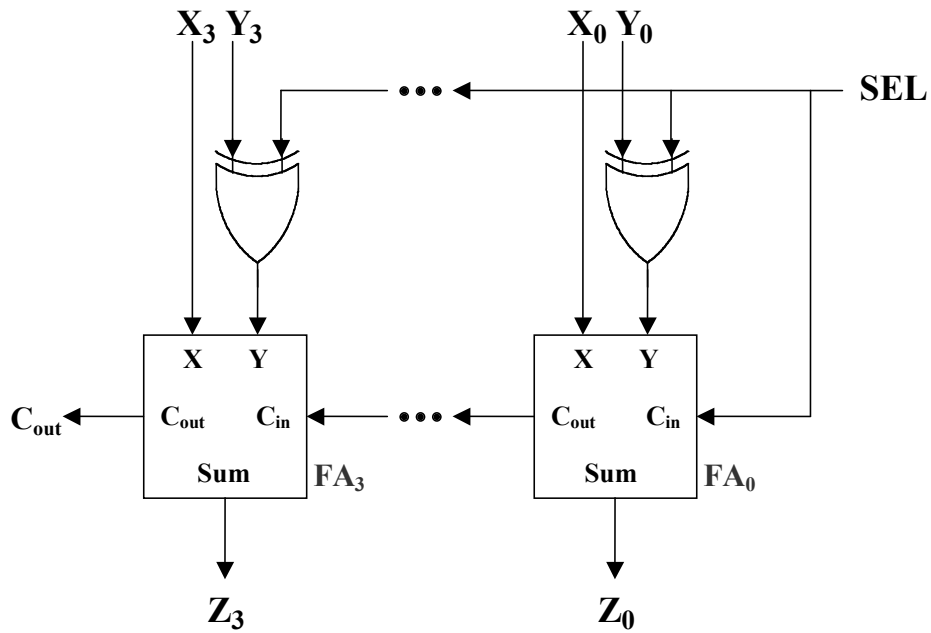


Figure 1: 4-bit adder/subtractor.

A diagram of a 4-bit adder/subtractor circuit is shown in Fig 1. It is composed of four 1-bit adders pieced together with some additional logic.

3 Results

4 VHDL

```
library IEEE;
use IEEE.STD_LOGIC_1164.all;
use work.project3_gates.all;

entity circuit is
```

X	Y	X	Y	X + Y	X - Y
3	1	0011	0001	0100	0010
1	5	0001	0101	0110	1100
-2	3	1110	0011	0001	1011
-2	-4	1110	1100	1010	0010
4	6	0100	0110	01010	1110

Table 1: Test vectors and expected values.

```

port (X      : in  std_logic_vector(3 downto 0);
      Y      : in  std_logic_vector(3 downto 0);
      Z      : out std_logic_vector(3 downto 0);
      SEL    : in  std_logic;
      Cout   : out std_logic);
end circuit;

architecture Structural of circuit is

    signal C : std_logic_vector(2 downto 0);
    signal S : std_logic_vector(3 downto 0);

begin

    x3 : ExclusiveOR port map(SEL, Y(3), S(3));
    x2 : ExclusiveOR port map(SEL, Y(2), S(2));
    x1 : ExclusiveOR port map(SEL, Y(1), S(1));
    x0 : ExclusiveOR port map(SEL, Y(0), S(0));

    fa3 : FullAdder port map(X(3), S(3), C(2), Cout, Z(3));
    fa2 : FullAdder port map(X(2), S(2), C(1), C(2), Z(2));
    fa1 : FullAdder port map(X(1), S(1), C(0), C(1), Z(1));
    fa0 : FullAdder port map(X(0), S(0), SEL, C(0), Z(0));

end Structural;

```