Microelectronics
Circuit Analysis and Design

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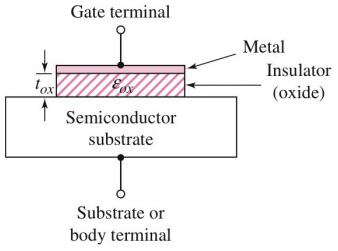
Chapter 3

The Field Effect Transistor

In this chapter, we will:

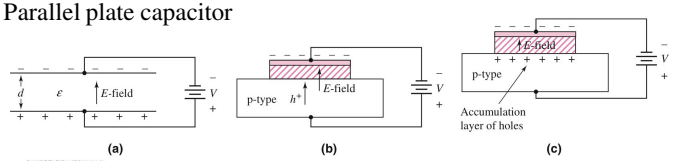
- Study and understand the operation and characteristics of the various types of MOSFETs.
- Understand and become familiar with the dc analysis and design techniques of MOSFET circuits.
- Examine three applications of MOSFET circuits.
- Investigate current source biasing of MOSFET circuits, such as those used in integrated circuits.

Basic Structure of MOS Capacitor



MOS Capacitor Under Bias: Electric Field and Charge

Parallel plate capacitor



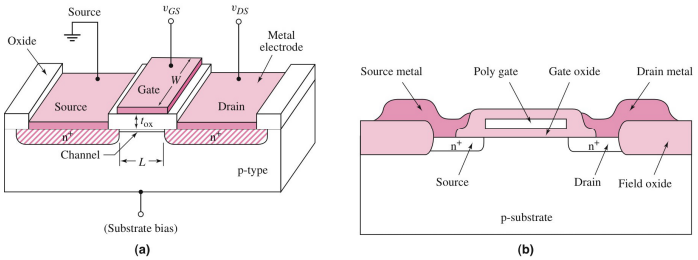
Negative gate bias:

Holes attracted to gate

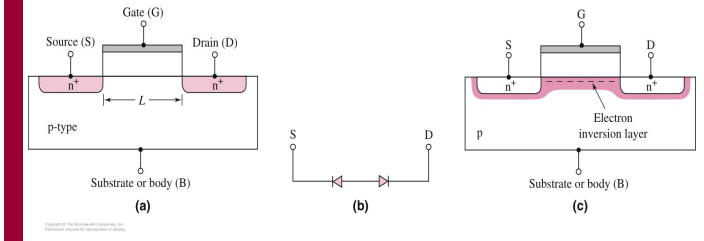
Positive gate bias:

Electrons attracted to gate

Schematic of n-Channel Enhancement Mode MOSFET



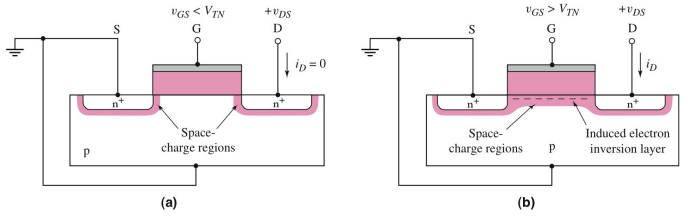
Basic Transistor Operation



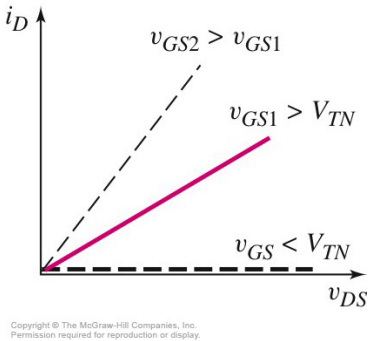
Before electron inversion layer is formed

After electron inversion layer is formed

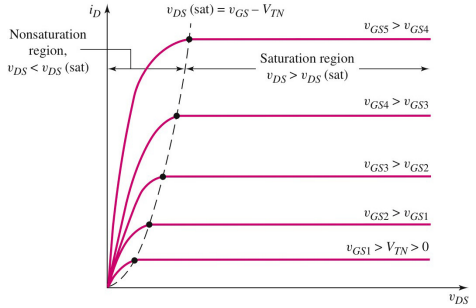
Basic Transistor Operation



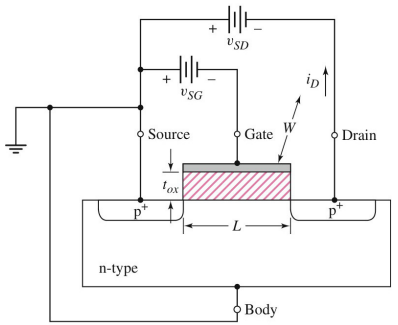
Current Versus Voltage Characteristics: Enhancement-Mode nMOSFET



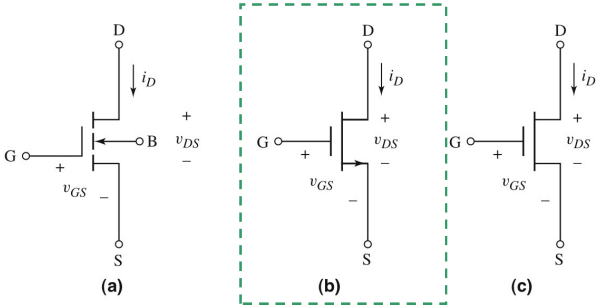
Family of i_D Versus v_{DS} Curves: Enhancement-Mode nMOSFET



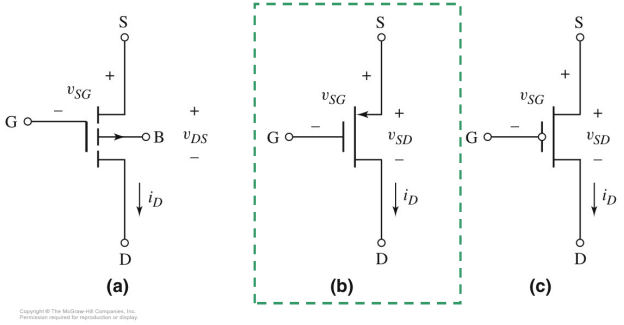
p-Channel Enhancement-Mode MOSFET



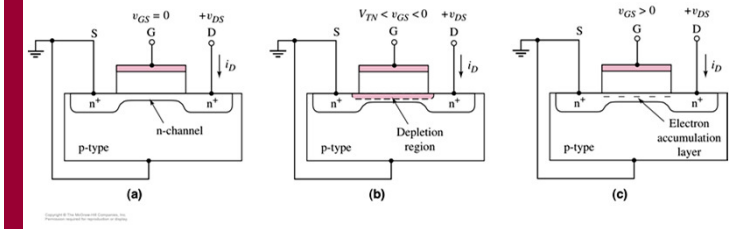
Symbols for n-Channel Enhancement-Mode MOSFET



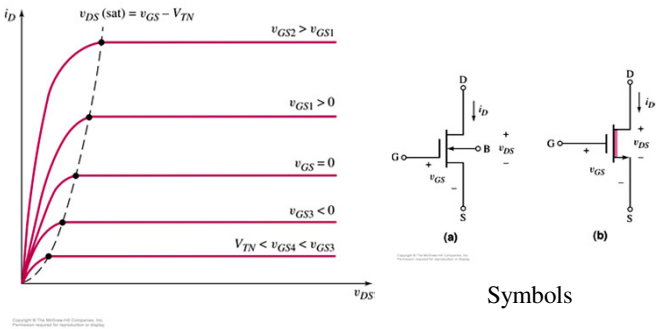
Symbols for p-Channel Enhancement-Mode MOSFET



n-Channel Depletion-Mode MOSFET

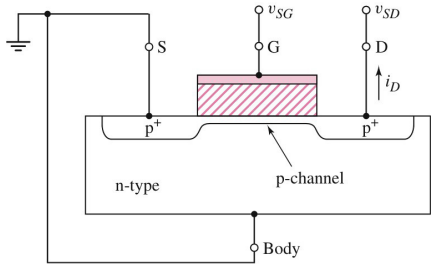


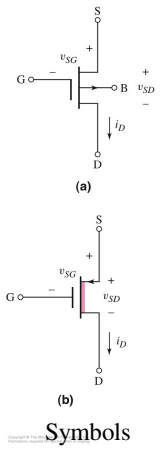
Family of i_D Versus v_{DS} Curves: Depletion-Mode nMOSFET



Symbols

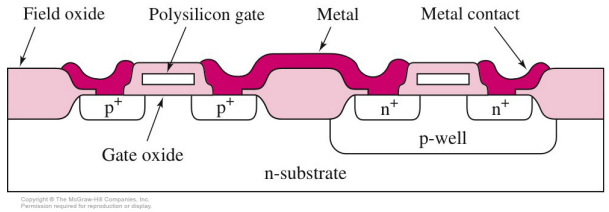
p-Channel Depletion-Mode MOSFET





Symbols

Cross-Section of nMOSFET and pMOSFET



Both transistors are used in the fabrication of CMOS circuitry.

Summary of I-V Relationships

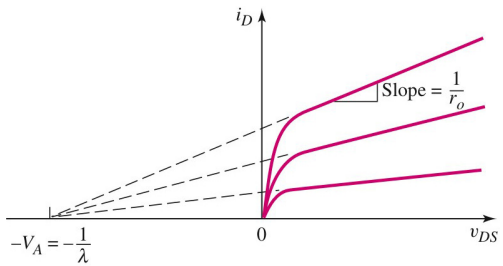
Region	NMOS	PMOS
Nonsaturation	$v_{DS}<v_{DS}(sat)$ $i_D = K_n[2(v_{GS}-V_{TN})v_{DS}-v_{DS}^2]$	$v_{SD}<v_{SD}(sat)$ $i_D = K_p[2(v_{SG}+V_{TP})v_{SD}-v_{SD}^2]$
Saturation	$v_{DS}>v_{DS}(sat)$ $i_D = K_n[v_{GS}-V_{TN}]^2$	$v_{SD}>v_{SD}(sat)$ $i_D = K_p[v_{SG}+V_{TP}]^2$
Transition Pt.	$v_{DS}(sat) = v_{GS} - V_{TN}$	$v_{SD}(sat) = v_{SG} + V_{TP}$
Enhancement Mode	$V_{TN} > 0V$	$V_{TP} < 0V$
Depletion Mode	$V_{TN} < 0V$	$V_{TP} > 0V$

Conduction Parameters

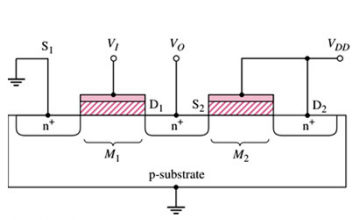
- NMOSFET $K_n = \frac{W\mu_n C_{ox}}{2L} = k_n' \frac{W}{2L}$
- PMOSFET $K_p = \frac{W\mu_p C_{ox}}{2L} = k_p' \frac{W}{2L}$

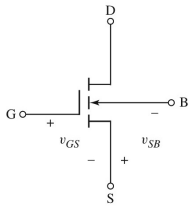
where: $C_{ox} = \varepsilon_o / t_{ox}$

Channel Length Modulation: Early Voltage



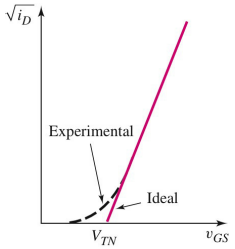
Body Effect





- Causes an increase in the required threshold voltage
- This is a small effect for a single device and will be ignored

Subthreshold Condition

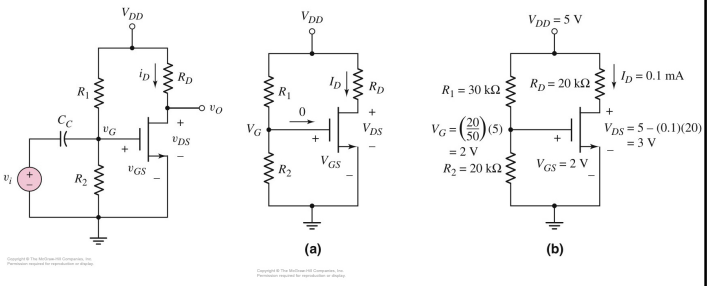


- Small current flows for voltages threshold voltage.
- This is a small effect for a single device and will be ignored.

Problem-Solving Technique: NMOSFET DC Analysis

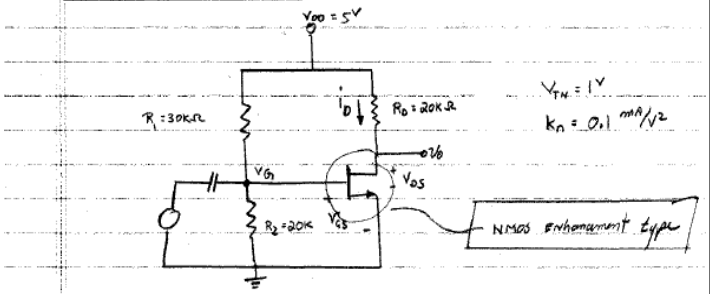
1. Assume the transistor is in saturation.
   a. $V_{GS} > V_{TN}$, $I_D > 0$, & $V_{DS} \geq V_{DS}(sat)$
2. Analyze circuit using saturation I-V relations.
3. Evaluate resulting bias condition of transistor.
   a. If $V_{GS} < V_{TN}$, transistor is likely in cutoff
   b. If $V_{DS} < V_{DS}(sat)$, transistor is likely in nonsaturation region
4. If initial assumption is proven incorrect, make new assumption and repeat Steps 2 and 3.

NMOS Common-Source Circuit



II. MOSFET DC ANALYSIS

A. Common-Source Circuit



$V_{TN} = 1^V$

$k_n = 0.1\ mA/V^2$

Find I_D, V_{DS}.

① $V_G = V_{GS} = \left(\frac{R_2}{R_1+R_2}\right)V_{DD} = \left(\frac{20}{20+30}\right)5 = 2^V$

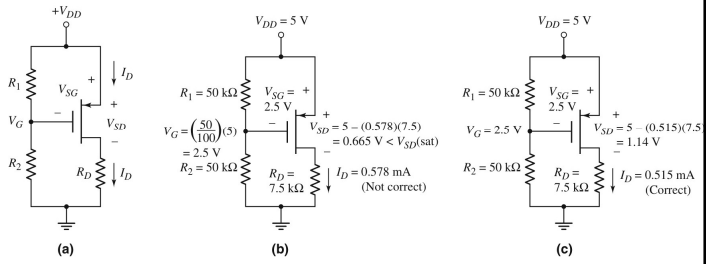
② Assuming transistor biased in SAT Region:

$I_D = k_n(V_{GS}-V_{TN})^2 = (0.1)(2-1)^2 = 0.1\ mA$

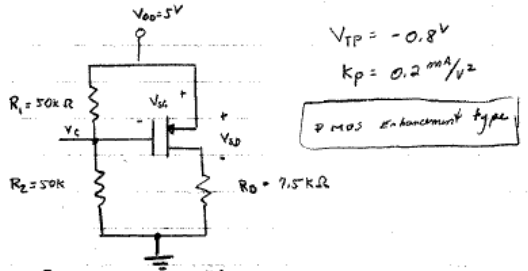
$V_{DS} = V_{DD} - I_D R_D = 5 - (0.1)(20) = 3^V$

Since: $V_{DS} = 3^V > V_{DS(SAT)} = V_{GS} - V_{TN} = 2-1 = 1^V$, the MOSFET is indeed Biased in SAT REGION.

PMOS Common-Source Circuit



Ex #2



$V_{TP} = -0.8^V$

$k_p = 0.2\ mA/V^2$

$V_G = 5\left(\frac{R_1}{R_1+R_2}\right) = 5\left(\frac{50}{100}\right) = 2.5^V$

$V_{SG} = V_{DD} - V_G = 5 - 2.5 = 2.5^V$

Assuming SAT: $I_D = k_p (V_{SG} + V_{TP})^2 = 0.2^{mA} (2.5 - 0.8)^2$

$= 0.578\ mA$

Then: $V_{SD} = V_{DD} - I_D R_D = 5 - (0.578^{mA})(7.5k) = 0.665^{V}$

Note: $V_{SD} = 0.665^{V} < V_{SD(SAT)} = V_{SG} + V_{TP} = 2.5 - 0.8 = 1.7^{V}$

∴ NOT BIASED in SAT Region !

$I_D = k_p [2 (V_{SG} + V_{TP}) V_{SD} - V_{SD}^2]$ ← Use Non Sat. EQN.

$V_{SD} = V_{DD} - I_D R_D$

$I_D = k_p [2(V_{SG} + V_{TP})(V_{DD} - I_D R_D) - (V_{DD} - I_D R_D)^2]$

$I_D = 0.2^{mA} [2(2.5 - 0.8)(5 - I_D(7.5k)) - (5 - I_D(7.5k))^2]$

$= 0.2^{mA} [17 - I_D(25.5k) - (25 + I_D^2(56.25\times10^4) - (75k) I_D)]$

$5k\, I_D = I_D(75k - 25.5k) - I_D^2(56.25\times10^4) \cdot 8$

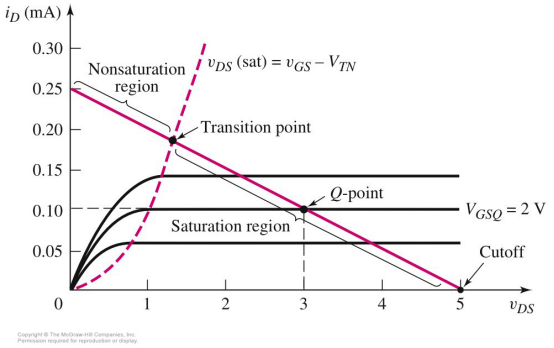
$56.25\times10^{6}\, I_D^2 - 44.5k\, I_D = 8$

$I_D = 0.515\ mA$ or $0.276\ mA$

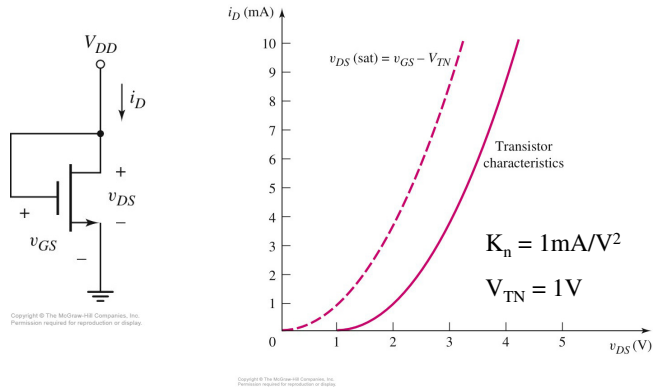
∴ $V_{SD} = 5 - (0.515)7.5 = \boxed{1.14^{V}} < V_{SD(SAT)} = 1.7^{V}$ ← correct solution

note: $V_{SD} = 5 - (0.276)7.5 = 2.93^{V} > V_{SD(SAT)}$ ← Not correct solution

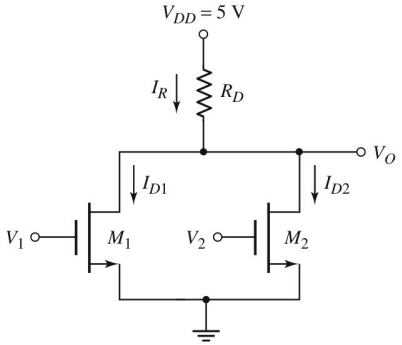
Load Line and Modes of Operation: NMOS Common-Source Circuit



Enhancement Load Device

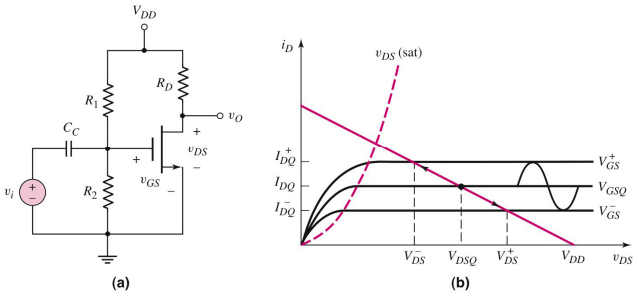


2-Input NMOS NOR Logic Gate



V_1 (V)	V_2 (V)	V_O (V)
0	0	High
5	0	Low
0	5	Low
5	5	Low

MOS Small-Signal Amplifier



Cross Section of n-Channel Junction Field Effect Transistor (JFET)