Serial I/O

ELEC 330

Digital Systems Engineering

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Images Courtesy of Ramesh Gaonkar and Delmar Learning

THE CITADEL
DEPARTMENT OF ELECTRICAL & COMPUTER ENGINEERING

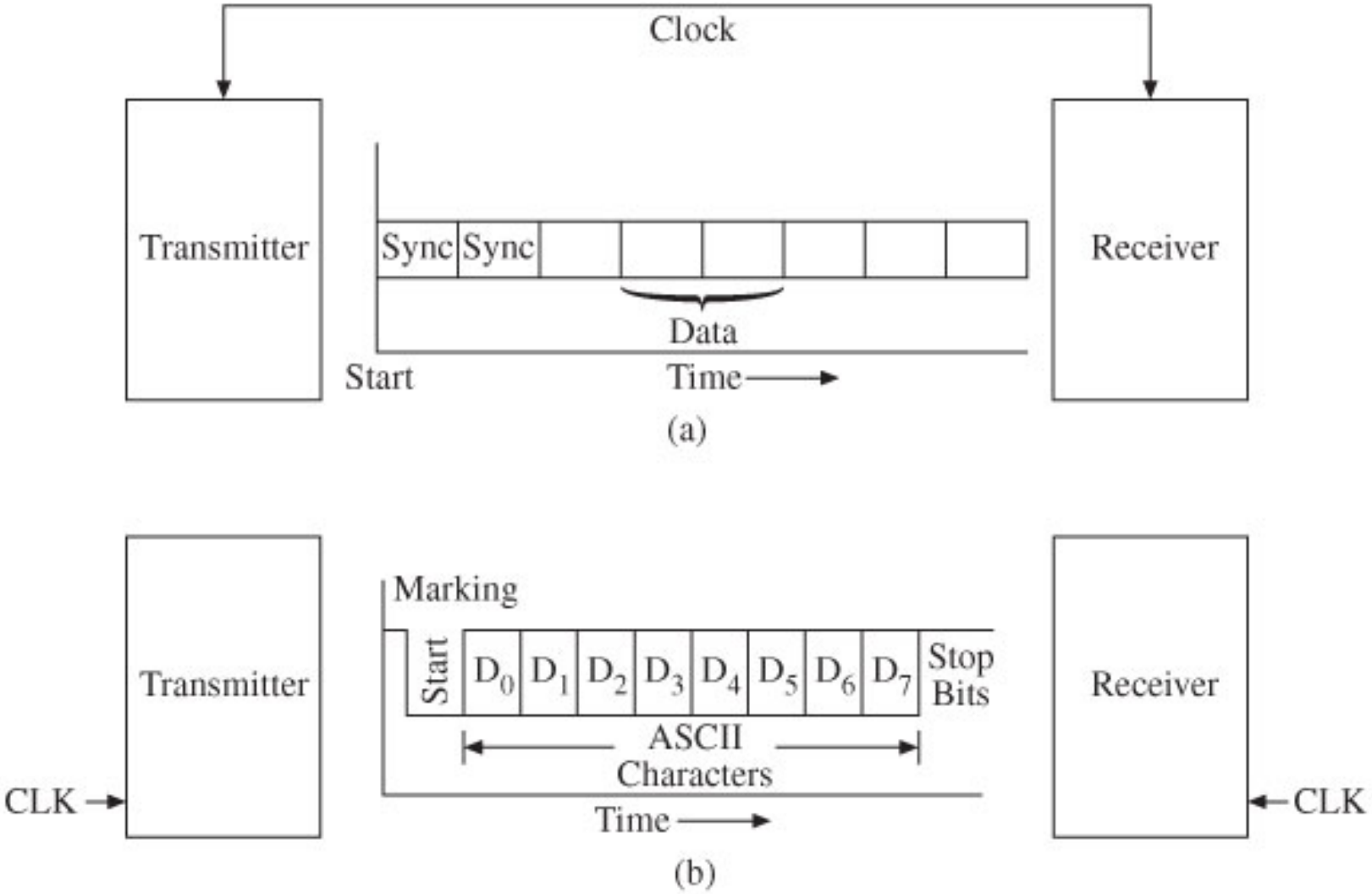
Serial I/O

- Serial I/O (Communication)
  - One bit transferred at a time
  - Over one line
- To transmit data serially
  - Microcontroller must convert its parallel word into a stream of serial bits
    - Parallel-to-serial conversion
- To receive data serially
  - Microcontroller must convert a stream of serial bits into a parallel word
    - Serial-to-parallel conversion

Basic Concepts

- Transmission issues
  - Synchronous vs Asynchronous
  - Simplex vs Duplex
  - Data Rate
  - Errors and Error Checks
  - Standards and Protocol

Synchronous vs Asynchronous



Simplex vs Duplex

- Simplex
  - Data flow in only one direction
    - Such as from a PC to its peripheral
- Full duplex
  - Data flow in both directions simultaneously
    - Such as a telephone conversation or communication via a modem
- Half duplex
  - Data flow in both directions, only one direction at a time
    - Such as a conversation over a CB radio

Rate of Transmission

- Baud and bits per second (BPS)
  - Baud is a measure of the "signaling rate"
    - Number of changes to the transmission medium per second in a modulated signal
  - At slow speeds
    - Only one bit of information is encoded in each electrical change
    - Baud and bits per second are equal
  - At higher speeds
    - Multiple bits are encoded in one electrical change
    - Generally expressed in bits per second (bps)

Transmission Errors

- Framing error
  - Start and Stop bits improperly frame a character
  - Recognized when the Stop bit is zero
    - Expected to be one
  - Flag in control register
- Overrun error
  - New byte overwrites the earlier byte
    - Before the receiver completes reading
  - Flag in control register

Error Checks

- Parity
  - Last bit is used as a parity bit
  - Either an even or odd number of 1s
- CheckSum
  - Used when blocks of data are transmitted
  - All bytes transmitted are XORed
    - Sent as the last byte
- Receiver recalculates Parity or CheckSum
  - Compares to the one transmitted
  - No match generates an error

Standards and Protocols

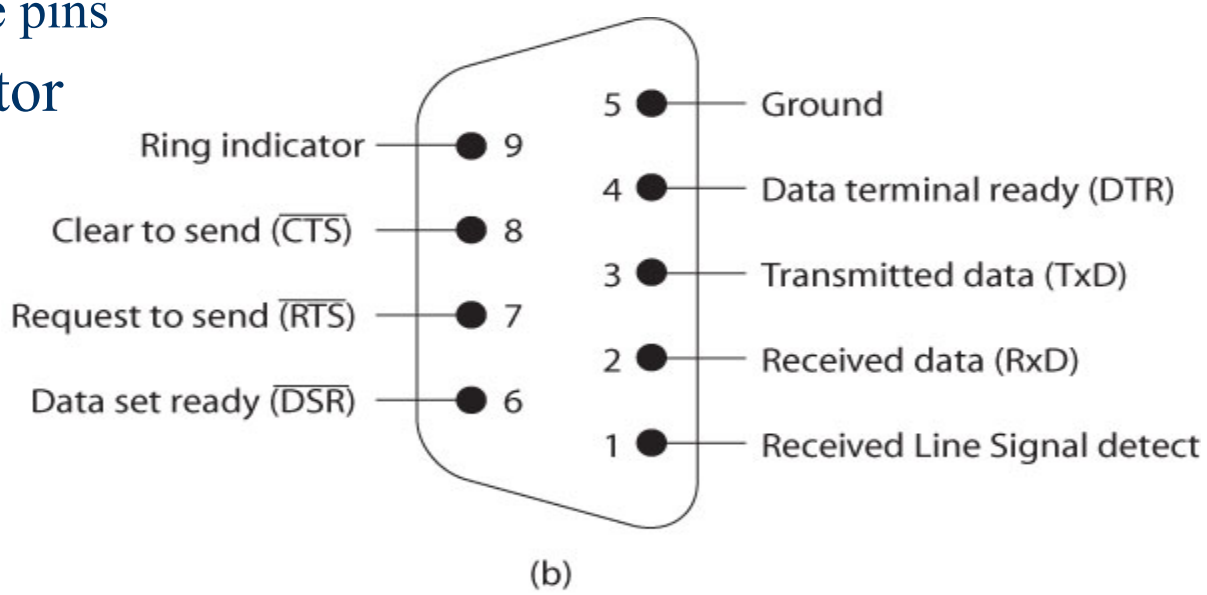
- EIA-232 (formerly known as RS-232)
- Serial Peripheral Interface (SPI)
- Inter-Integrated Circuit (I^2C)
- One-wire (1-Wire®) Bus
- Controller Area Network Bus (CAN)
- Local Interconnect Network (LIN)

PIC18 Serial Communications

- Includes two serial communication modules
  - Universal Synchronous Asynchronous Receiver Transmitter (USART)
    - Implements EIA-232
    - Also known as Serial Communications Interface (SCI)
  - Master Synchronous Serial Port (MSSP)
    - Also known as Serial Peripheral Interface (SPI)
    - Also implements I^2C mode

EIA-232 Serial I/O Standard

- Negative logic
  - Logic 1: –3 V to –25 V or Mark
  - Logic 0: +3 V to + 25 V or Space
- Connector
  - DB25 subminiature
    - Twenty-five pins
  - DB9 connector
    - Nine pins



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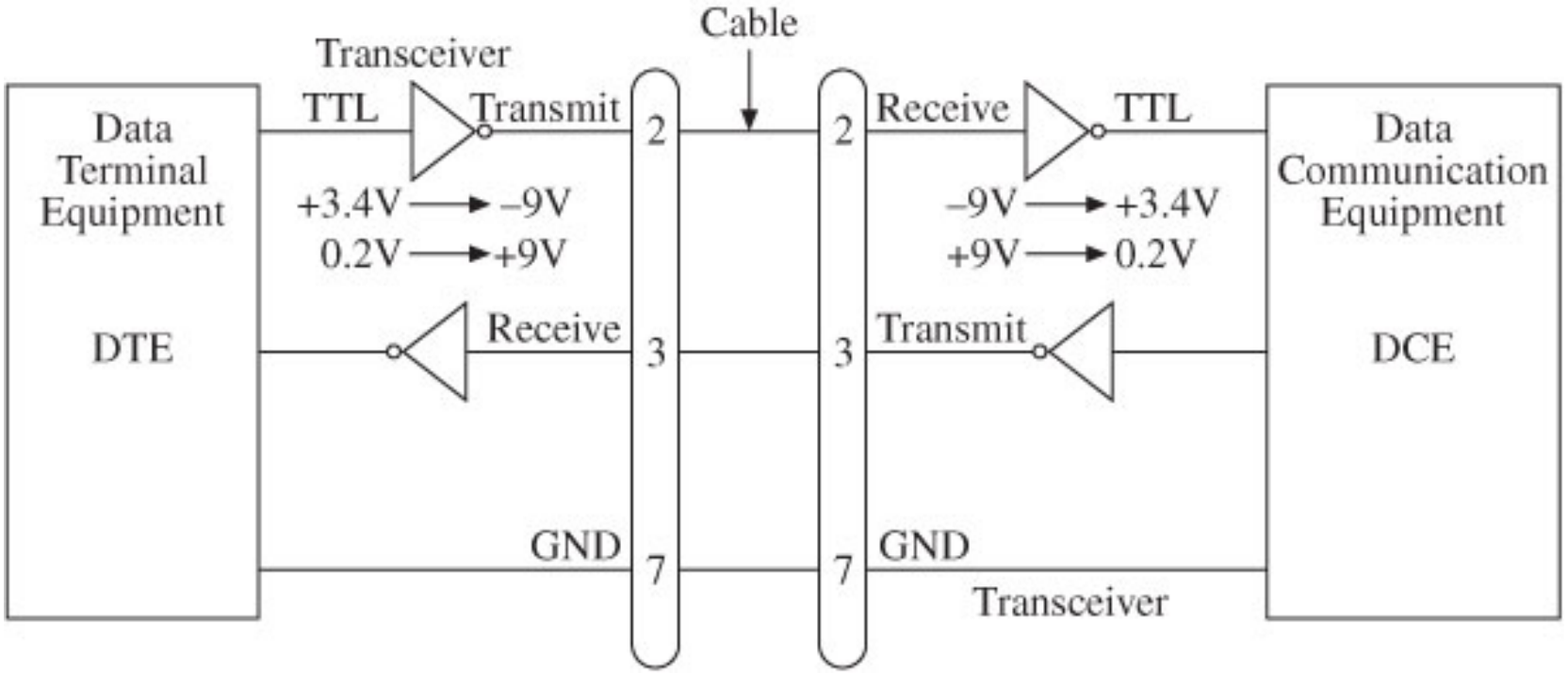
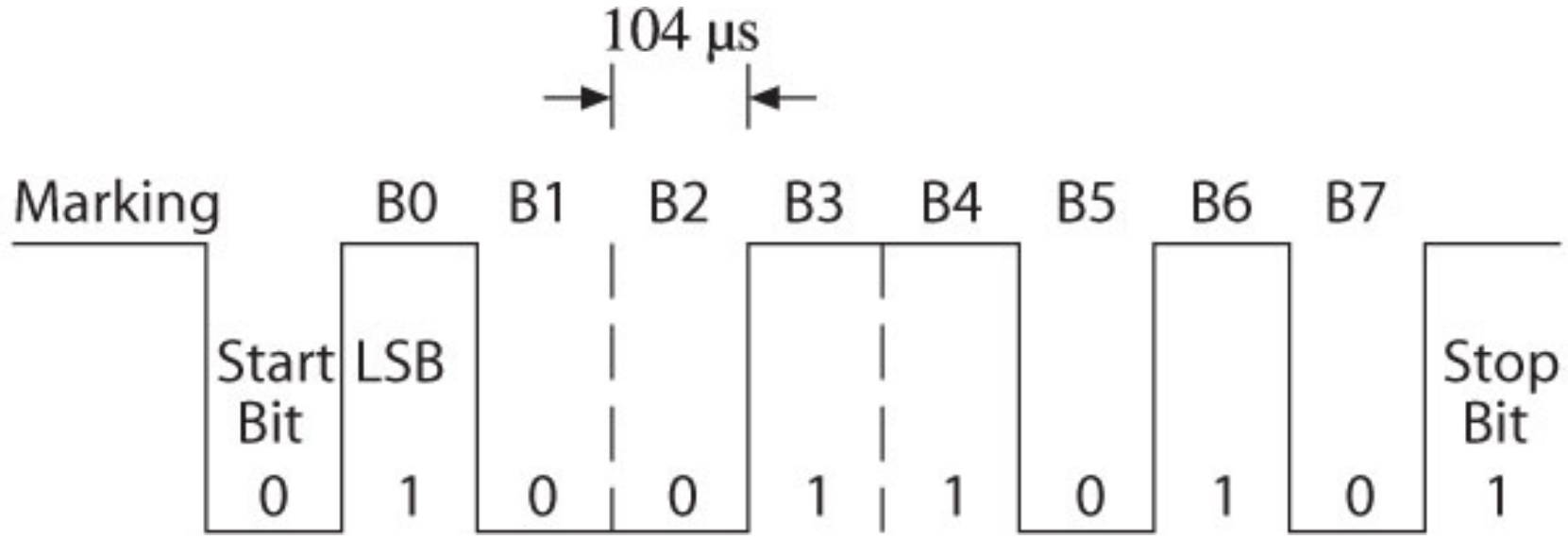
EIA-232 Serial I/O Standard

- EIA 232 DTE and DCE Minimum Connection



Framing

- ASCII Character Y (59H) – 9600 BAUD



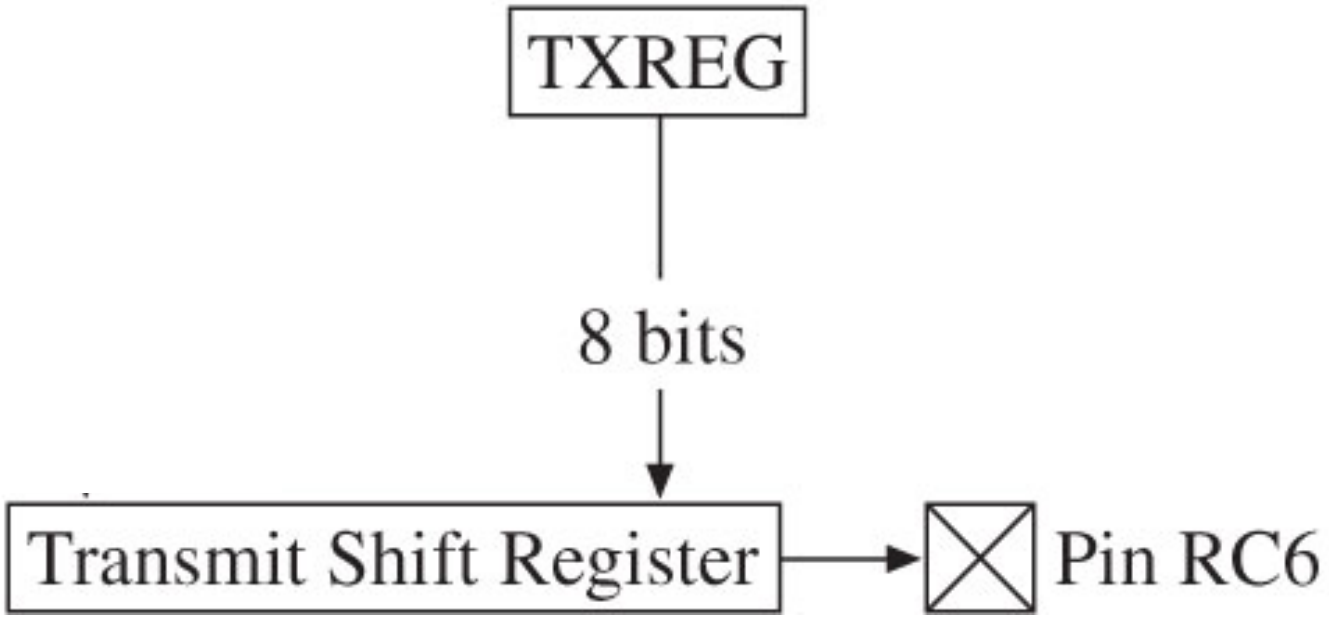
PIC18 USART Module

- Configuration Modes
  - Asynchronous
    - Full duplex
    - PC serial communication
      - EIA-232 protocol
  - Synchronous
    - Master or slave half duplex
    - Used to communicate with peripherals
      - A/D and D/A converters
      - Serial EEPROM

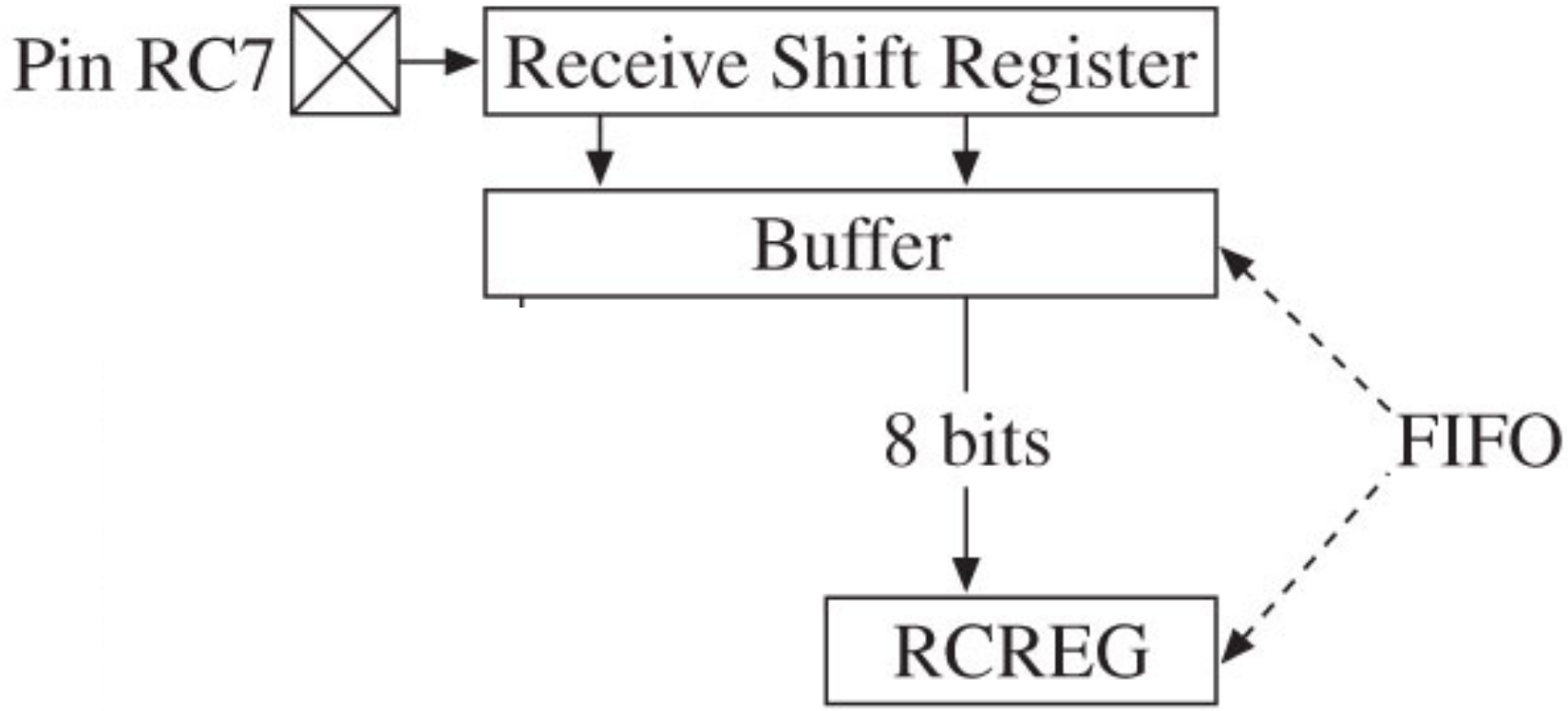
PIC18 USART Module

- Control Registers
  - SPBRG
    - Baud Rate Generator
  - TXSTA
    - Transmit Status and Control
  - RCSTA
    - Receive Status and Control
  - BAUDCON
    - Baud Rate Control

USART Transmission



USART Reception



Interrupts

- PIE1
  - TXIE (Bit4)
    - Transmit Interrupt Enable
  - RCIE (Bit5)
    - Receive Interrupt Enable
- PIR1
  - TXIF (Bit4)
    - Transmit Interrupt Flag
      - Bit is 1 when TXREG (Transmit Register) is empty
  - RCIF (Bit5)
    - Receive Interrupt Flag
      - Bit is 1 when RCREG (Receive Register) is full

Master Synchronous Serial Port

- Master Synchronous Serial Port (MSSP)
  - Serial interface used in communicating with other peripheral devices
- Can operate in one of two modes
  - Serial Peripheral Interface (SPI)
  - Inter-Integrated Circuit (I^2C)

Serial Peripheral Interface (SPI)

- Serial synchronous data exchange protocol
  - High-speed serial communication
    - Between a microcontroller and its peripheral devices
    - Between a master and a slave device
    - EEPROMs, data converters, and display drivers
  - Four-wire Interface
    - Clock, data in, data out, and slave select
  - Synchronous protocol
    - Clock signal is provided and controlled by the master device
  - Master-Slave protocol
    - Can communicate with multiple slave devices
  - Data Exchange protocol
    - Each device has two data lines

MSSP: SPI Mode

- Transmits and receives data simultaneously
- Uses following pins
  - Serial Data Out (SDO)
    - pin RC5/SDO on PORTC
  - Serial Data In (SDI)
    - pin RC4/SDI/SDA on PORTC
  - Serial Clock (SCK)
    - pin RC3/SCK/SCL on PORTC
  - Slave Select (/SS)
    - Available pin on a PORT
- Internal Registers
  - SSPSR (Shift Register)
  - SSPBUF (Buffer Register)

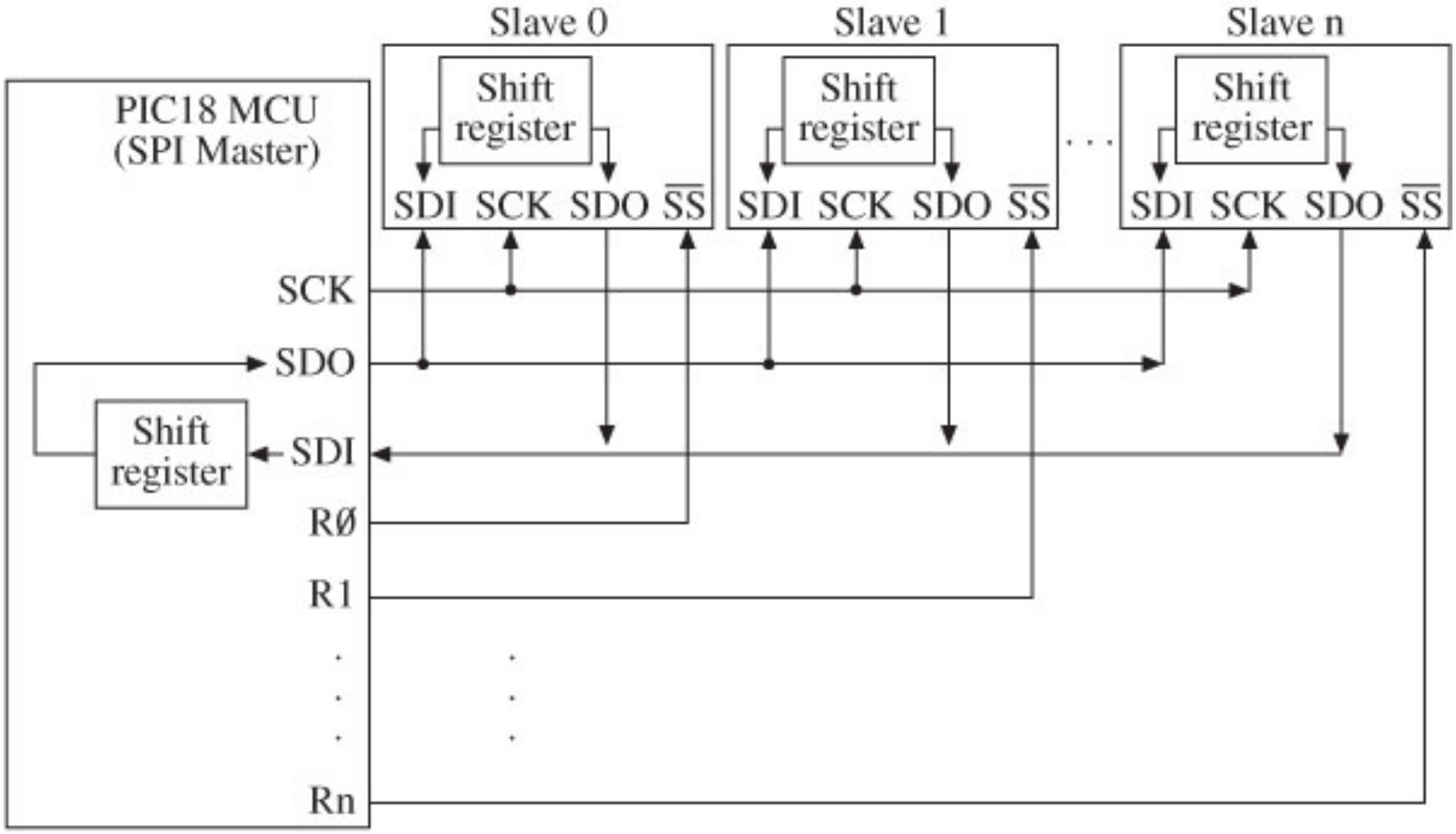
SPI Mode

- Write and Read operations
  - Must be performed for each byte
    - Some of data bytes may not have any use in a given application
  - Transmission
    - Master sends data and receives dummy data from slave device
  - Transmission and Reception
    - Both exchange data
  - Reception
    - Master receives data and sends dummy data to slave device

SPI Applications

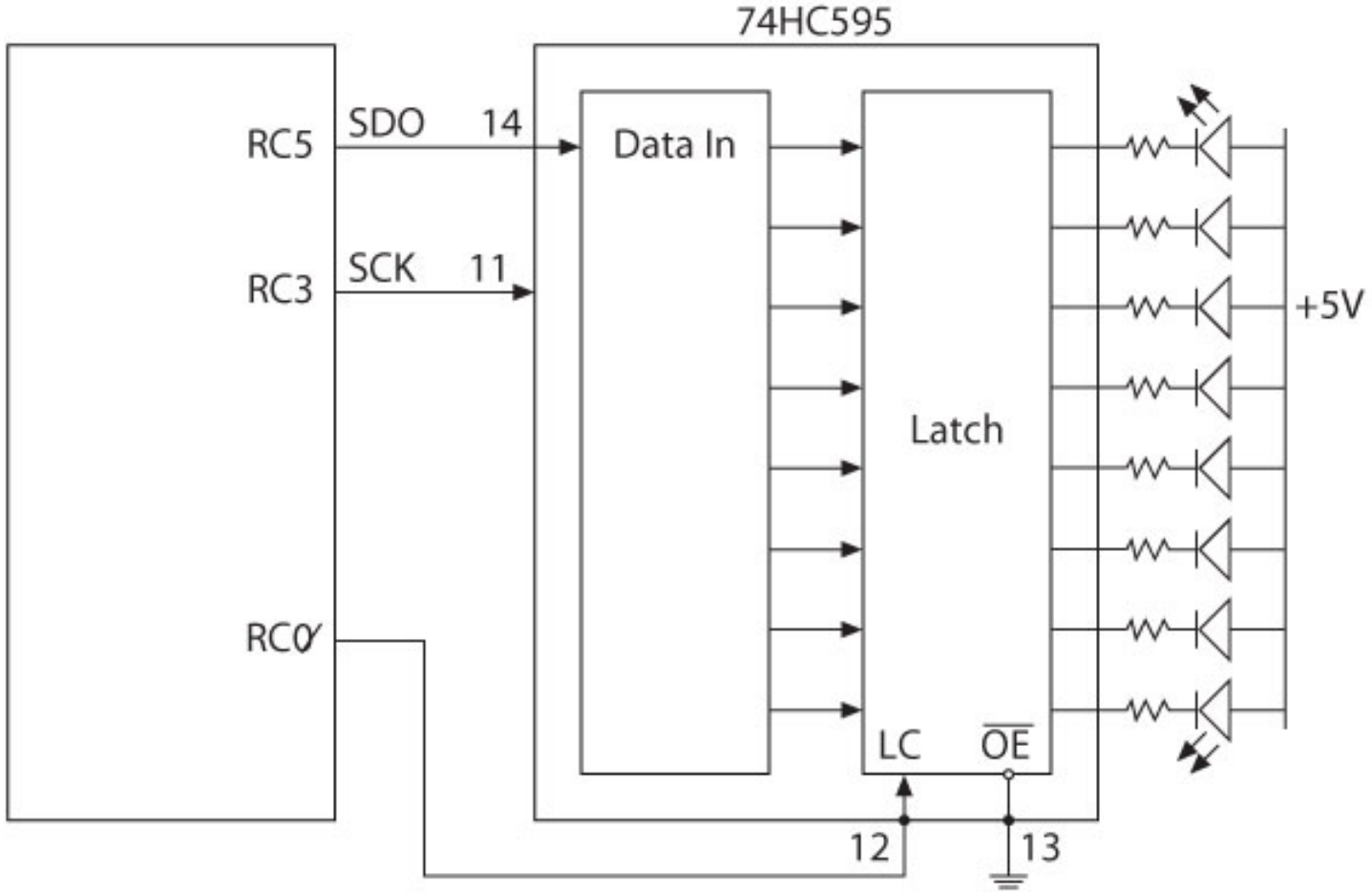
- SPI-compatible peripherals include
  - Converters (ADC and DAC)
  - Memories (EEPROM and Flash)
  - Sensors (temperature and pressure)
  - Real Time Clock (RTC)
  - Display (LCD)
  - Shift registers
- Master-slave configuration
  - One master device and multiple slave devices

Master and Multiple Independent Slave Connection



Example

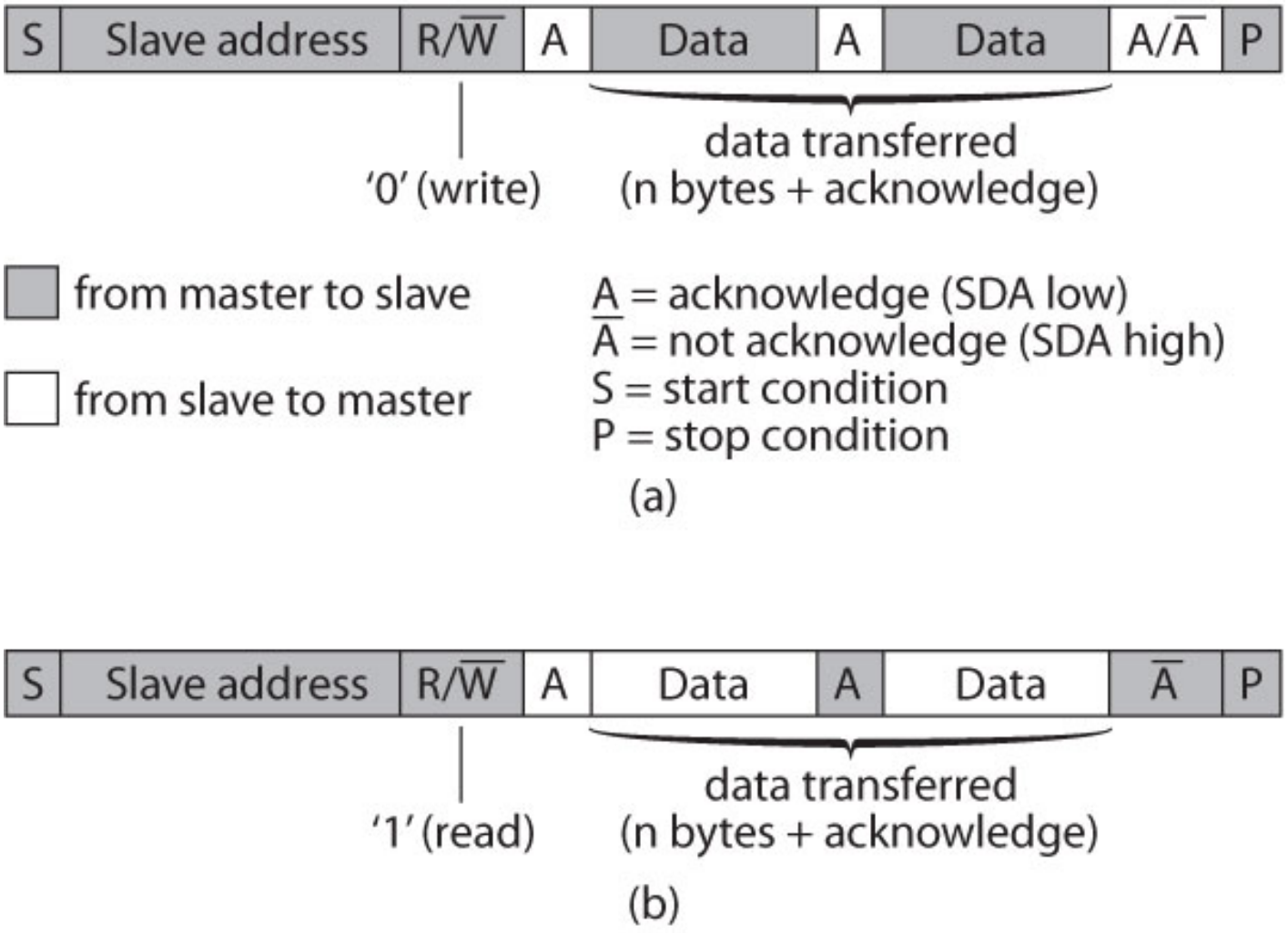
- Interfacing 74HC – Shift Register in SPI Mode



Inter-integrated Circuit Protocol

- Inter-integrated Circuit (I^2C)
  - Two-wire interface
    - Two open drain/collector lines
    - One for clock and one for data
  - Synchronous
    - Data are transferred with a synchronous clock initiated by the master device
    - Rate of data transfer is 100 kbps in standard mode
      - 400 kbps in fast mode
  - Master/Slave or Many Masters
    - Bus may have one master and many slaves or multiple masters

I²C Protocol



MSSP: I²C Mode

- Implements all master and slave functions
  - Provides interrupts on Start and Stop bits
- Uses the following pins
  - SCL (Serial Clock)
    - pin RC3/SCK/SCL on PORTC
  - SDA (Serial Data)
    - pin RC4/SDI/SDA on PORTC
- Internal Registers
  - SSPSR (Shift Register)
  - SSPBUF (Buffer Register)
  - SSPADD (Address Register)