ELEC-313
Lab 9: Common-Emitter Transistor Amplifier

December 3, 2013

Date Performed: November 20, 2013
Partners: Charles Pittman
Stephen Wilson

1 Objective

The objective is to construct and observe the operation of a common-emitter transistor amplifier.

2 Equipment

Transistor: 2N2222A	Capacitor: 0.1 µF
Resistors: 100 kΩ, 20 kΩ, 1 kΩ, 470 Ω	Power supply: HP E3631A
Function generator: HP 33120	Oscilloscope: Agilent 54622D
Multimeters: HP 34401A, Fluke 8010A (x2)	

3 Schematics

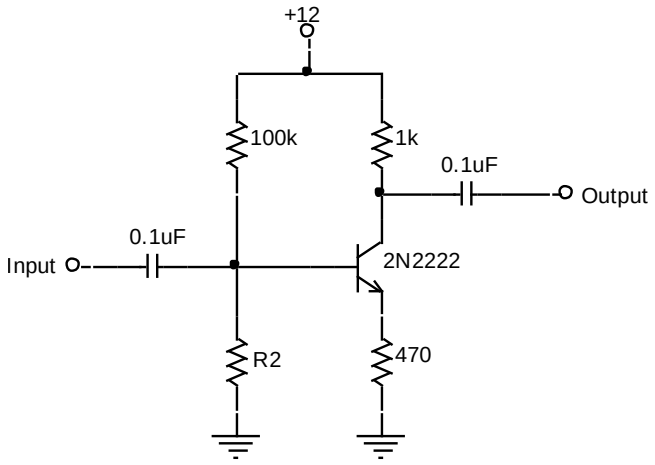

Figure 1: Common-emitter transistor amplifier (without the emitter bypass capacitor). $R_2 = 20\,\text{k}\Omega$

4 Procedure

The following procedure was used to evaluate the transistor amplifier of Figure 1:

1. The circuit of Figure 1 was constructed.
2. The DC voltage at each terminal of the transistor was measured and the values were recorded in Table ??.
3. The output of the function generator was connected to the input of the circuit. Then the function generator was set to a frequency of 30 kHz as a sine wave.

4. Channel 1 of the oscilloscope was connected to the input of the circuit and channel 2 connected to the output.

5. The amplitude of the sinusoidal waveform was adjusted to -250 mV to +250 mV (500 mVpp) at the circuit input as measured on the oscilloscope.

6. The peak-to-peak amplitude of the output waveform (V_o) was measured and recorded in Table ??.

7. Then, the voltage gain (A_V) of the amplifier was computed at 30 kHz and recorded in Table ??.

8. The decade resistance box was connected to the output of the circuit. Then the resistance was adjusted until the output voltage read as one-half the open circuit value measured in step 6. The displayed resistance value, which is also equivalent to the output resistance (Ro) of the circuit, was recorded in Table ??.

9. The function generator was disconnected from the circuit input and then connected to the oscilloscope to measure the open circuit voltage (V_{OC}) produced by the generator. The open-circuit voltage was recorded in Table ??.

10. The decade box was removed from the output and reconnected between the function generator and the open circuit input, so that the signal travels from the function generator and through the resistance box on its way to the circuit input.

11. The decade resistance box was adjusted so that the voltage measured at the circuit input is one-half the open circuit voltage measured in step 9. That displayed resistance is 50 Ω less than the input resistance (R_i) of the circuit. The input resistance was recorded in Table ??.

12. The decade resistance box was removed and the function generator was reconnected directly to the circuit input, and its frequency was left at 30 kHz.

13. The amplitude of the generator was slowly increased while the output waveform was carefully observed to determine the point at which the output waveform began to clip (V_{clip}). The peak-to-peak voltage was recorded in Table ??.

14. The 10 µF emitter bypass capacitor was inserted into the circuit.

15. Steps 2 through 7 were repeated, except the input voltage was first reduced until the waveform didnt clip. The input voltage was recorded in Table ?? and the measurements from steps 2 through 7 was recorded in Table ??.

V_B (V)	V_C (V)	V_E (V)	V_i (mV)	V_o (mV)	A_V
1.788	9.58	1.153	500	970	1.94

Table 1: Transistor amplifier characteristics

R (Ω)	V_{OC} (mV)
958	477

Table 2: Port impedances

5 Results

6 Conclusion

As seen in Table X, the small signal voltage gain A_V increased once the emitter bypass capacitor was added, even though it had relatively insignificant impact to the DC voltages of each terminal. The DC voltages shouldnt change because the capacitor that was added is ideally an open circuit to the DC voltage which would offer no new path for the DC current to take. But the emitter bypass resistor has a significant impact to the AC analysis because it is seen as a closed circuit and allows the I_E to pass un-resisted through the capacitor. As seen in eq. 6, the addition of the emitter bypass capacitor, reduced the denominator of the A_V eq. 4, thus increasing gain.

Table Y shows the percent difference of the theoretical input and output impedances (R_i and R_o respectively) and the small signal gains of the circuits of Part I and Part II of the experiment which were calculated using equations 1 through 7. R_i and R_o are relatively close and the small percent differences are probably because we took the nominal resistor values instead of the measured resistor values. Experience has shown that resistors are usually slightly less than their nominal value. The 5.7 percent difference between the A_V for Part I is caused from a combination of using nominal instead of measured resistance values, and the assumptions that β was assumed to be 150 and I_{CQ} was assumed to be 3 mA (both were given in the pre lab section of the lab). I_{CQ} was probably less than 3 mA because the voltage difference between the 12 V input (see Figure ??) and the 9.547 VC terminal (see Table ??) divided by the 1 kΩ resistor would have generated a smaller current than 3 mA. Their is sig-

R (kΩ)	V_i (V)
13.9	2.57

Table 3: Large-signal performance

V_B (V)	V_C (V)	V_E (V)	V_i (V)	V_o (V)	A_V
1.783	9.547	1.164	0.122	6.19	52.0

Table 4: Transistor amplifier characteristics (with emitter bypass capacitor)

nificant percent difference between the theoretical A_V versus the measured A_V in Part II. Eq. 6 shows that the calculcated A_V is more effected the I_{CQ} value, which as explained earlier was probably less than the assumed 3 mA. Also, the assumption that r_o is infinite and therefore an open circuit is not totally true (which was the assumption made in when calculating the theoretical voltage gain). The resistance of r_o in parallel with RC this would actually have been slightly less than the R_o used in the theoretical calculations. Also, we could have accidentally not reduced the voltage enough such that it was clipped as described in step 15.

Table Y shows the V_{OC} recorded during step 9. It is less than 500 mV probably because of noise could have affected the output reading. The table also shows the V_{clip}, which is the point at which the output voltage began to clip (see step 13). This clipping of the voltage happens when the transistor is saturated in which the current cannot go any higher.

7 Equations