1. Design a floating-point multiplier which uses the IEEE single precision floating-point format. Ignore special cases other than 0 and truncate the result.

a) Draw a block diagram for the multiplier showing the necessary registers and control signals.
b) Draw the SM Chart for the control circuit.
c) Write a complete VHDL model for the multiplier (use two processes).
d) Simulate for the following test data (using a testbench):

25.25 x -2.5 = -63.125
0 x 25.25 = ?
-7.5 x -7.5 = ?

Hints:

- The controller needs to handle FZ, FV, and EV (but not Fnorm).
- The fractions are unsigned (not 2's complement) multiplication. The sign bits are handled separately.
- Use the + and * operators to implement the exponent adder and fraction multiplier
  - `addout <= ('0' & E1) + ('0' & E2) - bias;`
  - `multout <= ('1' & F1) * ('1' & F2);`