ELEC-311
Project 3
Adder-Subtractor

Charles Pittman

October 28, 2013

1 Objective

- Given a function, design a combinational logic logic circuit.

- Minimize the circuit using a Karnaugh map.

- Create the circuit using only NAND gates.

2 Discussion

The circuit to be constructed was a 2-bit comparator. A 2-bit comparator takes two 2-bit numbers, $P = P_1 P_0$ and $Q = Q_1 Q_0$, and produces an output, $GT = 1 \iff P > Q$. The truth table describing this function is shown in Table 1. This can be displayed more concisely as a summation of min-terms: $\sum_m (P_1, P_0, Q_1, Q_0) = (4, 8, 9, 12, 13, 14)$.

Using a Karnaugh map (Fig **??**), a minimal form of the function was found: $GT = P_0 \overline{Q_1} \overline{Q_0} + P_1 P_0 \overline{Q_0} + P_1 \overline{Q_1}$. This function was then translated into the circuit shown in Fig **??**.

The NAND gate is considered to be a functionally complete set because any logic function can be created with only NAND gates. This is demonstrated graphically in Figure **??**. Using these conversions, the circuit was again translated into one using only NAND gates (Fig **??**), and truth table verified (not shown).

3 Results

X	Y	X	Y	X + Y	X - Y
3	1	0011	0001	0100	0010
1	5	0001	0101	0110	1100
-2	3	1110	0011	0001	1011
-2	-4	1110	1100	1010	0010
4	6	0100	0110	01010	1110

Table 1: Truth table for 2-bit comparator.