ELEC-311
Project 2
Combinational Circuit Design

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October 1, 2013

1 Objective

First Objective
Given a function, design a combinational logic logic circuit.

Second Objective
Minimize the circuit using a Karnaugh map.

Third Objective
Create the circuit using only NAND gates.

2 Discussion

The circuit being studied is shown in Figure **??**. Working from right to left, the Boolean equation for the circuit can be written: $(\overline{S} \cdot I_0 + I_1) \cdot E \cdot (I_0 + S \cdot I_1)$. A truth table for this equation is shown below.

After sketching the circuit with the Xilinx schematic capture, the logic was translated to run on a Basys2 (field-programmable gate array (FPGA) board used). Switches on the board were used to input a string of bits, with an LED showing the function's result.

P1	P0	Q1	Q0	GT
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

Table 1: Truth table for circuit in Figure **??**

3 Results

To verify the FPGA's configuration, each entry from the truth table was input and the output confirmed to match the expected value. As an additional

exercise, the circuit was simplified with Boolean algebra, and tested as above. The simplified circuit is shown in Figure **??**. The truth table, shown below, is identical since the two circuits are equivalent.

I_0	E	I_1	S	Z	I_0	E	I_1	S	Z
0	0	0	0	0	1	0	0	0	0
0	0	0	1	0	1	0	0	1	0
0	0	1	0	0	1	0	1	0	0
0	0	1	1	0	1	0	1	1	0
0	1	0	0	0	1	1	0	0	1
0	1	0	1	0	1	1	0	1	0
0	1	1	0	0	1	1	1	0	1
0	1	1	1	1	1	1	1	1	1

Table 2: Truth table for circuit in Figure **??**