1. Given a rising-edge triggered T flip-flop with an active-low asynchronous clear, a clock with a 20 ns period, and zero initial values for all signals: draw a timing diagram showing all inputs and outputs for 100 ns using the following input sequence.

	5ns	15ns	25ns	35ns	45ns	55ns	65ns	75ns	85ns	95ns
ClrN	0	1	1	1	0	1	1	1	1	1
T	0	0	1	0	0	1	0	1	1	0

2. Design a 3-bit left-shift register with the following functions:

Ld	Sh	Fn
0	0	Hold
0	1	Shift
1	X	Load

a. Draw the circuit using D flip-flops and multiplexers.
b. Write the next-state equations for the flip-flops.

3. Design a synchronous circuit that implements a 4-bit decade (modulo-10) counter (0000, 0001, … , 1001, 0000, …):
a. Fill in a transition table (using don't cares for undefined next states).
b. Minimize the next state (D FF) equations using Karnaugh maps.