Introduction

ELEC 418

Advanced Digital Systems

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Images Courtesy of Thomson Engineering

THE CITADEL

DEPARTMENT OF ELECTRICAL & COMPUTER ENGINEERING

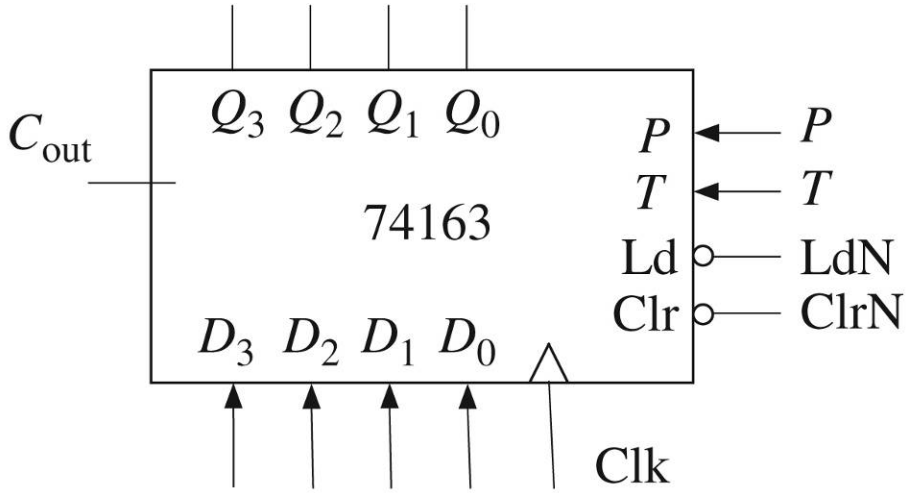
Admin

- Course materials available online
- http://ece.citadel.edu/hayne/
  - Students are encouraged to print lecture slides in advance and use them to take notes in class

Homework

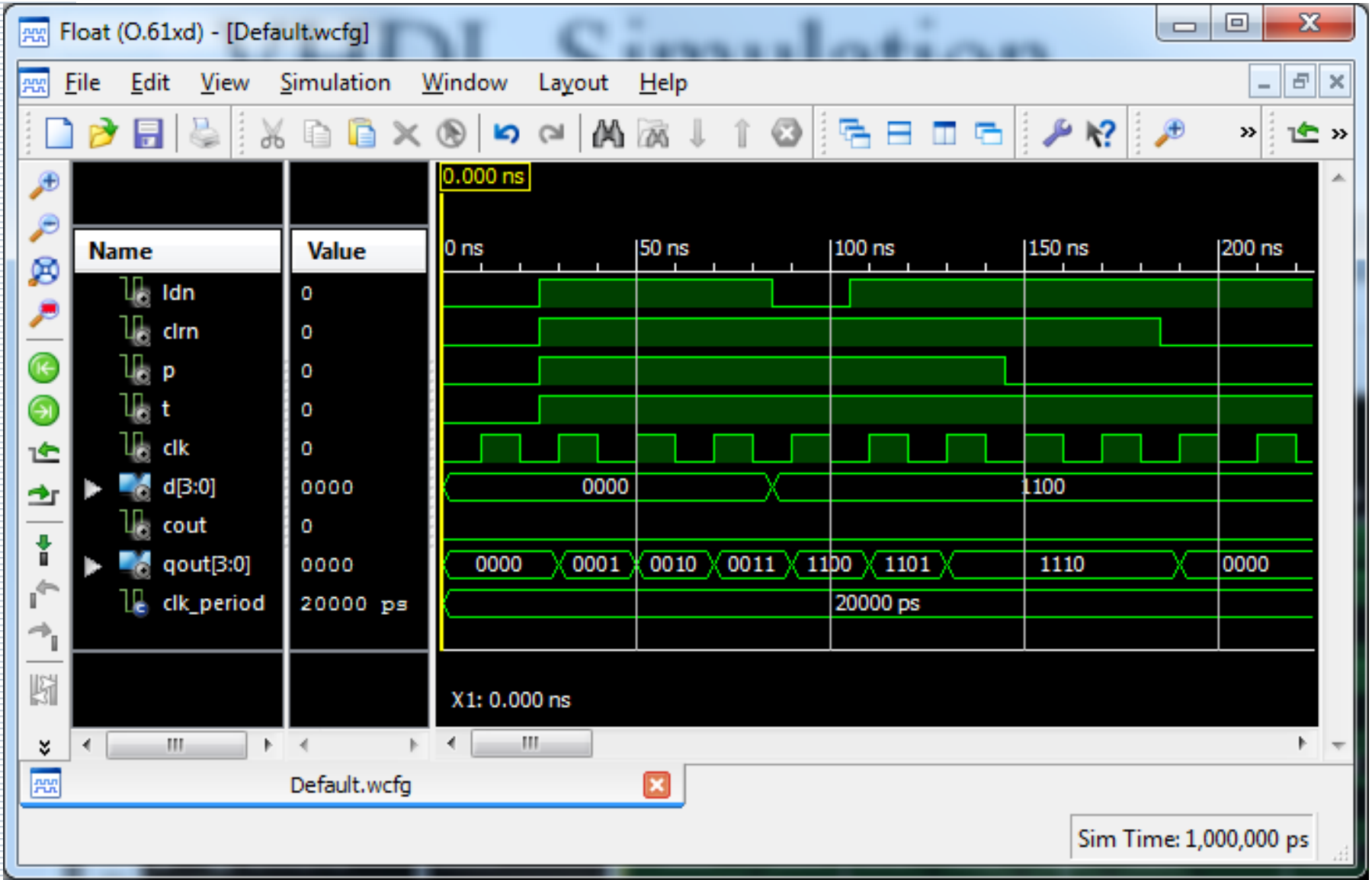
- Xilinx ISE
  - Xilinx ISE WebPACK VHDL Tutorial
    - Review from ELEC 311
      - Up to UCF File Creation
  - Xilinx ISE Simlulator (ISim) Tutorial
    - VHDL Simulator for ELEC 418
    - Will Need for Project 1

VHDL Counter Example

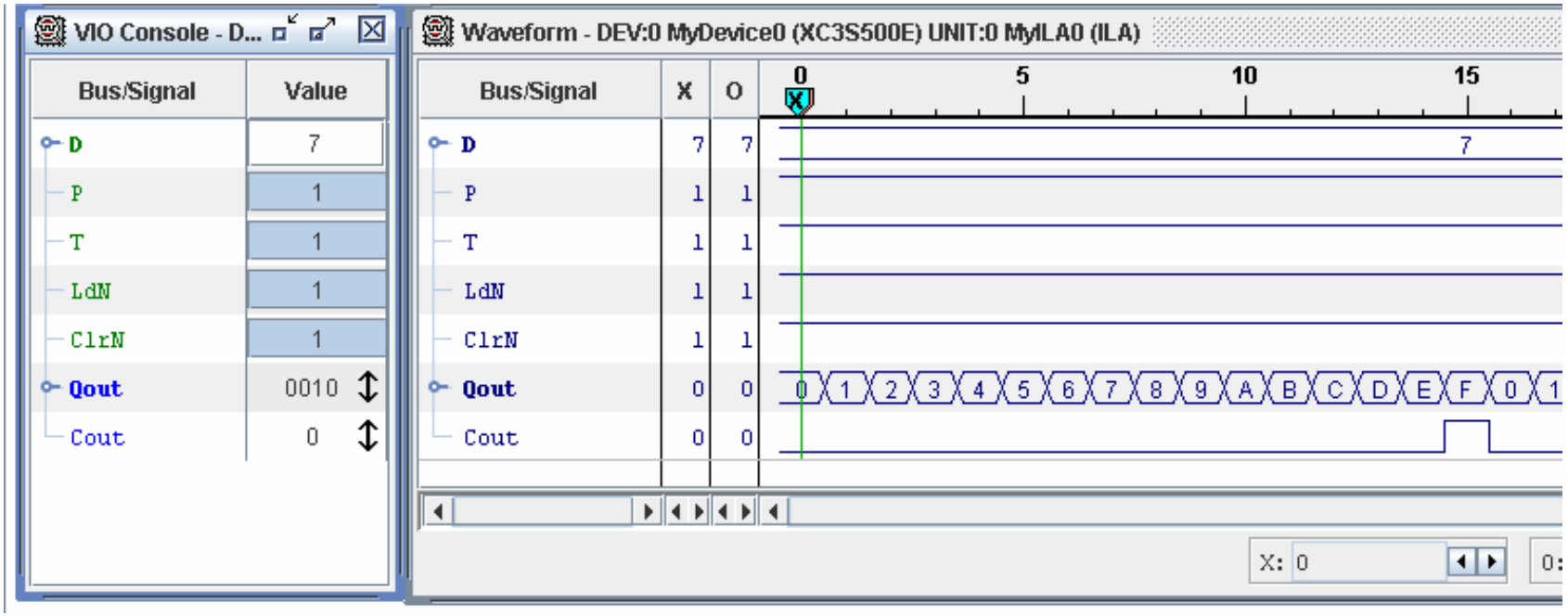


Control Signals			Next State				
ClrN	LdN	PT	Q_3^+	Q_2^+	Q_1^+	Q_0^+	
0	X	X	0	0	0	0	(clear)
1	0	X	D_3	D_2	D_1	D_0	(parallel load)
1	1	0	Q_3	Q_2	Q_1	Q_0	(no change)
1	1	1	present state + 1				(increment count)

VHDL Simulation (ISim)



Hardware Demonstration



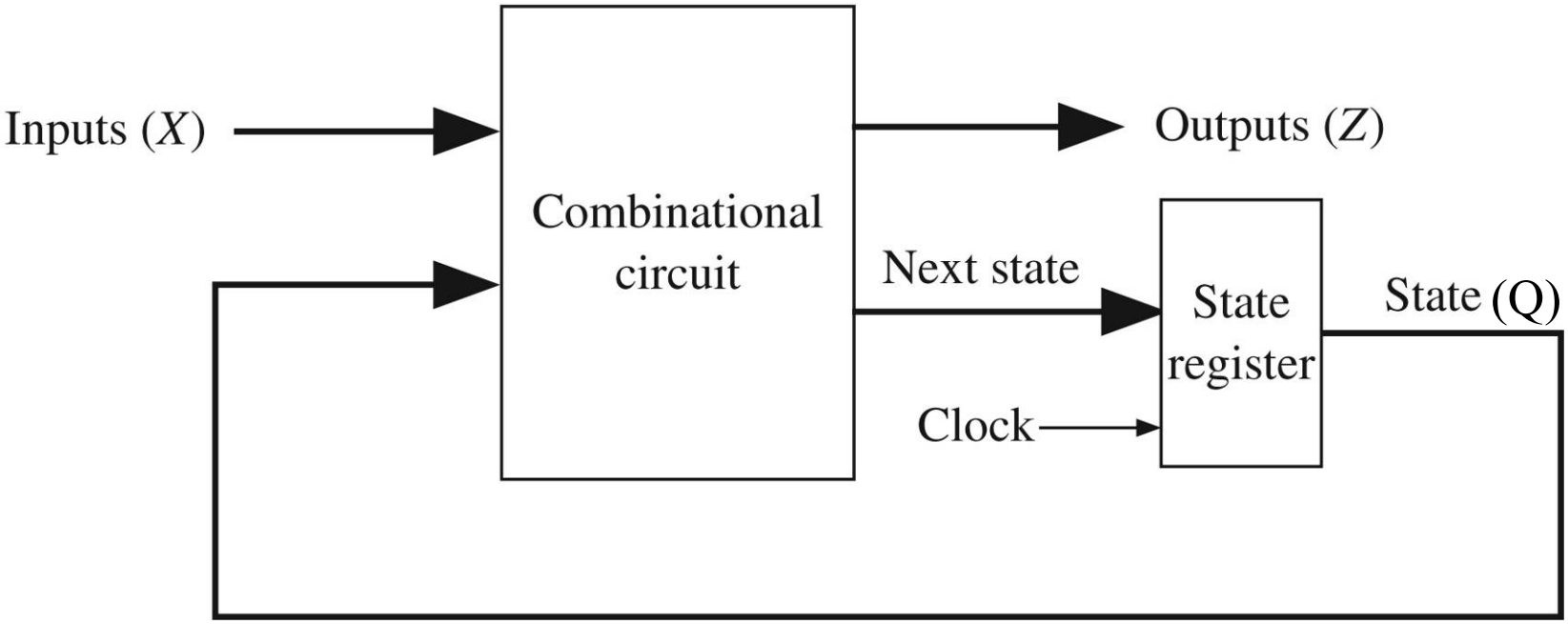
Questions?

Review of Logic Design

- Chapter 1
  - Combinational Logic
  - Boolean Algebra
  - Flip-Flops and Latches
  - Sequential Circuit Design
  - Tristate Logic and Busses

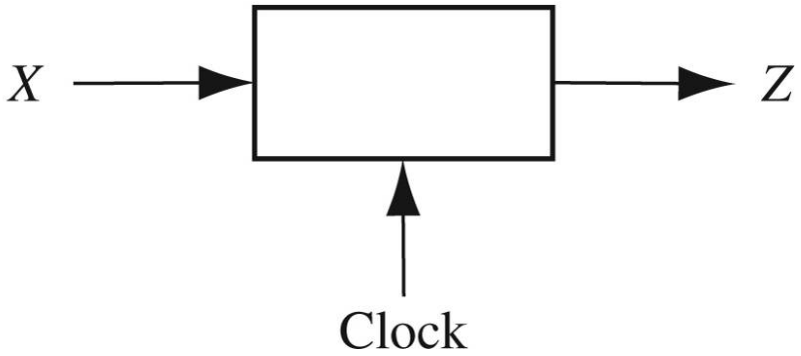
Sequential Circuit Design

- Moore
  - $Z = f(Q)$
- Mealy
  - $Z = f(X, Q)$



Design Example

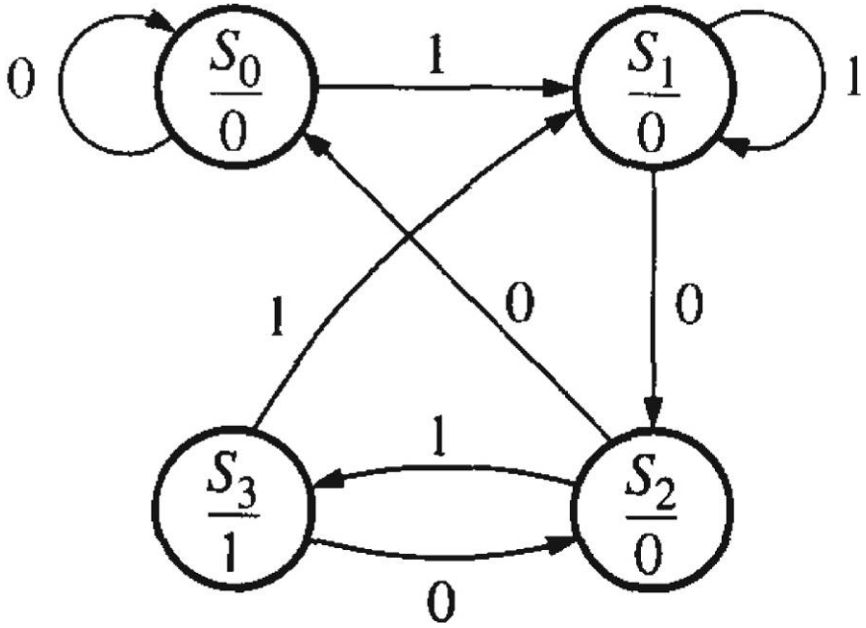
- Sequence Detector
  - The circuit will examine a string of 0's and 1's applied to the X input and generate an output Z = 1 only when the input sequence ends in 1 0 1



  - Typical Sequence

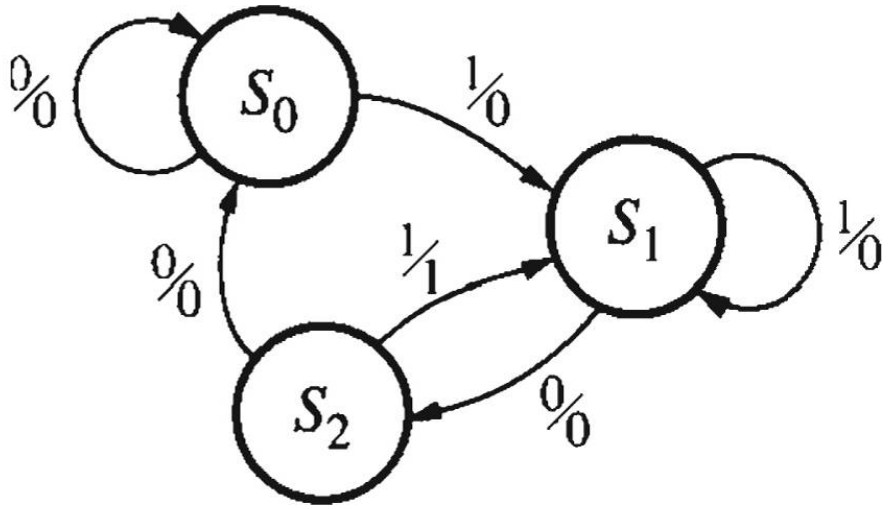
```
X = 0 0 1 1 0 1 1 0 0 1 0 1 0 1 0 0
Z = 0 0 0 0 0 1 0 0 0 0 0 1 0 1 0 0
```

Moore State Graph & Table



Present State	Next State $X = 0$	Next State $X = 1$	Present Output (Z)
S_0	S_0	S_1	0
S_1	S_2	S_1	0
S_2	S_0	S_3	0
S_3	S_2	S_1	1

Mealy State Graph & Table



Present State	Next State $X=0$	Next State $X=1$	Present Output $X=0$	Present Output $X=1$
S_0	S_0	S_1	0	0
S_1	S_2	S_1	0	0
S_2	S_0	S_1	0	1

Summary

- Admin
  - Course Outline
  - Grading
  - Homework
- Review of Logic Design
  - Sequential Circuit Design