# Chapter 5: Fabrication

ELEC 424

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# Another Look at Fabrication

- Back End Basics
  - Test
  - Packaging
- Packaging and Interconnect
- IC Resistors

# Back End Basics

- Two Major Components
  - Test
  - Packaging
- Silicon Run II

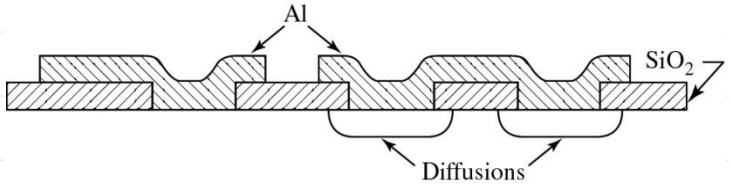
# Testing

- Wafer-, Packaged Device- and System-Level
- Wafer Level
  - Go-No Go
  - Very Limited Functionality
- Packaged Device
  - Speed Sort
  - Functionality
  - Reliability (Burn-In, Hostile Environments)
  - Special Needs
- Operating System
- Use Conditions

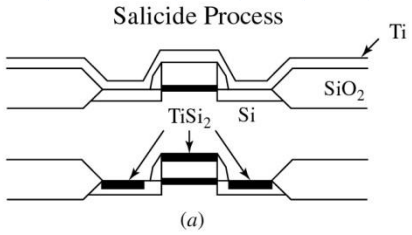
# Packaging

- Interconnection of Circuit Elements
  - First level – on chip
  - Second level – chip to package
  - Third level – between packages (on PCB)
- Wafer to Die
  - Wafers diced into individual integrated circuits
  - Known Good Die (KGD) are packaged.
- Chip on Board (COB) – high volume, inexpensive, miniature
- Packaged Devices for Broad Application
- Peripherally- or area-arrayed I/O
  - Hermetic or Encapsulated
  - Ceramic or Organic
  - Surface Mounted or Through Hole

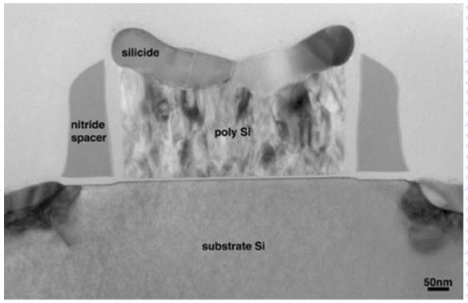
# First Level Interconnect




- Aluminum (3 *μΩ-cm*) or Copper (1.7 *μΩ-cm*)
  - Highly conductive "wires" between devices
- Polysilicon
  - Resistive gate electrodes/short interconnect
- Salicides (Self-Aligning Silicides)
  - Lower spreading resistance
  - Used over poly or shallow diffusions
- Barrier Metals
  - Promote adhesion
  - Prevent diffusion



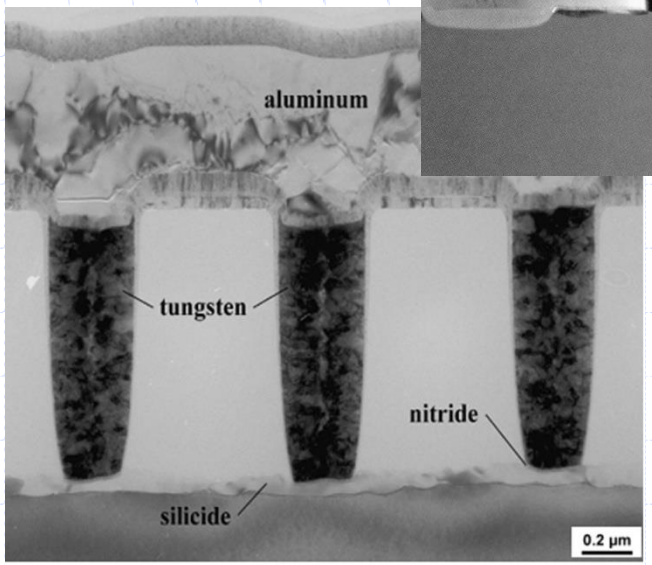

(*a*)



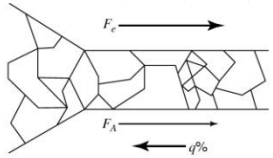

(*b*)

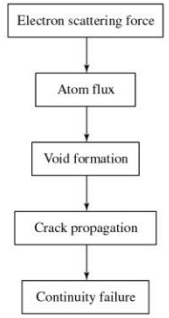
# Multi-Layer Interconnect

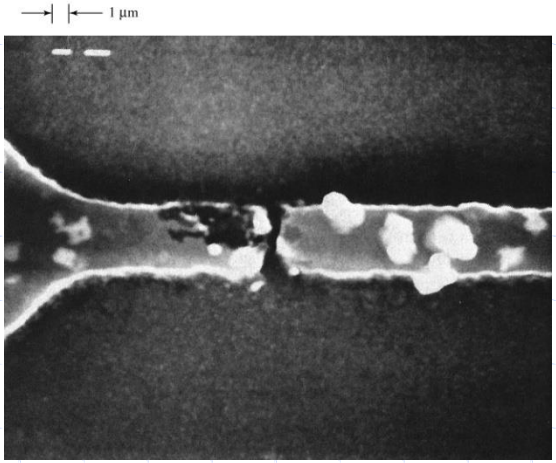
- Oxide insulating layers
- Vias
- Metallic “plugs”



# Do "Wires" Fail?




- Electromigration
  - High current densities
    - ~$10^6$ A/$cm^2$
  - Atoms are blown by the electron "wind"
  - Thinning at negative end, hillocks at positive end
- Electrical Overstress (EOS)
  - Joule heating at high currents
    - $P=I^2R$
  - Wires fuse
- Corrosion
- Thermo-mechanical Stress

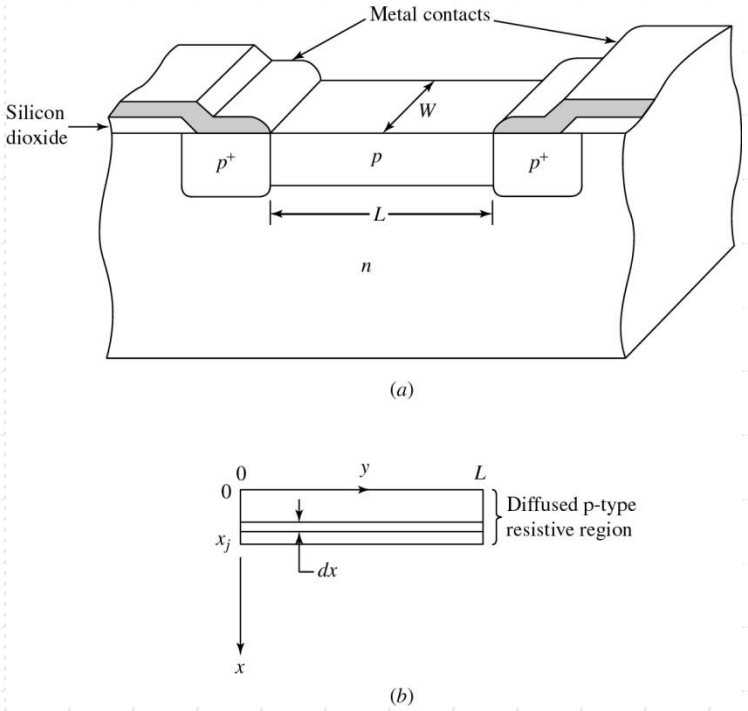
# IC Resistor

- Doped region of specific L and W
  - *p*-type in NMOS process
  - $p^+$ regions enhance termination

$$R = \frac{\rho L}{A}$$

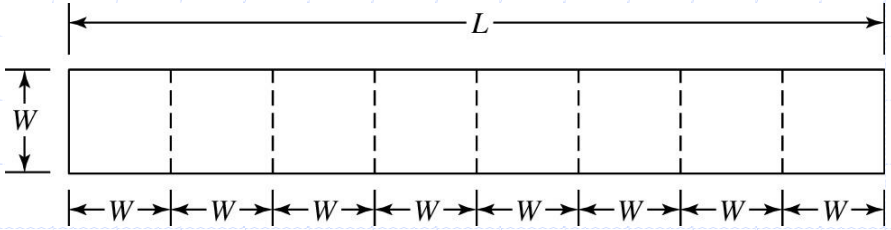
$$\sigma = \frac{1}{\rho} = (q\mu_n n + q\mu_p p)$$

$$dG(x) = q\mu_p p(x)\frac{W}{L}dx$$



# Resistance

- Use an average $\mu$ to approximate conductance

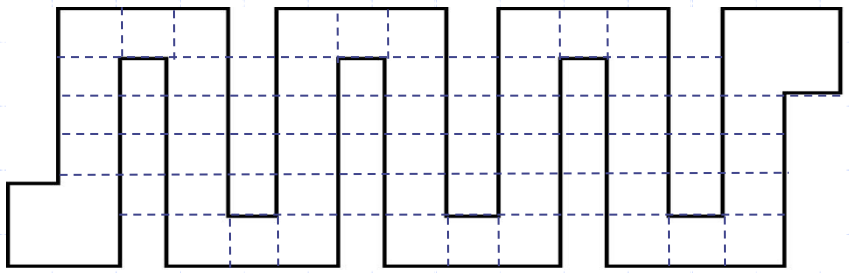


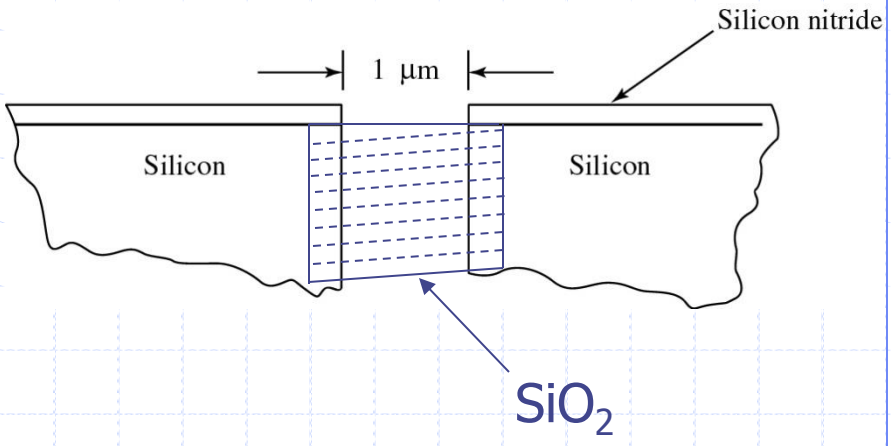

$$G = N'q\bar{\mu}_p \frac{W}{L} = g\frac{W}{L}$$

$$R = \frac{1}{G} = \frac{L}{W}\frac{1}{g}$$

# Sheet Resistance

- Patterns can be resolved to a number of L by W squares
- Each square has a sheet resistance, $R_{\square}$ (lets assume $R_{\square} = 200\Omega/\square$)
- 46 squares * $200\Omega/\square$ = $9.2k\Omega$






# For the fun of it

a) How wide will the 1 *µm* trench become when filled with $SiO^2$?

$SiO^2$ contains $2.2*10^{22}$ molecules/$cm^3$ and Si contains $5*10^{22}$ atoms/$cm^3$. Therefore every unit of $SiO^2$ will use up 44% of a unit of Si (2.2/5). The total width of the $SiO^2$ trench will be…

$$x = 0.44x + 1$$

$$x = 1.79\ \mu m$$