ELEC 428 Test 2 Review

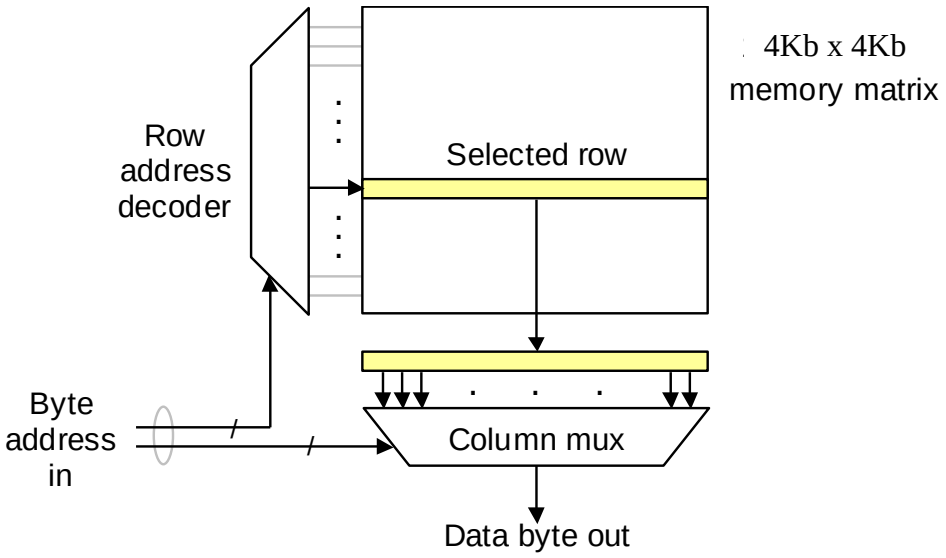
Practice Questions:

1. Given the Single-Cycle MicroMIPS data path in Figure 13.3 and the control signals in Table 13.2, determine the value of all control signals for the execution of the following instructions: andi, sw, jr.

2. Compare the execution cycles for the Single-Cycle MicroMIPS in Figure 13.3 versus the Multi-Cycle MicroMIPS in Figure 14.3.

3. Given the 5-stage Pipelined data path for the MicroMIPS in Figure 15.9, show what is stored in each of the pipelined registers at the boundary between consecutive stages for the following instructions: lui, jal.

4. Given the following DRAM chip organized as a 4M x 4 Memory, determine the number of control lines for the row address decoder and column multiplexer.



18.2 (a)