DUAL N-CHANNEL AND DUAL P-CHANNEL MATCHED MOSFET PAIR

GENERAL DESCRIPTION

The ALD1105 is a monolithic dual N-channel and dual P-channel complementary matched transistor pair intended for a broad range of analog applications. These enhancement-mode transistors are manufactured with Advanced Linear Devices' enhanced ACMOS silicon gate CMOS process. It consists of an ALD1116 N-channel MOSFET pair and an ALD1117 P-channel MOSFET pair in one package. The ALD1105 is a low drain current, low leakage current version of the ALD1103.

The ALD1105 offers high input impedance and negative current temperature coefficient. The transistor pair is matched for minimum offset voltage and differential thermal response, and it is designed for precision signal switching and amplifying applications in +2V to +12V systems where low input bias current, low input capacitance and fast switching speed are desired. Since these are MOSFET devices, they feature very large (almost infinite) current gain in a low frequency, or near DC, operating environment. When used in complementary pairs, a dual CMOS analog switch can be constructed. In addition, the ALD1105 is intended as a building block for differential amplifier input stages, transmission gates, and multiplexer applications.

The ALD1105 is suitable for use in precision applications which require very high current gain, beta, such as current mirrors and current sources. The high input impedance and the high DC current gain of the Field Effect Transistors result in extremely low current loss through the control gate. The DC current gain is limited by the gate input leakage current, which is specified at 30pA at room temperature. For example, DC beta of the device at a drain current of 3mA at 25°C is = 3mA/30pA = 100,000,000.

FEATURES

- Thermal tracking between N-channel and P-channel pairs
- Low threshold voltage of 0.7V for both N-channel & P-channel MOSFETS
- Low input capacitance
- Low Vos -- 10mV
- High input impedance -- $10^{13}\Omega$ typical
- Low input and output leakage currents
- Negative current (I_{DS}) temperature coefficient
- Enhancement mode (normally off)
- DC current gain 10^9
- Matched N-channel and matched P-channel in one package
- RoHS compliant

ORDERING INFORMATION ("L" suffix denotes lead-free (RoHS))

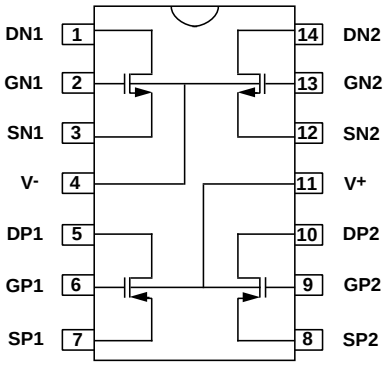
Operating Temperature Range*		
0°C to +70°C	0°C to +70°C	-55°C to +125°C
14-Pin Small Outline Package (SOIC)	14-Pin Plastic Dip Package	14-Pin CERDIP Package
ALD1105SBL	ALD1105PBL	ALD1105DB

* Contact factory for leaded (non-RoHS) or high temperature versions.

APPLICATIONS

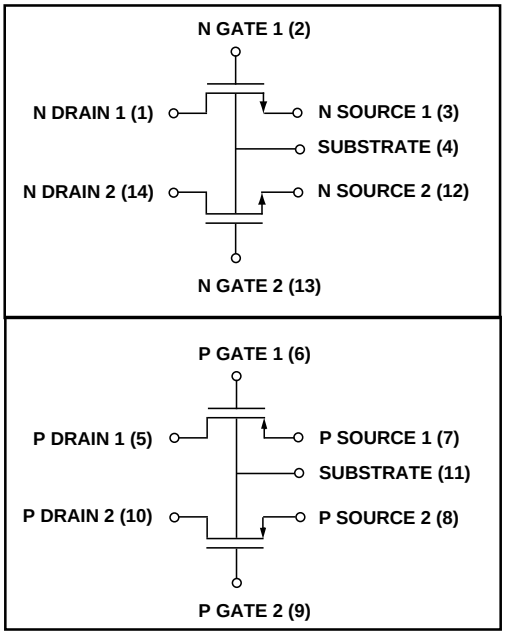
- Precision current mirrors
- Complementary push-pull linear drives
- Analog switches
- Choppers
- Differential amplifier input stage
- Voltage comparator
- Data converters
- Sample and Hold
- Analog inverter
- Precision matched current sources

PIN CONFIGURATION



TOP VIEW
SBL, PBL, DB PACKAGES

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

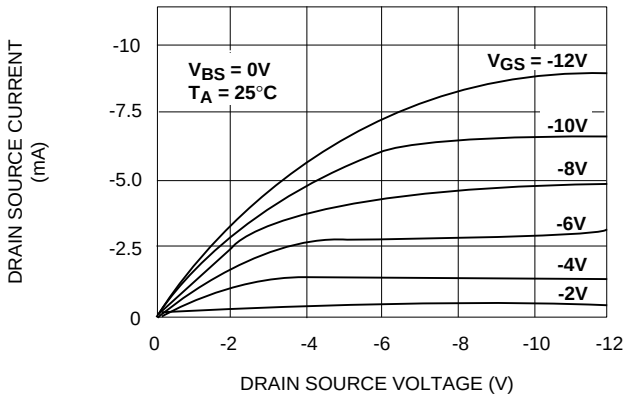
Drain-source voltage, V_{DS} ____ 10.6V
Gate-source voltage, V_{GS} ____ 10.6V
Power dissipation ____ 500mW
Operating temperature range SBL, PBL packages ____ 0°C to +70°C
DB package ____ -55°C to +125°C
Storage temperature range ____ -65°C to +150°C
Lead temperature, 10 seconds ____ +260°C
CAUTION: ESD Sensitive Device. Use static control procedures in ESD controlled environment.

OPERATING ELECTRICAL CHARACTERISTICS
T_A = 25°C unless otherwise specified

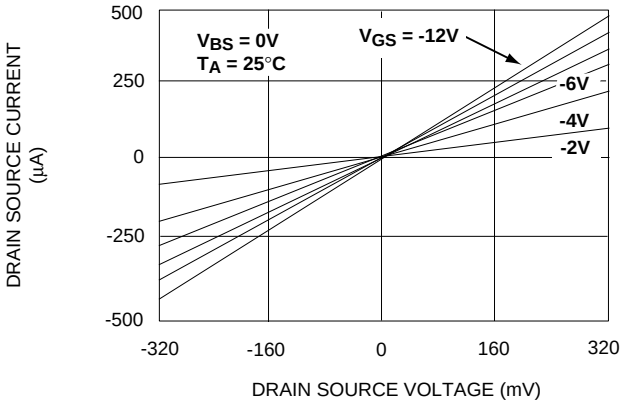
		N - Channel					P - Channel				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Gate Threshold Voltage	V_T	0.4	0.7	1.0	V	I_{DS} = 1µA V_{GS} = V_{DS}	-0.4	-0.7	-1.0	V	I_{DS} = -1µA V_{GS} = V_{DS}
Offset Voltage V_{GS1} - V_{GS2}	V_{OS}		2	10	mV	I_{DS} = 10µA V_{GS} = V_{DS}		2	10	mV	I_{DS} = -10µA V_{GS} = V_{DS}
Gate Threshold Temperature Drift	TC_{VT}		-1.2		mV/°C			-1.3		mV/°C	
On Drain Current	$I_{DS\ (ON)}$	3	4.8		mA	V_{GS} = V_{DS} = 5V	-1.3	-2		mA	V_{GS} = V_{DS} = -5V
Trans-. conductance	G_{fs}	1	1.8		mmho	V_{DS} = 5V I_{DS}= 10mA	0.25	0.67		mmho	V_{DS} = -5V I_{DS}= -10mA
Mismatch	ΔG_{fs}		0.5		%			0.5		%	
Output Conductance	G_{OS}		200		µmho	V_{DS} = 5V I_{DS} = 10mA		40		µmho	V_{DS} = -5V I_{DS} = -10mA
Drain Source ON Resistance	$R_{DS(ON)}$		350	500	Ω	V_{DS} = 0.1V V_{GS} = 5V		1200	1800	Ω	V_{DS} = -0.1V V_{GS} = -5V
Drain Source ON Resistance Mismatch	$\Delta R_{DS(ON)}$		0.5		%	V_{DS} = 0.1V V_{GS} = 5V		0.5		%	V_{DS} = -0.1V V_{GS} = -5V
Drain Source Breakdown Voltage	BV_{DSS}	12			V	I_{DS} = 1µA V_{GS} =0V	-12			V	I_{DS} = -1µA V_{GS} =0V
Off Drain Current	$I_{DS(OFF)}$		10 4	400 4	pA nA	V_{DS} =12V I_{GS} = 0V T_A = 125°C		10 4	400 4	pA nA	V_{DS} = -12V V_{GS} = 0V T_A = 125°C
Gate Leakage Current	I_{GSS}		0.1 1	30 1	pA nA	V_{DS} = 0V V_{GS} =12V T_A = 125°C		1 1	30 1	pA nA	V_{DS} = 0V V_{GS} =-12V T_A = 125°C
Input Capacitance	C_{ISS}		1	3	pF			1	3	pF	

TYPICAL P-CHANNEL PERFORMANCE CHARACTERISTICS

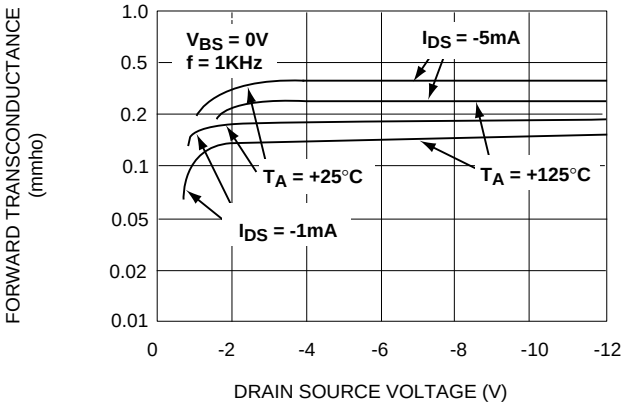
OUTPUT CHARACTERISTICS



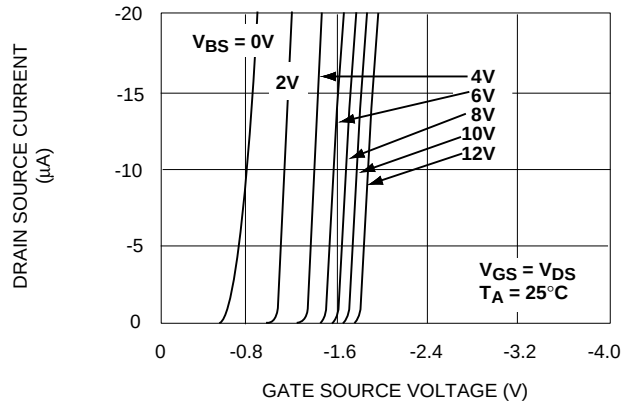
LOW VOLTAGE OUTPUT CHARACTERISTICS



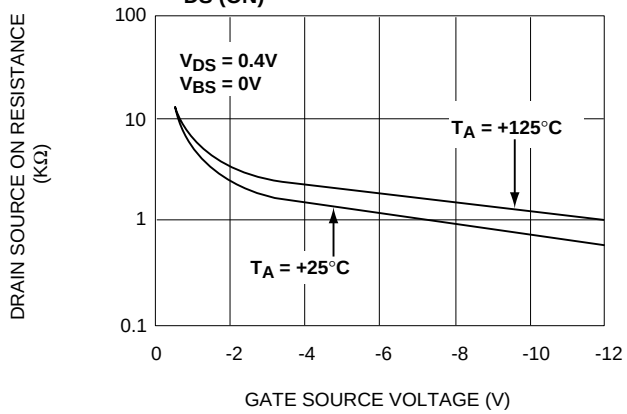
FORWARD TRANSCONDUCTANCE vs. DRAIN SOURCE VOLTAGE



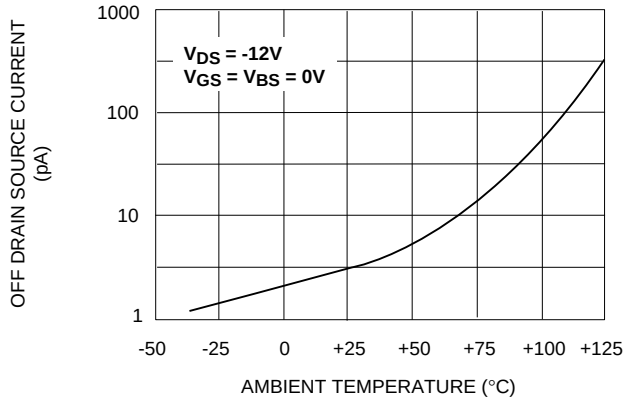
TRANSFER CHARACTERISTIC WITH SUBSTRATE BIAS



DRAIN SOURCE ON RESISTANCE $R_{DS\ (ON)}$ vs. GATE SOURCE VOLTAGE

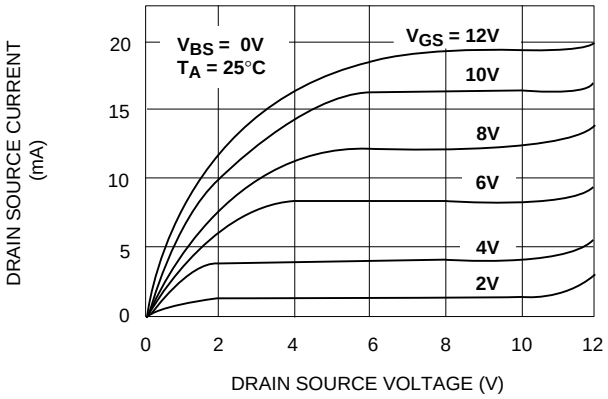


OFF DRAIN CURRENT vs. AMBIENT TEMPERATURE

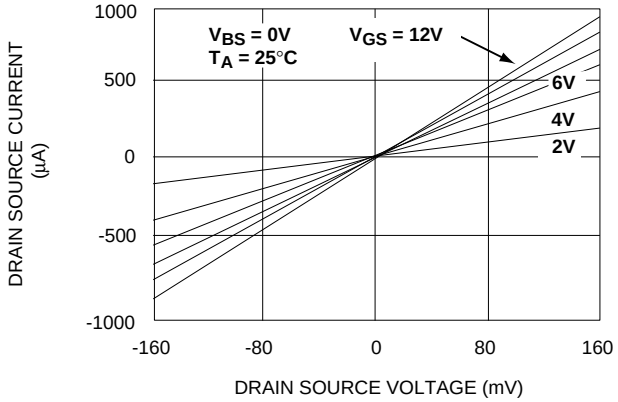


TYPICAL N-CHANNEL PERFORMANCE CHARACTERISTICS

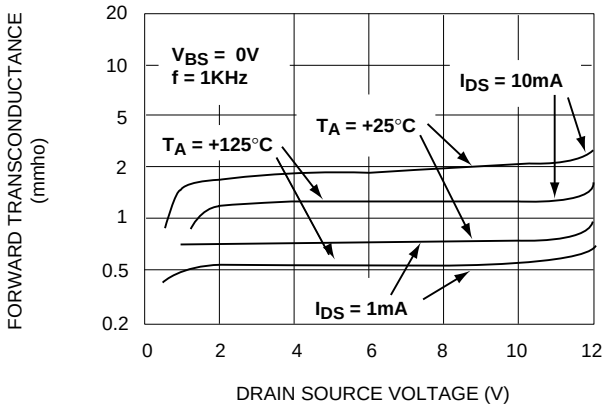
OUTPUT CHARACTERISTICS



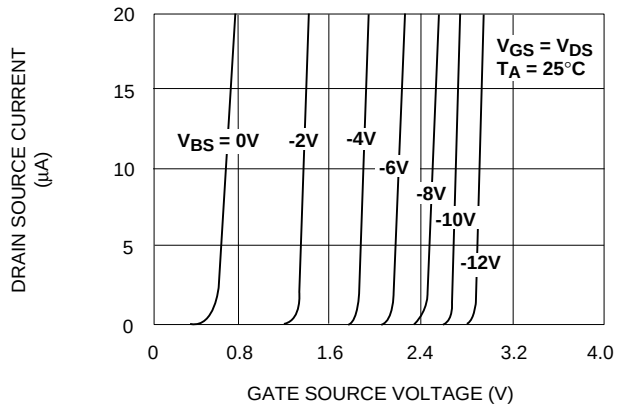
LOW VOLTAGE OUTPUT CHARACTERISTICS



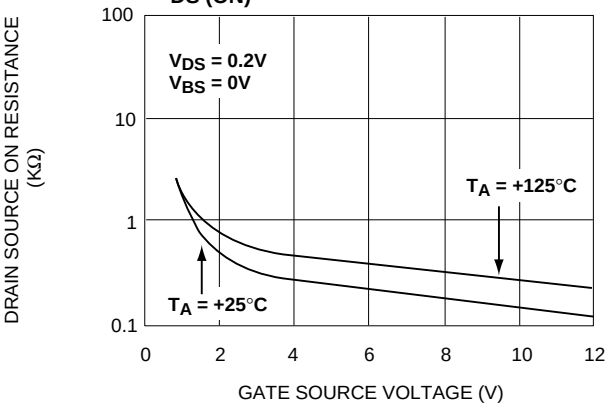
FORWARD TRANSCONDUCTANCE vs. DRAIN SOURCE VOLTAGE



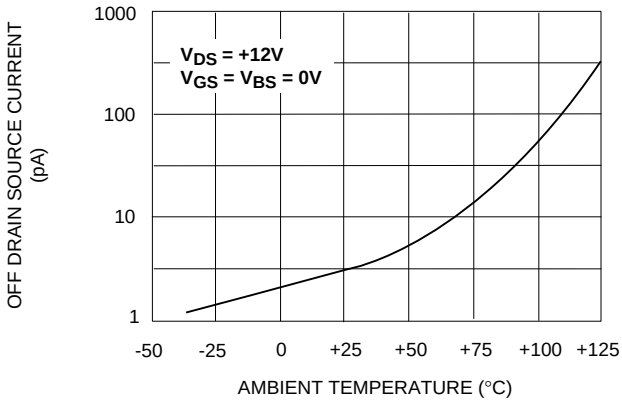
TRANSFER CHARACTERISTIC WITH SUBSTRATE BIAS



DRAIN SOURCE ON RESISTANCE $R_{DS\ (ON)}$ vs. GATE SOURCE VOLTAGE

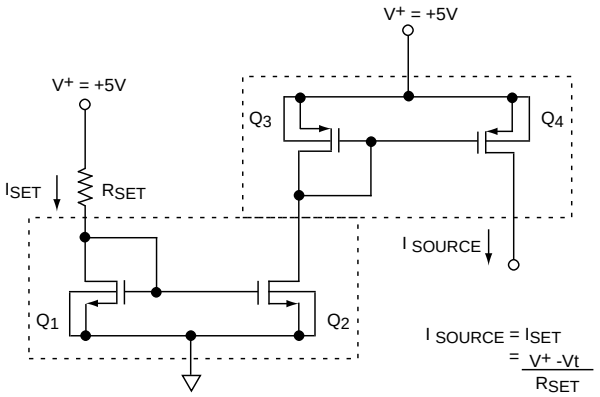


OFF DRAIN CURRENT vs. AMBIENT TEMPERATURE



TYPICAL APPLICATIONS

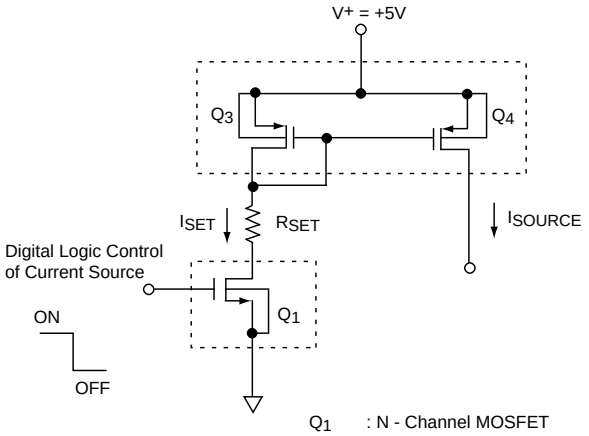
CURRENT SOURCE MIRROR



$I_{SOURCE} = I_{SET} = \frac{V^+ - Vt}{R_{SET}} \cong \frac{4}{R_{SET}}$

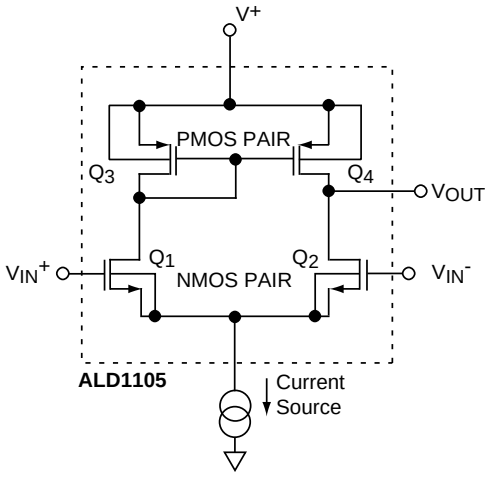
Q_1, Q_2: N - Channel MOSFET
Q_3, Q_4: P - Channel MOSFET

CURRENT SOURCE WITH GATE CONTROL



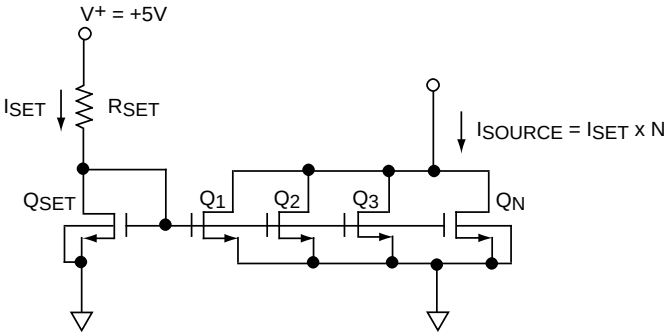
Q_1 : N - Channel MOSFET
$Q_{3,}Q_4$: P - Channel MOSFET

DIFFERENTIAL AMPLIFIER



Q_1, Q_2: N - Channel MOSFET
Q_3, Q_4: P - Channel MOSFET

CURRENT SOURCE MULTIPLICATION

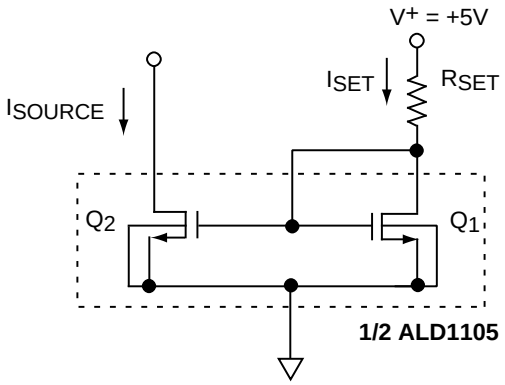


Q_{SET}, Q_1..Q_N: ALD 1106 or ALD 1105
N - Channel MOSFET

TYPICAL APPLICATIONS (cont.)

BASIC CURRENT SOURCES

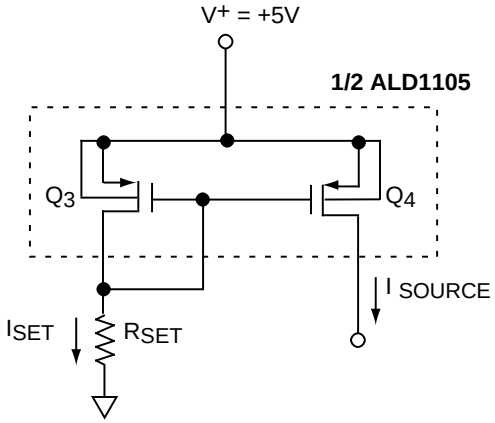
N-CHANNEL CURRENT SOURCE



$$I_{SOURCE} = I_{SET} = \frac{V^+ - Vt}{R_{SET}} \cong \frac{V^+ - 1.0}{R_{SET}} \cong \frac{4}{R_{SET}}$$

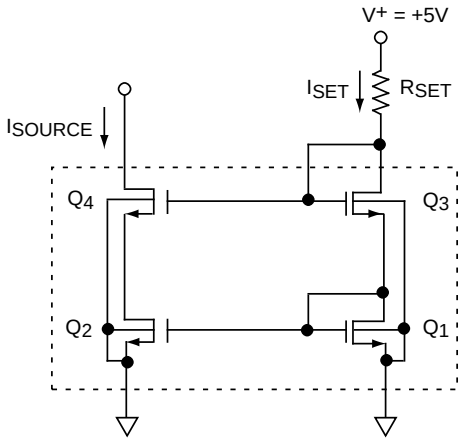
Q_1, Q_2 : N - Channel MOSFET

P-CHANNEL CURRENT SOURCE

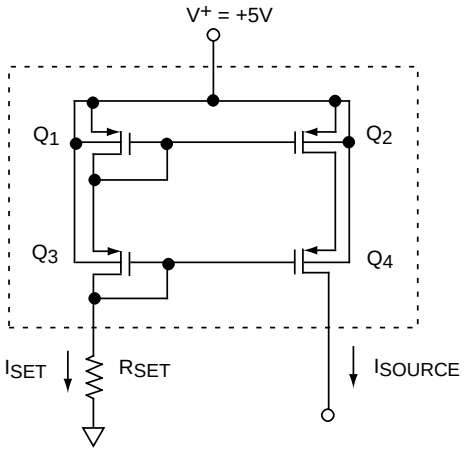


Q_3, Q_4: P - Channel MOSFET

CASCODE CURRENT SOURCES



Q_1, Q_2, Q_3, Q_4: N - Channel MOSFET
(1/2 ALD1105 + ALD1116)

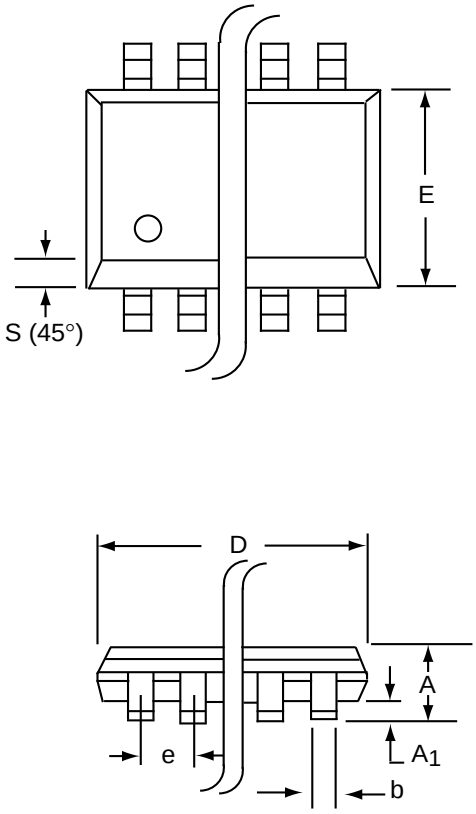


$$I_{SOURCE} = I_{SET} = \frac{V^+ - 2Vt}{R_{SET}} \cong \frac{3}{R_{SET}}$$

Q1, Q2, Q3, Q4: P - Channel MOSFET
(1/2 ALD1105 + ALD1117)

SOIC-14 PACKAGE DRAWING

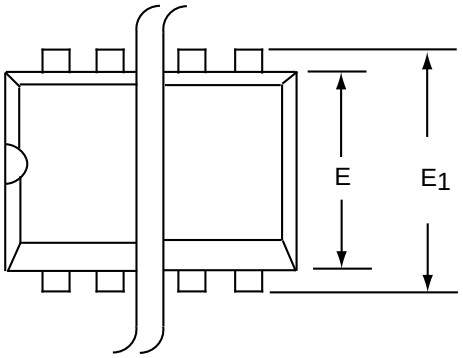
14 Pin Plastic SOIC Package

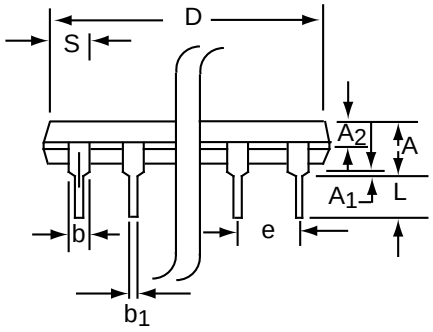


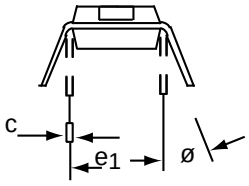
Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.25	0.004	0.010
b	0.35	0.45	0.014	0.018
C	0.18	0.25	0.007	0.010
D-14	8.55	8.75	0.336	0.345
E	3.50	4.05	0.140	0.160
e	1.27 BSC		0.050 BSC	
H	5.70	6.30	0.224	0.248
L	0.60	0.937	0.024	0.037
Ø	0°	8°	0°	8°
S	0.25	0.50	0.010	0.020

PDIP-14 PACKAGE DRAWING

14 Pin Plastic DIP Package



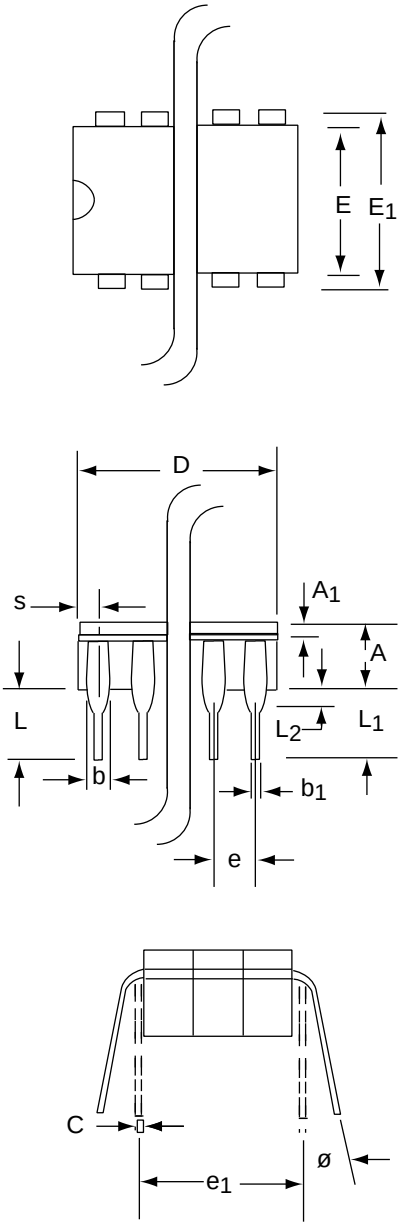




Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	3.81	5.08	0.105	0.200
A_1	0.38	1.27	0.015	0.050
A_2	1.27	2.03	0.050	0.080
b	0.89	1.65	0.035	0.065
b_1	0.38	0.51	0.015	0.020
c	0.20	0.30	0.008	0.012
D-14	17.27	19.30	0.680	0.760
E	5.59	7.11	0.220	0.280
E_1	7.62	8.26	0.300	0.325
e	2.29	2.79	0.090	0.110
e_1	7.37	7.87	0.290	0.310
L	2.79	3.81	0.110	0.150
S-14	1.02	2.03	0.040	0.080
ø	0°	15°	0°	15°

CERDIP-14 PACKAGE DRAWING

14 Pin CERDIP Package



Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	3.55	5.08	0.140	0.200
A_1	1.27	2.16	0.050	0.085
b	0.97	1.65	0.038	0.065
b_1	0.36	0.58	0.014	0.023
C	0.20	0.38	0.008	0.015
D-14	--	19.94	--	0.785
E	5.59	7.87	0.220	0.310
E_1	7.73	8.26	0.290	0.325
e	2.54 BSC		0.100 BSC	
e_1	7.62 BSC		0.300 BSC	
L	3.81	5.08	0.150	0.200
L_1	3.18	--	0.125	--
L_2	0.38	1.78	0.015	0.070
S	--	2.49	--	0.098
Ø	0°	15°	0°	15°