ELEC-311
Project 4
Synchronous Design

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1 Objective

- Design and test a synchronous sequential circuit which implements a 2-bit binary counter.
- Describe the circuit using VHDL.

2 Discussion

	Inputs		PS		NS		Outputs	
mt	EL	UP	Q1	Q0	Q1+	Q0+	Z1	Z0
0	0	0	0	0			0	0
1	0	0	0	1			0	1
2	0	0	1	0			1	0
3	0	0	1	1			1	1
4	0	1	0	0			0	0
5	0	1	0	1			0	1
6	0	1	1	0			1	0
7	0	1	1	1			1	1
8	1	0	0	0			0	0
9	1	0	0	1			0	1
10	1	0	1	0			1	0
11	1	0	1	1			1	1
12	1	1	0	0			0	0
13	1	1	0	1			0	1
14	1	1	1	0			1	0
15	1	1	1	1			1	1

Table 1

3 VHDL

```
library IEEE;
use IEEE.STD_LOGIC_1164.all;
use work.project3_gates.all;

entity circuit is
  port (X    : in  std_logic_vector(3 downto 0);
        Y    : in  std_logic_vector(3 downto 0);
        Z    : out std_logic_vector(3 downto 0);
        SEL  : in  std_logic;
        Cout : out std_logic;
        OVR  : out std_logic);
```

```
end circuit;

architecture Structural of circuit is

  signal C : std_logic_vector(3 downto 0);
  signal S : std_logic_vector(3 downto 0);

begin

  x3 : ExclusiveOR port map(SEL, Y(3), S(3));
  x2 : ExclusiveOR port map(SEL, Y(2), S(2));
  x1 : ExclusiveOR port map(SEL, Y(1), S(1));
  x0 : ExclusiveOR port map(SEL, Y(0), S(0));

  fa3 : FullAdder port map(X(3), S(3), C(2), C(3), Z(3));
  fa2 : FullAdder port map(X(2), S(2), C(1), C(2), Z(2));
  fa1 : FullAdder port map(X(1), S(1), C(0), C(1), Z(1));
  fa0 : FullAdder port map(X(0), S(0), SEL, C(0), Z(0));

  Cout <= C(3);
  OVR <= (((not X(3)) and (not Y(3)) and C(3)) or (X(3) and Y(3) and (not C(3))));

end Structural;
```