

Bio Inspired Technologies NEURO-BIT

User Manual

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ESD Warning



Warning! This product is ultra-sensitive to electrostatic discharge (ESD). When handling, care must be taken so that the memristor devices are not damaged.

The following precautions must be taken:

- Do not open the protective conductive packaging until you have read the following, and are at an approved anti-static work station.
- Use a conductive wrist strap attached to a good earth ground.
- Always discharge yourself by touching a grounded bare metal surface or approved anti-static mat before picking up an ESD sensitive electronic component.
- Never handle the packaged parts or test die with bare hands.
- Use an approved anti-static mat to cover your work surface.
- Always store devices in a dry, inert environment.



Dear Customer,

We at Bio Inspired Technologies believe that the future of electronics is based on adaptive intelligence technologies - technologies that enable biologically inspired circuits that think and learn. The Bio Inspired Technologies' Neuro-Bit Memristor device is the first in many steps toward that end. Because of the uncanny behavioral and operational similarities between the memristor and the biological synapse, we believe the memristor will play a pivotal role in advancing intelligent systems, and we hope that you find these devices instrumental to your role as researchers, engineers, inventors, or even hobbyists in implementing the future of neuromorphic designs.

Invent the future.

Thank you for your purchase,

The Bio Inspired Staff

www.bioinspired.net



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Overview

The Neuro-Bit PLCC, introduced by Bio Inspired Technologies, contains 20 functional chalcogenide-based ion-conducting memristor devices. If purchased, the raw die is supplied with 80 identical memristor devices. These ion-conducting memristors can be "written" and "erased" to turn the device on or off as desired. It is non-volatile in the sense that the device still remembers its programmed state after power has been removed. In a controlled pulsing scenario, the memristor retains a state that is a function of both the history of the device and the current applied signal. The memristor is a nano-scale, thin-film variable electrical resistor fabricated on a silicon wafer that has a memory.

The memristor, while exhibiting complex behavior, uses dendrite growth to change its resistance state and is fully reversible through the appropriate application of control signals.

The device is analog in nature and can be programmed to a variety of intermediate resistance states in between "on" and "off".

The dendrite circuit emulates the behavior and operates in nearly the exact way as that of a biological synapse, making it an ideal candidate for:

- Synthetic neurons
- Threshold logic and Reconfigurable circuit applications
- Neuromorphic circuits
- Tunable memristor-based resistors, capacitors, and inductors
- Adaptive intelligence and learning systems
- Neural networks and weighted feedback systems
- Spike-timing-dependent plasticity (STDP) experimentation
- Multi-level memory systems
- Implementing inhibitory and excitatory responses in circuits

Bio-Inspired Technologies is currently offering the following package options:

- Bare Die
- 44-pin PLCC Package (A breakout PCB is available for the PLCC option)



Memristor Specifications

• Write voltage 300-400 mV

• Post-write resistance Less than $500\Omega^*$

• Pre-programming resistance Greater than 50 M Ω^{**}

• Erase voltage (-300) to (-400) mV

• Post-erase resistance Roughly 5 M Ω

• Write speed Less than 5 nS

• Maximum cycles Greater than 2K***

^{*}The post-write resistance value is determined by several factors, including the current compliance, sweep range, or pulse conditions applied to the memristor. Different values can be achieved by tuning these parameters.

^{**}This is the value measured before the device has been programmed for the first time. This value can range widely from open to a few mega-Ohms. Once programmed, or "conditioned", the device will settle to the post-erase value.

^{**}The number of achievable cycles varies greatly with the "roughness" of the programming parameters, as well as the measurement techniques used. Careful attention to the operating parameters can result in devices that last nearly indefinitely.



Test Die

The test die contains 80 memristors with a yield above 75%. The locations and orientation are as shown below in Figure 1, with devices numbered 1 through 80. The large blocks are alignment features and the small crosses are Van Der Pauw structures to characterize the top and bottom metal layers. Sixteen additional memristors can be found between the row blocks of numbered devices. All memristors on the die are oriented with the positive terminal, or top-electrode, colored in purple on the left.

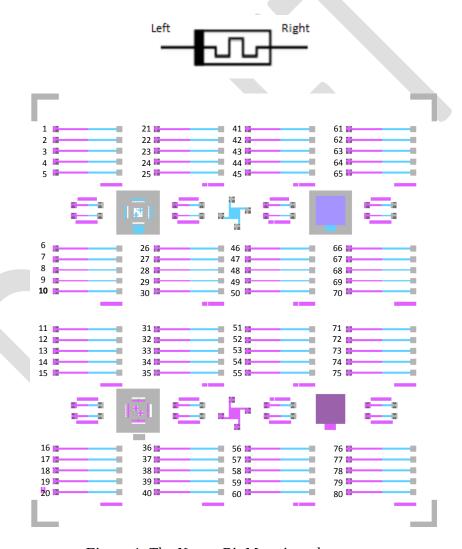


Figure 1. The Neuro-Bit Memristor layout



PLCC Package

The 44-pin PLCC package contains 20 bonded memristor devices, with 60 available for future bonding and use.



Figure 2. The Neuro-Bit PLCC package



Memristor to Package Pinout:

Memristor 1	TE = Pin43 - BE = Pin41	Memristor 11	TE = Pin18 - BE = Pin20
Memristor 2	TE = Pin01 - BE = Pin44	Memristor 12	TE = Pin19 - BE = Pin21
Memristor 3	TE = Pin03 - BE = Pin02	Memristor 13	TE = Pin22 - BE = Pin24
Memristor 4	TE = Pin05 - BE = Pin04	Memristor 14	TE = Pin26 - BE = Pin27
Memristor 5	TE = Pin06 - BE = Pin07	Memristor 15	TE = Pin28 - BE = Pin29
Memristor 6	TE = Pin08 - BE = Pin09	Memristor 16	TE = Pin31 - BE = Pin30
Memristor 7	TE = Pin10 - BE = Pin12	Memristor 17	TE = Pin33 - BE = Pin32
Memristor 8	TE = Pin11 - BE = Pin13	Memristor 18	TE = Pin37 - BE = Pin35
Memristor 9	TE = Pin14 - BE = Pin16	Memristor 19	TE = Pin40 - BE = Pin38
Memristor 10	TE = Pin15 - BE = Pin17	Memristor 20	TE = Pin42 - BE = Pin39



Breakout Board

The **Neuro-Bit Breakout Board** allows the user to place the Neuro-Bit chip in a 22-pin socket for ease of testing. Each pin is connected to a labeled header pin as seen in Figure 3. The memristors are labeled TE/BE on the header to designate the polarity of the connected electrode.

For example:

TE1 = Memristor 1 Top Electrode (+) **BE1** = Memristor 1 Bottom Electrode (-)



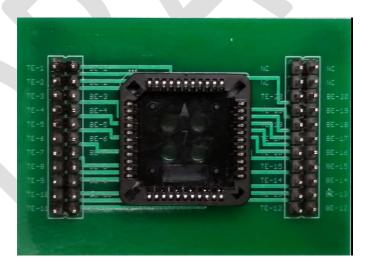


Figure 3. The Neuro-Bit Breakout Board



Measurement Equipment

The following equipment is highly recommended for use with the Neuro-Bit. Failure to do so can result in unwanted transients that produce faulty data and/or damaged devices. <u>Measurement transients are very common in many instruments and, unless correctly regulated, will result in irreparable damage to the devices.</u> It is recommended that any test equipment be carefully examined with an oscilloscope prior to testing actual memristors. Transients should not exceed a few millivolts. This includes any environmental noise as well.

Agilent B1500A Semiconductor Device Analyzer



• HP4145/56 Semiconductor Parameter Analyzers



Figure 4. Acceptable semiconductor device (top) and parameter (bottom) analyzers for safe device testing and use.



The Importance of a Carefully Controlled Measurement

The Neuro-Bit Memristors are highly sensitive and reactive devices that, when programmed correctly, may be used in a variety of neural or memory-based applications. However, the devices must be carefully controlled to ensure peak performance. A device that is carelessly operated will quickly short, making it nearly impossible to erase for future use. An explanation of a typical DC characterization task is illustrated below:

- The programming cycle. When freshly manufactured, the memristors have not yet developed preferential dendrite programming pathways. As a result, initial resistance measurements should indicate a very high resistance (nearly open). A simple resistance measurement should be done with a voltage of less than 50mV. Conventional multi-meters or unverified equipment should not be used because of the often very large open circuit voltages or unconstrained current parameters. It is important that the sample voltage be kept minimal to prevent the measurements from changing the state of the device. If the sample voltages are greater than 50mV, the device will begin to write while being sampled.
- The write cycle. The write cycle typically involves simply sweeping the device to a value above the expected switching threshold, or approximately 400mV for the Neuro-Bit devices. A typical sweep for these devices would be from zero to one volt. During DC sweeps, setting a current compliance for your measurement is extremely important and critical to preserving functioning devices. While sweeping the devices above the write threshold is important to perform a write, the current compliance you set will determine both the final resistance value of the memristor and how stable the device will be at that state. Reasonable current compliance values will range between 100nA and 30µA. When experimenting with the Neuro-Bit Memristors, it is best to begin with very conservative values until you are comfortable with the performance.

Note: The reason for this is that the devices form a conductive dendrite (or several) during the programming process. The dendrite effectively makes a connection between the top electrode and bottom electrode. The conductivity of the dendrites is set by the current allowed to pass through the device while being programmed. If the current is left unconstrained, the dendrites will effectively form a short circuit between the electrodes. This will make it nearly impossible to reverse the process during the erase cycle and the device will be "stuck". It may be possible to reverse this through repeated erase sweeps, but the process is difficult to implement and not always effective.



• The erase cycle. The erase cycle will reverse the effects of the write cycle, resetting the device back to a high resistance state. Since it is important to allow the device to consume the necessary current to reverse the dendrite growth, a current compliance is not normally required. A typical sweep would be from zero the negative one volt, setting the current compliance to between 1mV and 10mV as a safety precaution. After the erase step, the resistance of the device should be significantly less than the as-deposited values, and the device is now considered "conditioned". Occasionally, the erase cycle may be repeated to achieve the desired resistance values if the first cycle does not erase effectively. There are no ill-effects from repeating the erase cycle.

The Intrinsic Variability of the Neuro-Bit Memristors

The Neuro-Bit Memristors are intrinsically variable devices and no two devices operate identically. While physically the devices are the same size and configuration, and will use the same programming and erase methodology, they will produce many different responses. In the semiconductor world where the ultimate goal is to have devices that are all identical, this behavior is unwanted. In the neural circuit world, this behavior is ideal. Additionally:

- Most neural circuits use a weighting system, in which the final output is a function of the tuned input weights. A correctly trained system that converges typically requires a set of randomly weighted inputs. The intrinsic variability of the Neuro-Bit Memristor provides this controlled randomness naturally.
- The state of the memristor is a function of the sum of the previous signals the device has experienced (both positive and negative), as well as the current signal. This provides for a direct analog to the biological synapse in which weighting is achieved through repeated activity. This can be reinforcing or inhibiting, depending on the sum and nature of the signals.
- For small compliance values, the memristor demonstrates a relaxation effect, in which the resistance slowly but predictably returns to either an intermediate value or a pre-write resistance value. This behavior could be considered the analog to "forgetting", and would be very useful in circuits where signal strength and repetitive use determine functionality or preferred circuit pathways.
- The Neuro-Bit Memristors are continuously variable resistance (CVR) devices in that many discrete programming values can be achieved by carefully controlling the input pulses. The number of levels achieved is simply a function of the ability of the measurement system (or circuits) to resolve them. In many instances, the discrete states resulting from carefully controlled pulsing conditions form very stable and repeatable resistance values.



DC Measurements

DC Voltage Sweep of CVR (Shown using an Agilent B1500)

Memristor devices are typically operated under pulsed conditions since DC (quasi-static) sweeps do not provide true operational information (unless the device will be used in a circuit in a similar manner to the conditions of a DC sweep). However, the DC sequence is often the simplest way to confirm device functionality as well as provide a valuable tool to understanding the behavior of the devices.

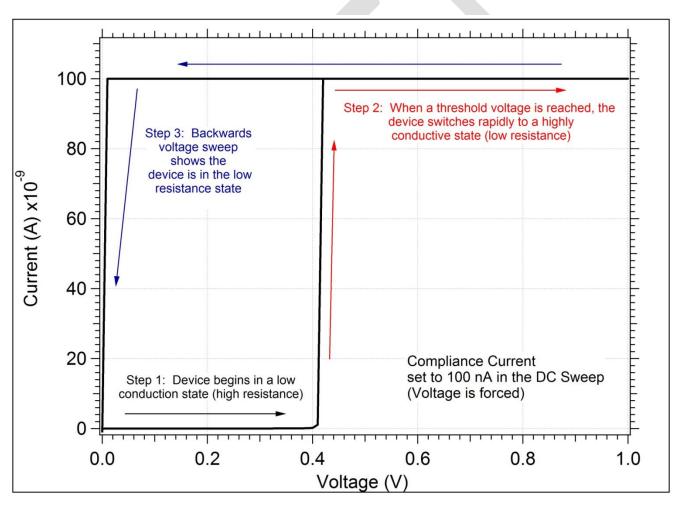


Figure 5. A typical write-erase cycle



AC Pulsed Measurements

Measurement Setup for Pulsed Testing

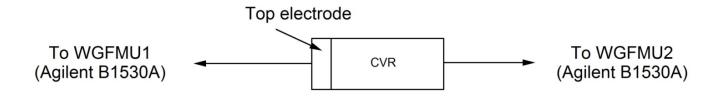
(Agilent B1500A and B1530A WGFMUs)

Pulsed measurements are best performed in a circuit similar to that which will use the device. Alternatively, using an instrument like the Agilent B1500A equipped with the fast pulsing units (WGFMU, B1530A) is an option (we use this for wafer-level device testing).

The Waveform Generator/Fast Measurement Units (WGFMUs) are operated in Pulse-Generation (PG) mode with 5V max range when measuring voltage across the device during pulsing.

Fast I-V mode is used to measure current through the device during pulsing. A major drawback of this measurement is the lack of current limiting. The devices can be forced into very low resistance states (~50 to 100 Ohms in this case) and the measured current through the device can be in the mA range. This is indicative of how the device must be operated, but does show that it can be operated at very low resistance if desired.

Memristor = CVR = Continuous Variable Resistor





Voltage across a device during Pulse Testing

This is the raw data as it is provided by the test instrument. Figure 6 shows the voltage measured at node 1 (see CVR measurement set up in the previous diagram) and at node 2, presented on the same graph, with node 1 voltage on the left axis and node 2 voltage on the right axis. Observe that these both have different zero lines and ranges. The pulse train applied is a 3x repetition of the pulse sequence consisting of a read/erase/read/write/read. Because this pulse sequence is repeated 3 times, there are two regions with two consecutive read pulses. **Note:** The erase is a negative pulse used to increase the device resistance, whereas the write is a positive pulse used to decrease the device resistance. Read pulses are selected not to perturb the device.



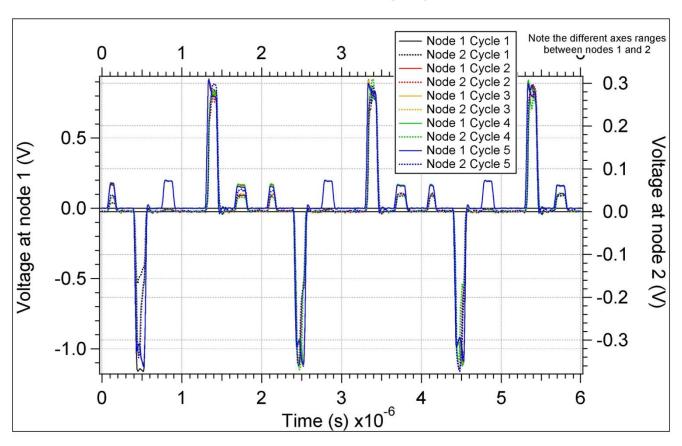


Figure 6. Memristor pulsing cycles of Nodes 1(left-axis) and 2 (right-axis) over a 6μs period.



Figure 7 demonstrates the difference in voltage data between node 1 and node 2. This is the voltage as seen by the device during each programming/erase/reading pulse sequence through five testing cycles. The impact of the switching and erase events on the voltage pulse is an indication that the device is changing state during the application of the pulse. Additionally, the minimal impact of the read measurements is an important indication that the sample voltage is sufficiently small to have no appreciable impact on the current device state.

Voltage Across A Device During Five Consecutive Repetitions of a Three Cycle Test Sequence

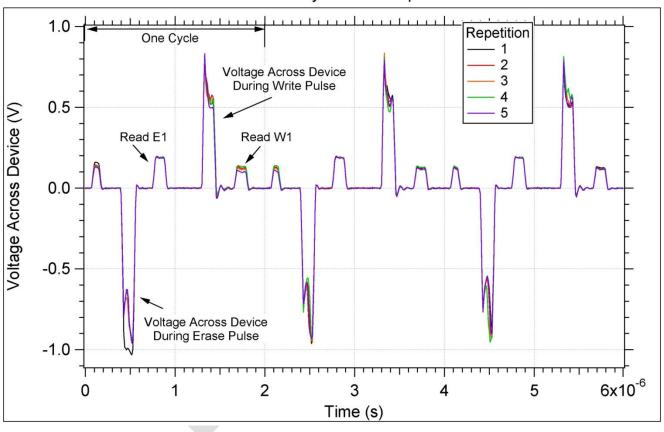


Figure 7. Voltage potential as seen by the device



The sequence of pulses (the 3x repetition of the sequence previously described) is repeated 5 times (for a total of 15 pulse sequence cycles). Figure 8 demonstrates the voltage across the device at the read pulses corresponding to the read after erase 1, write 1, erase 2, write 2, erase 3, and write 3. This is an indication of the stability and repeatability of the Neuro-Bit Memristor throughout several programming cycles.

Voltage Across the Device During the Read Operation Post Erase and Write Programming (see Read E1, Read W1, and the similar read operations in last two cycles of the sequence)

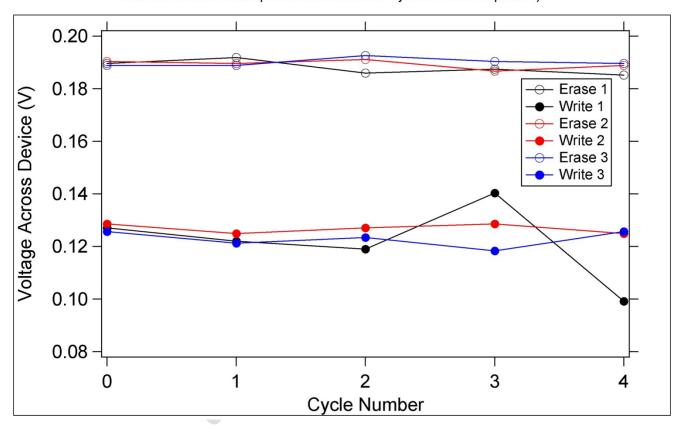


Figure 8. Device stability and repeatability



Current through a device during Pulse Testing

The raw data collected using the Fast IV mode to measure current through the device during pulse testing is shown in Figure 9. This data is procured from the same device used to collect the other data presented in this document.

There is no current limiting during this measurement, so the device resistance gets to values approaching 100 Ohms in this example. Therefore, the measured current through the device is quite high. Note that the device operates nicely in current ranges from nano-Amps through milli-Amps.

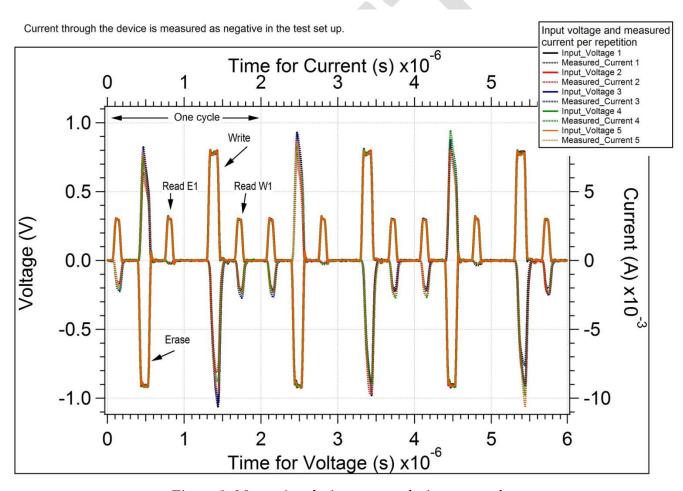


Figure 9. Measuring device current during test cycles



DC Test Data

Prior to shipment, the packaged memristor devices are tested using DC signals to write/read and erase. Each tested device is written and erased, and then written and erased once again. The resulting waveforms are saved and shipped with the package in the USB drive under the Test Data directory to demonstrate functionality of the devices included in the package.

DC Write

For the write, a DC signal is increased from 0V to 1V with $30\mu A$ compliance, and an example of the subsequent waveform is shown in Figure 10. The figure demonstrates a successful write cycle with a switching event at 400mV.

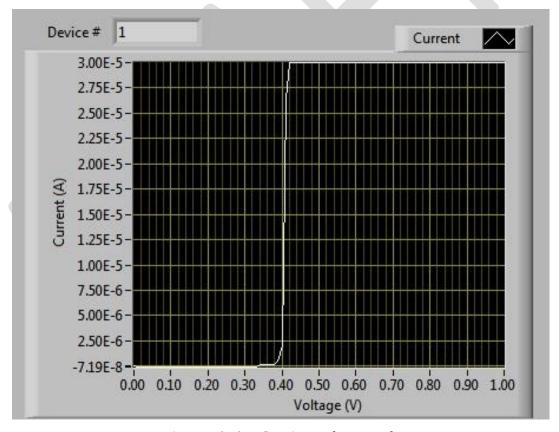


Figure 10. A DC write cycle example



DC Erase

For the erase, a DC signal is swept from 0V to -1V with 1mA compliance, and an example of the subsequent waveform is shown below in Figure 11. An erased memristor will have a typical resistance values greater than $1M\Omega$. Notice the transition occurs around -100mV. While these values may vary between devices, the characteristic erase shape is evident and is characteristic of a successful transition to a high resistance state.

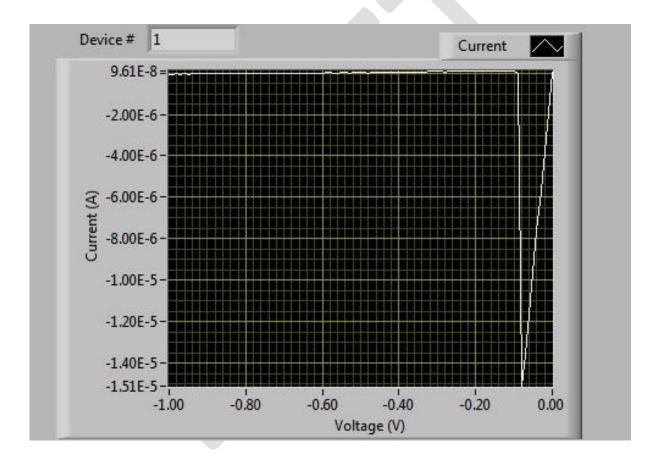


Figure 11. A DC erase cycle included with each part



Contact us

If there are any problems or requirements when testing or using our Neuro-Bit Memristor products, please contact Bio Inspired Technologies, LLC, or visit: www.bioinspired.net. The most recent version Neuro-Bit User Manual is also located on the website.

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Revision History





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