1. Design a falling-edge triggered J-K flip-flop with an active-high asynchronous clear.

 a) Draw the logic symbol and a truth table.
 b) Write a complete VHDL model (entity and behavioral architecture).

2. Draw the circuit generated by the following VHDL model. Completely label all components and signals.

```
entity SR2 is
  port(S, CLK: in bit;
       D : in bit_vector(1 downto 0);
       Q: out bit_vector(1 downto 0));
end SR2;

architecture DATAFLOW of SR2 is
  signal M, R: bit_vector(1 downto 0);
begin
  M <= D when S = '1' else (R(0)&R(1));
  process(CLK)
  begin
    if rising_edge(CLK) then
      R <= M;
    end if;
  end process;
  Q <= R;
end DATAFLOW;
```

① J-K Flip-Flop

a)

CLR	J	K	CLK	Q^+
1	x	x	x	0
0	0	0	↓	Q
0	1	0	↓	1
0	0	1	↓	0
0	1	1	↓	Q'

b)
```
entity JKFF is
    port (CLR, J, K, CLK : in bit;
              Q : out bit);
end JKFF;

architecture Behave of JKFF is
    signal QI : bit;
begin
    process (CLR, CLK)
    begin
        if CLR = '1' then
        Q <= '0';
        elsif falling_edge (CLK) then
        if J = '1' and K = '0' then
        QI <= '1';
            elsif J = '0' and K = '1' then
        QI <= '0'
```

```
            elsif J = '1' and k = '1' then
                 QI <= not QI;
              end if;
            end if;
          end process
          Q <= QI;
       end Behave;
```

②

SR2