Sequential Arithmetic

ELEC 311

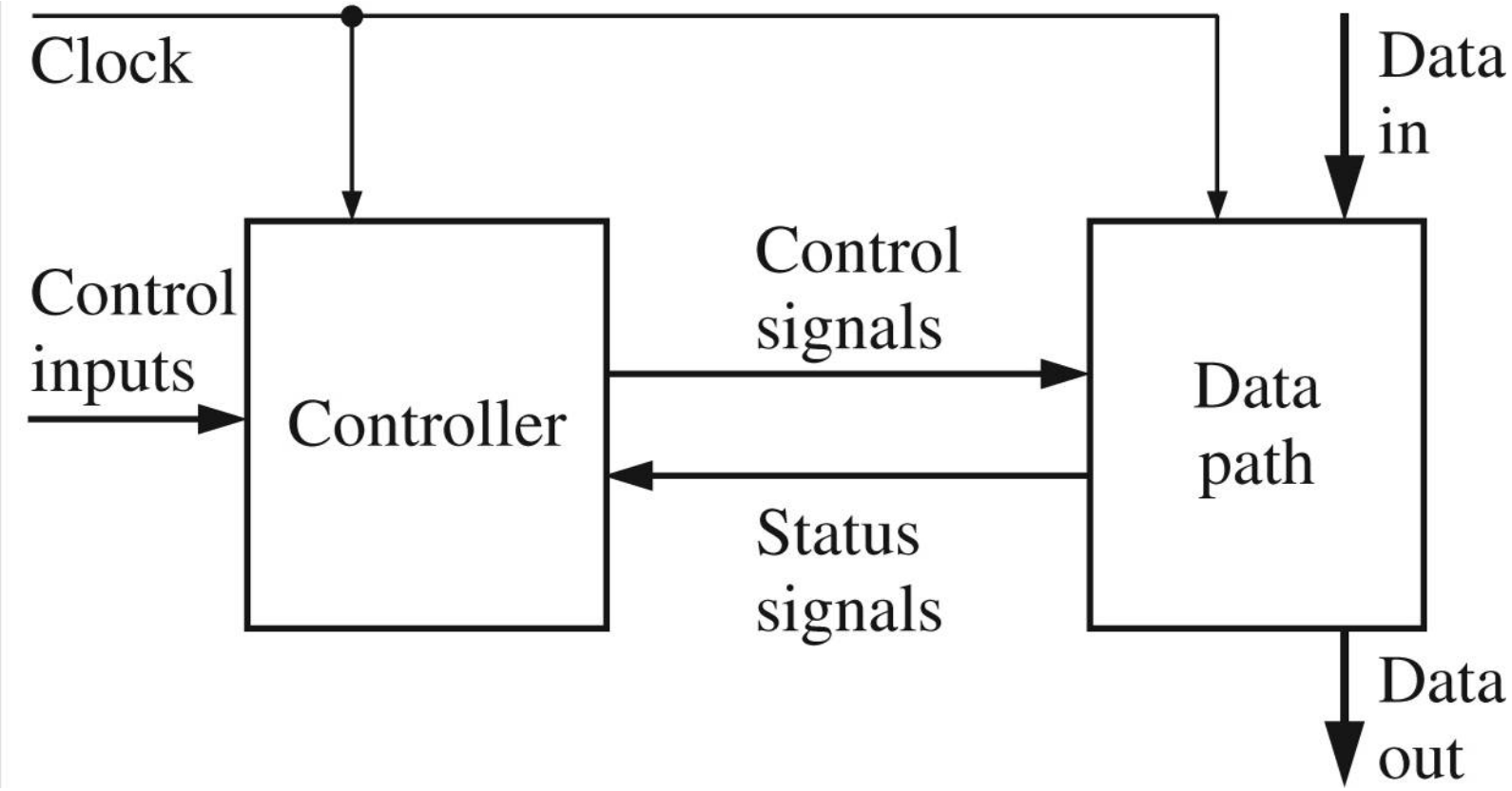
Digital Logic and Circuits

Dr. Ron Hayne

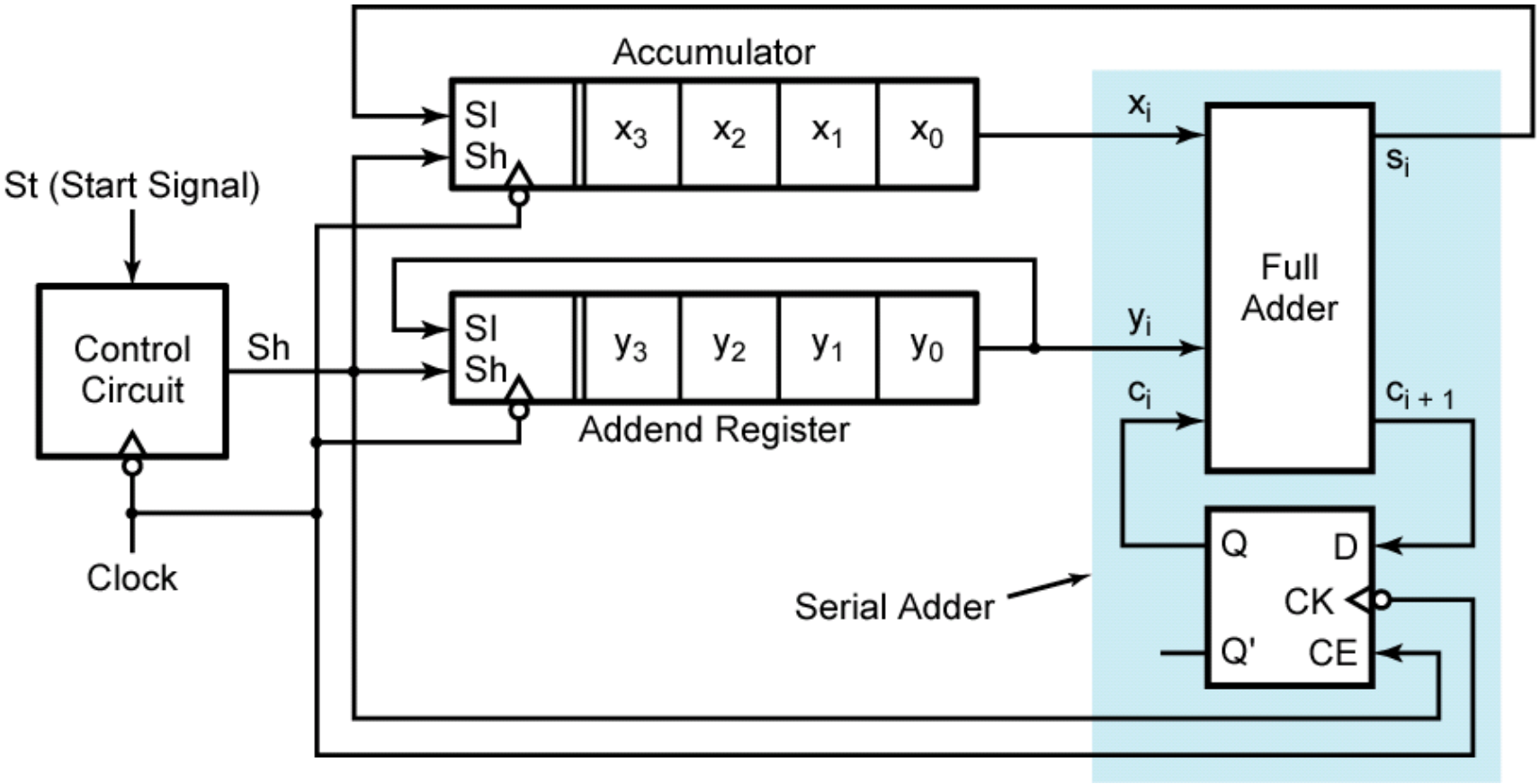
Images Courtesy of Cengage Learning

THE CITADEL
DEPARTMENT OF ELECTRICAL & COMPUTER ENGINEERING

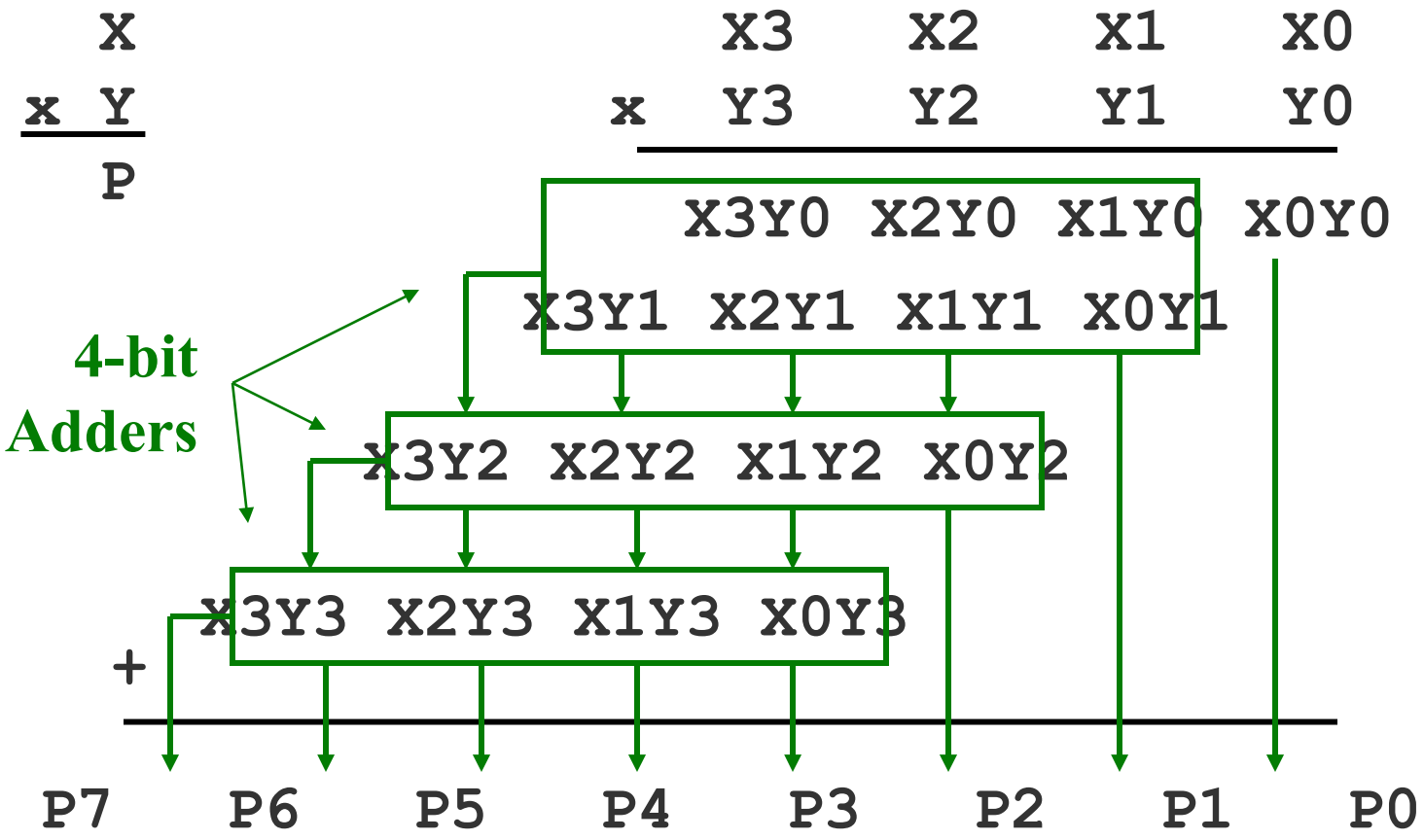
Data Path and Controller



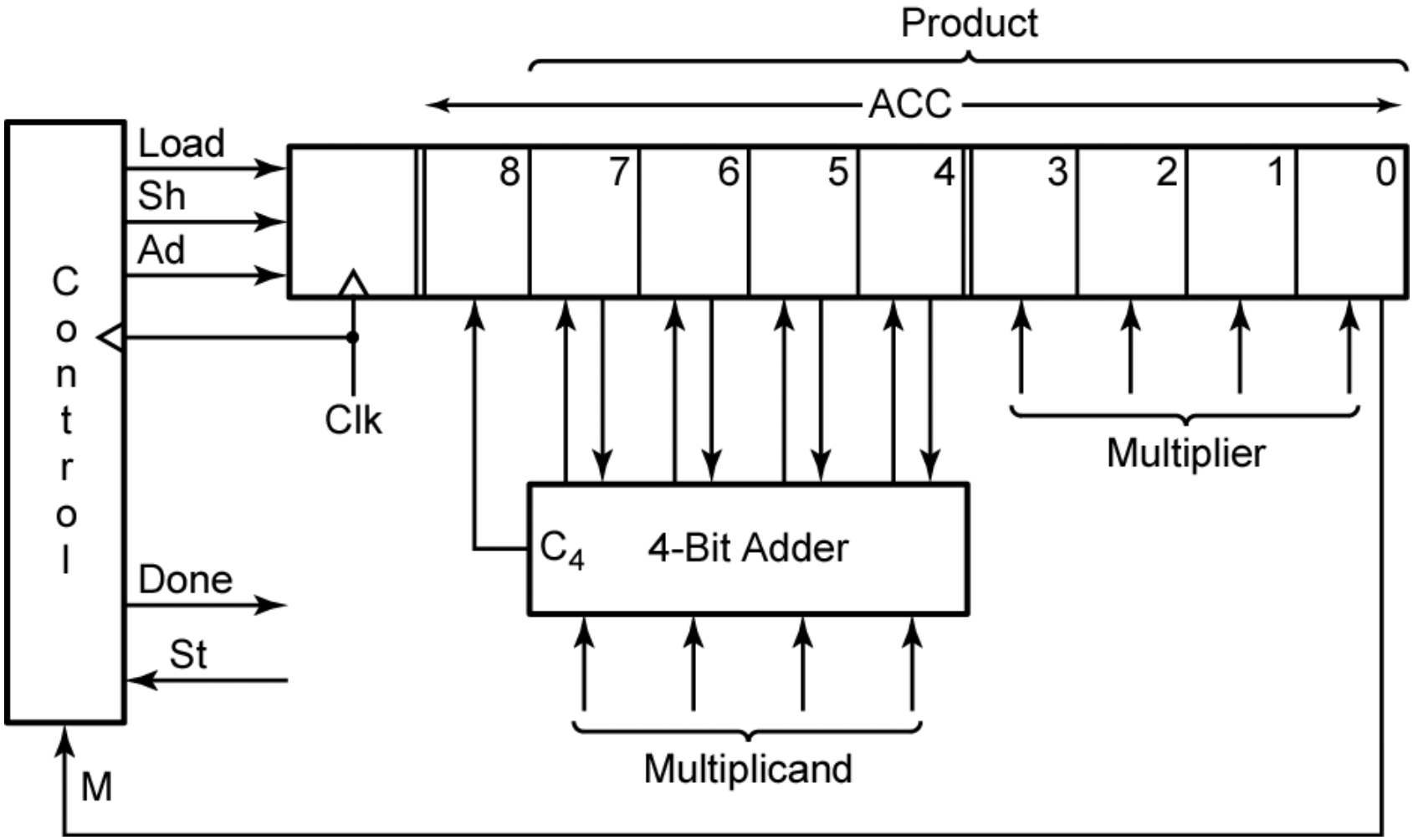
Serial Adder with Accumulator



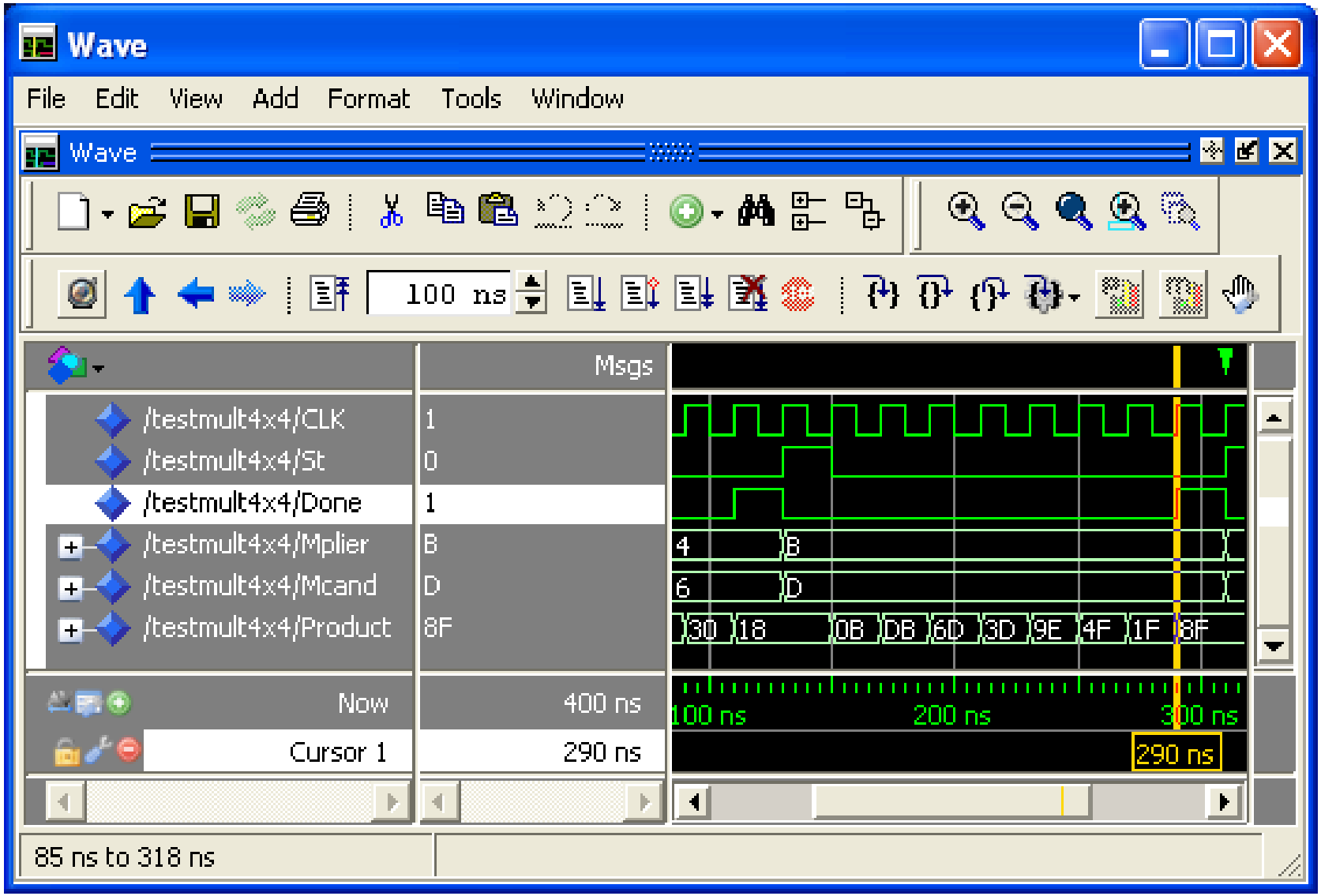
Combinational Multiplier



Parallel Binary Multiplier



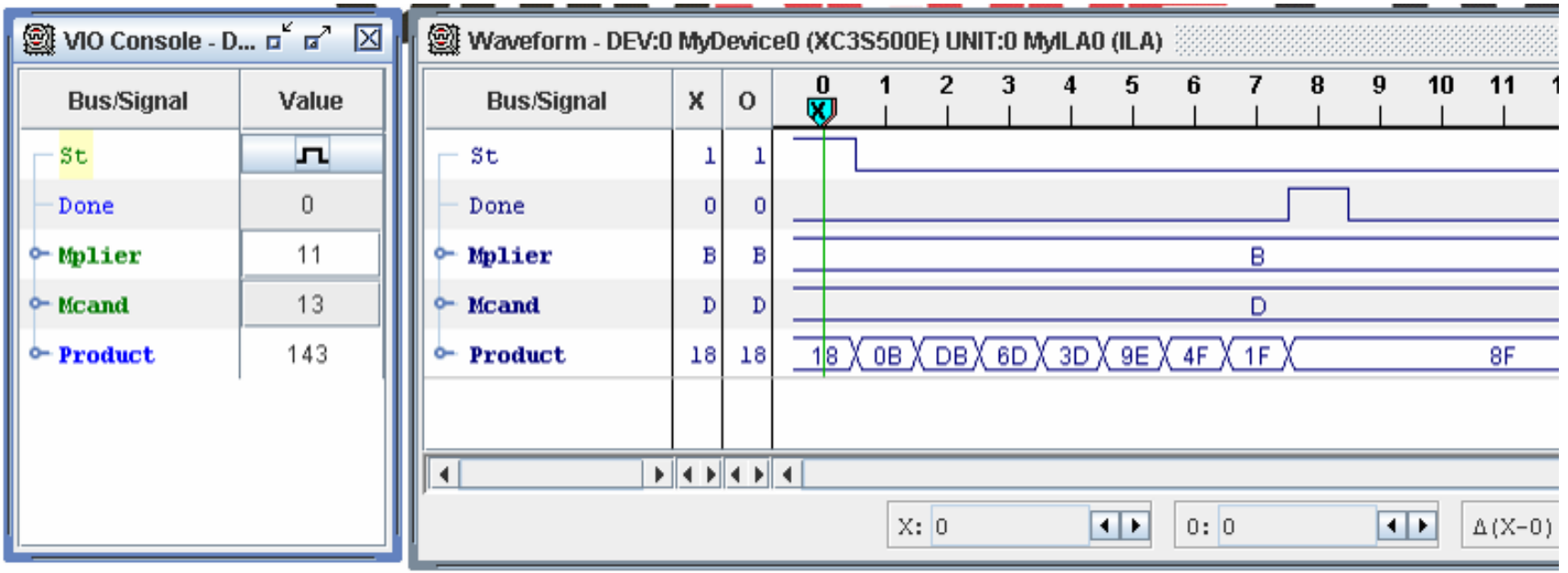
ModelSim Simulation



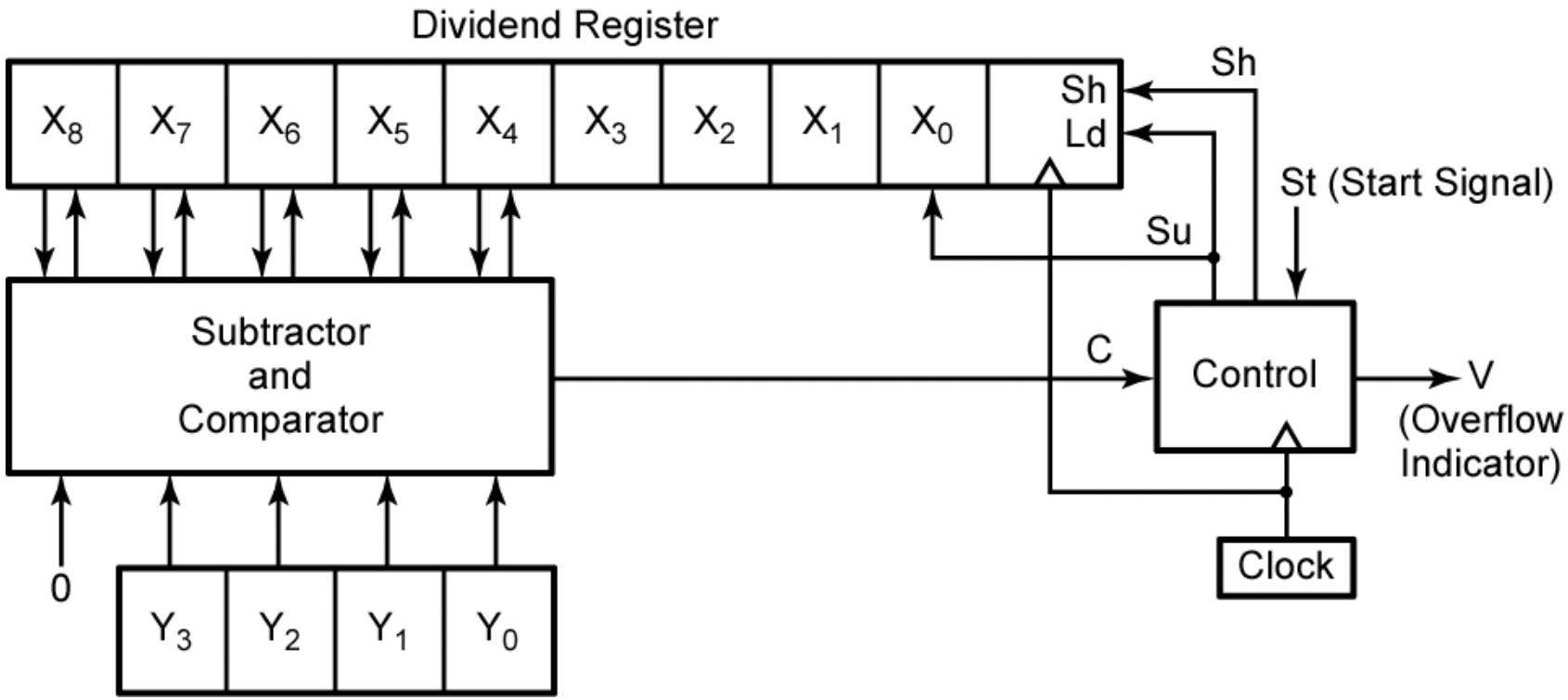
FPGA Implementation

- Xilinx Spartan3e
  - 500K System Gates
  - 50 MHz Clock
- ChipScope Pro
  - Virtual Input/Output Core (VIO)
  - Integrated Logic Analyzer (ILA)
- Real-Time Verification
  - Captures On-chip Signals
  - Off-chip Analysis via JTAG Programming Cable

ChipScope Pro Analyzer



Binary Divider



Summary

- Serial Adder
- Combinational Multiplier
- Parallel Multiplier
  - ModelSim Simulation
  - FPGA Implementation
- Binary Divider