

# BJT and Integrated Circuits

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## Chapter 6 & 9 – THE END!

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ELEC 424

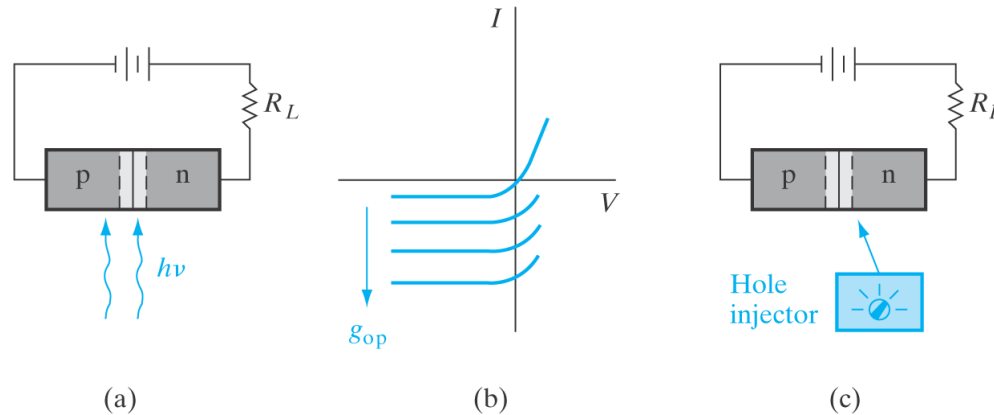
John Peeples

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# Bipolar Junction Transistors

## Reverse Biased P-N Junction

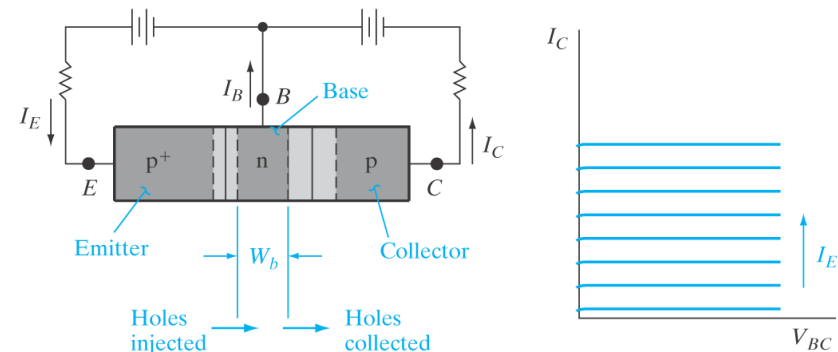
- $I_o$  (reverse saturation current) depends on generation current, not electric field.



# Bipolar Junction Transistors

*Why not use a forward biased  $p^+$ - $n$  junction as the generation source?*

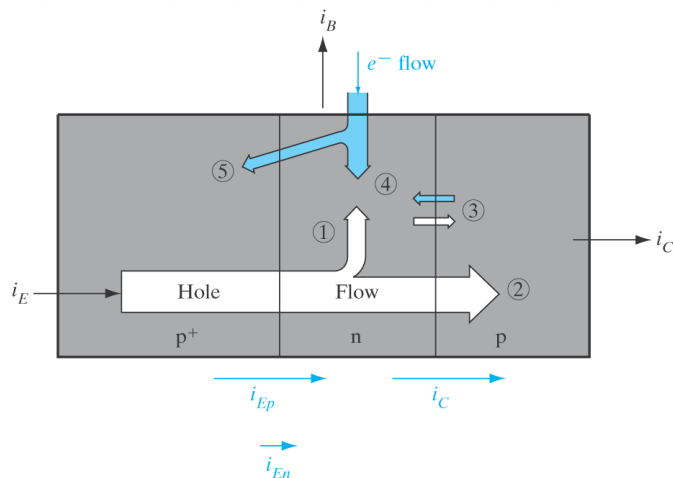
Common Base Configuration



Since the collected current will have little dependence on the load resistance, this is a pretty good constant current source.

# Bipolar Junction Transistors

So, what is really going on?

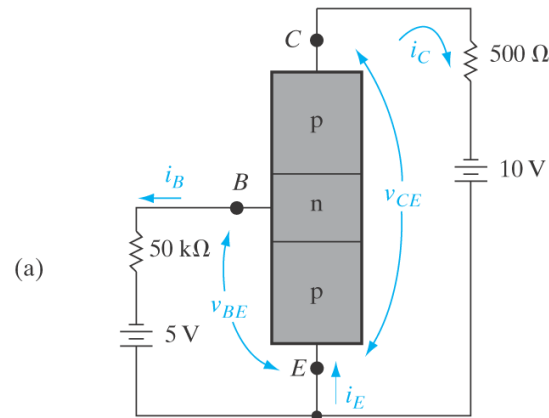


- The base (n) region should be very thin relative to hole lifetime.
- Current at the emitter/base junction should be nearly entirely holes. Thus p<sup>+</sup> doping.

- A small amount of base current recombines with injected holes in the thin base region.
- A very small amount of base current will be injected into the emitter region across the forward biased junction.
- Some holes and electrons will recombine across the base collector junction (thermally generated)

# Bipolar Junction Transistors

## Amplification



$$\tau_p = 10 \mu s$$

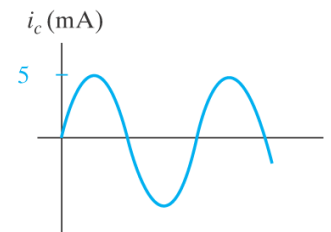
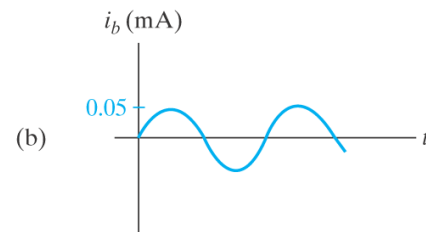
$$\tau_t = 0.1 \mu s$$

$$\frac{i_C}{i_B} = \beta = \frac{\tau_p}{\tau_t} = 100$$

Neglecting  $v_{BE}$

$$I_B = \frac{5 \text{ V}}{50 \text{ k}\Omega} = 0.1 \text{ mA}$$

$$I_C = \beta I_B = 10 \text{ mA}$$



# Semiconductor Processing

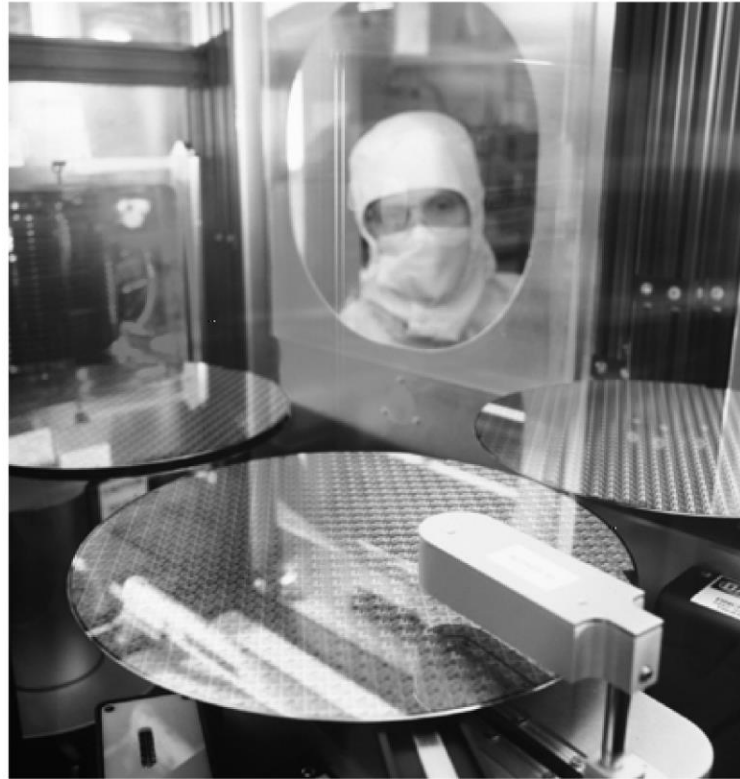
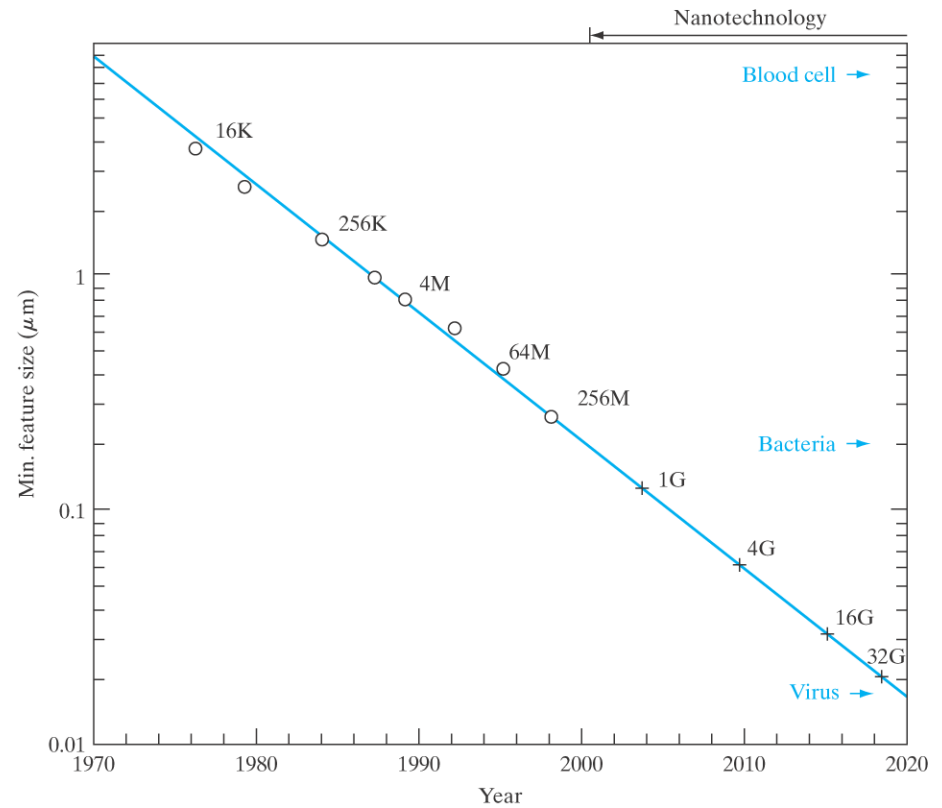
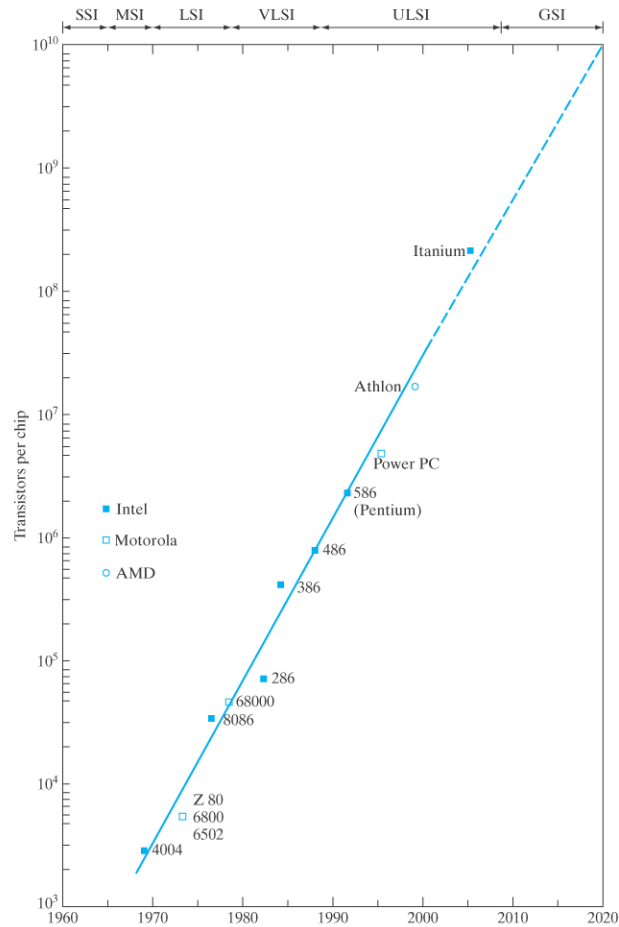


Figure 9.1

A 300-mm diameter (about 12-inch) wafer of integrated circuits. The circuits are tested on the wafer and then sawed apart into individual chips for mounting into packages. (Photograph courtesy of Texas Instruments.)

# Moore's Law



# CMOS

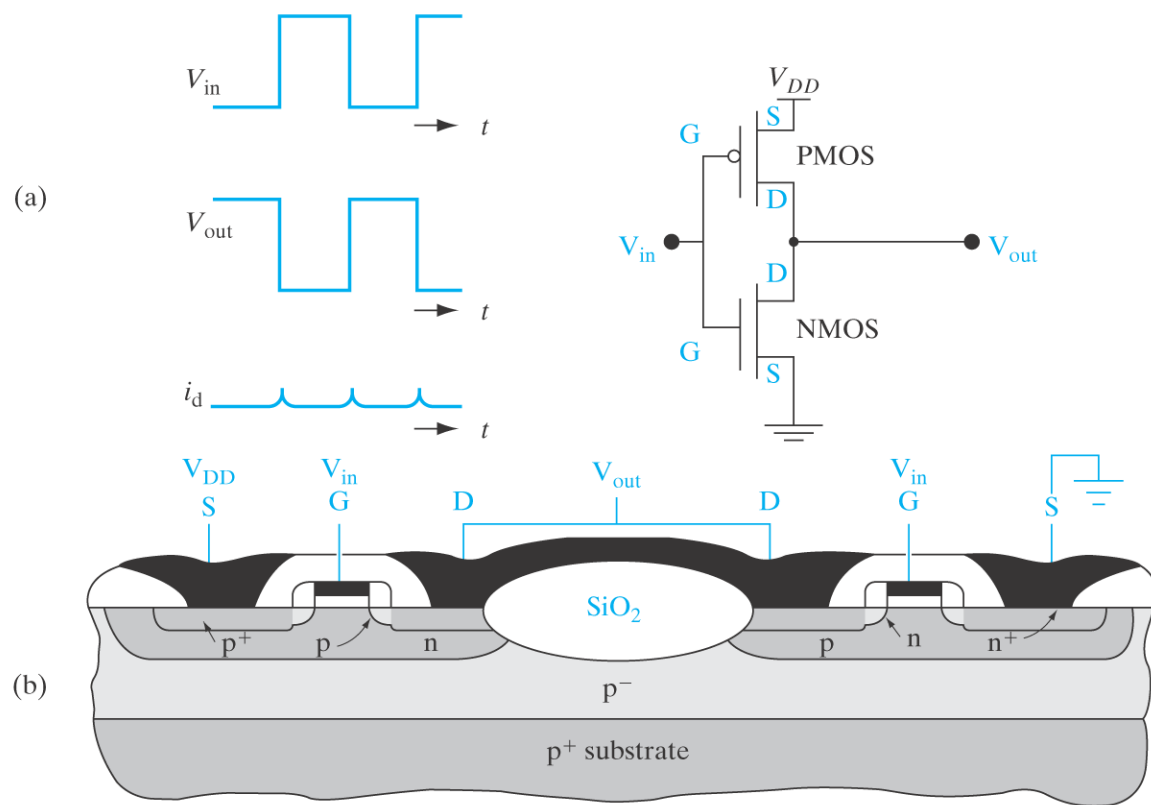
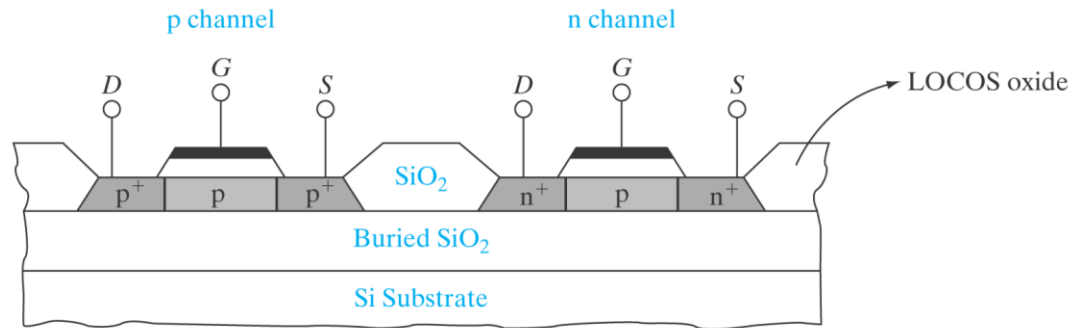


Figure 9.4

Complementary MOS structure: (a) CMOS inverter; (b) formation of p-channel and n-channel devices together.



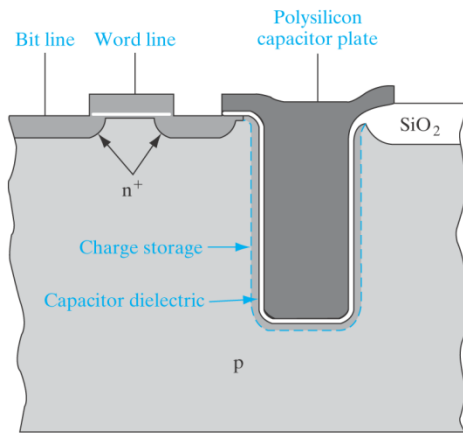
# Speed and Power Enhancements



SOI

Figure 9.11

Silicon on insulator. Both n-channel and p-channel enhancement transistors are made in islands of Si film on the insulating substrate. These devices can be interconnected for CMOS applications.

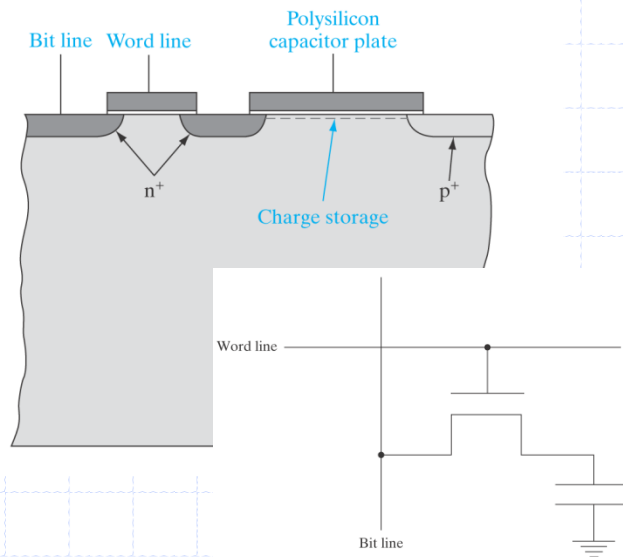
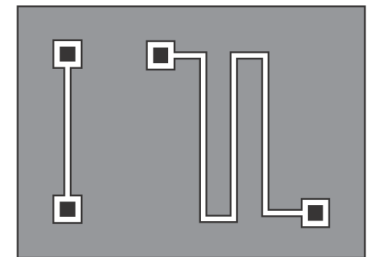
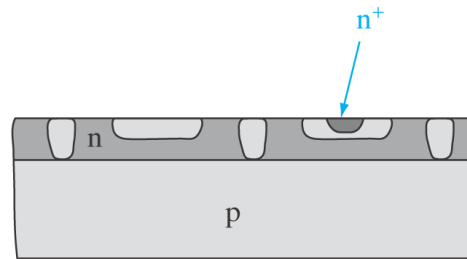


(a)

Vertical Integration

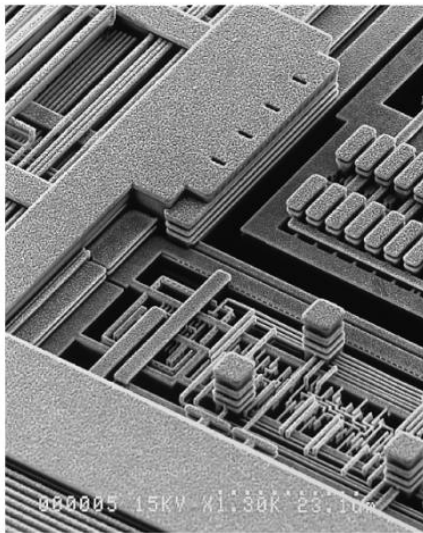
# Resistors and Capacitors are Easy

## Monolithic Resistors

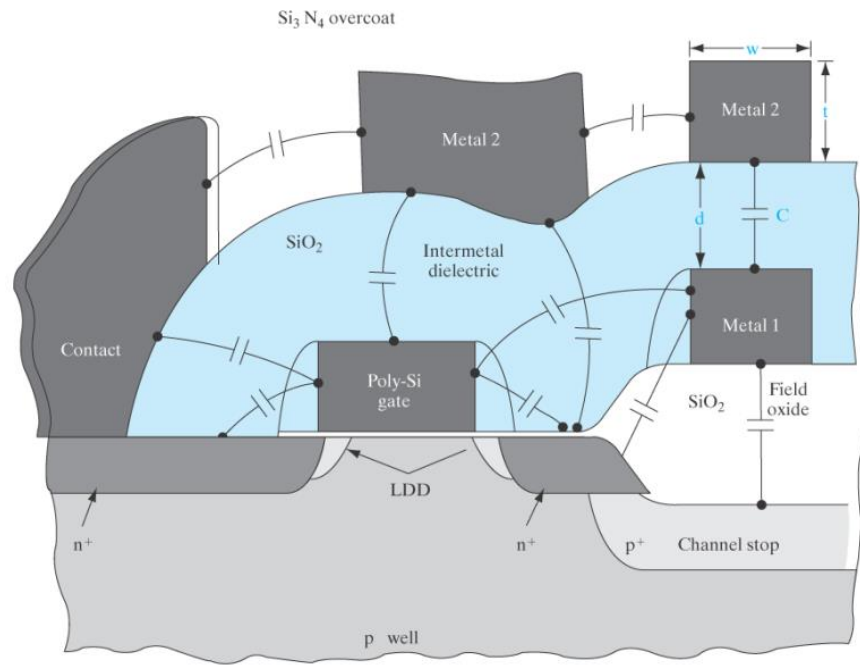


Memory cell capacitor  
and its bit and word lines

# Wires (Interconnections) can be Hard



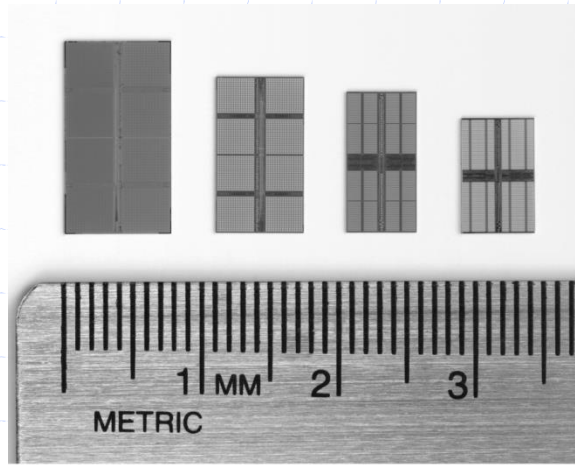
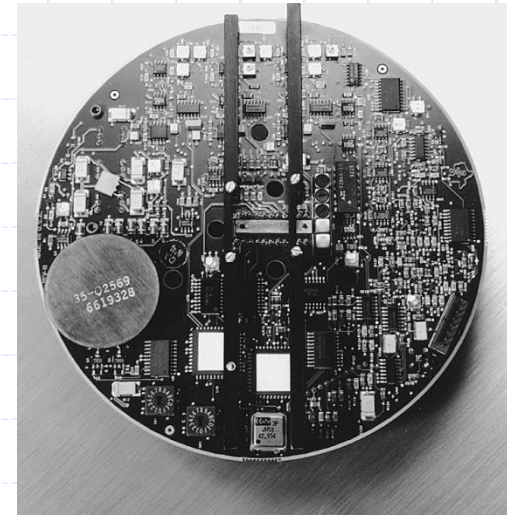
(a)



(b)

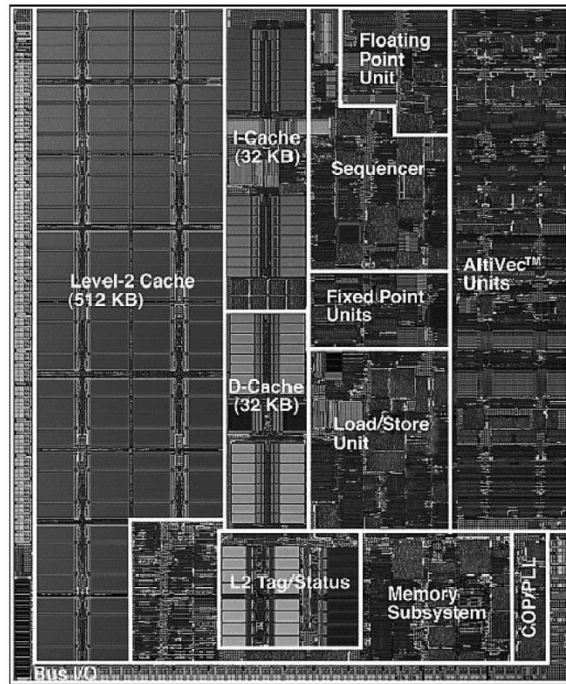
# What Great Applications

CCD Imaging (digital cameras)  
is just a bunch of capacitors.



DRAMS are getting smaller (or  
larger) all the time

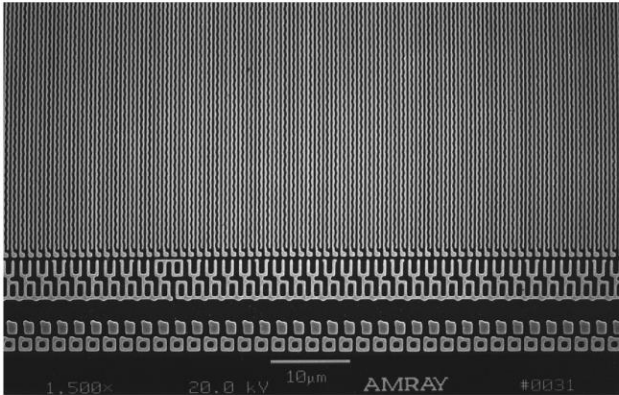
# Smaller Features mean More on Each Chip



G4 Power PC for you Mac fans.

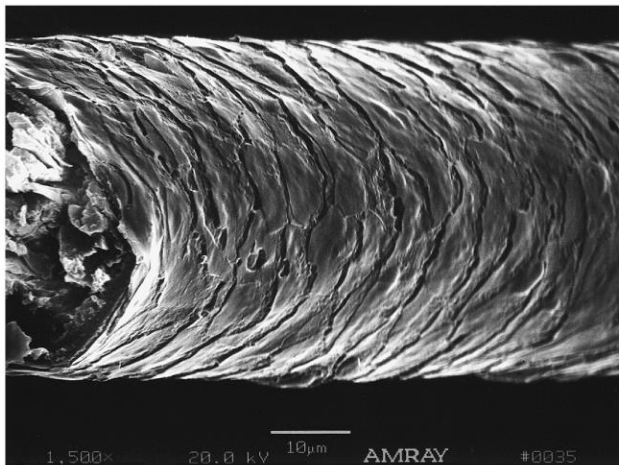
90 nm  
1.5 GHz

# Small is Pretty Small



(a)

180 nm features  
(the thin lines)



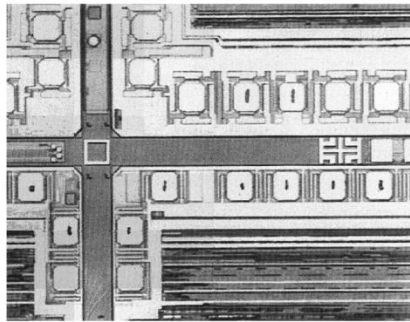
(b)

A big fat human hair

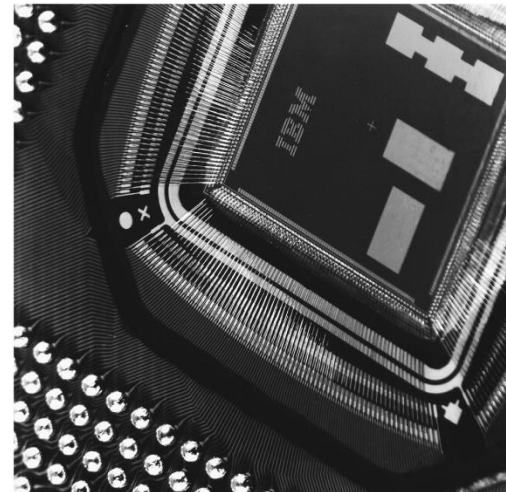


# The Back End is Critical

Testing is expensive



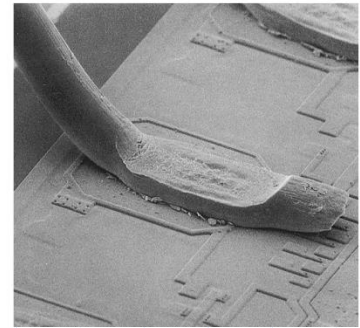
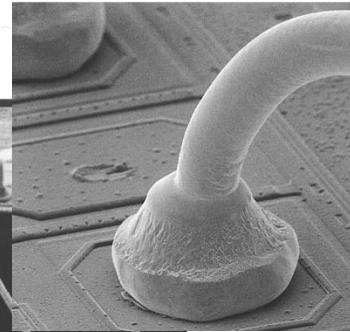
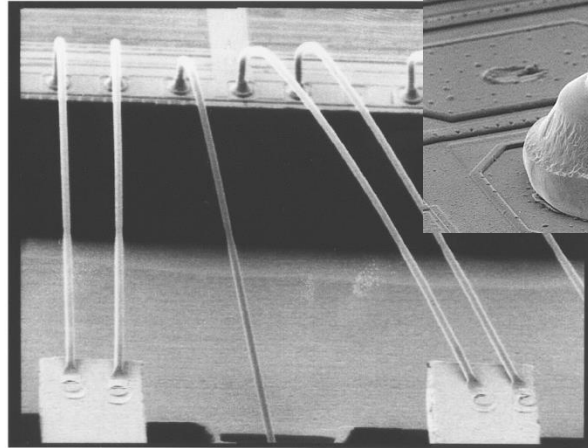
and so is packaging



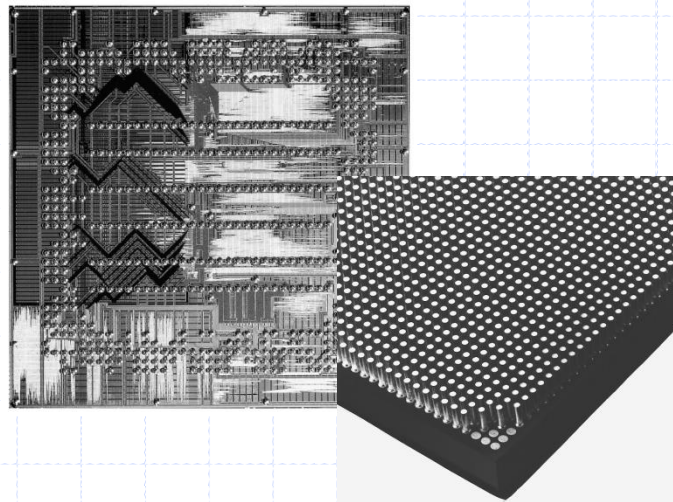
# Many Packaging Options



Cut 'em



Bond 'em

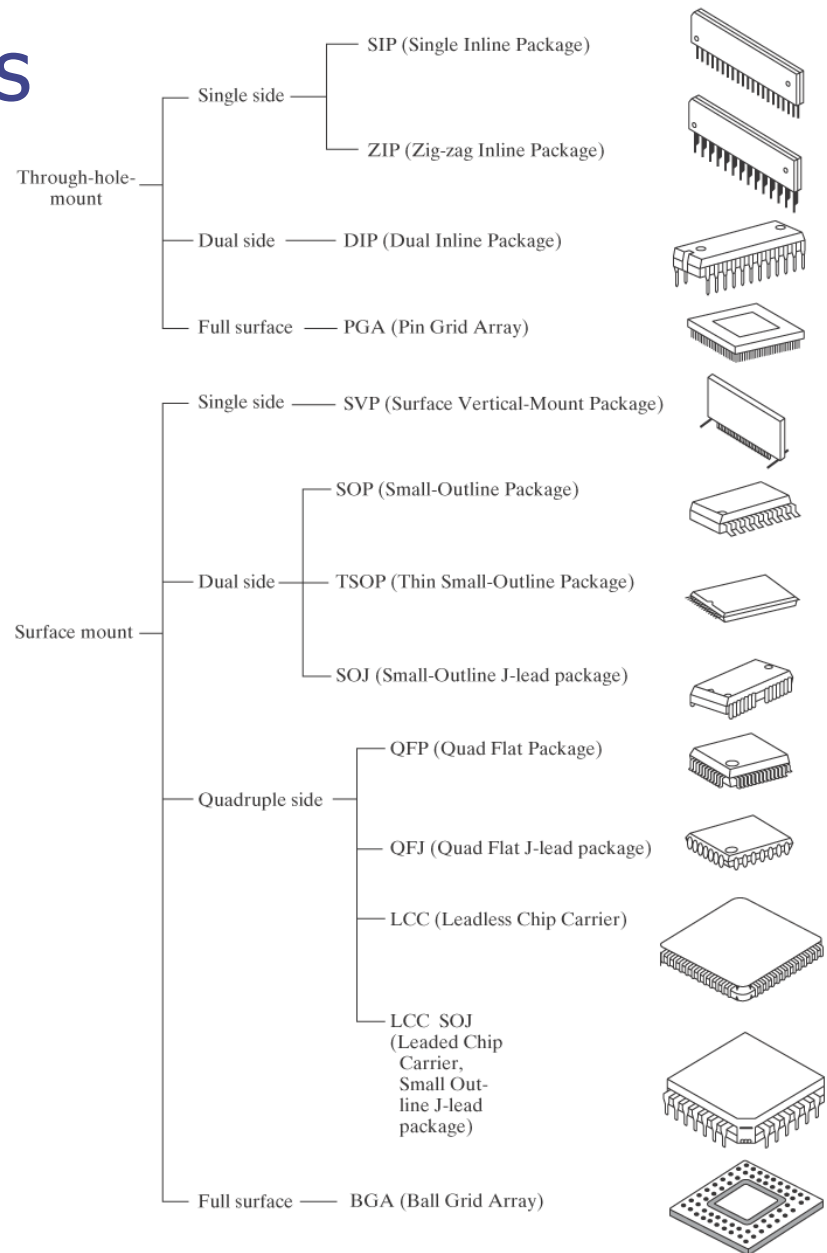


or Flip and/or  
Grid 'em



# Many Packaging Options

Smaller costs initially,  
but once it is commodity,  
is less expensive



# Closing Thought

Regardless of your career choices, you will continue to be influenced by semiconductor technology in your everyday and professional lives. Knowing a little about its genesis, capabilities and promises is a good thing.

Thanks for taking my course.

A handwritten signature in black ink, reading "John W. Bepler". The signature is fluid and cursive, with the first name "John" being the most prominent.

April 18, 2014