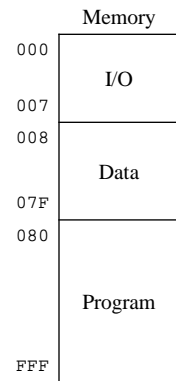
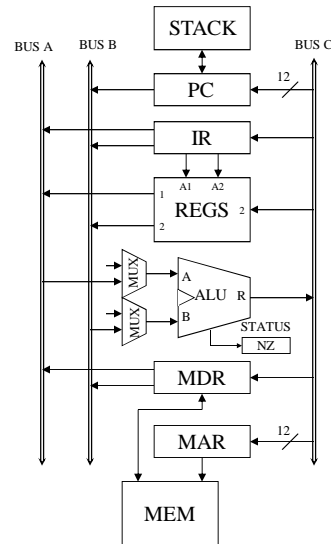
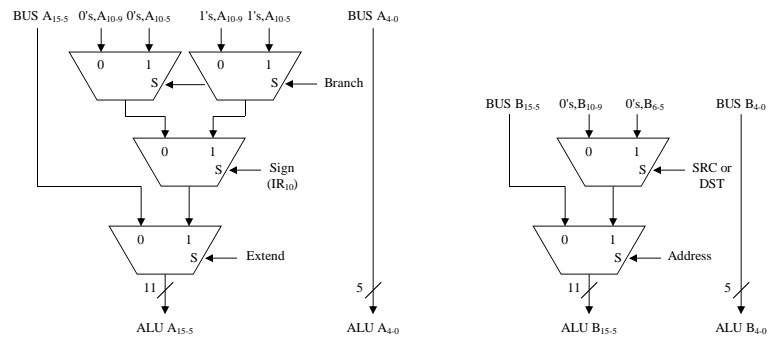


# Instructional Processor



1

# ALU Multiplexers



418\_09

2

## Control Signals

- ◆ BUS\_A
- ◆ BUS\_B
- ◆ REGS\_Read1
- ◆ REGS\_Read2
- ◆ Extend
- ◆ Address
- ◆ ALU\_Op
- ◆ MEM\_Read
- ◆ MEM\_Write
- ◆ Inc\_PC
- ◆ Load\_PC
- ◆ Push\_PC
- ◆ Pop\_PC
- ◆ Load\_IR
- ◆ REGS\_Write
- ◆ Load\_STATUS
- ◆ Load\_MDR
- ◆ Load\_MAR
- ◆ Clear

418\_09

3

## Branch Instruction Format

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

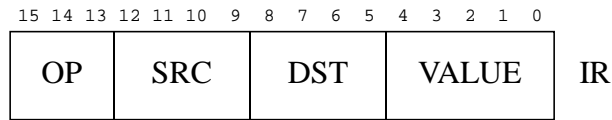


OP	MD	Fn	Assy Lang	RTN
111	00	BRA	BRA Offset	PC ← PC + Offset
	01	BGTZ	BGTZ Offset	PC ← PC + Offset (STATUS > 0)
	10	BSR	BSR Offset	STACK ← PC; PC ← PC + Offset
	11	RTN	RTN	PC ← STACK

418\_09

4

# Data Instruction Format



	Mode	REG #	Name	Syntax	Effective Address
SRC or DST	00	00-11	Register Direct	Rn	EA = Rn
	01	00-11	Register Indirect	(Rn)	EA = [Rn]
	10	vv	Absolute	Value	EA = Value
	11*	vv	Immediate	#Value	Operand = Value

EA = Effective Address  
 vv = Upper 2 bits of Value  
 \* = SRC only

# Data Instructions

OP	Fn	Assembly Language	Register Transfer Notation (RTN)
000	MOVE	MOVE SRC , DST	DST ← SRC
001	ADD	ADD SRC , DST	DST ← SRC + DST
010	INV	INV SRC , DST	DST ← not SRC
011	AND	AND SRC , DST	DST ← SRC and DST
100	ROTL	ROTL SRC , DST	DST ← SRC(14 dt 0) & SRC(15)
...			