# Latches and Flip-Flops

ELEC 311

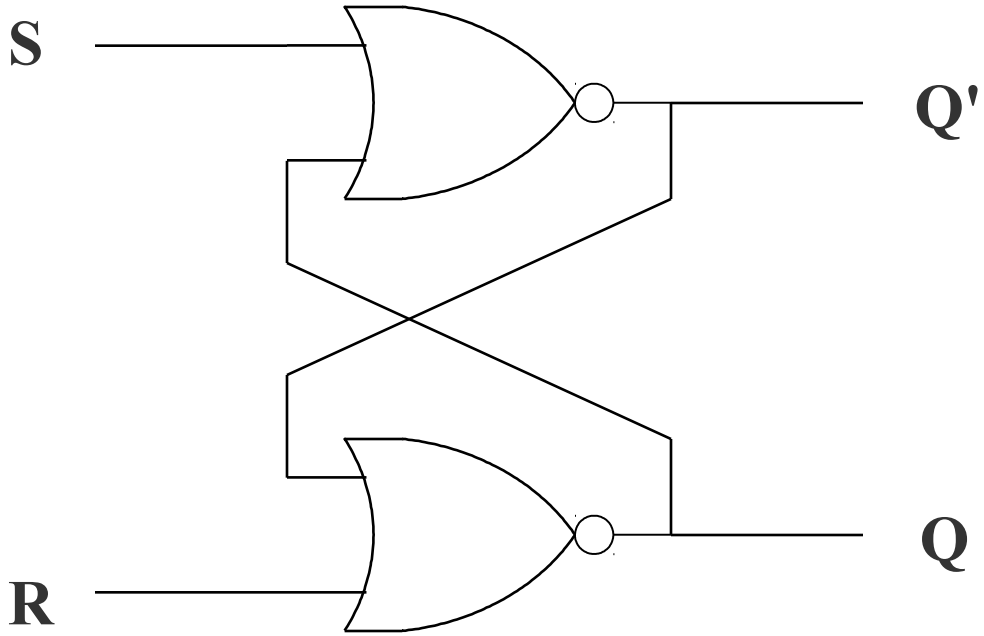
Digital Logic and Circuits

Dr. Ron Hayne

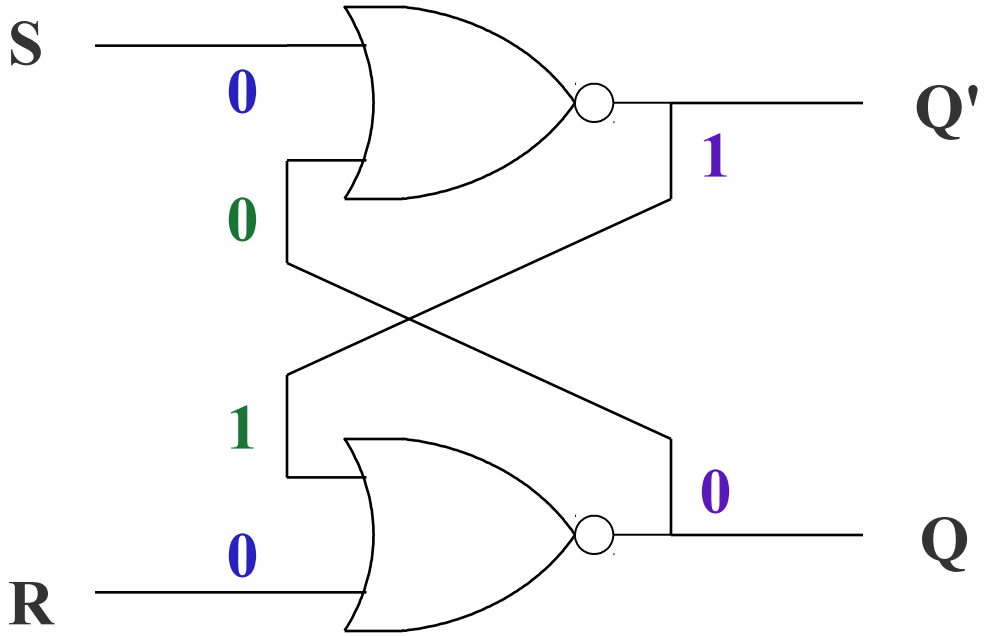
*Images Courtesy of Cengage Learning*

THE CITADEL
DEPARTMENT OF ELECTRICAL & COMPUTER ENGINEERING

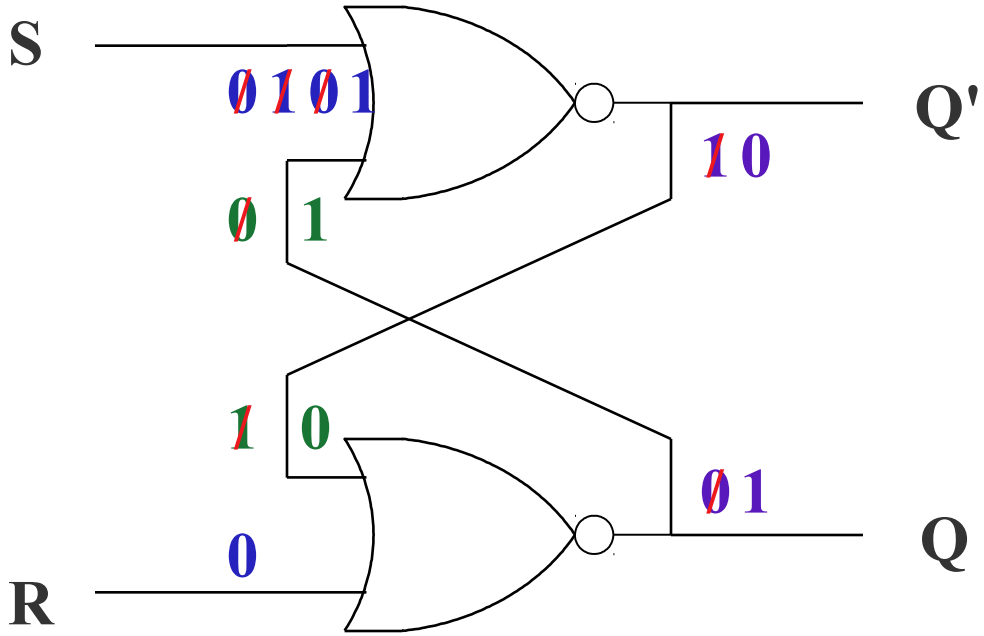
# Set-Reset Latch



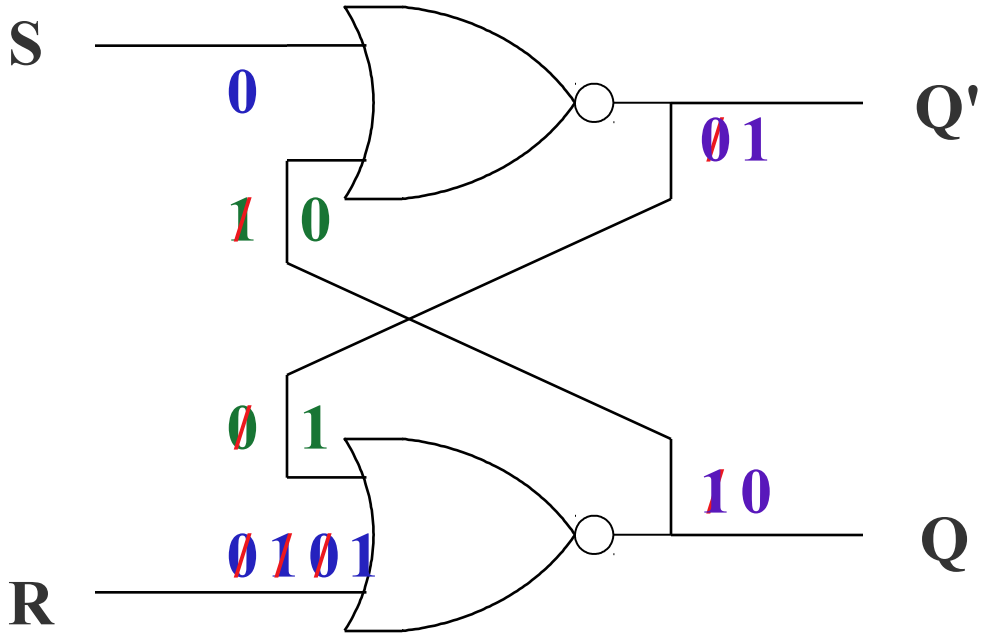
# Set-Reset Latch



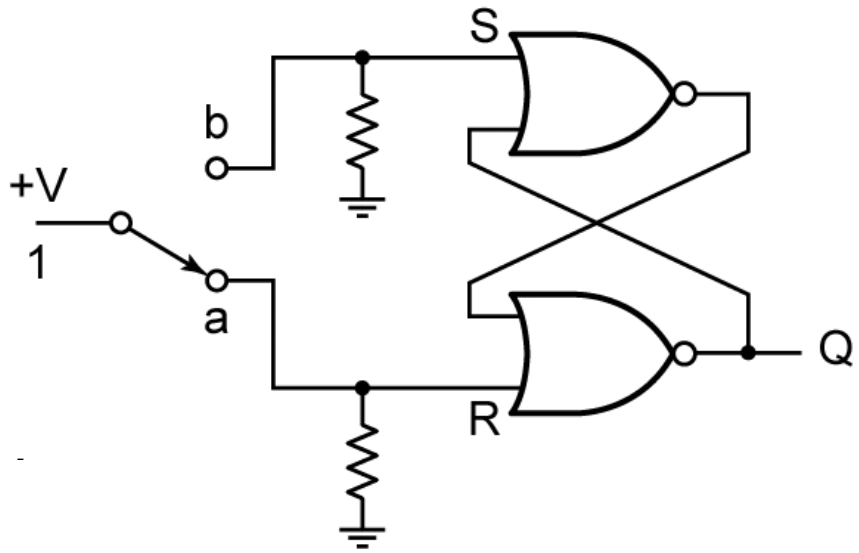
# Set-Reset Latch

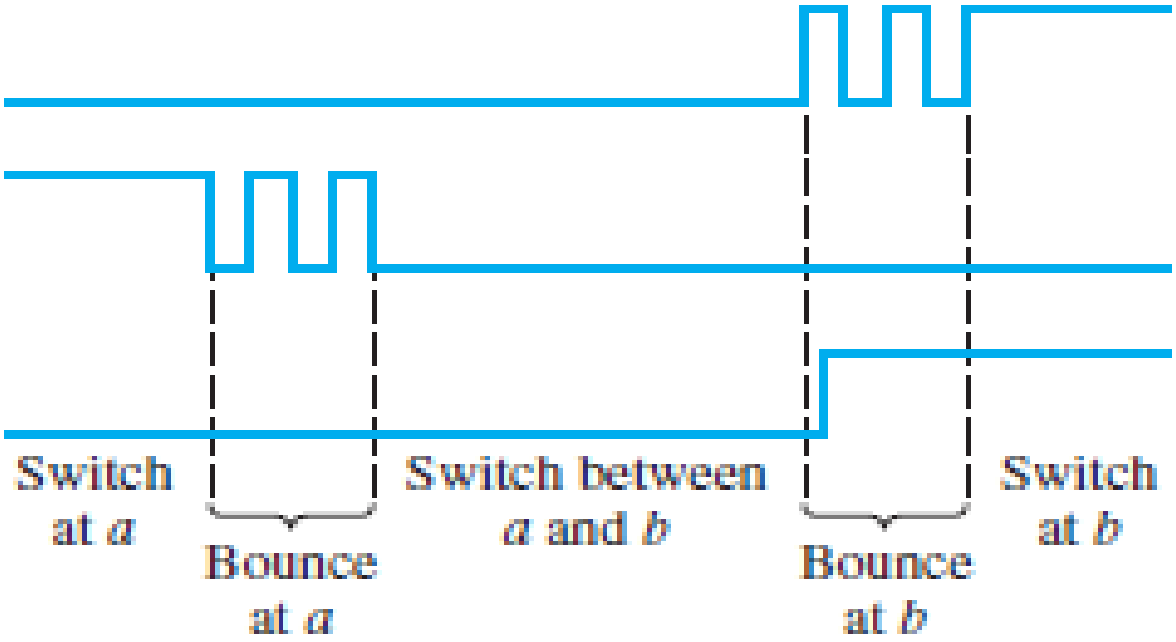


# Set-Reset Latch

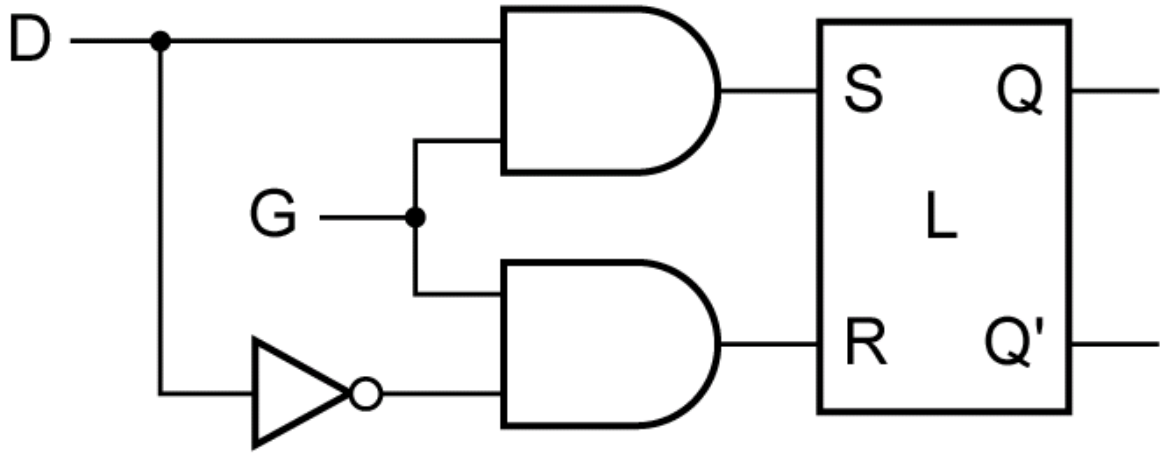


# Switch Debouncing

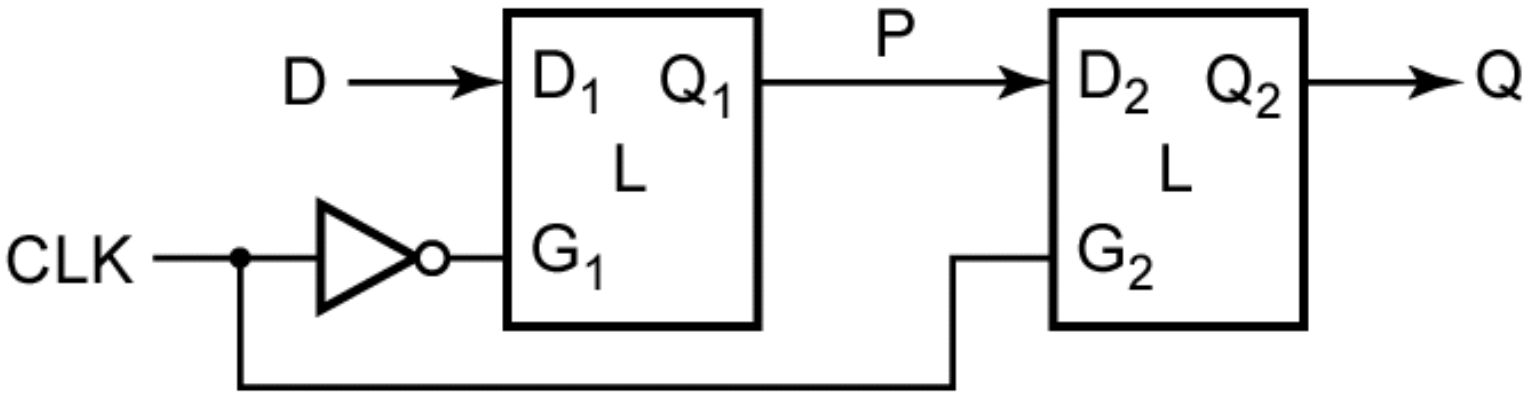


# D Latch



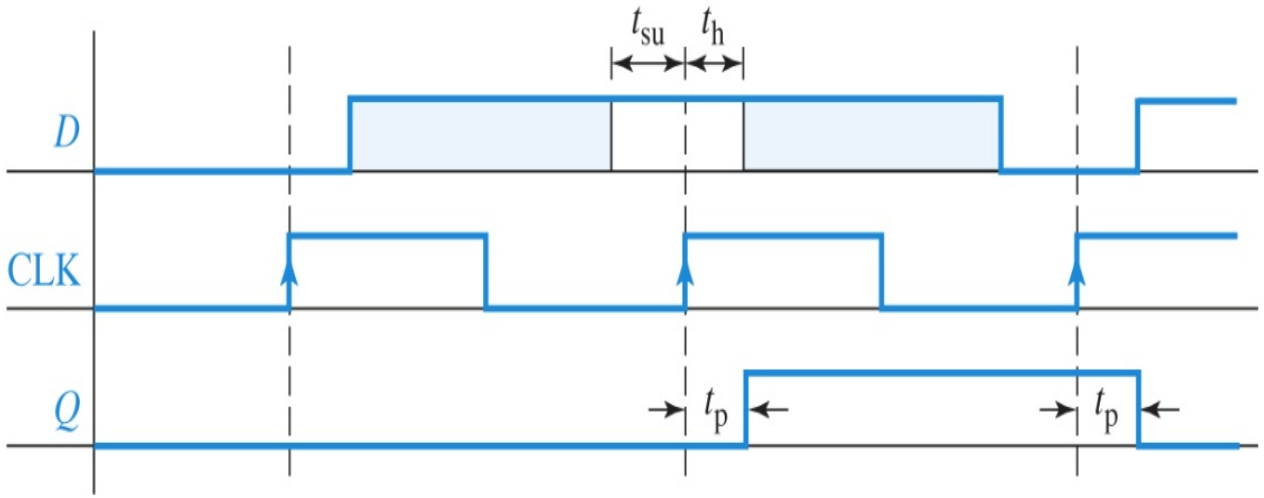
# Edge-Triggered D Flip-Flop



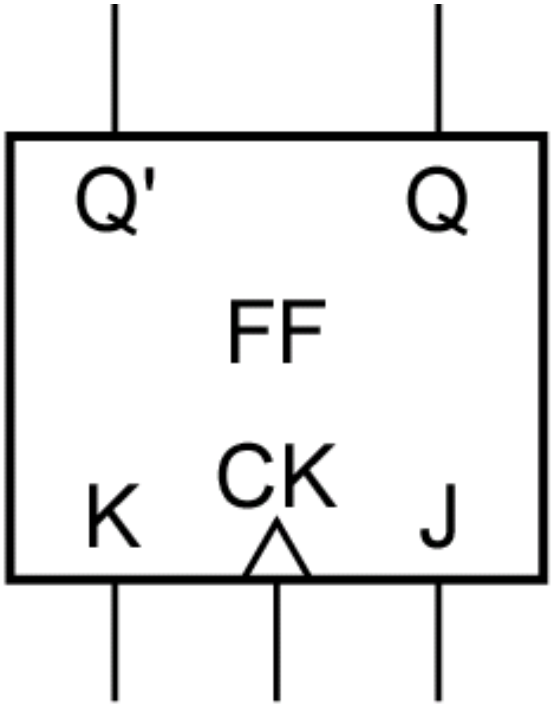
# Timing Parameters

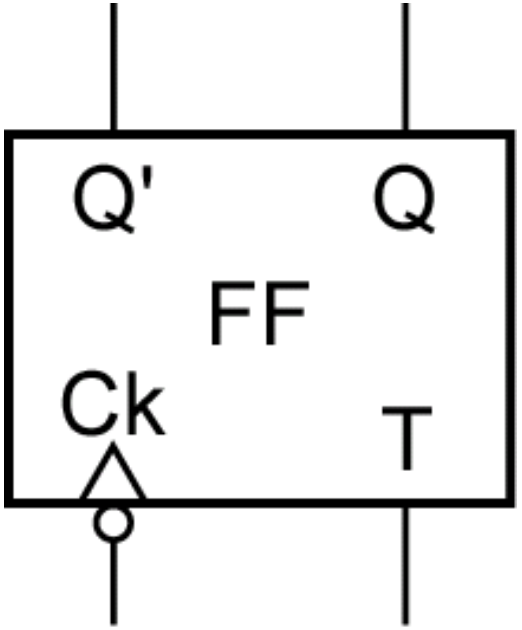
**FIGURE 11-20**
Setup and Hold Times for an Edge-Triggered D Flip-Flop





# J-K and T Flip-Flops

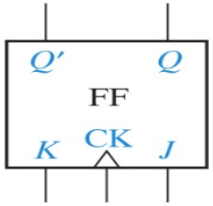


# J-K FF Timing Diagram

**FIGURE 11-24**
J-K Flip-Flop
(*Q* Changes on the Rising Edge)



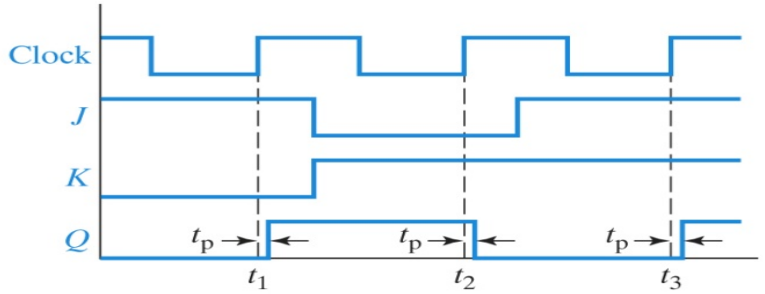



(a) J-K flip-flop

| J | K | Q | $Q^+$ |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |

$$Q^+ = JQ' + K'Q$$

(b) Truth table and characteristic equation

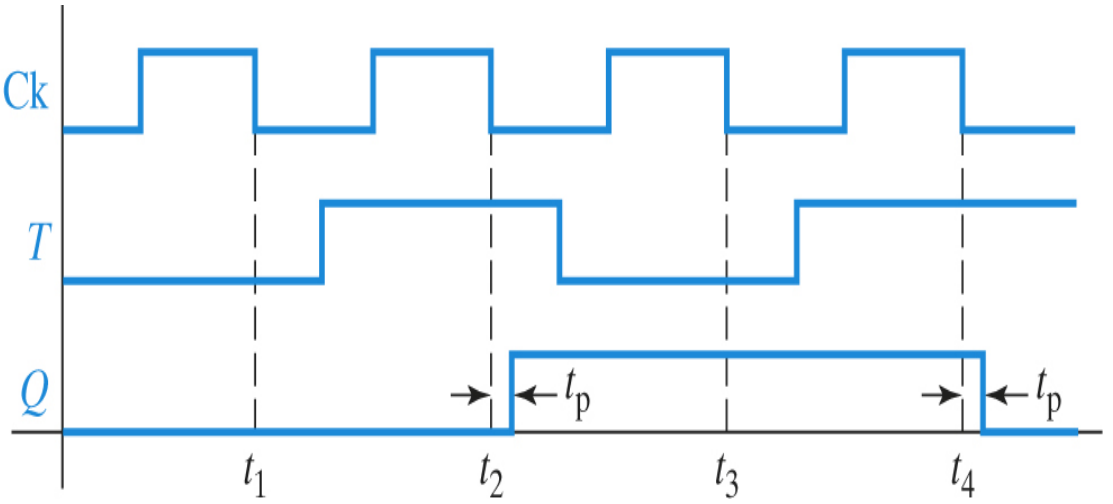



(c) J-K flip-flop timing

# T FF Timing Diagram

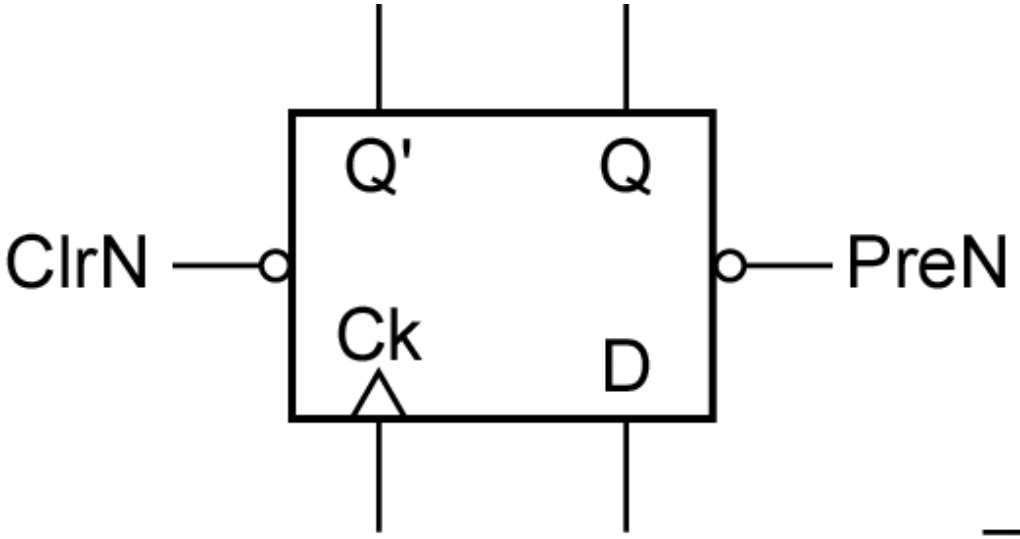
**FIGURE 11-27**
Timing Diagram for T Flip-Flop (Falling-Edge Trigger)

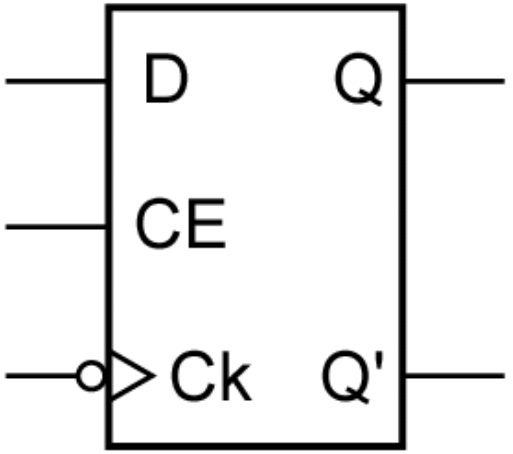




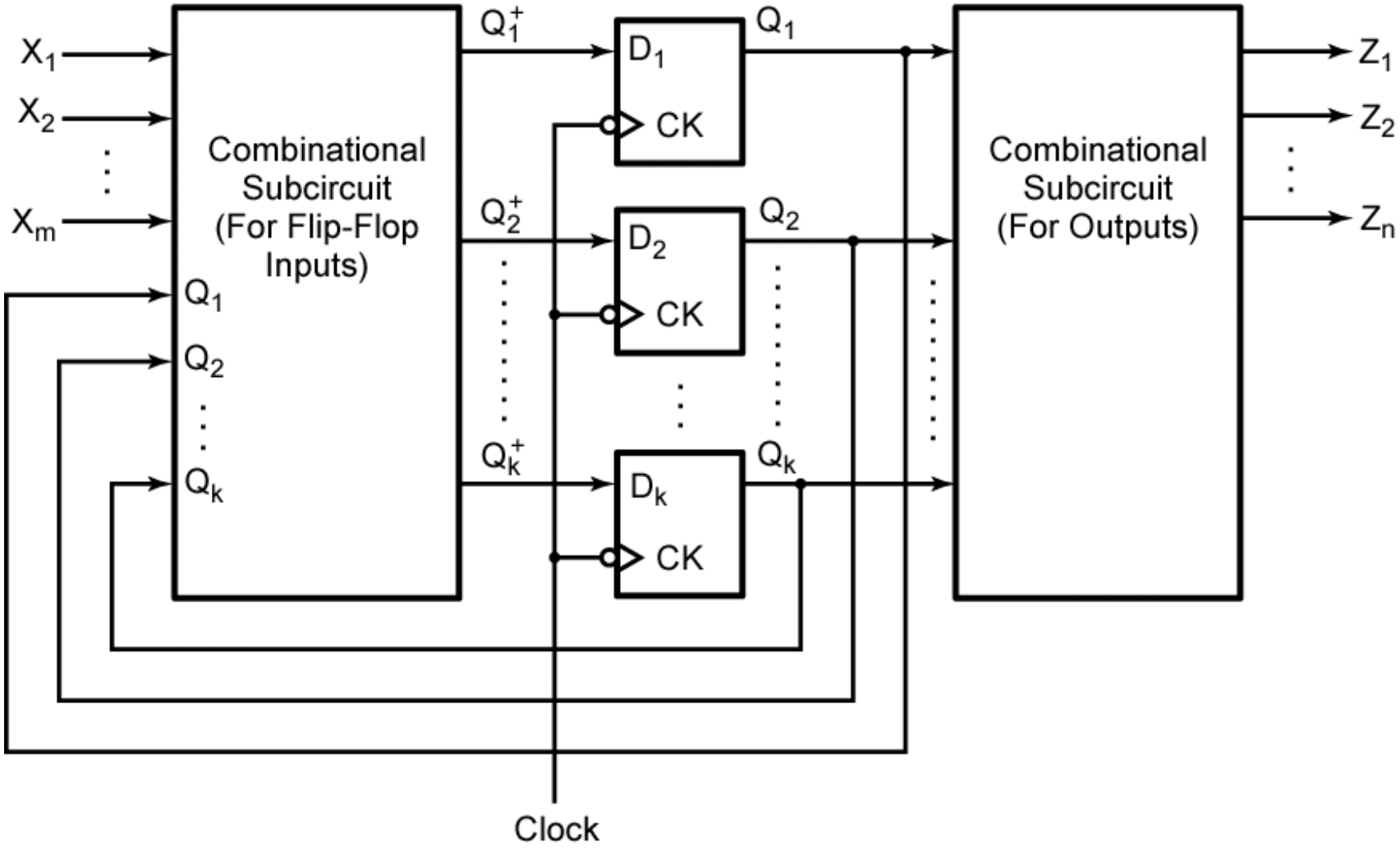

(Falling-Edge Triggered)

# Additional Inputs



# Sequential Circuits



# Summary

- Latches
  - S-R (Set-Reset)
  - D (Data)
- Flip-Flops (Edge-Triggered)
  - D (Data)
  - J-K (Set-Reset-Toggle)
  - T (Toggle)