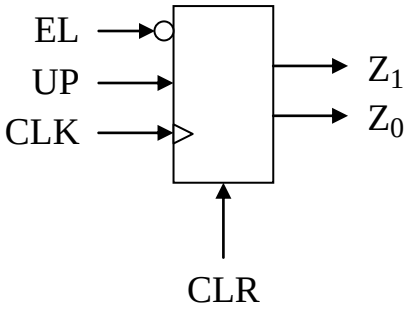
Project 4: Synchronous Design

Objectives

Design and test a synchronous sequential circuit which implements a 2-bit binary counter. Describe the logic circuit using VHDL.

Specific Instructions

Design a 2-bit binary counter with the following characteristics:



- An active-low enable, EL
  - When EL = 0, the counter changes state
  - When EL = 1, the counter maintains its current state
- An active-high control signal, UP
  - When UP = 1, the counter counts up in the sequence 00, 01, 10, 11, 00, …
  - When UP = 0, the counter counts down in the sequence 00, 11, 10, 01, 00, …
- An active-high asynchronous clear, CLR
  - When CLR = 1, the count is reset to 00 (independent of the clock)
- A rising-edge triggered clock, CLK

1. Fill in the transition table below.
2. Derive the next state equations to implement the circuit using D flip-flops.
3. Write a VHDL model to implement the circuit, including the following:
   a. Entity declaration.
   b. Dataflow/Structural architecture using the FDC component from the UNISIM Library and the clock divider from the provided project4_pkg.vhd.
4. Implement the circuit in hardware, using the Spartan3E FPGA on the BASYS Board.
   a. Constrain the design with the following pin assignments.

I/O Name	Location	BASYS	BASYS2
EL	SW1	P36	L3
UP	SW0	P38	P11
CLR	BTN3	P41	A7
CLK	Clock	P54	B8

I/O Name	Location	BASYS	BASYS2
Z(1)	LD1	P14	M11
Z(0)	LD0	P15	M5

   b. Generate a programming file (.bit) for the FPGA.
   c. Download the design onto the BASYS Board.
5. Test the circuit on the BASYS Board.
6. Demonstrate the correct operation of your circuit to your professor and obtain his initials on your cover sheet.
7. Write a project report containing the following:
   a. Cover sheet with project name/number, date, and authors names.
   b. Objective section describing what was to be accomplished.
   c. Discussion section with your circuit design and resulting VHDL description.
   d. Results and Conclusions.

Transition Table

	Inputs		PS		NS		Outputs	
mt	EL	UP	Q_1	Q_0	Q_1^+	Q_0^+	Z_1	Z_0
0	0	0	0	0			0	0
1	0	0	0	1			0	1
2	0	0	1	0			1	0
3	0	0	1	1			1	1
4	0	1	0	0			0	0
5	0	1	0	1			0	1
6	0	1	1	0			1	0
7	0	1	1	1			1	1
8	1	0	0	0			0	0
9	1	0	0	1			0	1
10	1	0	1	0			1	0
11	1	0	1	1			1	1
12	1	1	0	0			0	0
13	1	1	0	1			0	1
14	1	1	1	0			1	0
15	1	1	1	1			1	1