ELEC 313 Lab 5
CMOS Circuits

REFERENCE: Fundamentals of Logic Design, Roth & Kinney, Cengage, Appendix A

OBJECTIVE: The objective of this experiment is to construct and observe the operation of a CMOS inverter and NAND gate.

EQUIPMENT: ALD1105 Dual N-channel and Dual P- channel matched pair MOSFET
Power Supply (Vdc)
Function Generator
Oscilloscope

PRIOR PREPARATION (Pre-Lab):

1. Download and review the specification sheet for the ALD1105 Dual N and P channel matched pair MOSFET.
2. Using your text or other resources review the circuit operation of CMOS Inverter and NAND gate circuits similar to those of figure 1 and figure 2.
3. Annotate a copy of both figure 1 and figure 2 with the appropriate pin numbers from the ALD1105 spec sheet, and place in your lab notebook.
4. Create a truth table for the expected outputs of the NAND gate.

EXPERIMENT

The following procedure will be used to evaluate the CMOS inverter.

1) Construct the circuit of figure 1.
2) Connect the V^+ terminal (Pin 11) to the + supply voltage.
3) Connect the V- terminal (Pin 4) to the circuit ground.
4) Set V_{DD} to 5 volts using the HP source.
5) Use the function generator for input v_i. Set the function generator to a frequency of 20 kHz and select a triangle wave. Set the wave for 0 to 5 volts using the offset.
6) Connect CHANNEL 1 of the oscilloscope to the input and CHANNEL 2 to the output.
7) Use the x-y plot function of the scope to produce the transfer characteristic v_o vs. v_i. (Press the main key, then the *xy* softkey, then adjust the voltage scales as needed.)
8) Capture the v_o vs. v_i data, so you can recreate the plot for the lab report.
9) Adjust the amplitude and offset of the function generator for an input square wave of 0 to 5 V *as measured on the oscilloscope.*
10) Adjust the scope and capture both input and output on one screen for the report.
11) Measure the propagation delay times of the output waveform.

The following procedure will be used to evaluate the CMOS NAND gate.

1) Construct the circuit of figure 2.
2) Connect the V^+ terminal (Pin 11) to the + supply voltage.
3) Connect the V- terminal (Pin 4) to the circuit ground.
4) Set the + supply voltage to 5 volts DC using the HP source.
5) Set input A to 0 volts.

6) Use the function generator for input B. Set the function generator to a frequency of 20 kHz and select a square wave. Set the square wave for 0 to 5 volts using the offset.
7) Connect CHANNEL 1 of the oscilloscope to the input and CHANNEL 2 to the output.
8) Adjust the scope and capture both input and output on one screen for the report.
9) Repeat step 8 with input A set to +5 volts.

LAB REPORT

Your report should be completed in the format requested by the instructor. The lab report should be in standard format and include the following additional items:

1) Using the transfer characteristic for the inverter, explain the circuit operation.
2) Discuss the operation of the NAND gate circuit and explain how it achieves its truth table.
3) Discuss how the screen capture relates to the truth tables for the NAND gate circuit.

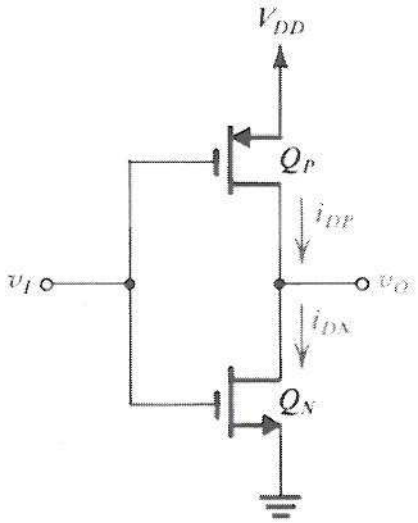


Figure 1: CMOS Inverter.

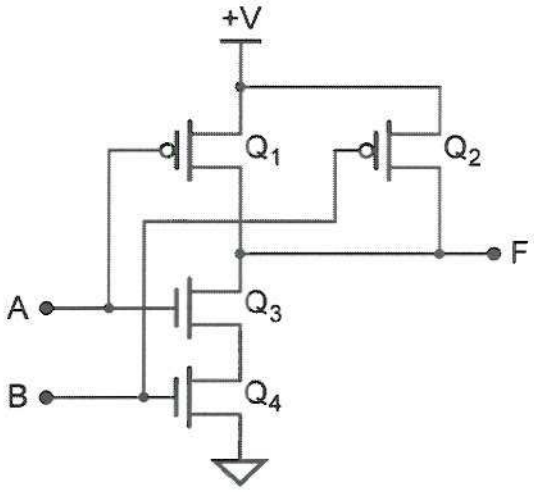


Figure 2: CMOS NAND Gate.

DUAL N-CHANNEL AND DUAL P-CHANNEL MATCHED PAIR MOSFET

GENERAL DESCRIPTION

The ALD1105 is a monolithic dual N-channel and dual P-channel complementary matched transistor pair intended for a broad range of analog applications. These enhancement-mode transistors are manufactured with Advanced Linear Devices' enhanced ACMOS silicon gate CMOS process. It consists of an ALD1116 N-channel MOSFET pair and an ALD1117 P-channel MOSFET pair in one package. The ALD1105 is a low drain current, low leakage current version of the ALD1103.

The ALD1105 offers high input impedance and negative current temperature coefficient. The transistor pair is matched for minimum offset voltage and differential thermal response, and it is designed for precision signal switching and amplifying applications in +1V to +12V systems where low input bias current, low input capacitance and fast switching speed are desired. Since these are MOSFET devices, they feature very large (almost infinite) current gain in a low frequency, or near DC, operating environment. When used in complementary pairs, a dual CMOS analog switch can be constructed. In addition, the ALD1105 is intended as a building block for differential amplifier input stages, transmission gates, and multiplexer applications.

The ALD1105 is suitable for use in precision applications which require very high current gain, beta, such as current mirrors and current sources. The high input impedance and the high DC current gain of the field effect transistors result in extremely low current loss through the control gate. The DC current gain is limited by the gate input leakage current, which is specified at 30pA at room temperature. For example, DC beta of the device at a drain current of 3mA at 25°C is = 3mA/30pA = 100,000,000.

FEATURES

- Thermal tracking between N-channel and P-channel pairs
- Low threshold voltage of 0.7V for both N-channel & P-channel MOSFETs
- Low input capacitance
- Low Vos -- 10mV
- High input impedance -- $10^{13}\Omega$ typical
- Low input and output leakage currents
- Negative current (I_{DS}) temperature coefficient
- Enhancement mode (normally off)
- DC current gain 10^9
- Matched N-channel pair and matched P-channel pair in one package

ORDERING INFORMATION

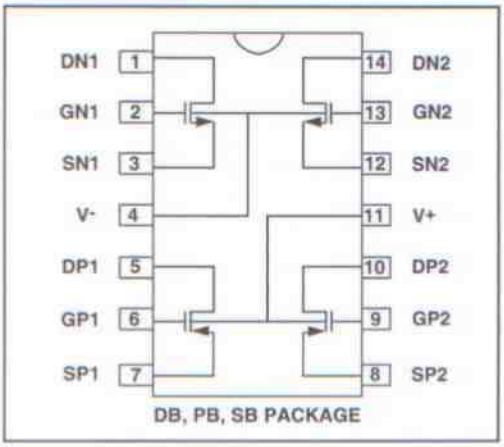
Operating Temperature Range*		
-55°C to +125°C	0°C to +70°C	0°C to +70°C
14-Pin CERDIP Package	14-Pin Plastic Dip Package	14-Pin SOIC Package
ALD1105 DB	ALD1105 PB	ALD1105 SB

* Contact factory for industrial temperature range.

APPLICATIONS

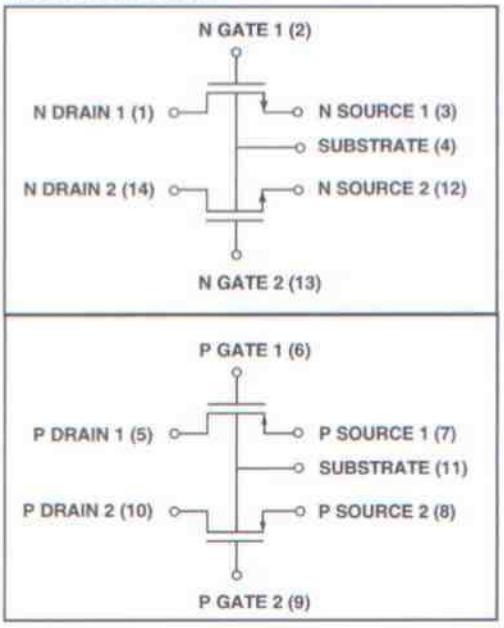
- Precision current mirrors
- Complementary push-pull linear drives
- Discrete Analog switches
- Analog signal Choppers
- Differential amplifier input stage
- Voltage comparator
- Data converters
- Sample and Hold
- Analog current inverter
- Precision matched current sources

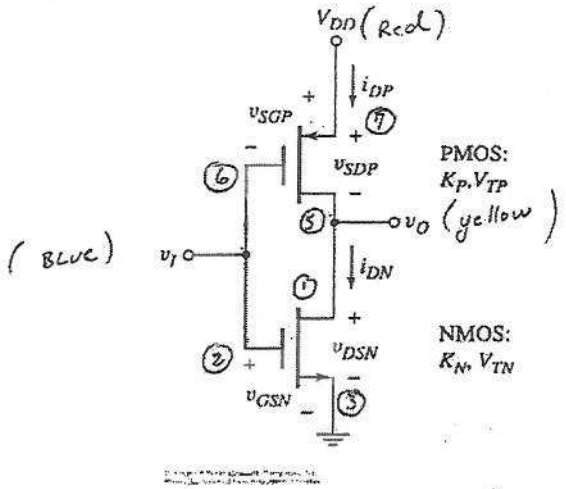
PIN CONFIGURATION



DB, PB, SB PACKAGE

BLOCK DIAGRAM





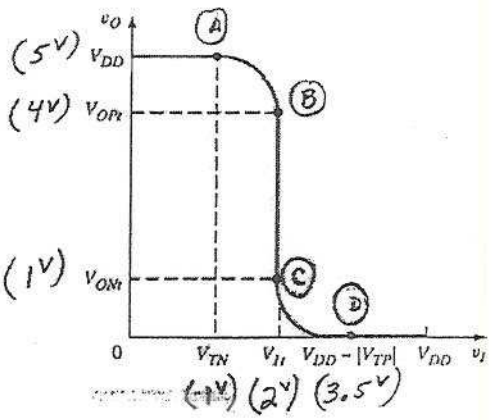


Figure (2) CMOS INVERTER & transfer characteristic.

(A) $v_I < V_{TN}$ Q_N off, Q_P ON

$I_{DN} = 0 = I_{DP} \Rightarrow V_{SDP} = 0 \Rightarrow \boxed{V_O = V_{DD}}$

(B) $v_I > V_{TN}$ Q_N SAT, Q_P NON SAT

$$v_{It} = \frac{V_{DD} + V_{TP} + \sqrt{\frac{K_N}{K_P}}(V_{TN})}{1 + \sqrt{\frac{K_N}{K_P}}}$$ EQN 16.41

V_S V_G

$V_O = V_{DD} - V_{SDP(SAT)} = V_{DD} - (V_{DD} - V_{It} + V_{TP})$

$\boxed{V_{OPt} = V_{It} - V_{TP}}$

(C) $V_I > V_{It}$ Q_N non SAT, Q_P SAT

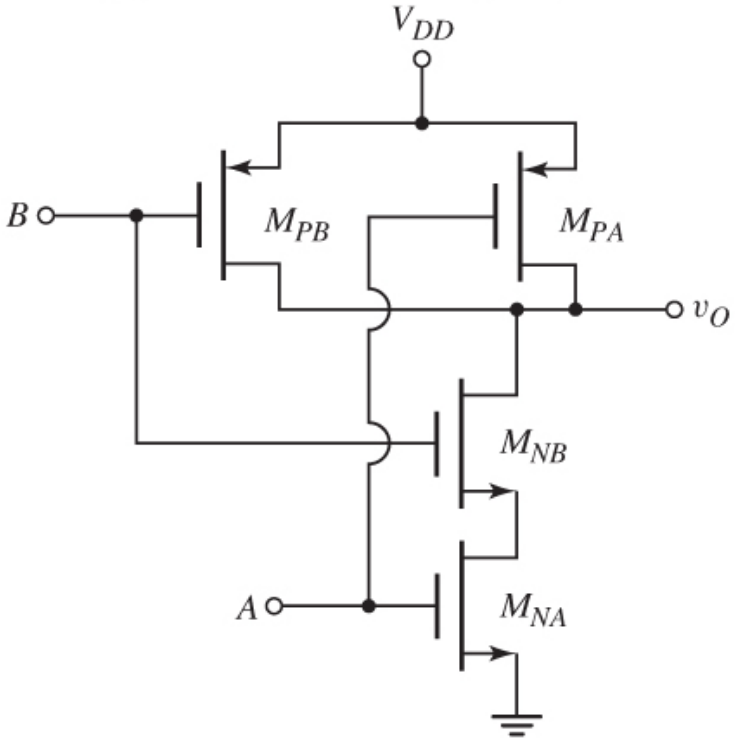
$V_O = V_{DSN(SAT)} = V_{GSN} - V_{TN}$

$\boxed{V_O = V_{It} - V_{TN}}$

(D) $V_I > \{V_{DD} - |V_{TP}|\}$ Q_N ON, Q_P OFF

$V_O = V_{DSN} = 0$ Since $I_{DP} = 0 \Rightarrow I_{DN} = 0 \Rightarrow V_{DSN} = 0$

CMOS NAND GATE



(a)

A	B	v_O
0	0	V_{DD}
V_{DD}	0	V_{DD}
0	V_{DD}	V_{DD}
V_{DD}	V_{DD}	0

(b)