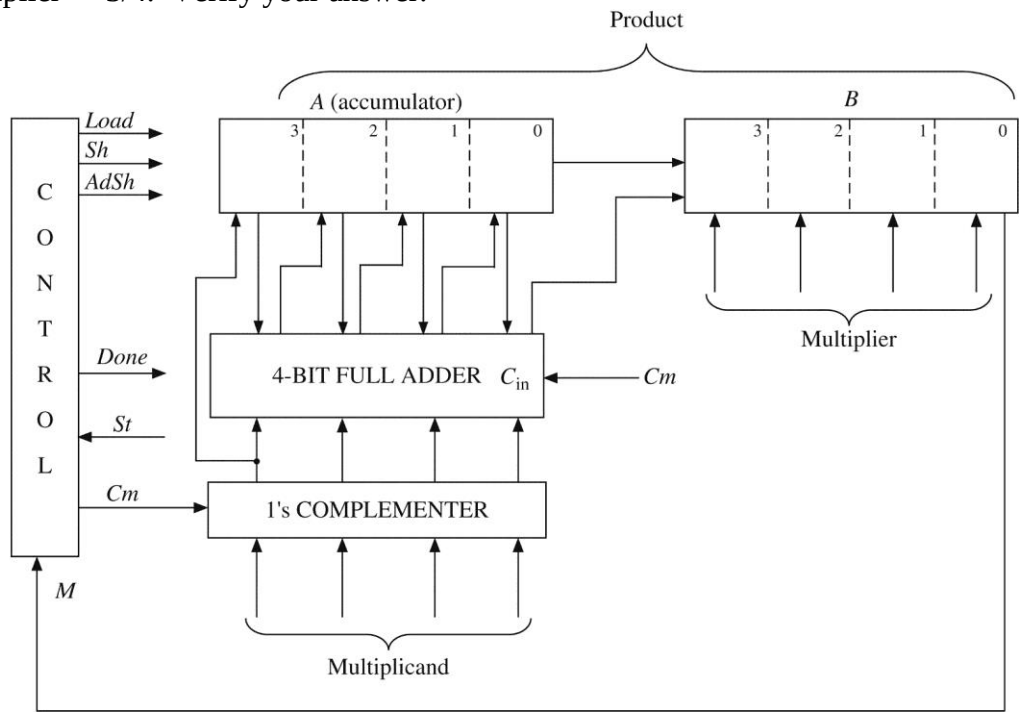
1. Given the block diagram for the signed 2's complement multiplier below, show the contents of registers A and B for each clock cycle when the multiplicand = -1/4 and the multiplier = -3/4. Verify your answer.



2. Design a BCD adder that adds two BCD numbers (0 to 9) and produces a sum in BCD. The circuit should correct the sum by adding 6 if it is out of range. Assume that the two BCD numbers are already loaded into two 4-bit registers (A and B) and that there is a 5-bit sum register (SUM).

a) Illustrate the process for 8 + 7.
b) Draw a block diagram of the system using multiplexers to select the appropriate inputs to a single 4-bit adder at each step. Define and label all control signals.
c) Draw the state graph for the control circuit.