ELEC 311 Test 1 Review

<u>TOPICS</u>

Number Systems
 - Base conversion (2, 10, 16)
 - Negative numbers: sign and magnitude, 2's complement
 - Arithmetic: addition (subtraction), overflow, multiplication
Codes
 - BCD, Gray, ASCII
Boolean Algebra
 - Logic gates: AND, OR, NOT, XOR
 - Circuit analysis: logic equations, truth tables
 - Laws and theorems: identity, complements, simplification (adjacency)
 - Sum-of-products (SOP), product-of-sums (POS)
Combinational Design
 - Word problem -> truth table
 - Minterms and Maxterms
 - Incompletely specified functions (don't cares)
 - Propagation delay, timing diagrams, and hazards
Minimizing Switching Functions
 - Adjacency theorem, essential prime implicants
 - Karnaugh maps
 - Quine McCluskey
NAND and NOR Gates
 - DeMorgan's Laws
 - SOP -> NAND-NAND, POS -> NOR-NOR
 - CMOS logic gates
 - Noise Margin

<u>Practice Questions</u>

1. Perform the following subtraction using 8-bit 2's complement arithmetic and verify your answer in base 10.

$$5.A_{16} - 3.2_{16} = \underline{\hspace{2cm}}_{16}$$

2. Minimize the following function using a Karnaugh-map and draw a NAND-NAND circuit diagram that implements your result.

$$F(A,B,C,D) = \Sigma m(1,9,11,12,13) + \Sigma d(0,3)$$

3. Minimize the function above using Quine-McCluskey.

4. Design a truth table for a combinational logic circuit which indicates whether the difference between 2 bits is greater than or equal to a 3rd bit.

5. Determine the noise margin of a CMOS NAND gate with the following specs:
$$V_{OHmin} = 3.9 \text{ V}, V_{OLmax} = 0.2 \text{ V}, V_{IHmin} = 2.8 \text{ V}, V_{ILmax} = 1.4 \text{ V}$$