ELEC-311
Project 2
Combinational Circuit Design

Charles Pittman

October 1, 2013

1 Objective

- Given a function, design a combinational logic logic circuit.
- Minimize the circuit using a Karnaugh map.
- Create the circuit using only NAND gates.

2 Discussion

The circuit to be constructed was a 2-bit comparator. A 2-bit comparator takes two 2-bit numbers, $P = P_1P_0$ and $Q = Q_1Q_0$, and produces an output, $GT = 1 \iff P > Q$. The truth table describing this function is shown in Table 1. This can be displayed more concisely as a summation of min-terms: $\sum_m(P_1, P_0, Q_1, Q_0) = (4, 8, 9, 12, 13, 14)$.

Using a Karnaugh map (Fig 1), a minimal form of the function was found: $GT = P_0\overline{Q_1Q_0} + P_1P_0\overline{Q_0} + P_1\overline{Q_1}$. This function was then translated into the circuit shown in Fig 2.

The NAND gate is considered to be a functionally complete set because any logic function can be created with only NAND gates. This is demonstrated graphically in Figure 4. Using these conversions, the circuit was again translated into one using only NAND gates (Fig 3), and truth table verified (not shown).

3 Results

mt	P	Q	P_1	P_0	Q_1	Q_0	GT $(P > Q)$
0	0	0	0	0	0	0	0
1	0	1	0	0	0	1	0
2	0	2	0	0	1	0	0
3	0	3	0	0	1	1	0
4	1	0	0	1	0	0	1
5	1	1	0	1	0	1	0
6	1	2	0	1	1	0	0
7	1	3	0	1	1	1	0
8	2	0	1	0	0	0	1
9	2	1	1	0	0	1	1
10	2	2	1	0	1	0	0
11	2	3	1	0	1	1	0
12	3	0	1	1	0	0	1
13	3	1	1	1	0	1	1
14	3	2	1	1	1	0	1
15	3	3	1	1	1	1	0

Table 1: Truth table for 2-bit comparator.

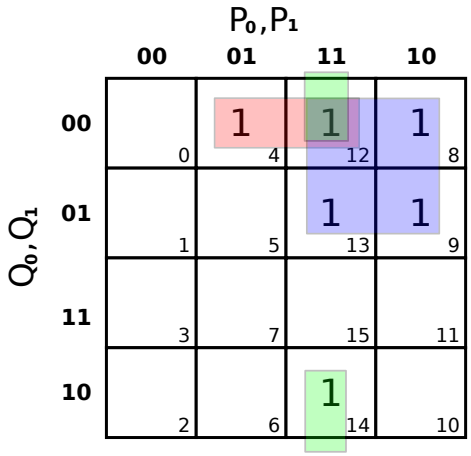


Figure 1: Karnaugh map used to minimize function.

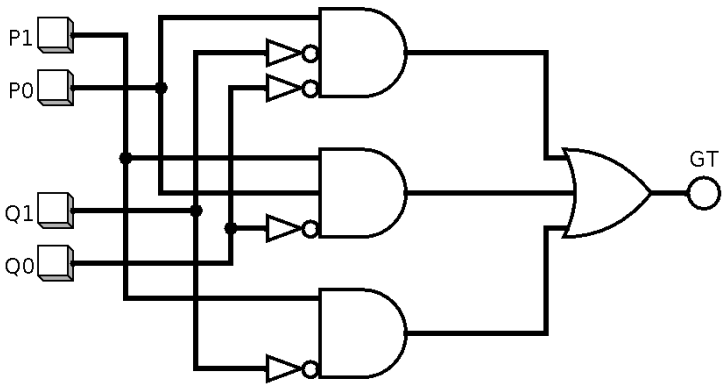


Figure 2: Circuit implemented from function.

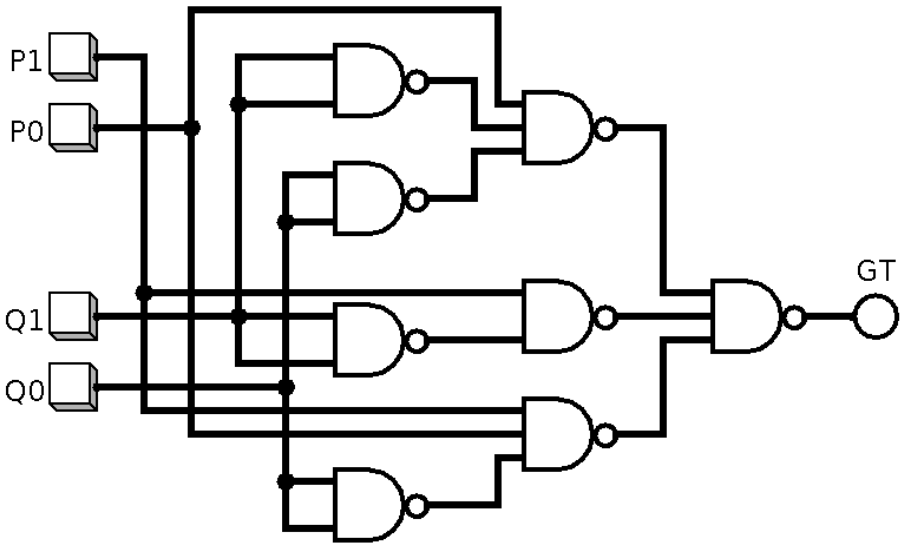
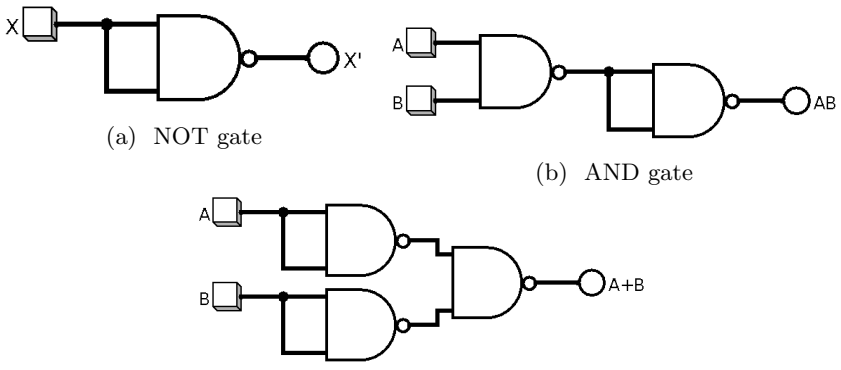


Figure 3: Identical circuit using only NAND gates.



(a) NOT gate

(b) AND gate

(c) OR gate

Figure 4: NAND implementing other logic functions.