ELEC-311
Project 1
Combinational Circuit Analysis

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1 Objective

First Objective

Analyze a combinational logic circuit and determine its behavior.

Second Objective

Use the Xilinx ISE Design Suite to simulate the logic circuit and program a field-programmable gate array (FPGA) board to verify the behavior.

2 Discussion

The circuit being studied is shown in Figure 1. Working from right to left, the Boolean equation for the circuit can be written: $(\overline{S} \cdot I_0 + I_1) \cdot E \cdot (I_0 + S \cdot I_1)$. A truth table for this equation is shown below.

After sketching the circuit with the Xilinx schematic capture, the logic was translated to run on a Basys2 (FPGA board used). Switches on the board were used to input a string of bits, with an LED showing the function's result.

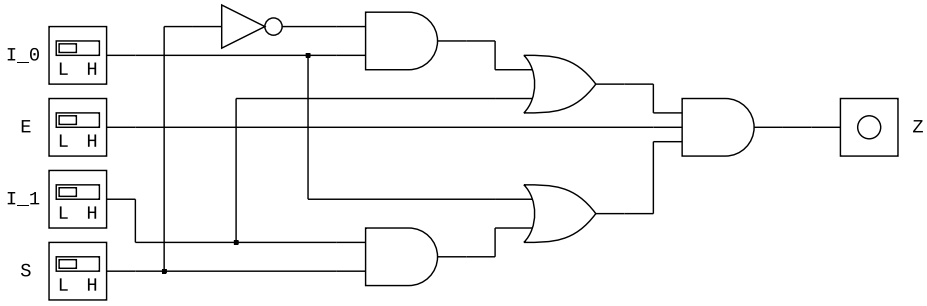

Figure 1: Circuit to be analyzed.

I_0	E	I_1	S	Z	I_0	E	I_1	S	Z
0	0	0	0	0	1	0	0	0	0
0	0	0	1	0	1	0	0	1	0
0	0	1	0	0	1	0	1	0	0
0	0	1	1	0	1	0	1	1	0
0	1	0	0	0	1	1	0	0	1
0	1	0	1	0	1	1	0	1	0
0	1	1	0	0	1	1	1	0	1
0	1	1	1	1	1	1	1	1	1

Table 1: Truth table for circuit in Figure 1

3 Results

To verify the FPGA's configuration, each entry from the truth table was input and the output confirmed to match the expected value. As an additional exercise, the circuit was simplified with Boolean algebra, and tested as above. The simplified circuit is shown in Figure 2. The truth table, shown below, is identical since the two circuits are equivalent.

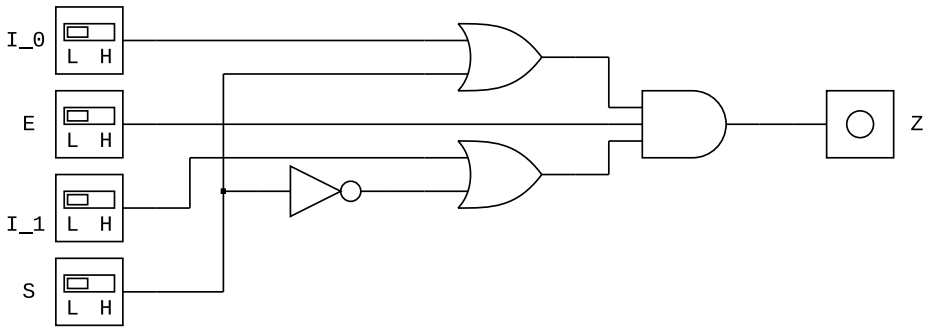

Figure 2: Simplified version of the circuit in Figure 1

I_0	E	I_1	S	Z	I_0	E	I_1	S	Z
0	0	0	0	0	1	0	0	0	0
0	0	0	1	0	1	0	0	1	0
0	0	1	0	0	1	0	1	0	0
0	0	1	1	0	1	0	1	1	0
0	1	0	0	0	1	1	0	0	1
0	1	0	1	0	1	1	0	1	0
0	1	1	0	0	1	1	1	0	1
0	1	1	1	1	1	1	1	1	1

Table 2: Truth table for circuit in Figure 2