Sequential Design

ELEC 311

Digital Logic and Circuits

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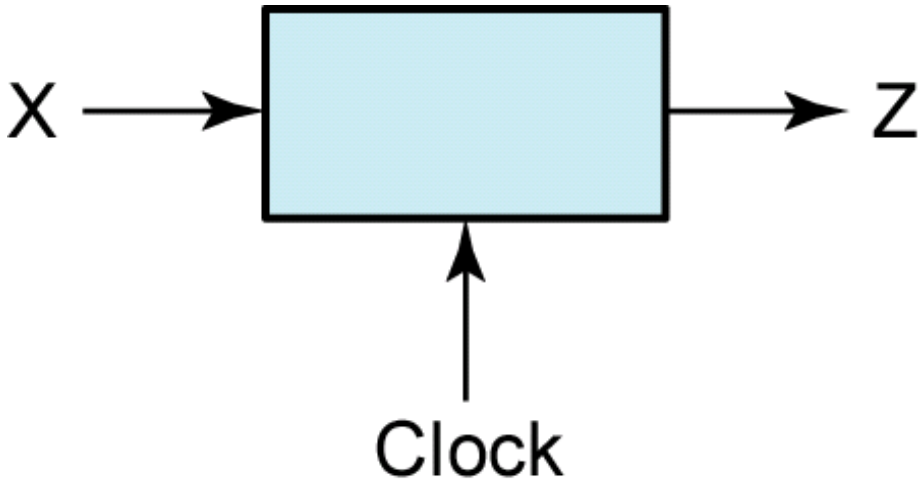
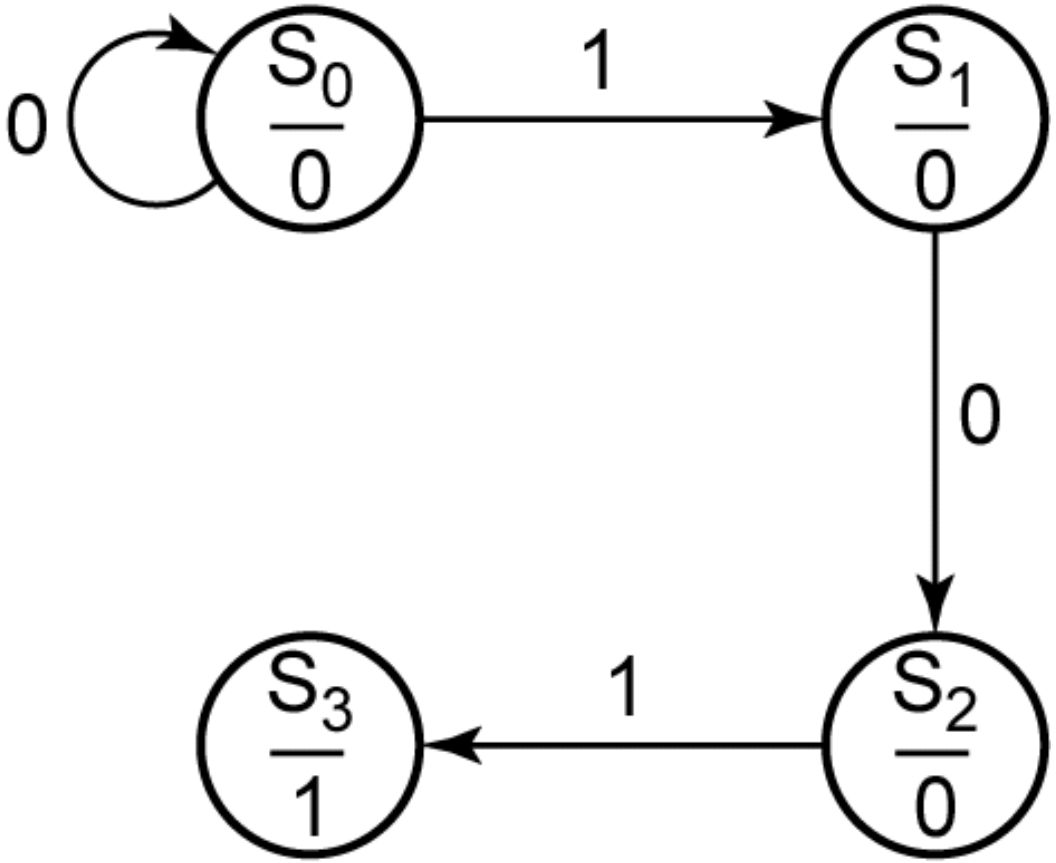
THE CITADEL
DEPARTMENT OF ELECTRICAL & COMPUTER ENGINEERING

Sequence Detector

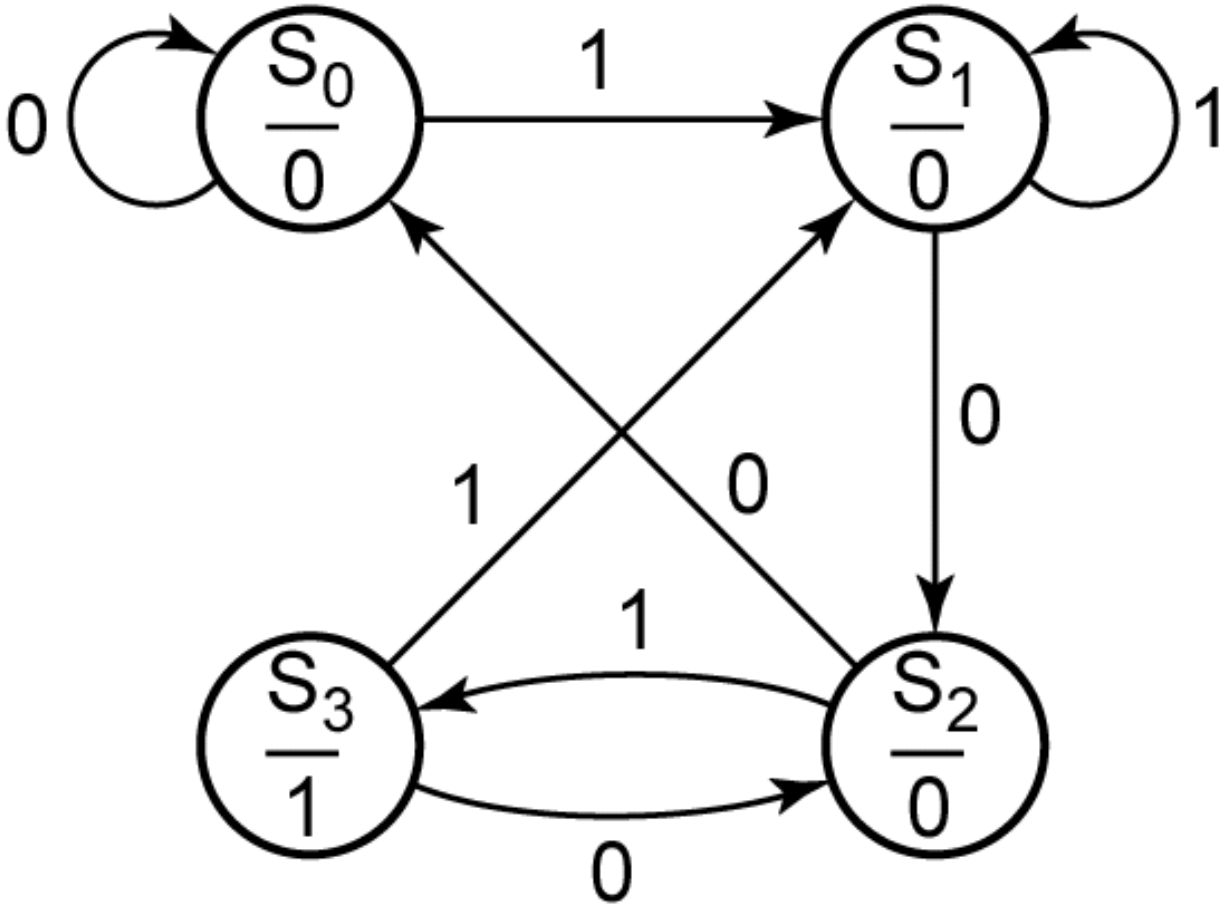
- Design a circuit that will produce an output Z=1 for any sequence (X) ending in 101
  - The circuit does not reset when a 1 output occurs



State Graph



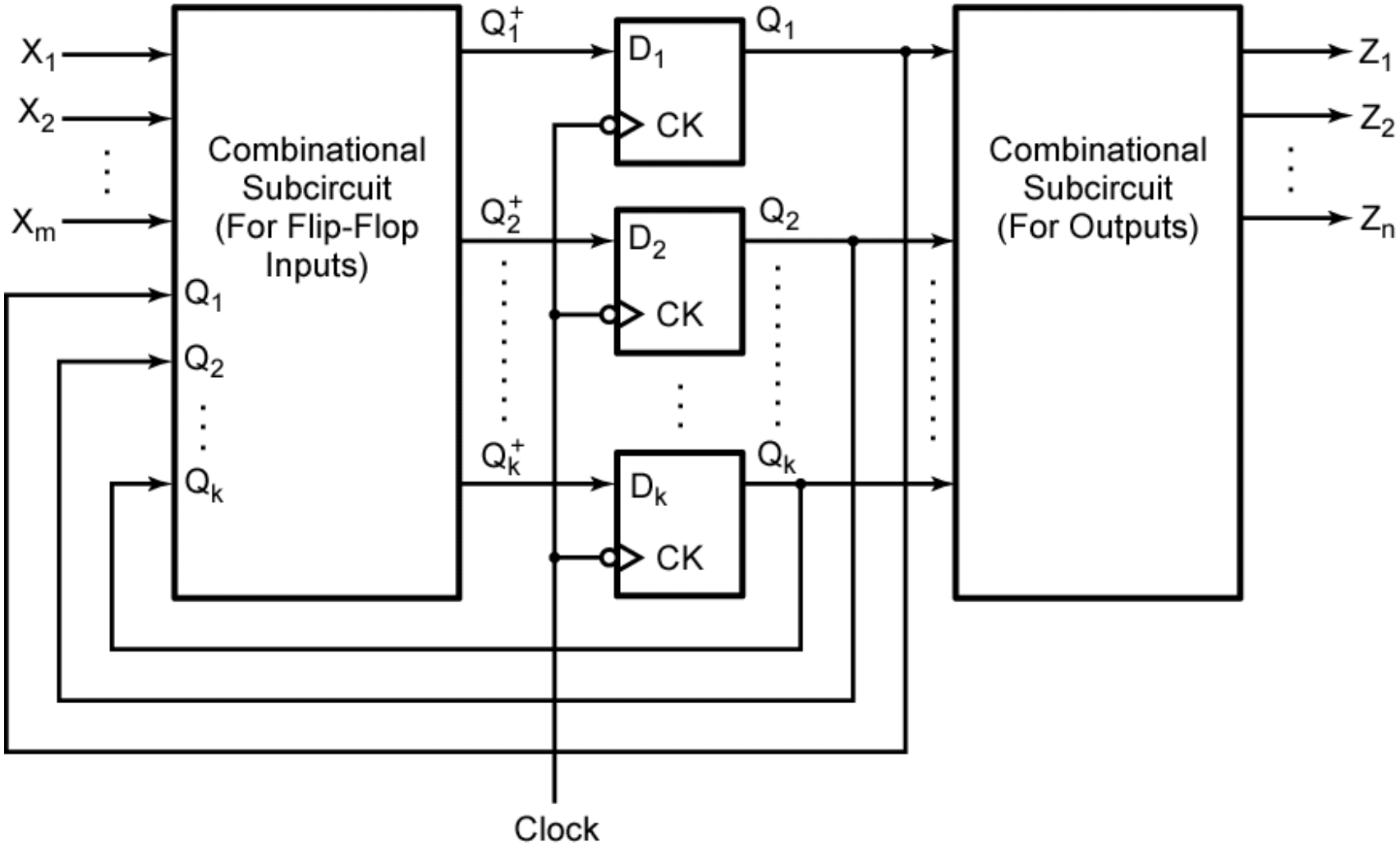
State Graph



State Table

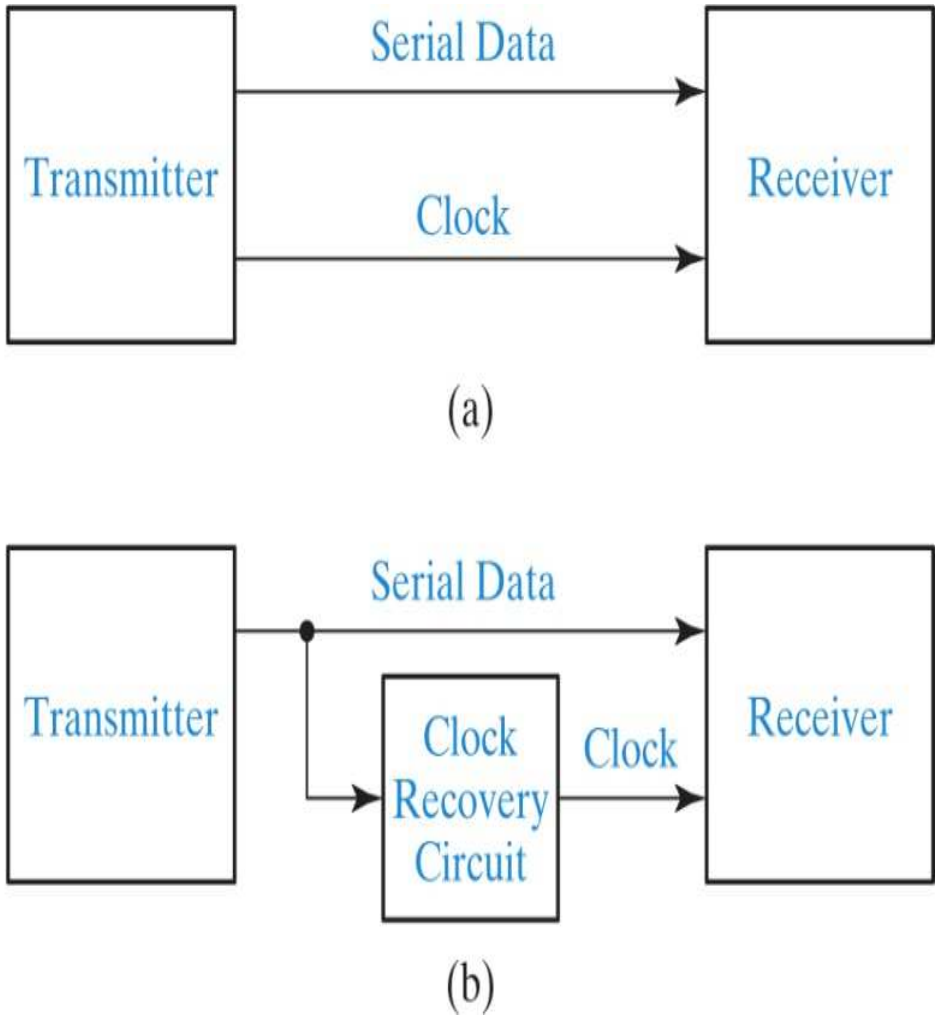
Present State	Next State $X = 0$	Next State $X = 1$	Present Output(Z)
S_0	S_0	S_1	0
S_1	S_2	S_1	0
S_2	S_0	S_3	0
S_3	S_2	S_1	1

Sequential Circuits



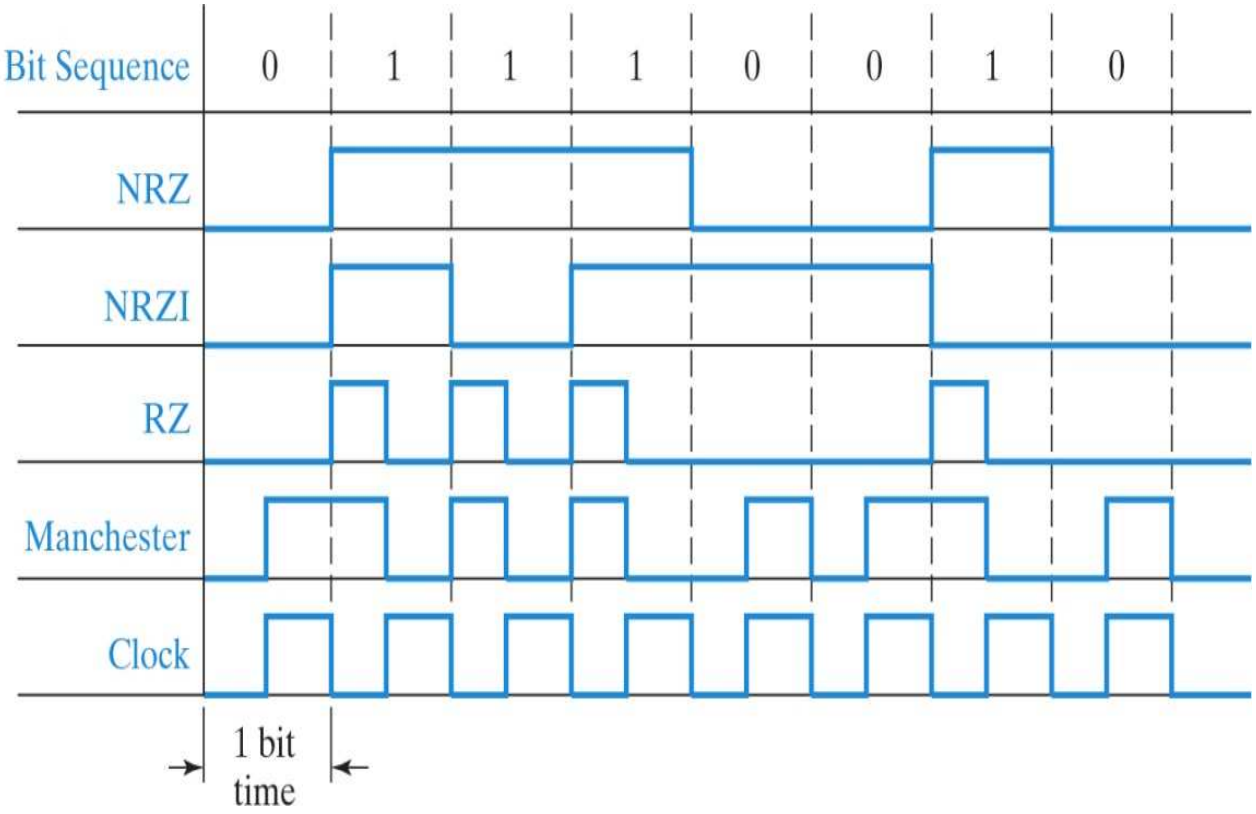
Serial Data Transmission

FIGURE 14-19
Serial Data Transmission



Serial Data Coding Schemes

FIGURE 14-20
Coding Schemes for Serial Data Transmission



NRZ to Manchester Conversion

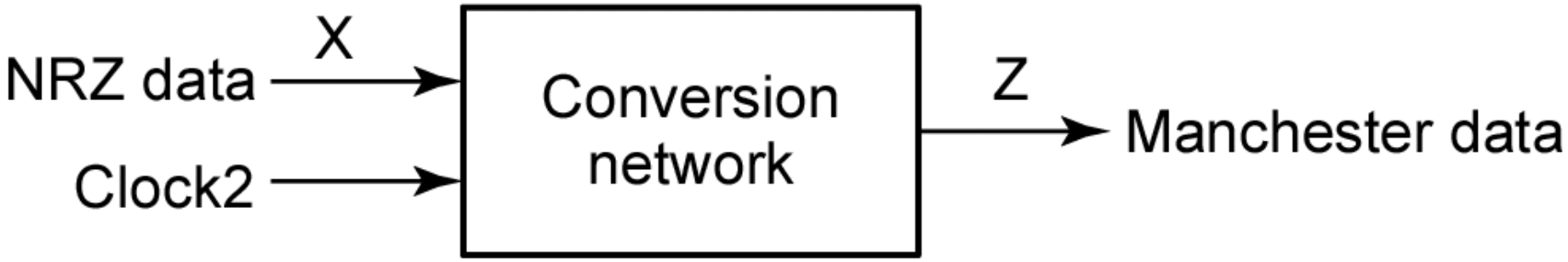
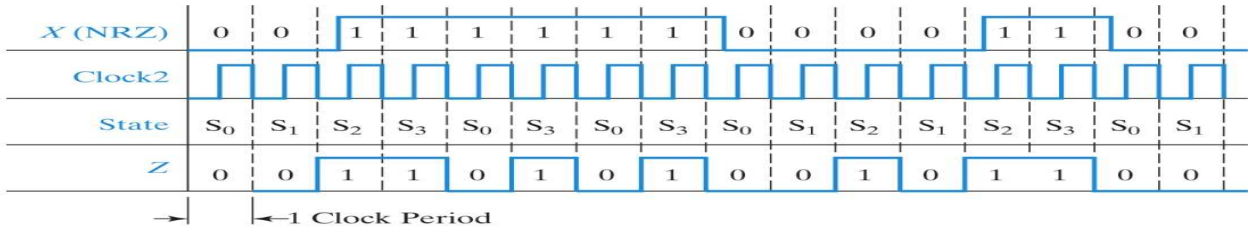
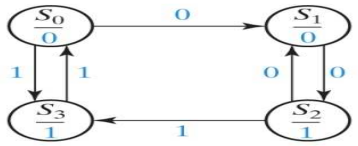


FIGURE 14-22
Moore Circuit for NRZ to Manchester Conversion



(a) Timing chart

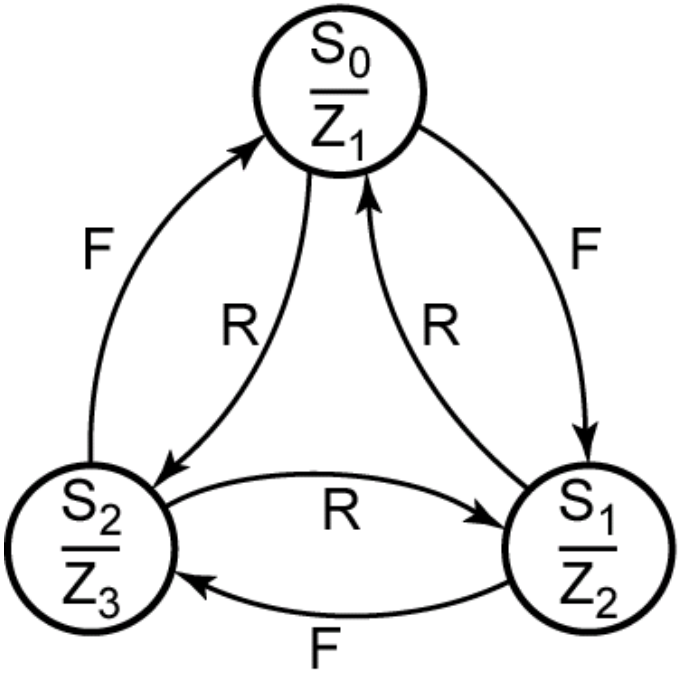


(b) State graph

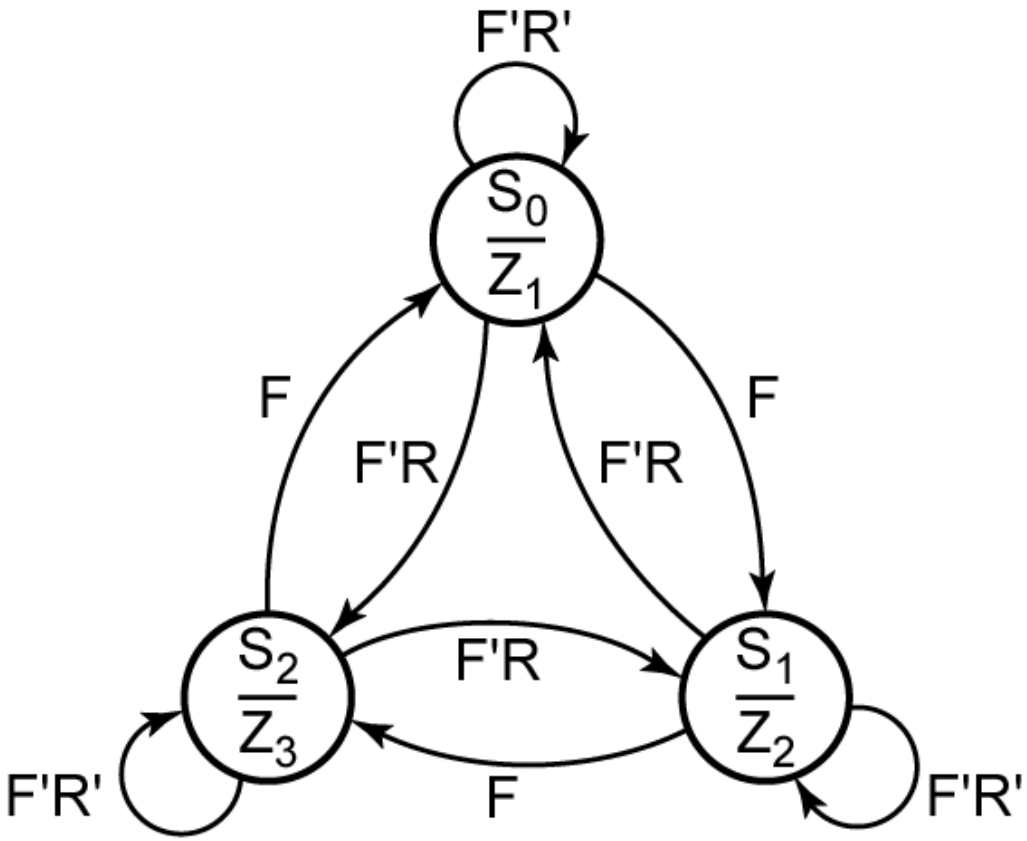
Present State	Next State $X = 0$	Next State $X = 1$	Present Output (Z)
S_0	S_1	S_3	0
S_1	S_2	–	0
S_2	S_1	S_3	1
S_3	–	S_0	1

(c) State table

State Graphs



State Graphs



Summary

- Sequential Design
  - State Graph
  - State Table
  - Transition Table
  - Next State Maps
  - Sequential Circuit