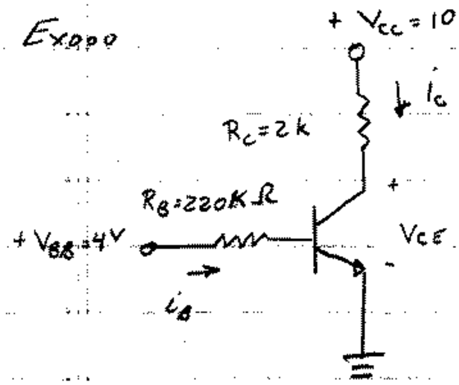


IV. D.C. ANALYSIS & LOAD LINES

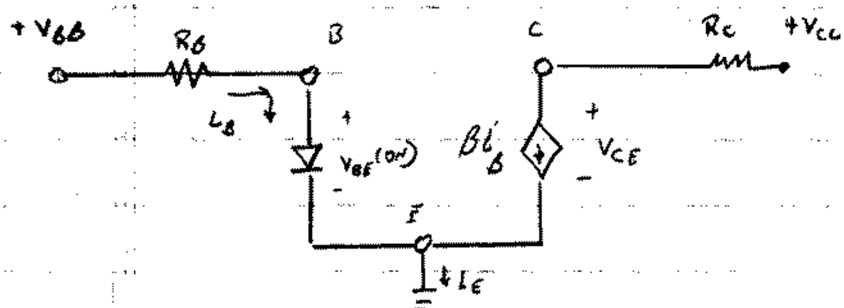
A. THE COMMON Emitter Circuit

Ex000 **FIND** i_B, i_C, i_E & V_{CE}



$\beta = 200$

DC Piecewise Linear Model



① $V_{BE} = 0.7^V$

② $i_B = \dfrac{4 - 0.7}{220k\Omega} = \underline{15\mu A}$

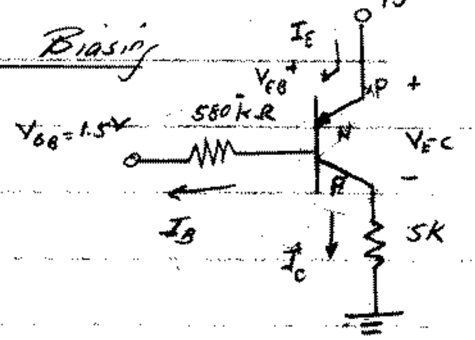
③ $I_C = \beta I_B = (200)(15\mu A) = \underline{3mA}$

④ $I_E = (1+\beta) I_B = \underline{3.02^{mA}}$

⑤ $V_{CE} = V_{CC} - I_C R_C = 10 - (3)(2) = \underline{4V}$

Note: Since $V_{BB} > V_{BE}(ON)$ & $V_{CE} > V_{BE}(ON)$ $\Rightarrow$ Fwd Active Mode

Exam PNP Biasing



Find I_B, I_C, I_E, V_{EC}

$V_{EB} = 0.6$

$\beta = 100$

① KVL: $-5 + V_{EB} - I_B(580k) + 1.5 = 0$

$$I_B = \frac{5 - 0.6 - 1.5}{580k} = 5\mu A$$

② $I_C = \beta I_B = 0.5mA$

③ $I_E = (\beta+1) I_B = 0.505mA$

④ KVL: $-5^V + V_{EC} + I_C 5K = 0 \Rightarrow V_{EC} = 5 + (.5)(5) = 2.5^V$

Note: ① The E-B junction is fwd biased since $\underbrace{V_{CC} - V_{BB}}_{V_{EB}\,(open)} > 0.6^V$

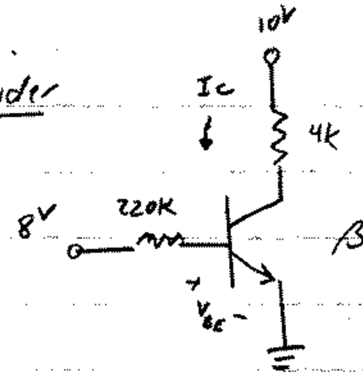
② The C-B junction is reverse biased since

$$V_{BC} = \underset{V_B}{(5 - 0.7)} - \underset{V_C}{(.5 \times 5)} = 4.3 - 2.5 = \underline{\underline{2.8}}$$

Thus transistor is in Linear Active mode

also: $V_{EC} = 2.5^V > V_{EB}(ON)$ ✓

Consider



① $I_B = \frac{8-0.7}{220k} = 33.2\,\mu A$

② $I_C = \beta I_B = 3.32\,mA$

③ $V_{CE} = V_{CC} - I_C R_C = 10 - 3.32(4)$
$= -3.28^V$

CAN'T BE

CAN'T have neg V_{CE} in Common Emitter NPN. (See characteristic curve)

∴ Transistor is not in Active Region

∴ $I_C \neq \beta I_B$

So: Set $V_{CE} = V_{CE\,(SAT)} = 0.2^V$ ← Typical

then: $I_C = I_{C\,(SAT)} = \dfrac{V_{CC} - V_{CE\,(SAT)}}{R_C} = \dfrac{10 - 0.2}{4k} = \underline{2.45^{mA}}$

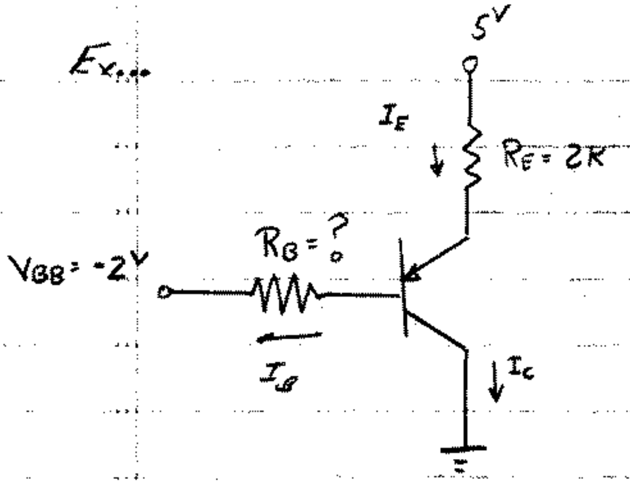
and $I_E = I_B + I_C = 33.2^{\mu A} + 2.45^{mA} = \underline{\underline{2.48^{mA}}}$

Notes: ① Typically $V_{CE\,(SAT)}$ = constant and is given, this is another piecewise linear approx of the transistor characteristic

② $I_C/I_B = \dfrac{2.45}{0.0332} = 74 < \beta$ which is typical of saturation.

So If $I_C < \beta I_B$ the transistor is in saturation.

Ex...



Given: $V_{EB}(ON) = 0.6^V$

$\beta = 60$

Find: R_B so $V_{ECQ} = 2.5^V$

1. EC Loop KVL: $-5^V + I_E\,2k + V_{EC} = 0$

$$I_E = \frac{5 - 2.5}{2K} = \underline{1.25^{mA}}$$

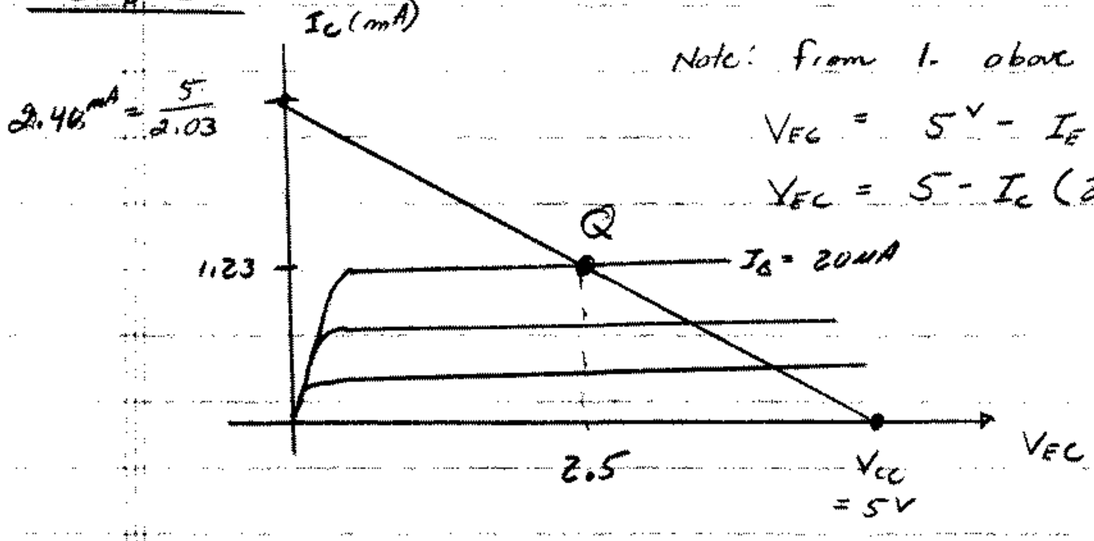
2. $I_C = \frac{\beta}{1+\beta} I_E = \left(\frac{60}{61}\right) 1.25 = \underline{1.23^{mA}}$

3. $I_B = I_E/(1+\beta) = \underline{0.02^{mA}}$

4. EB Loop KVL: $-5 + I_E\,2K + V_{EB}(ON) + I_B R_B - 2 = 0$

$$R_B = \frac{7 - 0.6 - 1.25(2)}{.02^{mA}} = \boxed{190K\Omega}$$

Load Line



Note: from 1. above

$$V_{EC} = 5^V - I_E\,2K = 5^V - \left(\frac{61}{60}\right) I_C\,2K$$

$$V_{EC} = 5 - I_C\,(2.03k)$$

Ex...

Given: $R_B = 240\Omega$ FIND: currents, V_o, power dissipated

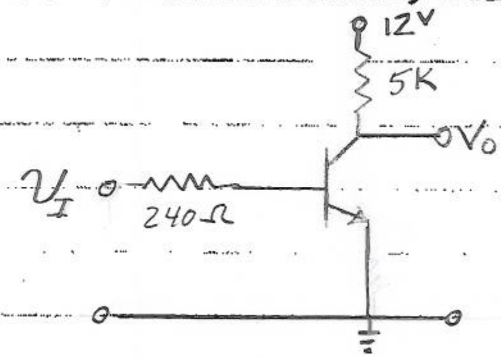
$V_{CC} = 12^V$

$V_{BE}(ON) = 0.7^V$

$V_{CE}(sat) = 0.1$

$\beta = 75$

$R_C = 5\Omega$



① $V_I = 0$: transistor is c-o, $i_B = i_C = 0$, $V_o = V_{CC} = 12^V$

② $V_I = 12^V$: $I_B = \dfrac{V_I - V_{BE}(on)}{R_B} = \dfrac{12 - 0.7}{240} = 47.1\ mA$

Assuming Saturation:

$$I_C = \frac{V_{CC} - V_{CE}(SAT)}{R_C} = \frac{12 - 0.1}{5} = 2.38^A$$

Large for most transistors. Would need a power transistor

ck: $\dfrac{I_C}{I_B} \overset{?}{<} \beta$

$2.38/0.0471 = 50.6 < \beta$ ✓

$V_o = V_{CE}(SAT) = 0.1^V$

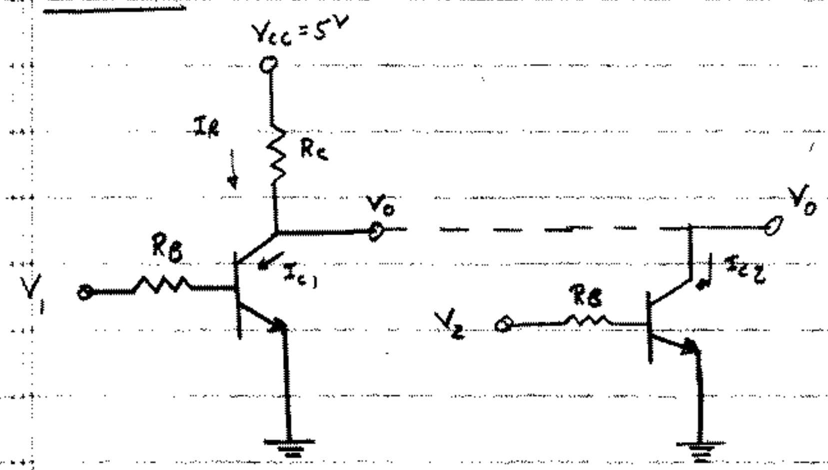
③ power dissipated in transistor $= P = i_C V_{CE} + i_B V_{BE}$

$= (2.38)(0.1) + (0.0471)(0.7)$

$= \underline{\underline{0.271^W}}$

B. Digital Logic

Consider



For $V_1 = 0$, Q1 is cutoff, $i_B = 0$, $i_C = 0$, $V_0 = V_{CC} = 5^V$

For $V_1 = 5^V$, Q1 is SATURATED, $V_0 = V_{CE} \cong 0.2^V$

Now add a second transistor: 2 INPUT NOR GATE

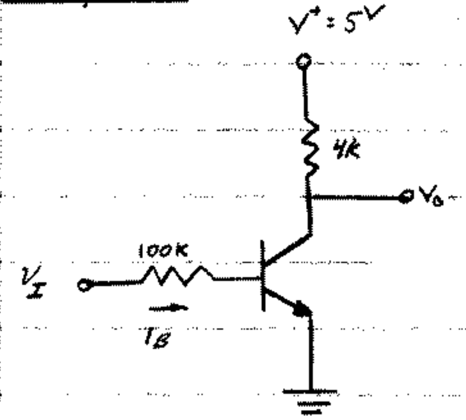
V_1	V_2	V_0
0	0	5^V
5	0	0.2^V
0	5	0.2
5	5	0.2

Ex... $\beta = 50$, $V_{BE(ON)} = 0.7^V$, $V_{CE(SAT)} = 0.2^V$

$R_C = 1K$, $R_B = 20k$

V_1	V_2	V_0	I_R	Q_1	Q_2
0	0	5	0	$I_{B1} = I_{C1} = 0$	$I_{B2} = I_{C2} = 0$
5	0	0.2	$\frac{5-0.2}{1k} = 4.8^{mA}$	$I_{B1} = \frac{5-0.7}{20k} = 0.215^{mA}$ $I_1 = I_R = 4.8^{mA}$	$I_{B2} = I_{C2} = 0$
0	5	0.2	4.8^{mA}	$I_{B1} = I_{C1} = 0$	$I_{B2} = 0.215^{mA}$ $I_{C2} = 4.8^{mA}$
5	5	0.2	4.8^{mA}	$I_{B1} = 0.215^{mA}$ $I_{C1} = I_R/2 = 2.4^{mA}$	$I_{B2} = 0.215^{mA}$ $I_{C2} = I_R/2 = 2.4^{mA}$

C. Amplifier



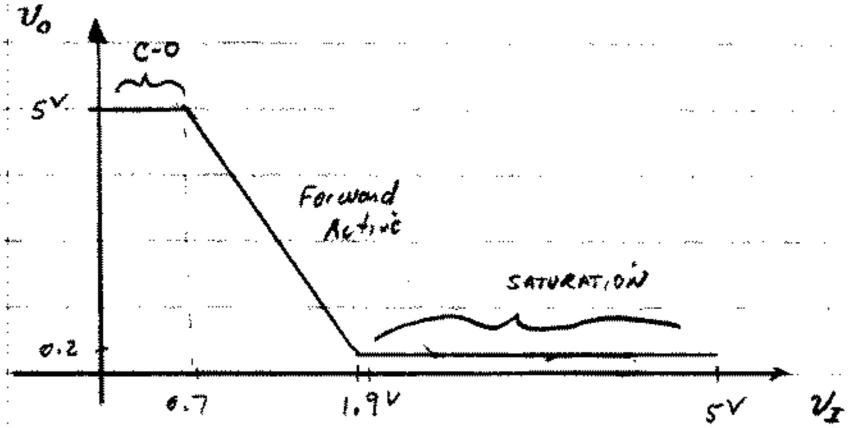
$\beta_F = 100$

$V_A = \infty$

$V_{BE(on)} = 0.7$

$V_{CE(SAT)} = 0.2$

SKETCH TRANSfer Characteristic (v_o vs. v_I)



For $v_I < 0.7^V$, Q is C-O & $v_o = 5^V$

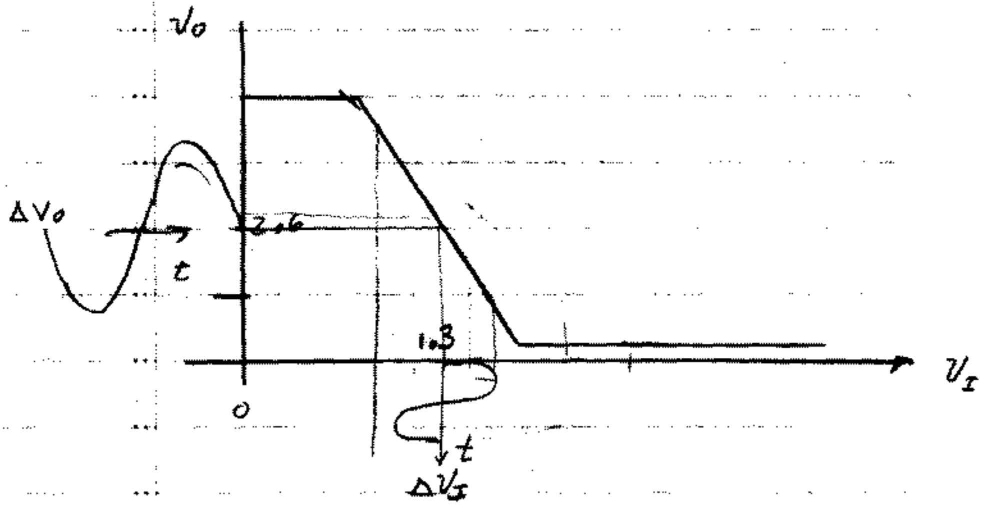
For $V_I > 0.7$, Q is ON $\quad i_B = \dfrac{v_I - V_{BE(ON)}}{R_E} = \dfrac{V_I - 0.7}{100k}$

$$v_o = V^+ - \beta i_B R_C = 5 - 100\left[\frac{v_I - 0.7}{100k}\right]4k = 7.8 - 4v_I$$

at $v_I > 1.9 \quad v_o = 0.2$ in SAT

AC Analysis

- Set $v_I = 1.3^V = V_{BB}$ and input an AC source Δv_I.



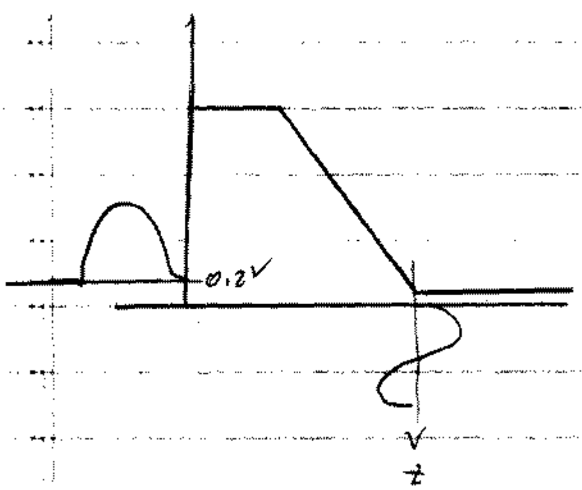
Note: $i_B = \dfrac{V_{BB} + \Delta v_I - V_{BE}(ON)}{R_B} = \dfrac{(1.3-0.7) + \Delta v_I}{100k\Omega}$

$$v_O = V^+ - \beta i_B R_C = 5 - (100)\left[\frac{0.6 + \Delta v_I}{100k}\right]4k$$

$$\boxed{v_O = 2.6 - 4\Delta v_I}$$

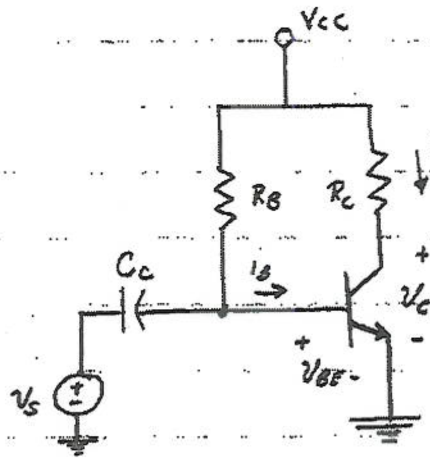
$$\text{Gain} = A_V = \frac{\Delta v_O}{\Delta v_I} = -4$$

Suppose $v_I = 1.9V$



B. Single Base Resistor Biasing

1.



DC ANALYSIS

INPUT CIRCUIT

KVL: $I_{BQ} = \dfrac{V_{CC} - V_{BE}}{R_B}$

OUTPUT CIRCUIT

KVL: $I_{CQ} = \dfrac{V_{CC} - V_{CEQ}}{R_C}$

Exam. Consider $V_{CC} = 12^V$, $V_{BE(ON)} = 0.7^V$, $R_C = 6k\Omega$, $R_B = 1.13M\Omega$

then for $\beta_F = 100$:

$$I_{BQ} = \frac{V_{CC} - V_{BE(ON)}}{R_B} = \frac{12 - 0.7}{1.13M} = 10\mu A$$

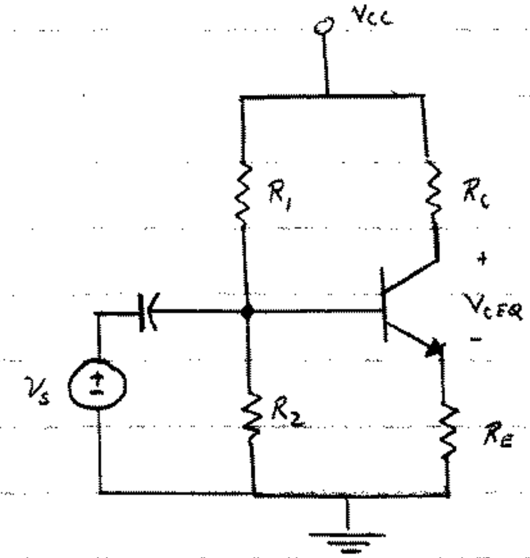
$$V_{CEQ} = V_{CC} - \beta_F I_B R_C = 12 - (100)(10\mu A)(6k) = \underline{6^V}$$

for $\beta_F = 50$;

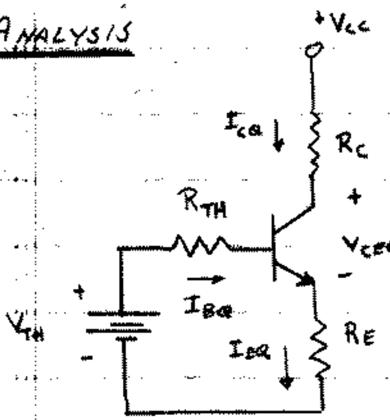
$$V_{CEQ} = 12 - (50)(10\mu A)(6k) = \underline{9^V}$$

50% ↓ β_F , 50% ↑ V_{CEQ}

C. Voltage Divider Biasing & the Emitter Resistor



ANALYSIS



WHERE: $V_{TH} = \dfrac{R_2}{R_1 + R_2} V_{CC}$

$R_{TH} = R_1 // R_2 = \dfrac{R_1 R_2}{R_1 + R_2}$

Again: $V_{CEQ} = V_{CC} - \beta_F I_{BQ} R_C$

However: KVL: $-V_{TH} + I_{BQ} R_{TH} + V_{BE} + (\beta_F + 1) I_{BQ} R_E$

So $I_{BQ} = \dfrac{V_{TH} - V_{BE}}{R_{TH} + (\beta_F + 1) R_E}$

$\therefore \quad V_{CEQ} = V_{CC} - \beta_F \left[\dfrac{V_{TH} - V_{BE}}{R_{TH} + (\beta_F + 1) R_E} \right] R_C$

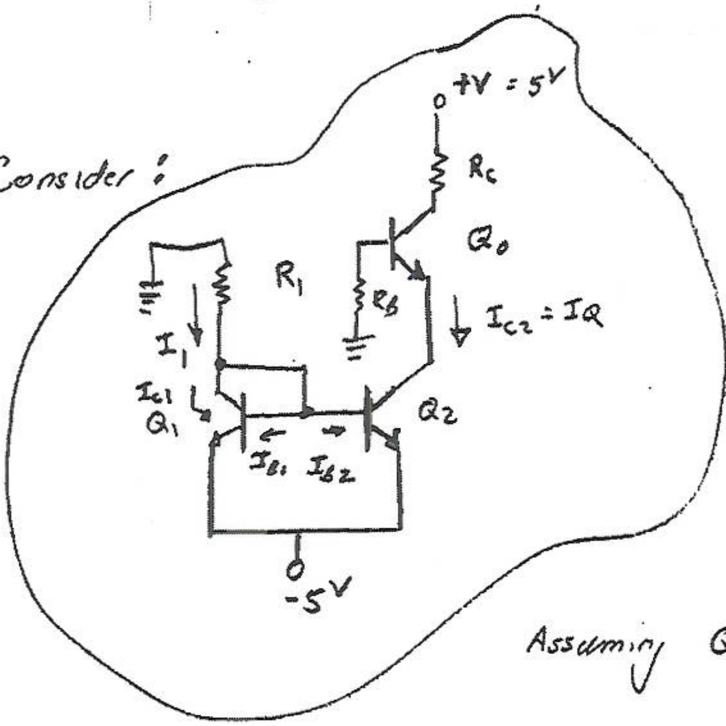
If by design $R_{TH} << (\beta_F + 1) R_E$;

then $V_{CEQ} \cong V_{CC} - \overbrace{\left(\dfrac{\beta_F}{\beta_F + 1} \right)}^{\approx 1} \left[V_{TH} - V_{BE} \right] \dfrac{R_C}{R_E}$

$\boxed{\text{NEARLY INDEPEDENT OF } \beta \text{ CHANGES.}}$

D. Integrated Circuit Biasing

Consider:



$R_1 - Q_1$ Loop

$$0 = I_1 R_1 + V_{BE(ON)} + V^-$$

$$I_1 = \frac{-(V^- + V_{BE(ON)})}{R_1}$$

ALSO

$$I_1 = I_{C1} + I_{B1} + I_{B2}$$

Assuming Q_1 & Q_2 are identical:

$$I_1 = I_{C1} + 2 I_{B2} = I_{C2}(1 + 2/\beta)$$

$$\boxed{I_{C2} = I_Q = \frac{I_1}{1 + 2/\beta}}$$

Ex. Let $R_1 = 10k\Omega$, $\beta = 50$, $V_{BE(ON)} = 0.7^V$

then

$$I_1 = \frac{-(V^- + V_{BE(ON)})}{R_1} = \frac{-(-5 + 0.7)}{10k} = \underline{0.43\,mA}$$

$$I_{C2} = \left(\frac{I_1}{1 + 2/\beta}\right) = \frac{0.43^{mA}}{(1 + 2/50)} = \underline{0.413^{mA}}$$

$$I_{B1} = I_{B2} = I_{C2}/\beta = \frac{0.413}{\beta} = \underline{8.26\,\mu A}$$