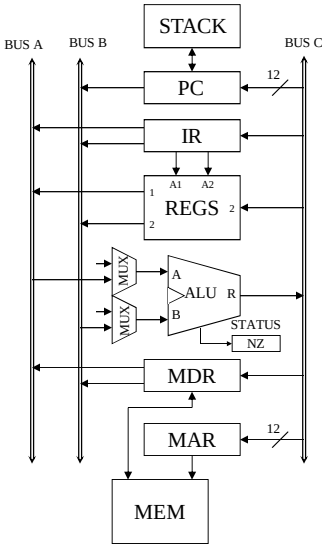
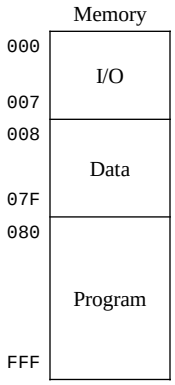
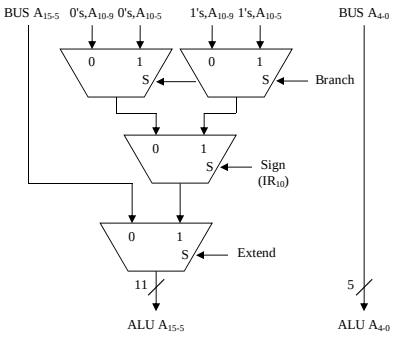
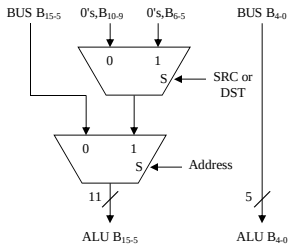
Instructional Processor





ALU Multiplexers

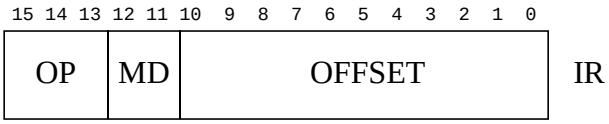




Control Signals

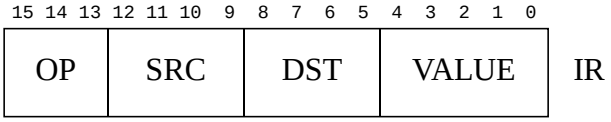
- BUS_A
- BUS_B
- REGS_Read1
- REGS_Read2
- Extend
- Address
- ALU_Op
- MEM_Read
- MEM_Write
- Inc_PC
- Load_PC
- Push_PC
- Pop_PC
- Load_IR
- REGS_Write
- Load_STATUS
- Load_MDR
- Load_MAR
- Clear

Branch Instruction Format



OP	MD	Fn	Assy Lang	RTN
111	00	BRA	`BRA Offset`	PC ← PC + Offset
	01	BGTZ	`BGTZ Offset`	PC ← PC + Offset (STATUS > 0)
	10	BSR	`BSR Offset`	STACK ← PC; PC ← PC + Offset
	11	RTN	`RTN`	PC ← STACK

Data Instruction Format



	Mode	REG #	Name	Syntax	Effective Address
SRC or DST	00	00-11	Register Direct	Rn	EA = Rn
	01	00-11	Register Indirect	(Rn)	EA = [Rn]
	10	vv	Absolute	Value	EA = Value
	11*	vv	Immediate	#Value	Operand = Value

EA = Effective Address
vv = Upper 2 bits of Value
* = SRC only

Data Instructions

OP	Fn	Assembly Language	Register Transfer Notation (RTN)
000	MOVE	`MOVE SRC,DST`	DST ← SRC
001	ADD	`ADD SRC,DST`	DST ← SRC + DST
010	INV	`INV SRC,DST`	DST ← not SRC
011	AND	`AND SRC,DST`	DST ← SRC and DST
100	ROTL	`ROTL SRC,DST`	DST ← SRC(14 dt 0) & SRC(15)
...			