Boolean Algebra (Continued)

ELEC 311

Digital Logic and Circuits

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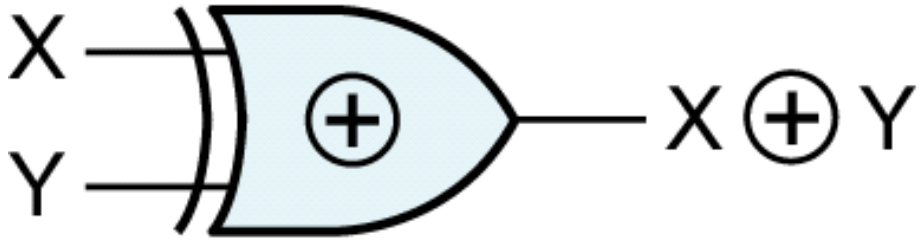
Images Courtesy of Cengage Learning

THE CITADEL
DEPARTMENT OF ELECTRICAL & COMPUTER ENGINEERING

Exclusive-OR (XOR)



X	Y	X ⊕ Y
0	0	0
0	1	1
1	0	1
1	1	0

$$X \oplus Y = X'Y + XY'$$

XOR Theorems

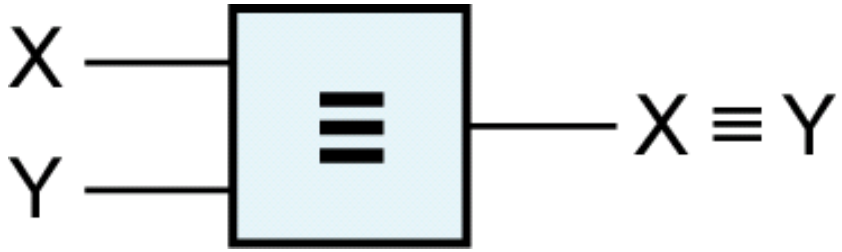
$$X \oplus 0 = X$$

$$X \oplus 1 = X'$$

$$X \oplus X = 0$$

$$X \oplus X' = 1$$

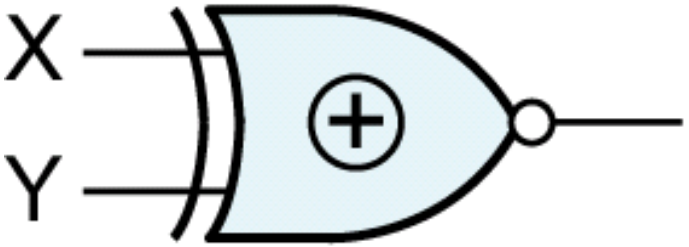
Equivalence



X	Y	X ≡ Y
0	0	1
0	1	0
1	0	0
1	1	1

$$(X \equiv Y) = XY + X'Y'$$

Equivalence (XNOR)



$$(X \oplus Y)' = (X \equiv Y)$$

X	Y	$X \oplus Y$
0	0	0
0	1	1
1	0	1
1	1	0

X	Y	$X \equiv Y$
0	0	1
0	1	0
1	0	0
1	1	1

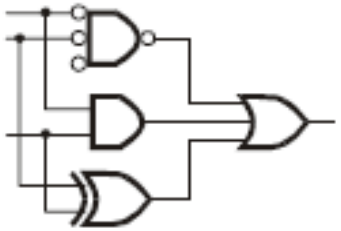
Project 1

- Combinational Circuit Analysis
  - Determine input/output relationship of function
    - Boolean Equation
    - Truth Table
  - Implement logic circuit with FPGA
    - Schematic capture design tools
  - Test circuit to verify operation
  - Project Report
- Teams of 2 persons

Xilinx ISE Design Suite

- Enter description of logic circuit
  - Schematic editor
  - VHDL
- Use a logic synthesizer to generate a netlist
- Use implementation tools to map logic gates and interconnections into the FPGA
- Generate a bitstream programming file
- Configure device
  - Download the bitstream to the FPGA chip

Schematic



or

VHDL Source Code

```
entity leddcd is
   port(
      d: in std_logic_vector(3 downto 0);
      s: out std_logic_vector(6 downto 0);
   );
end;

architecture leddcd_arch of leddcd is
begin
   s <= "1110111" when d="0000" else
        "0010010" when d="0001" else
        "1101101";
end leddcd_arch;
```

Synthesize

Netlist

routing resources

FPGA

Map, Place & Route

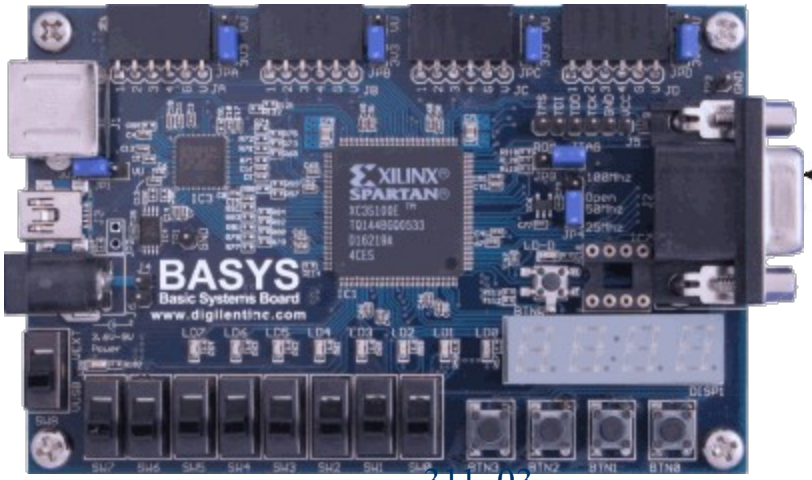
look-up table

configurable function block

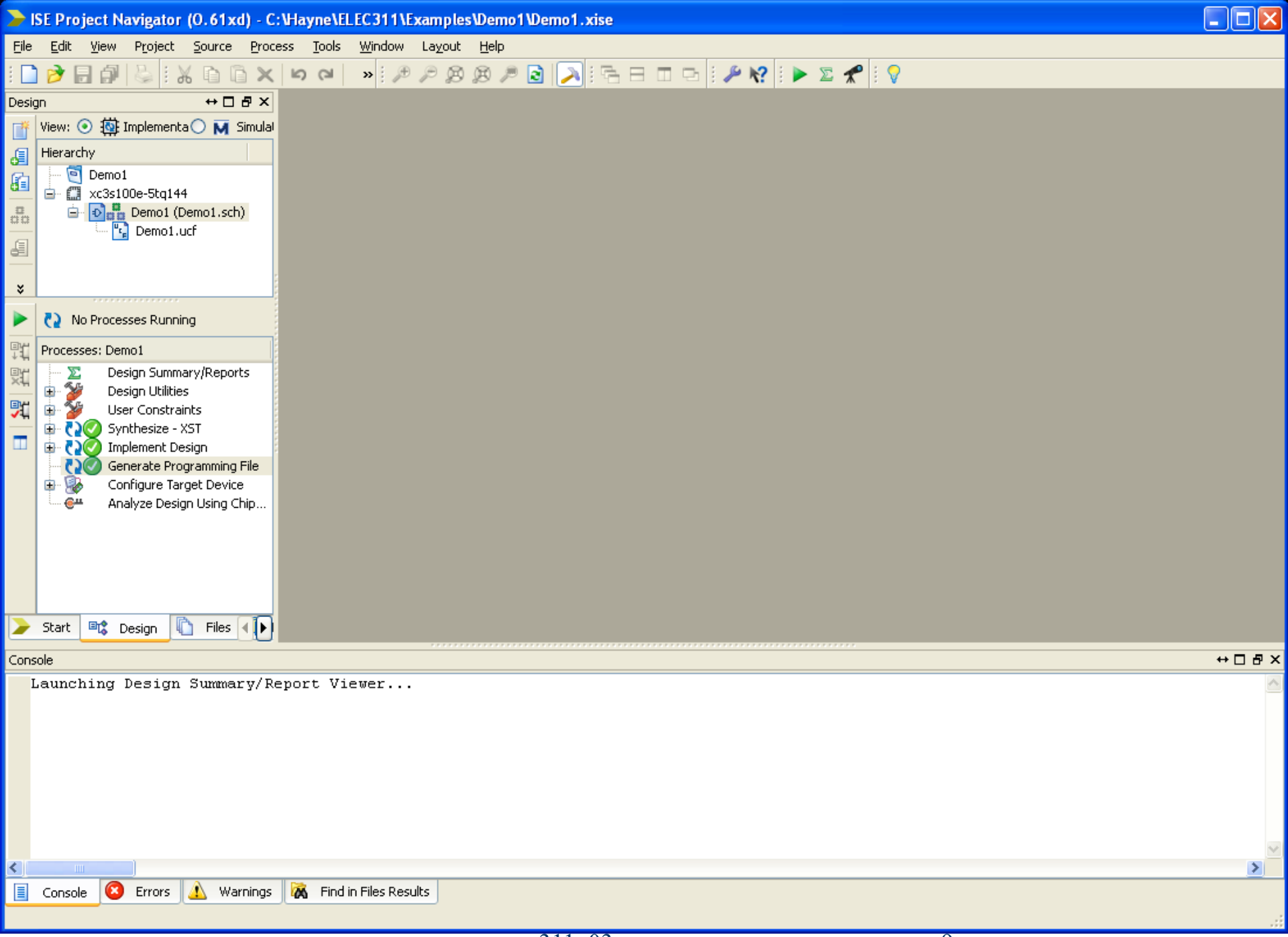
Generate Bitstream

Bitstream

```
101010010101100101
010110101010110101
010110100101101011
010101001010101010
101010101001101010
110110110101001010
110100101011001011
001011001010101001
010101101001101001
011001100010101010
101010100110010101
```



Download and Test


ISE Project Navigator (O.61xd) - C:\Hayne\ELEC311\Examples\Demo1\Demo1.xise
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementa Simulat
Hierarchy
Demo1
xc3s100e-5tq144
Demo1 (Demo1.sch)
Demo1.ucf
No Processes Running
Processes: Demo1
Design Summary/Reports
Design Utilities
User Constraints
Synthesize - XST
Implement Design
Generate Programming File
Configure Target Device
Analyze Design Using Chip...
Start Design Files
Console
Launching Design Summary/Report Viewer...
Console Errors Warnings Find in Files Results

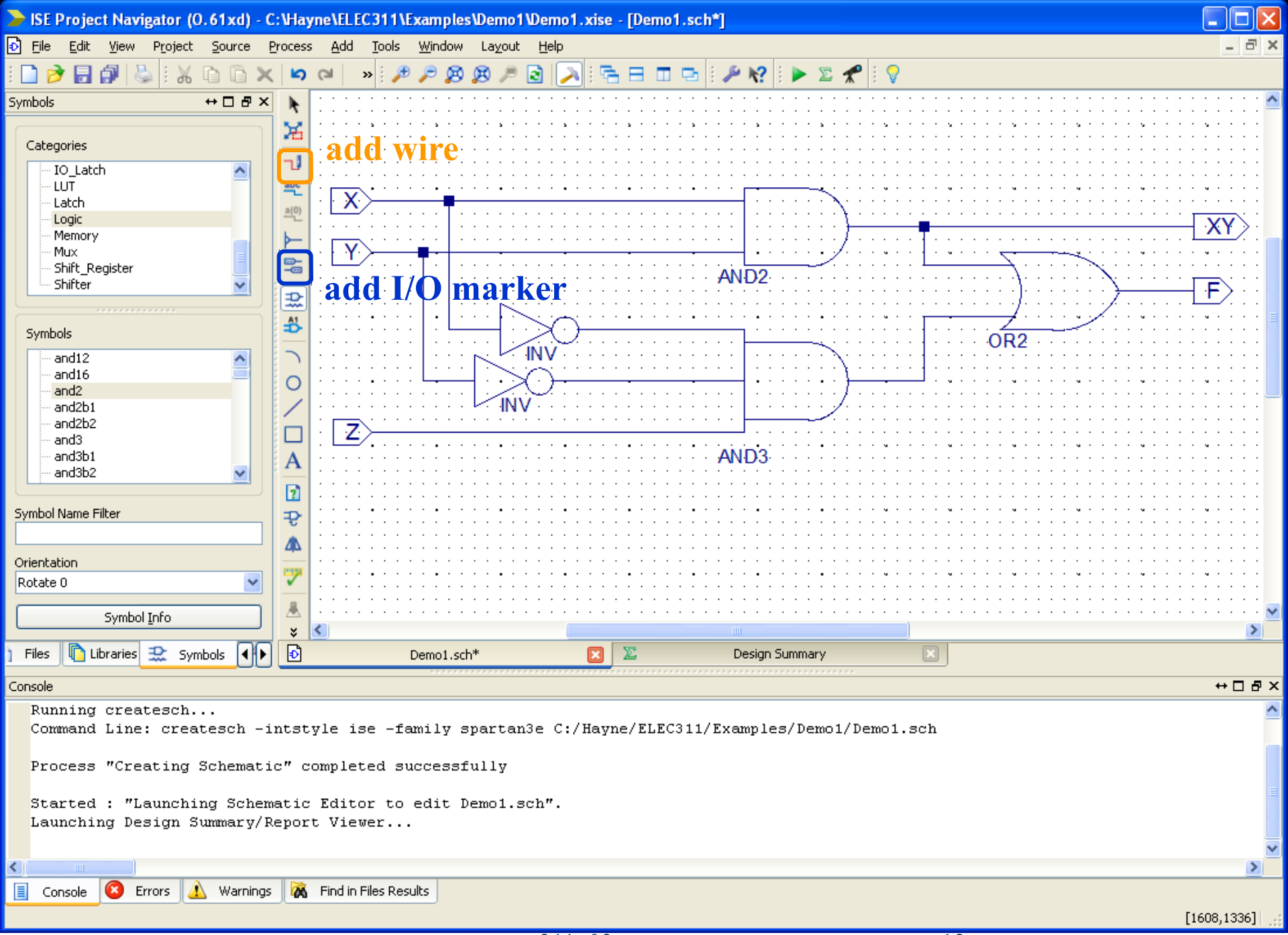
New Project

- File → New Project
  - Project Name
    - Demo1
  - Project Location
    - C:\xxx\xxx
  - Top-Level Module Type
    - Schematic
  - Device Family
    - Spartan3E
  - Device
    - XC3S100E
  - Package
    - TQ144 (BASYS)
    - CP132 (BASYS 2)
  - Speed Grade
    - -5

New Source

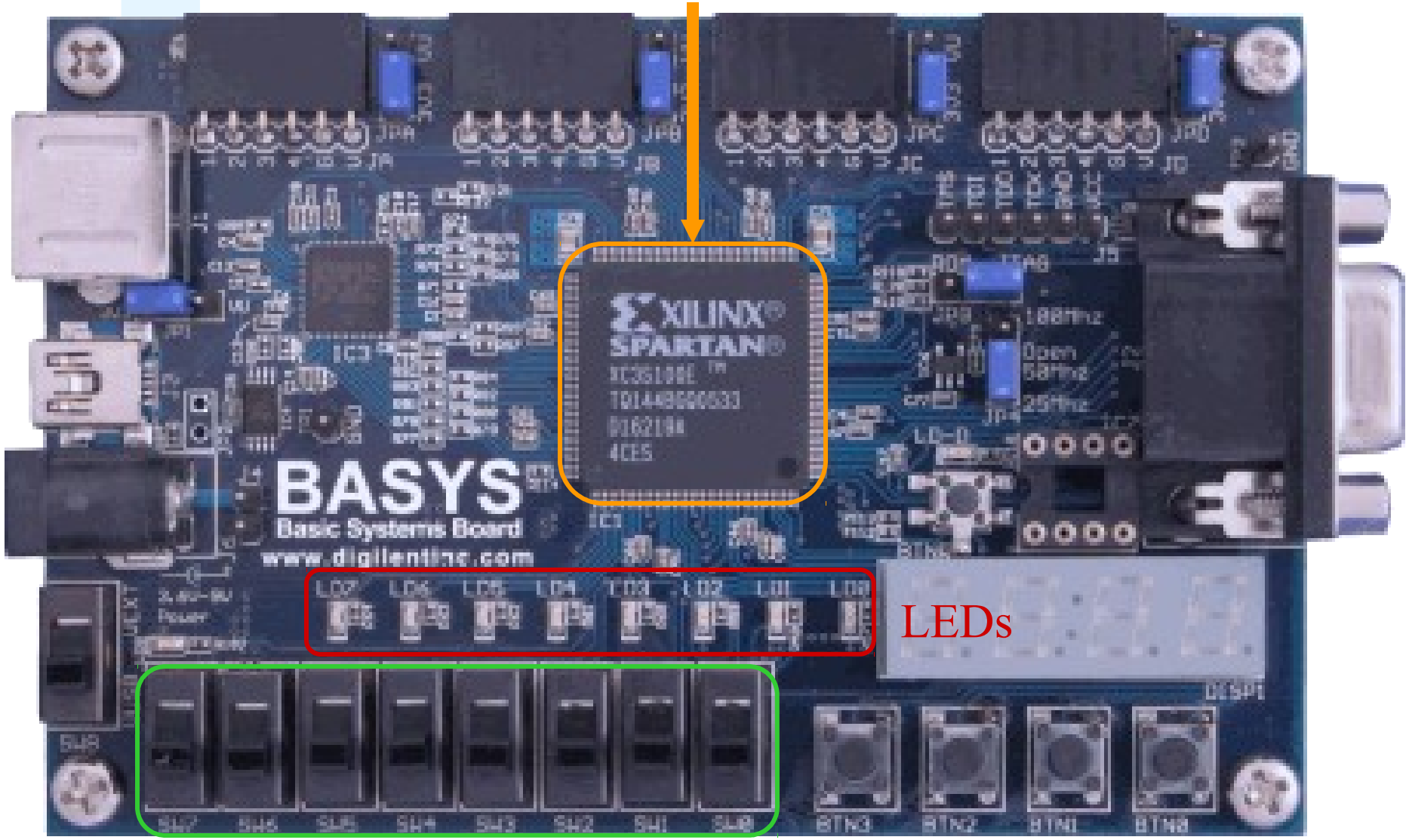
- Project → New Source
  - Schematic
    - Demo1

- Schematic Editor
  - Symbols
    - Category list
    - Symbol list
  - Drawing area
  - Tools
    - Add wire
    - Add I/O marker

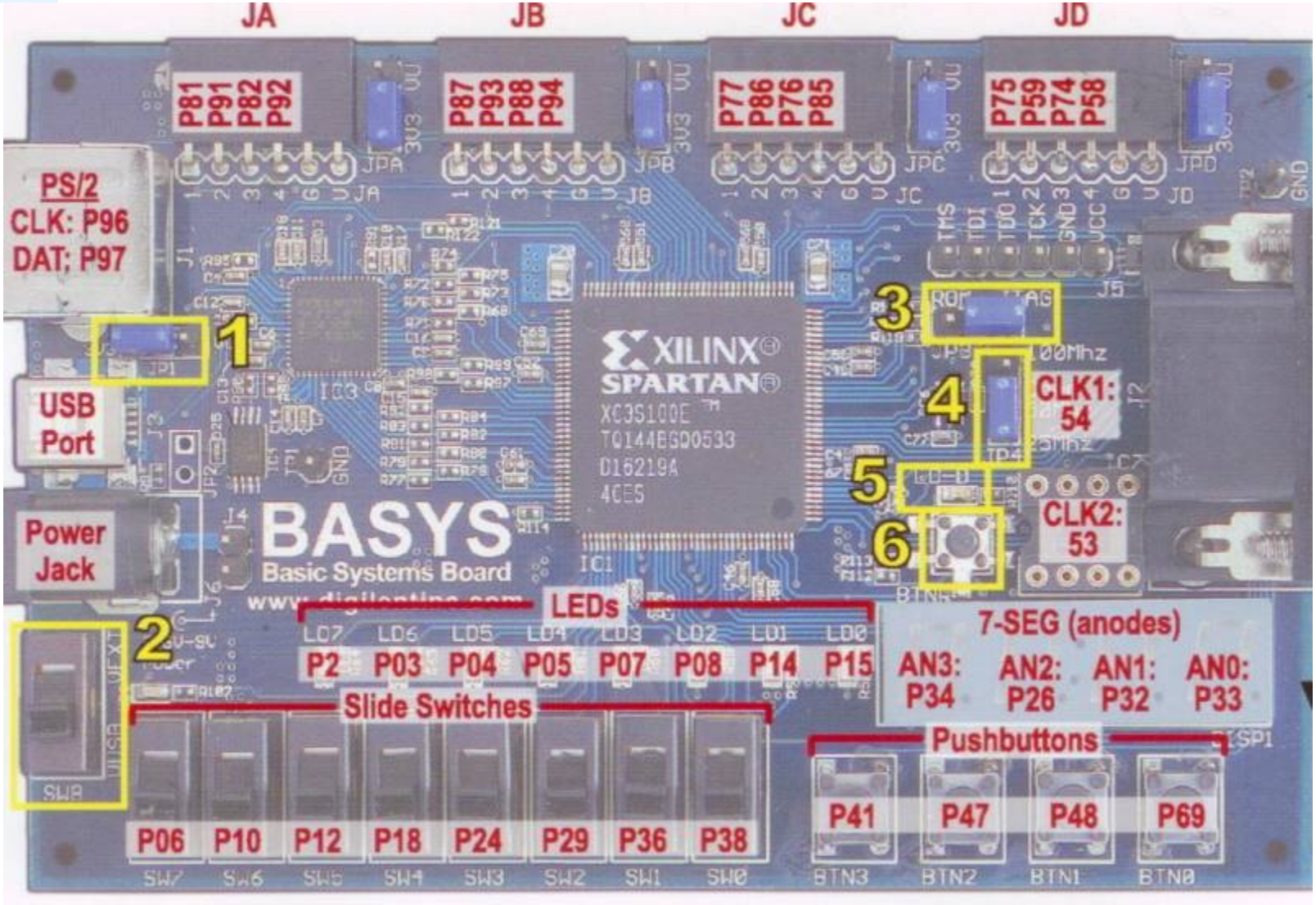

ISE Project Navigator (O.61xd) - C:\Hayne\ELEC311\Examples\Demo1\Demo1.xise - [Demo1.sch*]
File Edit View Project Source Process Add Tools Window Layout Help
Symbols
Categories
IO_Latch
LUT
Latch
Logic
Memory
Mux
Shift_Register
Shifter
Symbols
and12
and16
and2
and2b1
and2b2
and3
and3b1
and3b2
Symbol Name Filter
Orientation
Rotate 0
Symbol Info
add wire
add I/O marker
X
Y
Z
AND2
AND3
INV
INV
OR2
XY
F
Files
Libraries
Symbols
Demo1.sch*
Design Summary
Console
Running createsch...
Command Line: createsch -intstyle ise -family spartan3e C:/Hayne/ELEC311/Examples/Demo1/Demo1.sch
Process "Creating Schematic" completed successfully
Started : "Launching Schematic Editor to edit Demo1.sch".
Launching Design Summary/Report Viewer...
Console
Errors
Warnings
Find in Files Results
[1608,1336]

Demo1 Schematic

- Categories
  - Logic
- Symbols
  - and2
  - and3
  - inv
  - or2
- Add wires
  - Point to point
  - Stubs
- I/O Markers
  - Input marker
  - Output marker
  - Rename Port


FPGA
XILINX
SPARTAN
BASYS
Basic Systems Board
www.digilentinc.com
LEDs
Switches

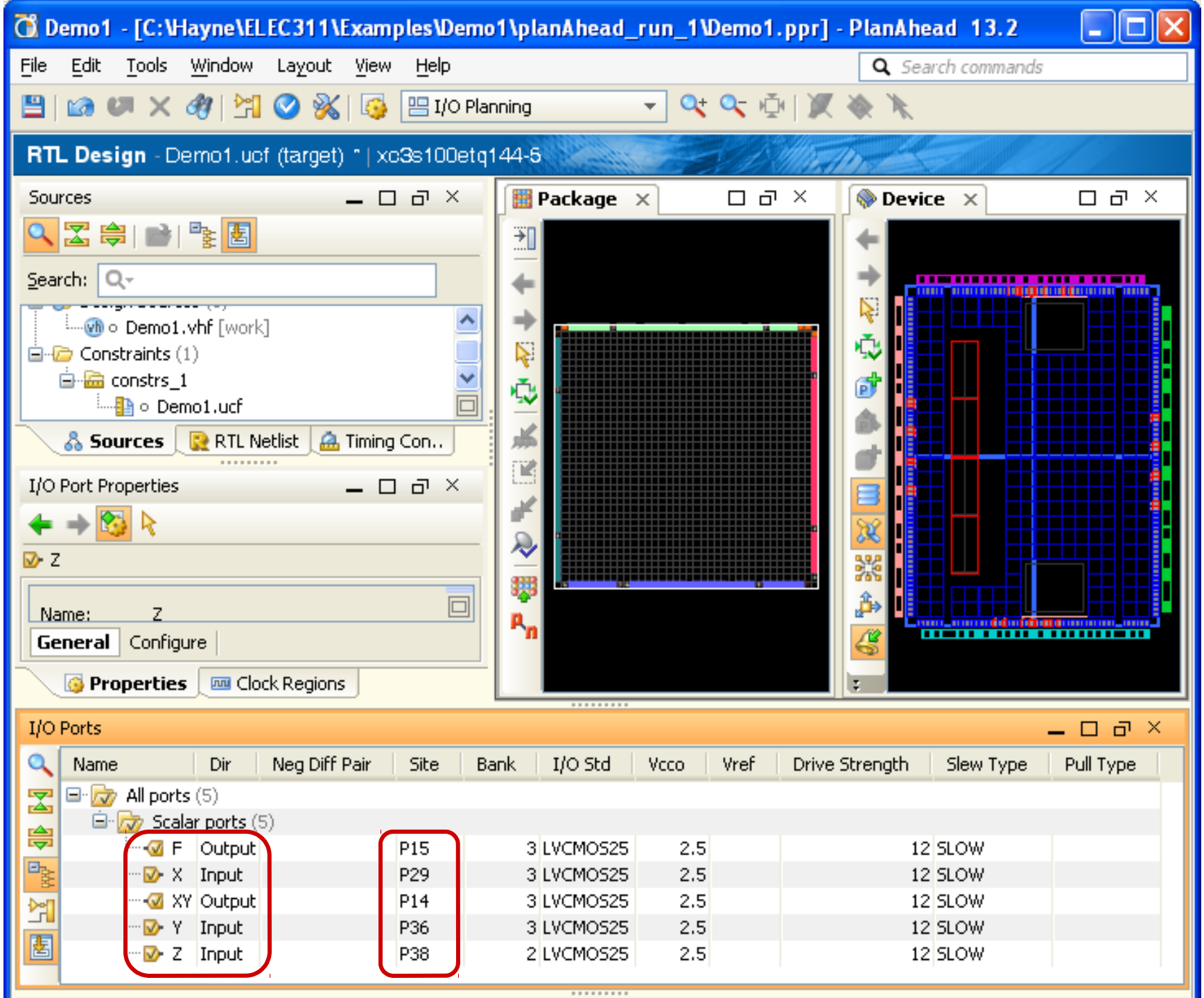
FPGA Pins


JA
JB
JC
JD
P81 P91 P82 P92
P87 P93 P88 P94
P77 P86 P76 P85
P75 P59 P74 P58
PS/2
CLK: P96
DAT: P97
USB Port
Power Jack
1
2
3
4
5
6
XILINX
SPARTAN
XC3S100E
BASYS
Basic Systems Board
CLK1: 54
CLK2: 53
LEDs
LD7 LD6 LD5 LD4 LD3 LD2 LD1 LD0
P2 P03 P04 P05 P07 P08 P14 P15
7-SEG (anodes)
AN3: P34
AN2: P26
AN1: P32
AN0: P33
Slide Switches
P06 P10 P12 P18 P24 P29 P36 P38
SW7 SW6 SW5 SW4 SW3 SW2 SW1 SW0
Pushbuttons
P41 P47 P48 P69
BTN3 BTN2 BTN1 BTN0

Constrain the Design

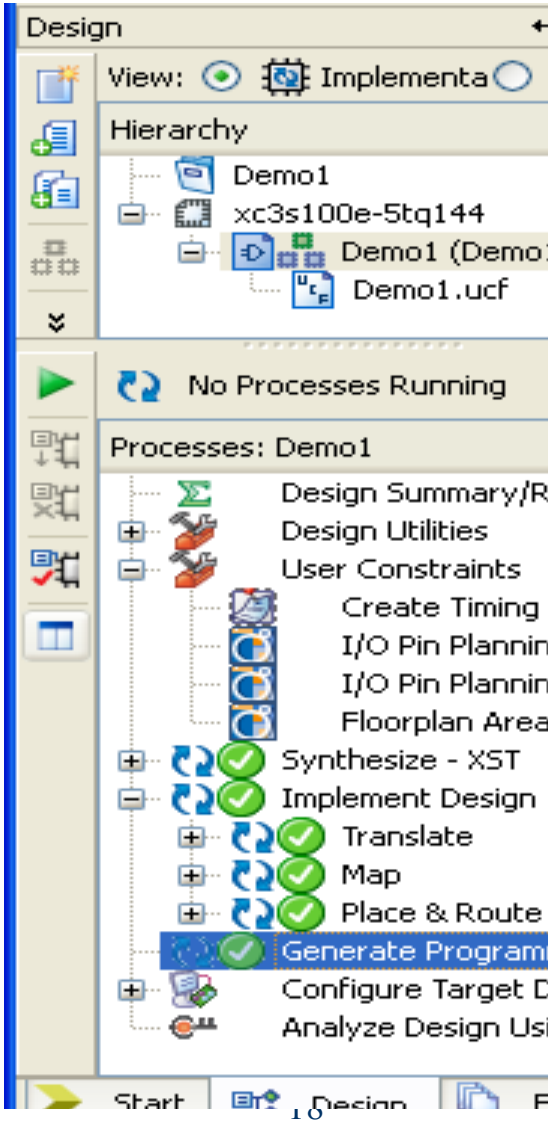
- User Constraints ⟶ I/O Pin Planning – Pre-Synthesis
  - Implementation Constraints File
    - Demo1.ucf
  - PlanAhead
    - I/O Ports
      - Site

I/O Name	Location	BASYS	BASYS 2
X	SW2	P29	K3
Y	SW1	P36	L3
Z	SW0	P38	P11
XY	LD1	P14	M11
F	LD0	P15	M5

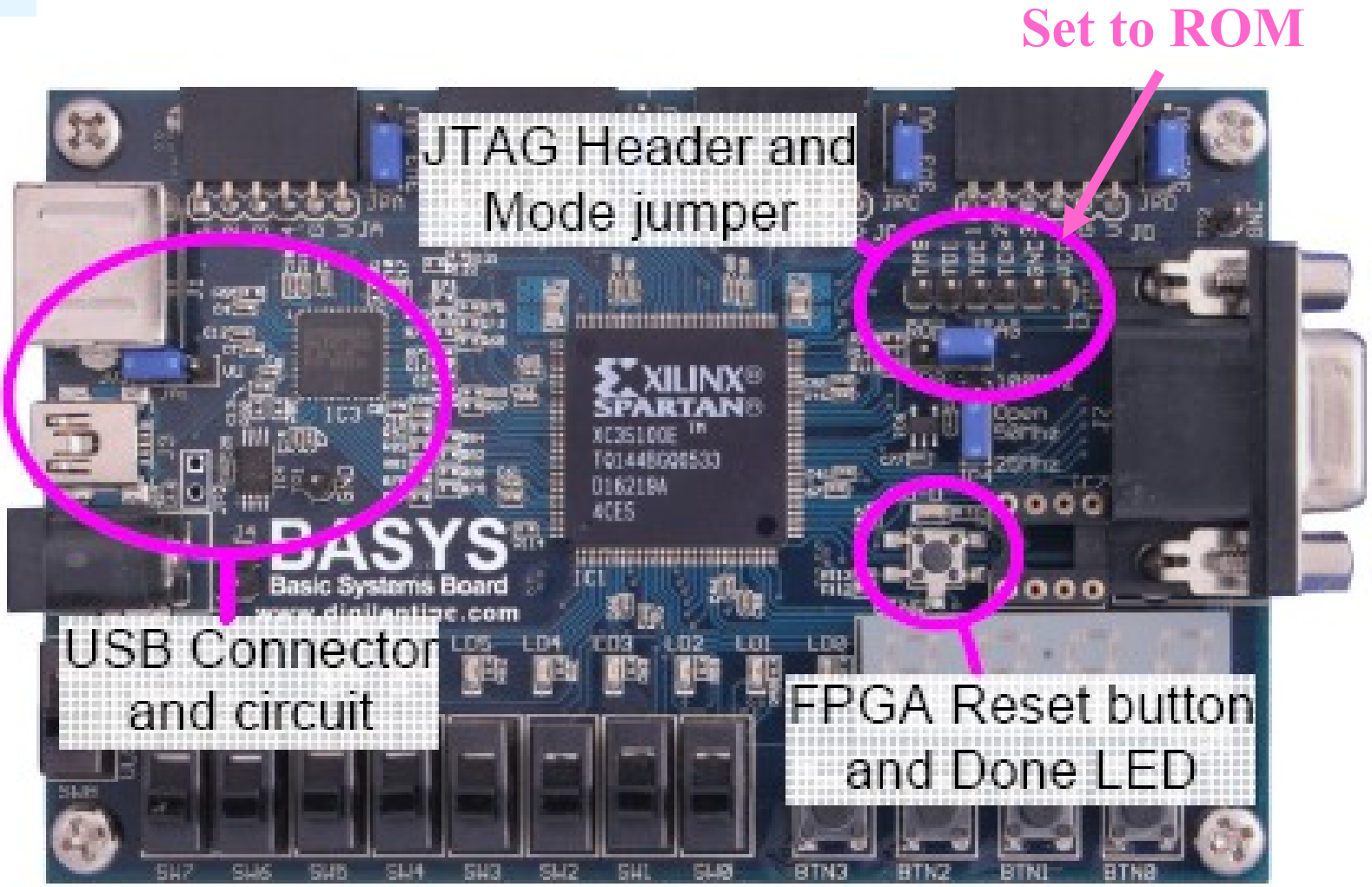

Demo1 - [C:\Hayne\ELEC311\Examples\Demo1\planAhead_run_1\Demo1.ppr] - PlanAhead 13.2
File Edit Tools Window Layout View Help
Search commands
I/O Planning
RTL Design - Demo1.ucf (target) * | xc3s100etq144-5
Sources
Search:
Demo1.vhf [work]
Constraints (1)
constrs_1
Demo1.ucf
Sources RTL Netlist Timing Con..
I/O Port Properties
Z
Name: Z
General Configure
Properties Clock Regions
Package
Device
I/O Ports
Name Dir Neg Diff Pair Site Bank I/O Std Vcco Vref Drive Strength Slew Type Pull Type
All ports (5)
Scalar ports (5)
F Output P15 3 LVCMOS25 2.5 12 SLOW
X Input P29 3 LVCMOS25 2.5 12 SLOW
XY Output P14 3 LVCMOS25 2.5 12 SLOW
Y Input P36 3 LVCMOS25 2.5 12 SLOW
Z Input P38 2 LVCMOS25 2.5 12 SLOW

Synthesize & Implement

- Synthesize Design
- Implement Design
- Generate Programming File

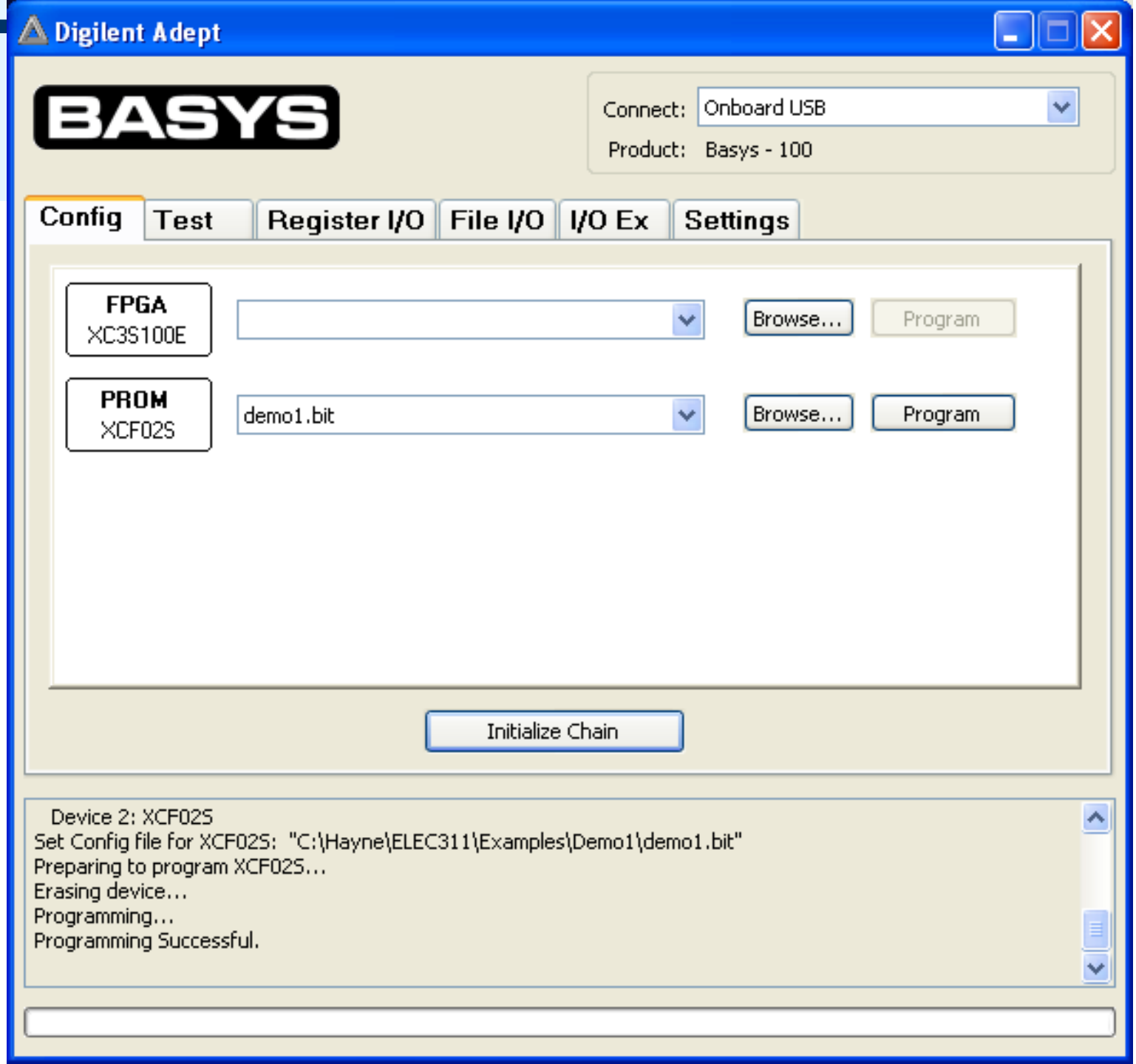


BASYS Configuration



Configure Device

- Configure Device (Adept)
  - Initialize Chain
  - XCF02S (PROM)
    - demo1.bit
  - Program
  - Cycle Power (Reset)


Digilent Adept
BASYS
Connect: Onboard USB
Product: Basys - 100
Config
Test
Register I/O
File I/O
I/O Ex
Settings
FPGA
XC3S100E
Browse...
Program
PROM
XCF02S
demo1.bit
Browse...
Program
Initialize Chain
Device 2: XCF02S
Set Config file for XCF02S: "C:\Hayne\ELEC311\Examples\Demo1\demo1.bit"
Preparing to program XCF02S...
Erasing device...
Programming...
Programming Successful.

Test the Design

Project Report

- Cover Sheet
  - Project Name/Number
  - Authors
  - Professor's Initials
- Objectives
- Discussion
  - Boolean Equation
  - Truth Table
  - Circuit Schematic
- Conclusion
  - Test Results