# Combinational Circuit Design

ELEC 311

Digital Logic and Circuits

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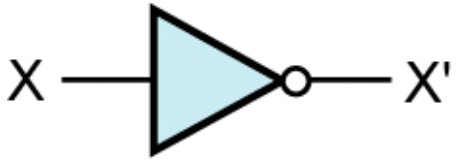
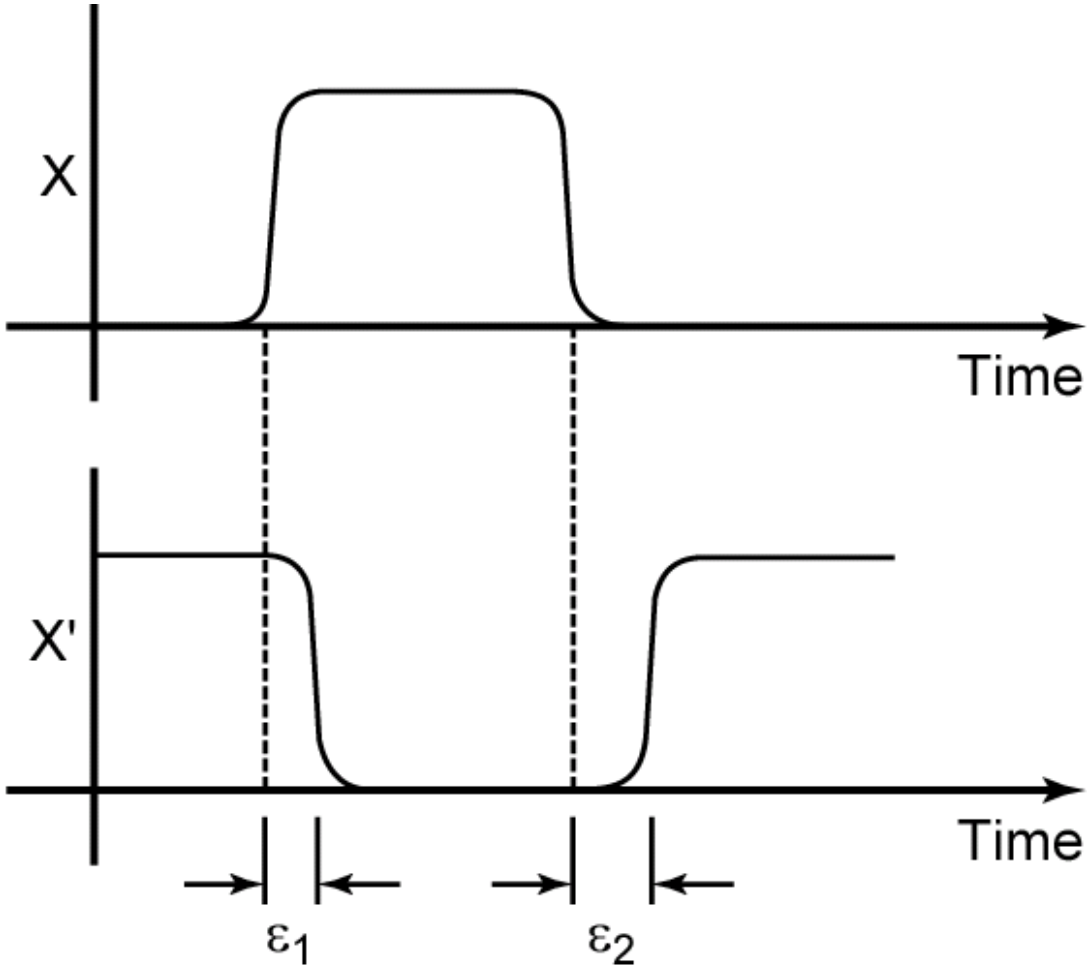
*Images Courtesy of Cengage Learning*

THE CITADEL
DEPARTMENT OF ELECTRICAL & COMPUTER ENGINEERING

# Propagation Delay



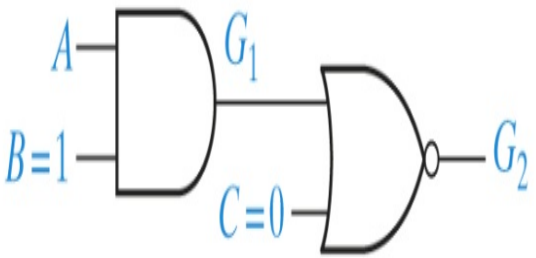



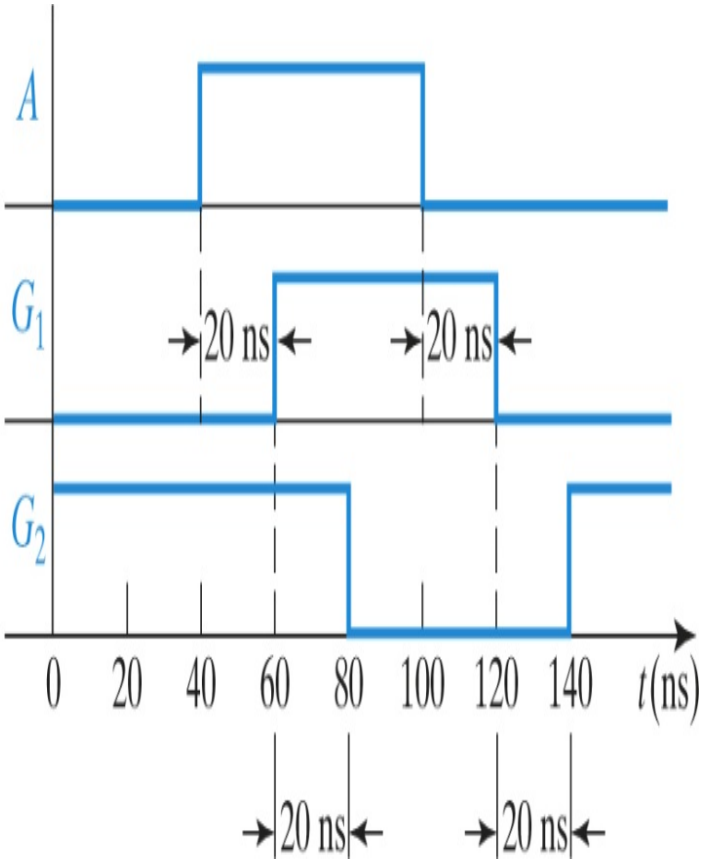
# Timing Diagrams

**FIGURE 8-5**

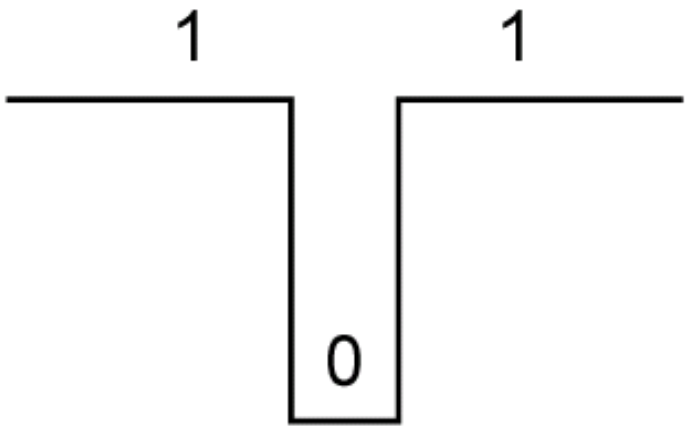
Timing Diagram for AND-NOR Circuit



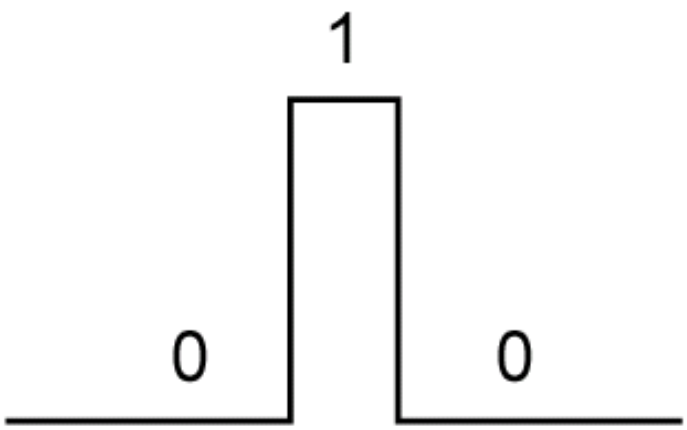


# Static Hazards




(a) Static 1-hazard

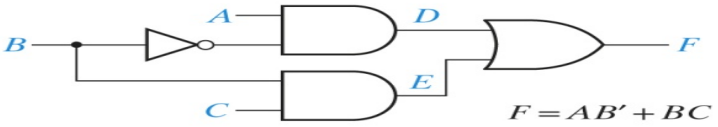



(b) Static 0-hazard

# Detection of a Static Hazard

**FIGURE 8-8**
Detection of a 1-Hazard

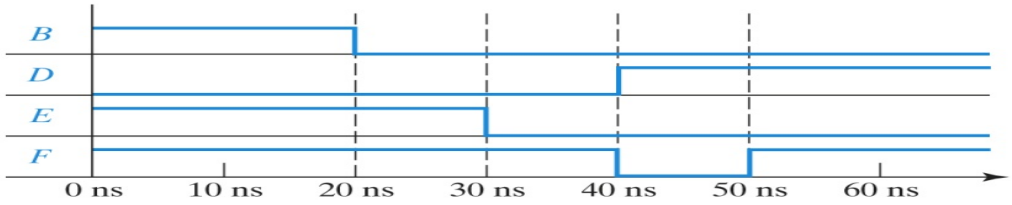





| BC \ A | 0 | 1 |
|---|---|---|
| 00 | 0 | 1 |
| 01 | 0 | 1 |
| 11 | 1 | 1 |
| 10 | 0 | 0 |

1-hazard

(a) Circuit with a static 1-hazard

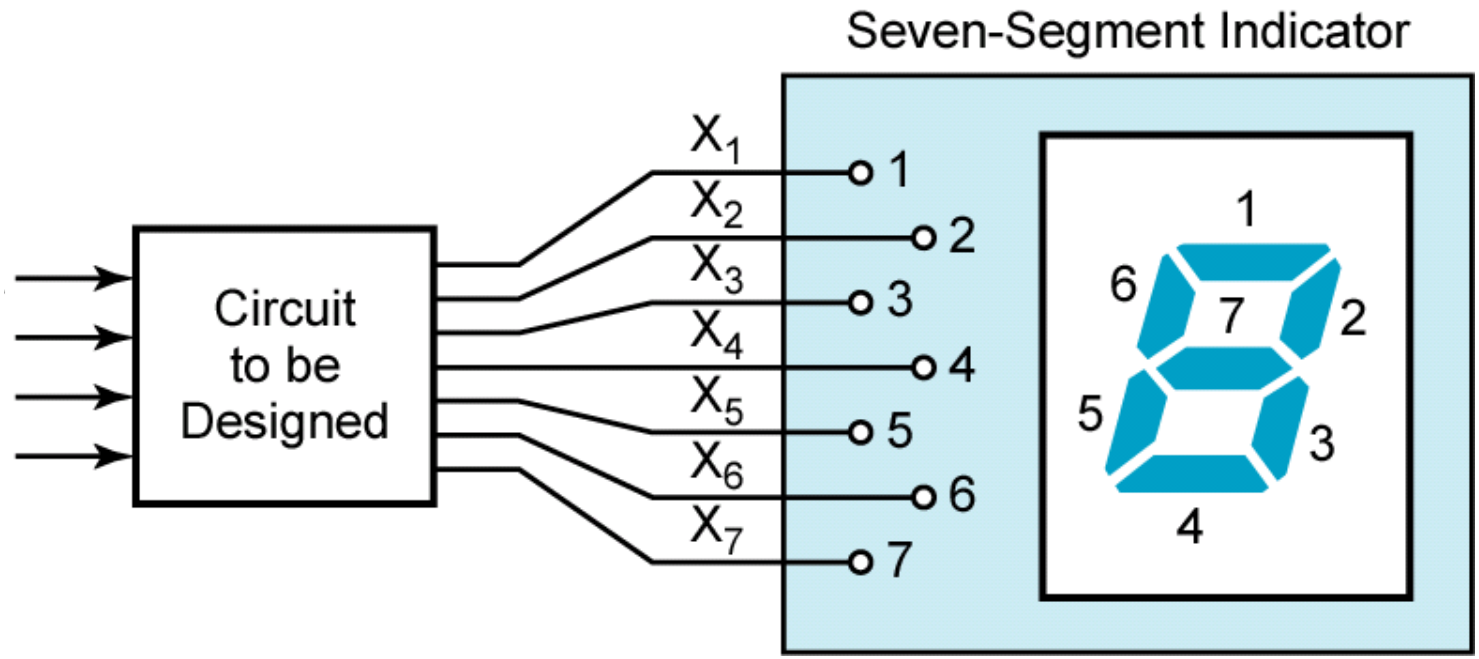


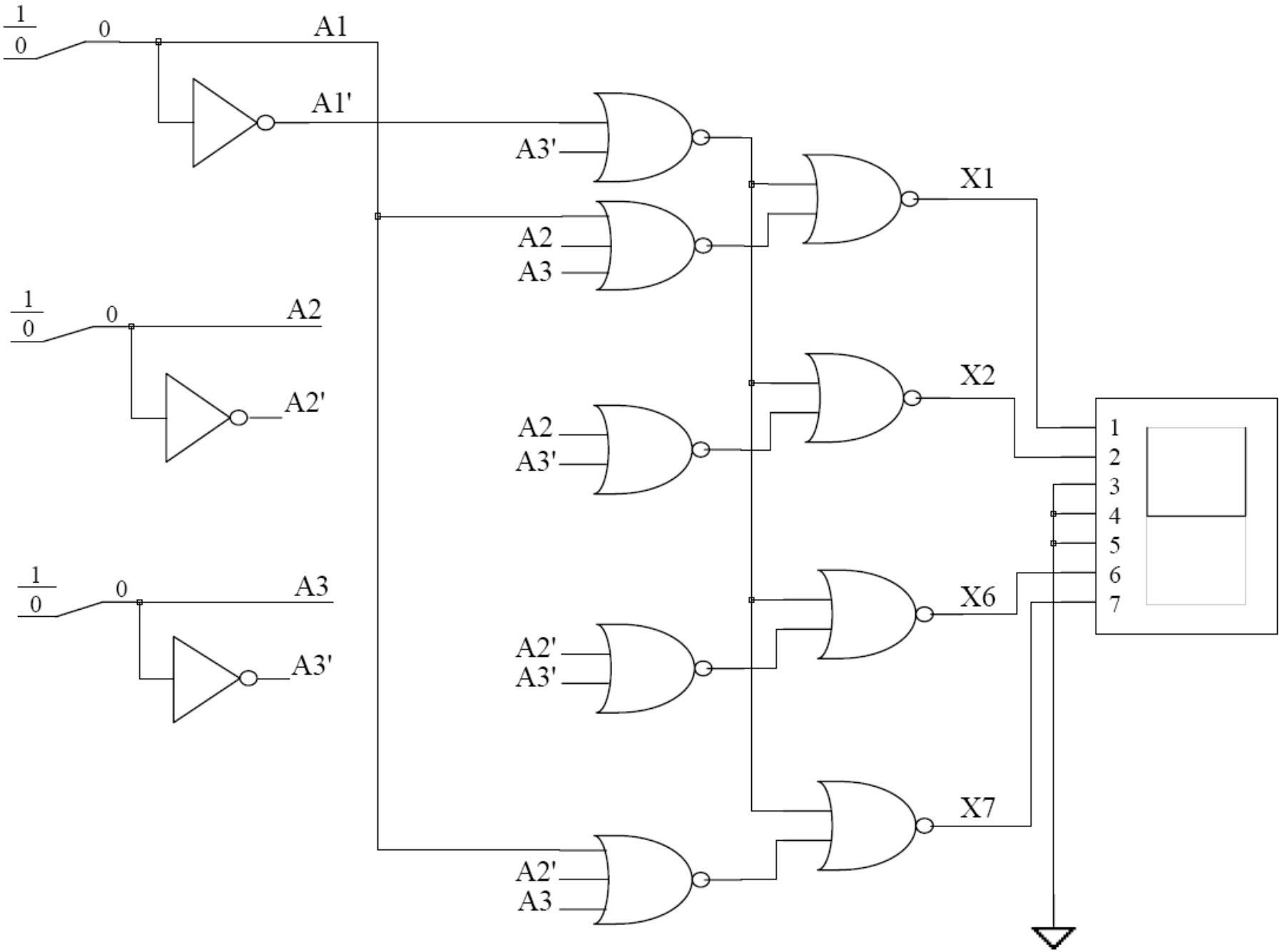

(b) Timing chart

# Testing of Logic Circuits

- Truth Table
  - Input Combinations
  - Verify Outputs
- Incorrect Outputs
  - Error Design
  - Error in Wiring
  - Error in Gate

# Design Example




1
0
0
A1
A1'
A3'
A2
A3
X1
1
0
0
A2
A2'
A2
A3'
X2
1
0
0
A3
A3'
A2'
A3'
X6
A2'
A3
X7
1
2
3
4
5
6
7