

ELEC 418 Test 1 Review

Practice Questions:

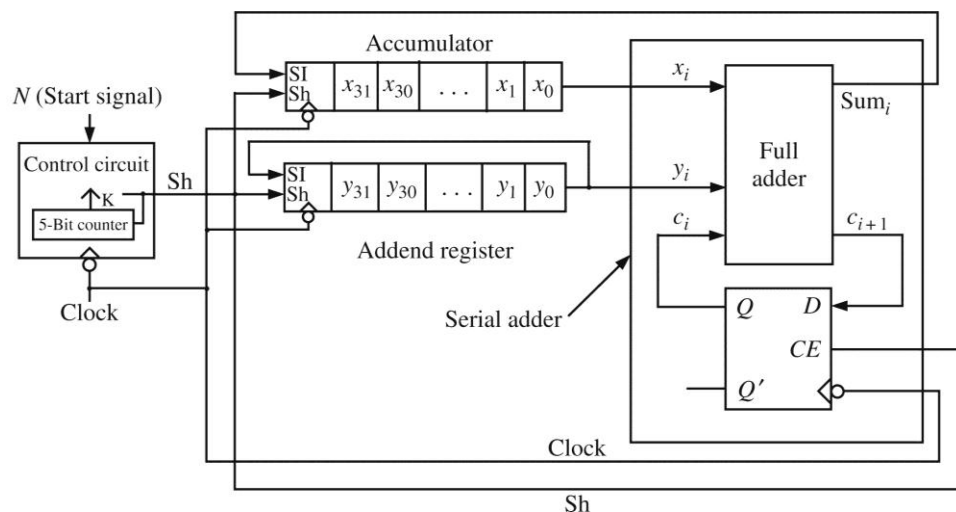
1. Perform the following 4-bit two's complement multiplication and verify your answer in base 10: $3/4 \times -1/2 = ?$.
2. Draw the circuit generated by the following VHDL model:

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entity Review is
  port(A, C, S: in bit;
        B: in bit_vector(0 to 1);
        Y: out bit);
end Review;
architecture Behave of Review is
  signal X: bit_vector(0 to 1);
begin
  Y <= X(0) when S = '0' else X(1);
  process(C)
  begin
    if C'event and C = '1' then
      X <= A&A or B;
    end if;
  end process;
end Behave;

```

3. Write a VHDL model for a 16-bit serial-in, serial-out shift register with inputs SI (serial input), EN (enable), and CK (rising-edge triggered clock) and a serial output (SO).
4. Given the following block diagram for a 32-bit serial adder. The control circuit uses a 5-bit counter, which outputs a signal $K = 1$ when it is in state 11111. When a start signal (N) is received, the registers and counter are loaded. When the addition is complete, the control circuit should go to a stop state and remain there until N is changed back to 0.



- a. Draw the state diagram for the control circuit.
- b. Write a complete VHDL model for the adder. Use two processes: one to generate the control signals and one to update the registers based on those signals.