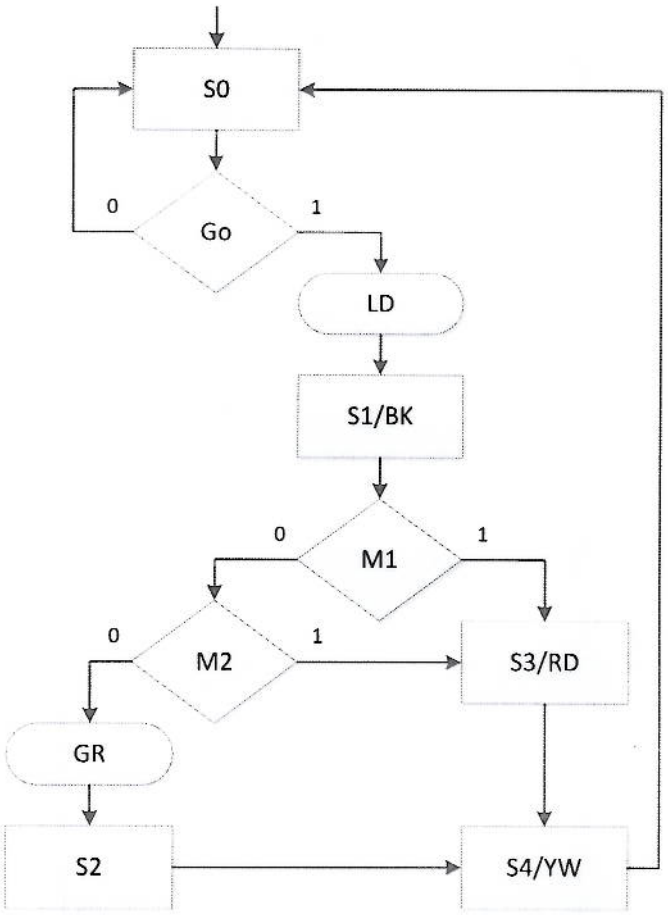
Given the following SM Chart:



1. Write a complete VHDL model (entity and behavioral architecture) for the controller. Use two processes for the combinational and sequential parts of the circuit.

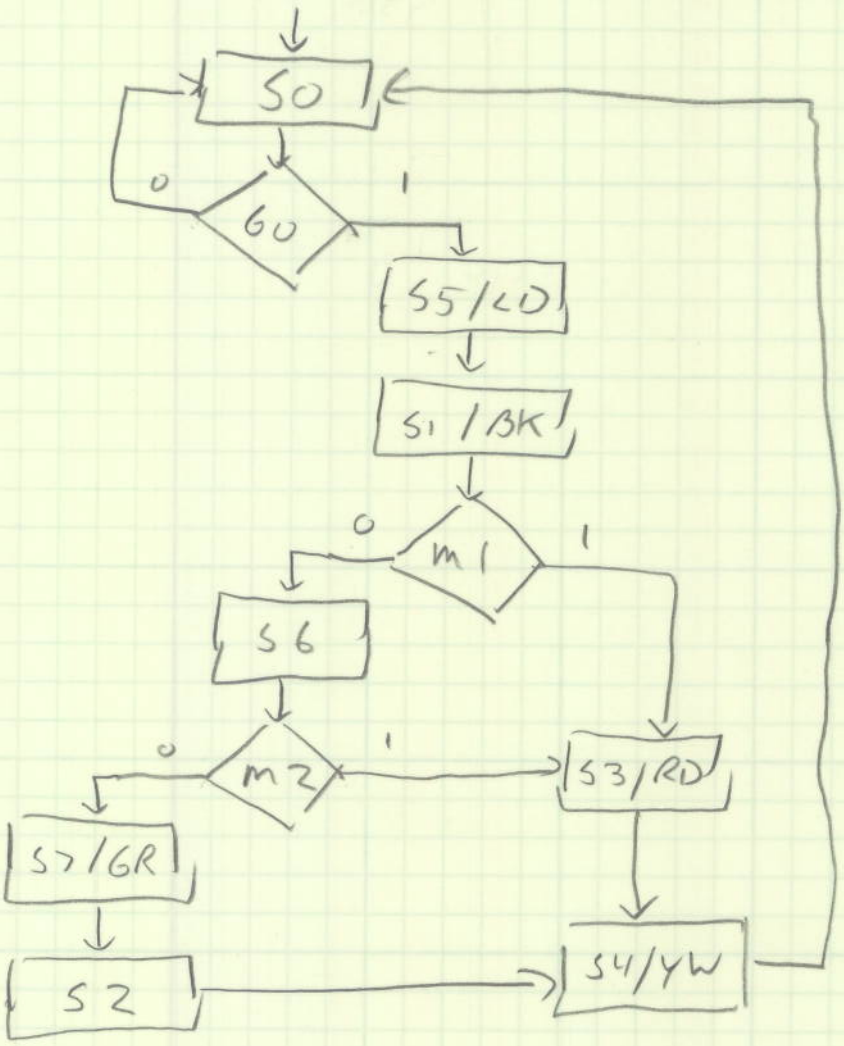
2. Realize the controller using a two-address microprogram.
   a) Convert the SM chart to proper form by adding a minimum number of states.
   b) Write the microprogram required to implement the circuit.

(1)


```
entity Controller is
  port (Go, clk : in bit;
        M : in bit_vector (1 to 2);
        LD, BK, GR, RD, YW : out bit);
end Controller;
architecture Behave of Controller is
  signal PS, NS : integer 0 to 4;
begin
  process (Go, M, PS)
  begin
    LD <= '0'; BK <= '0'; GR <= '0'; RD <= '0'; YW <= '0';
    case PS in
      when 0 =>
        if Go = '0' then
          NS <= 0;
        else
          LD <= '1'; NS <= 1;
        end if;
      when 1 =>
        BK <= '1';
```

```
        if m(1) = '0' then
            if m(2) = '0' then
                GR <= '1'; NS <= 2;
            else
                NS <= 3;
            end if;
        else
            NS <= 3;
        end if;
    when 2 =>
        NS <= 4;
    when 3 =>
        RD <= '1'; NS <= 4;
    when 4 =>
        YW <= '1'; NS <= 0;
    end case
end process;
process (clk)
begin
    if rising_edge(clk) then
        PS <= NS;
    end if;
end process;
end Behave;
```

(2) a)



TEST	
00	GO
01	m1
10	m2
11	1

b)

STATE	ADDR	TEST	NSF	NST	LD	BK	GR	RD	YW
S0	000	00	000	101	0	0	0	0	0
S1	001	01	110	011	0	1	0	0	0
S2	010	11	100	100	0	0	0	0	0
S3	011	11	100	100	0	0	0	1	0
S4	100	11	000	000	0	0	0	0	1
S5	101	11	001	001	1	0	0	0	0
S6	110	10	111	011	0	0	0	0	0
S7	111	11	100	100	0	0	1	0	0