ELEC-313
Lab 5: CMOS Circuits

October 30, 2013

Date Performed: October 16, 2013
Partners: Charles Pittman
Stephen Wilson

Contents

1 Objective **3**

2 Equipment **3**

3 Schematics **3**

4 Procedure **3**
4.1 CMOS Inverter 3
4.2 CMOS NAND 4

5 Results **5**

6 Conclusion **7**

List of Figures

1 Circuits used in this lab. 3
2 Output of CMOS inverter 5
3 Transition point in CMOS inverter 6
4 Output of CMOS NAND gate 6

List of Tables

1 NAND logic table 5

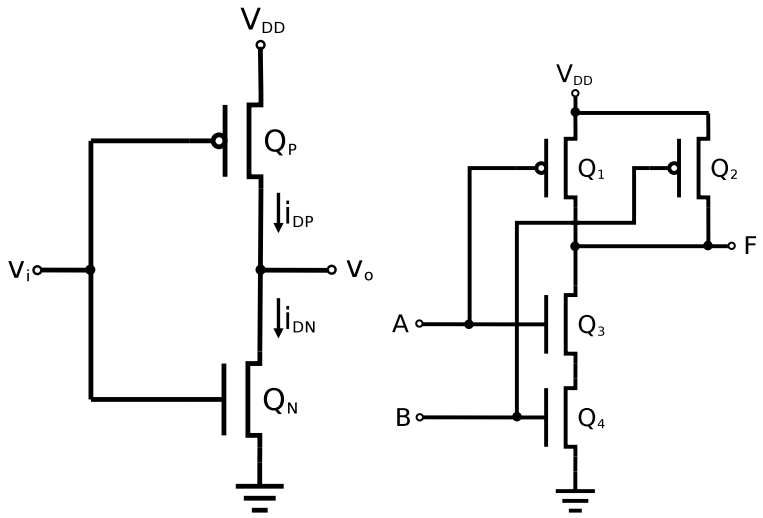
1 Objective

The objective is to construct and observe the operation of a CMOS inverter and NAND gate.

2 Equipment

- ALD1105 Dual N-channel and P-channel matched pair MOSFET
- Power supply: HP E3631A
- Oscilloscope: Agilent 54622D
- Function generator: HP 33120A

3 Schematics



(a) CMOS Inverter (b) CMOS NAND

Figure 1: Circuits used in this lab.

4 Procedure

4.1 CMOS Inverter

1. Construct the circuit of figure 1a.
2. Connect the V+ terminal (Pin 11) to the + supply voltage

3. Connect the V− terminal (Pin 4) to the circuit ground.

4. Set VDD to 5 V using the HP source.

5. Use the function generator to input V_i. Set the function generator to a frequency of 20 kHz and select a triangle wave. Set the wave for 0 to 5 volts using the offset.

6. Connect CHANNEL 1 of the oscilloscope to the input and CHANNEL 2 to the output.

7. Use the x-y plot function of the scope to produce the transfer characteristic V_o vs. V_i. (Press the main key, then select the xy softkey, then adjust the voltage scales as needed.)

8. Capture the V_o vs. V_i. data, so you can recreate the plot for the lab report.

9. Adjust the amplitude and offset of the function generator for an input square wave of 0 to 5 V as measured on the oscilloscope.

10. Adjust the scope and capture both input and output on one screen for the report.

11. Measure the propagation delay times of the output waveform.

4.2 CMOS NAND

1. Construct the circuit of figure 1b.

2. Connect the v+ terminal (Pin 11) to the + supply voltage.

3. Connect the V− terminal (Pin 4) to the circuit ground.

4. Set the + supply voltage to 5 volts DC using the HP source.

5. Set input A to 0 volts.

6. Use the function generator for input B. Set the function generator to a frequency of 20 kHz and select a square wave. Set the square wave for 0 to 5 V using the offset.

7. Connect CHANNEL 1 of the oscilloscope to the input and CHANNEL 2 to the output.

8. Adjust the scope and capture both input and output on one screen for the report.

9. Repeat step 8 with the input A set to +5 V.

5 Results

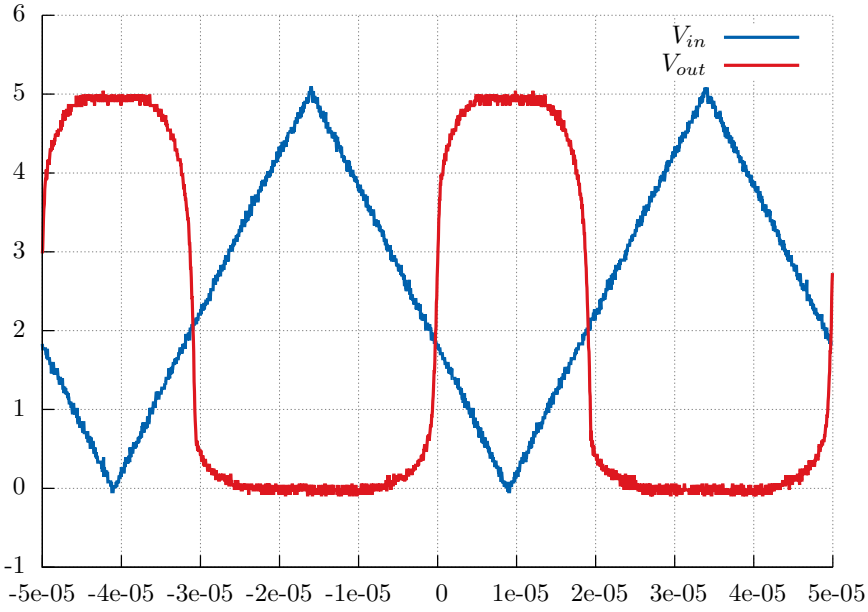


Figure 2: Output of CMOS inverter

A	B	F
0	0	1
0	1	1
1	0	1
1	1	0

Table 1: NAND logic table

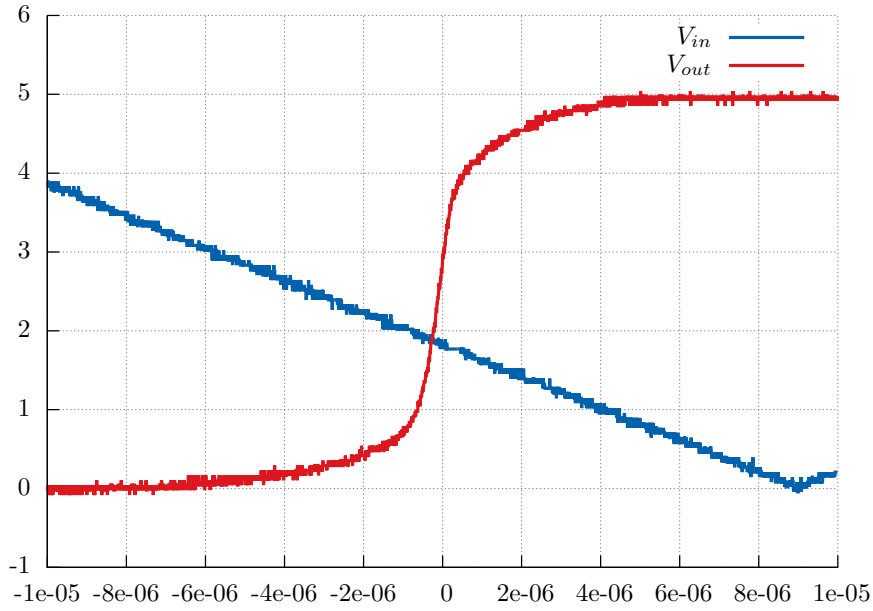


Figure 3: Transition point in CMOS inverter

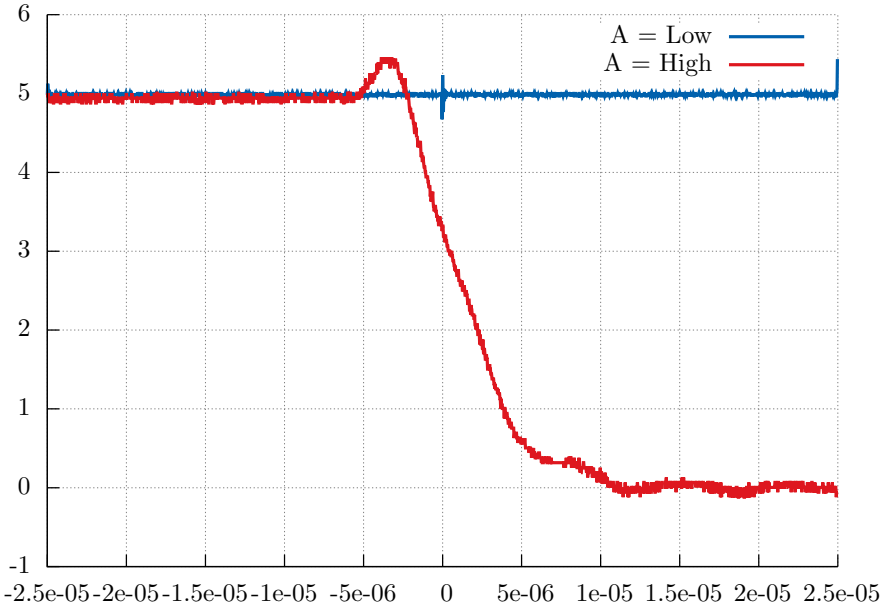


Figure 4: Output of CMOS NAND gate

6 Conclusion

As seen in Figure 2, as the input voltage (V_i) is low (0 V), V_o is high (5 V). Conversely, when V_i is high, V_o is low. This relationship of V_i to V_o is why the configuration is called an inverter. Also, the transition from high to low on the output happens when the input is approximately between 1 and 3V at V_i; that is, when the input voltage is less than one, the output voltage is almost exactly 5 V and when the input voltage is greater than 3V, the output voltage is almost exactly 0 V. (Refer to Figure 2 for a close up of the V_i to V_o). Additionally, the output voltage closely represents a square wave or an on/off relationship as the input voltage is swept back and forth between low and high. It should also be noted that it takes 58.8 nanoseconds for the output voltage response to change from high to low.

The circuit in Figure 1b operates as a NAND gate because when input A is low (0 V), as is the case in the first portion of CMOS NAND experiment, the inverting gate (Q_1) is shorted and the non-inverting gate Q_3 is open. Therefore no matter what input B is shown, the output voltage is high (5 V). In the second half of the experiment, when input A is high (5 V), Q_1 is inverted and therefore open and Q_3 is shorted. During this state, when input B is low, Q_2 is inverted and shorted allowing current to flow through it, but Q_4 is open blocking the current and the output voltage is again high. The only time the output voltage is low, is when A is high and B is high, which means both the inverting gates Q_1 and Q_2 are open and don't allow any current to flow through them.

Figure 4 illustrates the NAND gate logic table (Table 1) exactly. When input A is low, V_o is high whether input B is high or low. When input A is high, V_o is high while input B is low; when input B goes high, V_o drops to low.