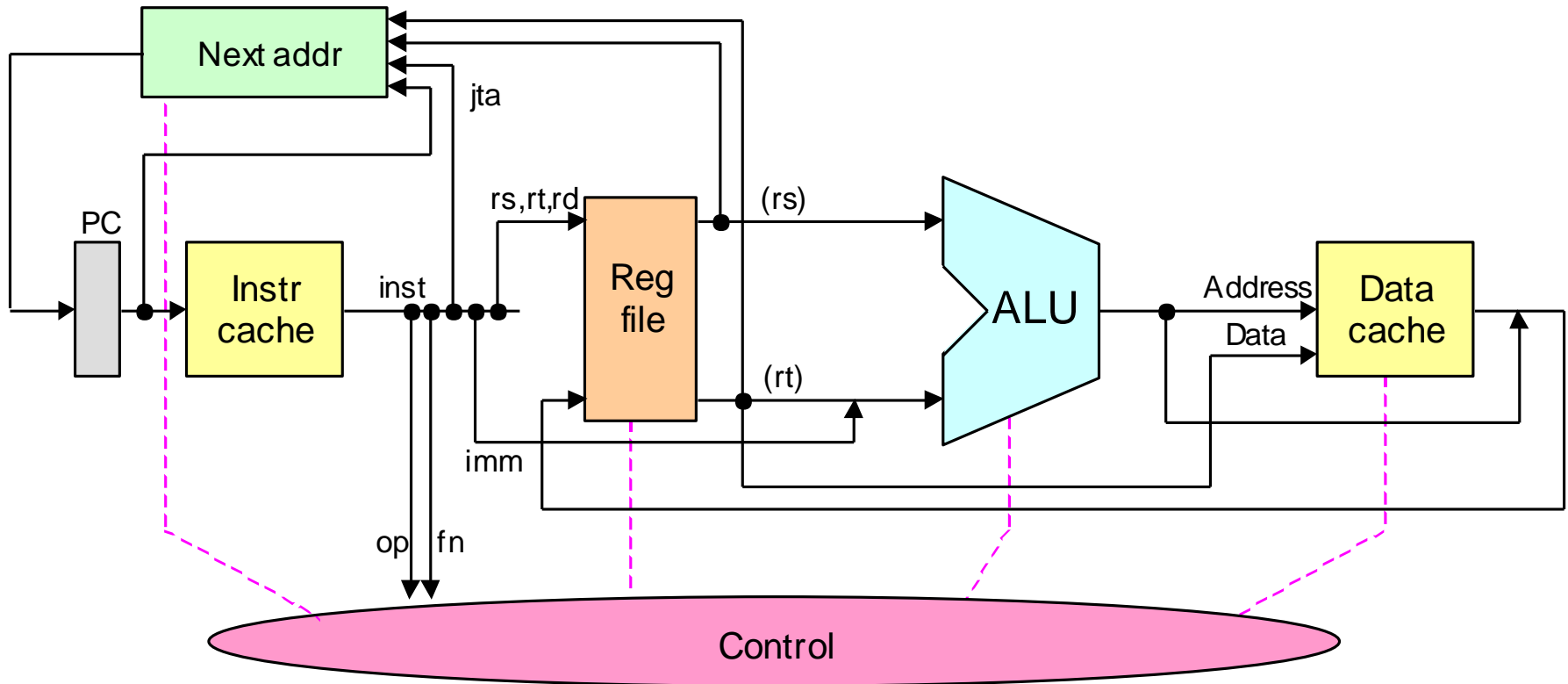# MicroMIPS

Fig. 13.2   Abstract view of the instruction execution unit for MicroMIPS.

MicroMIPS Addressing Modes
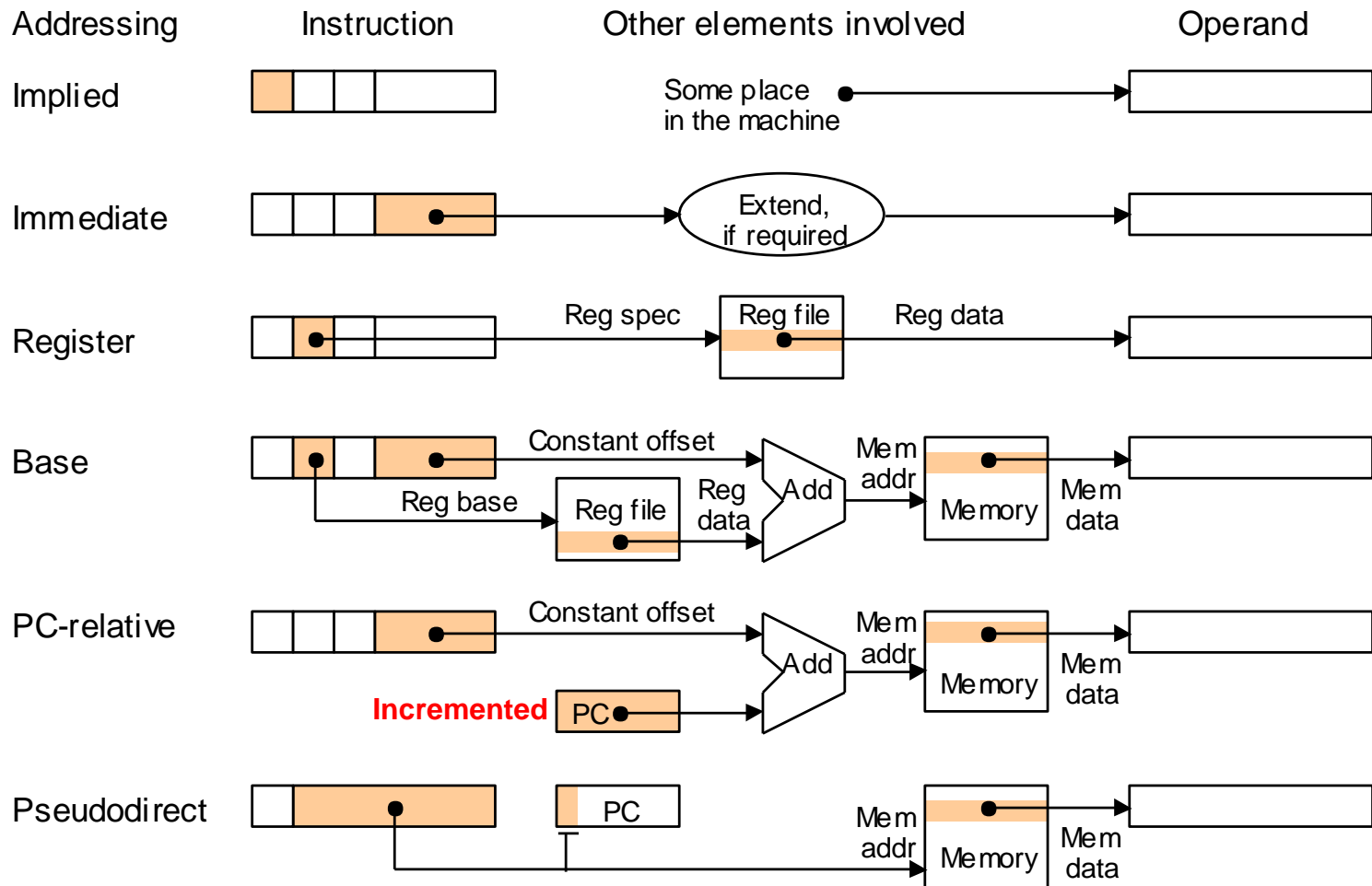

Figure 5.11   Schematic representation of addressing modes in MicroMIPS.
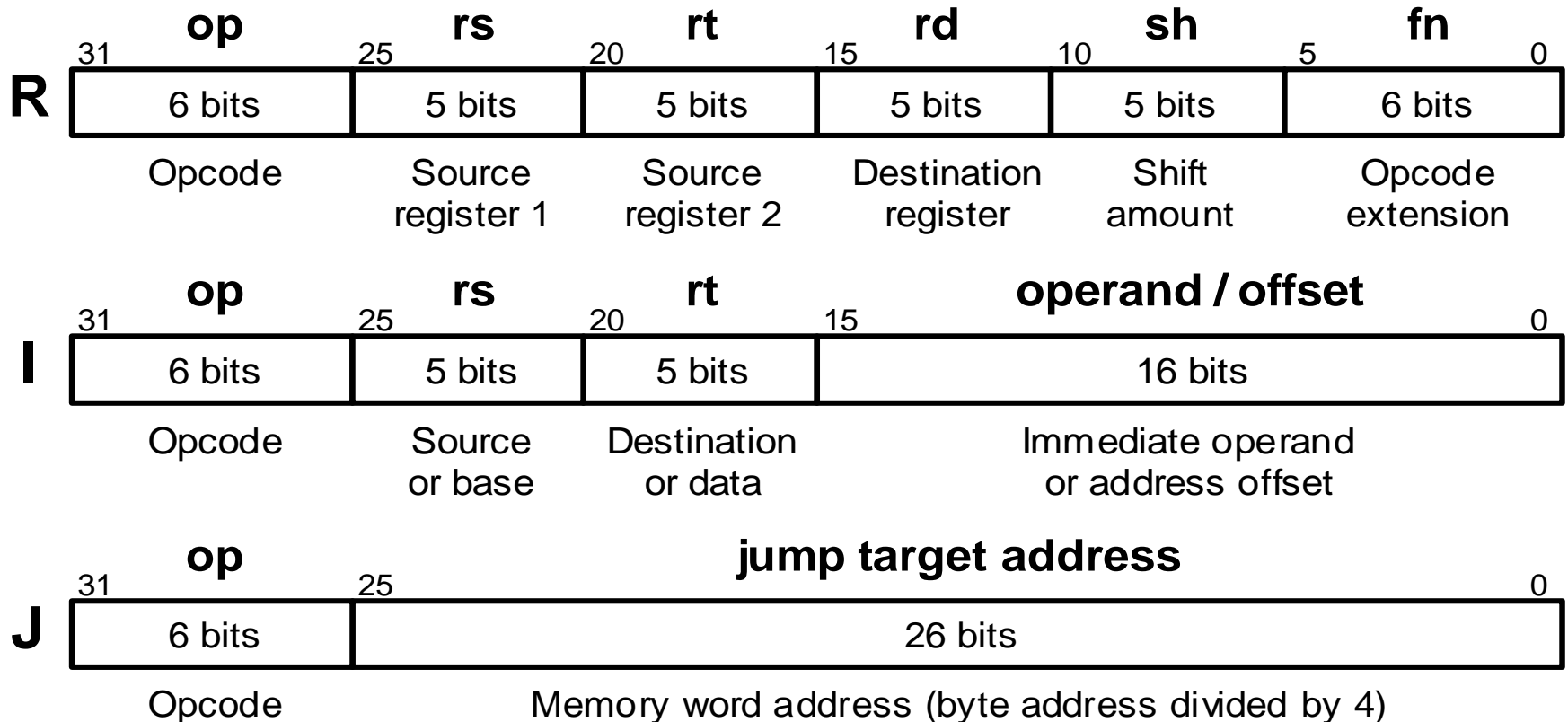
MIPS Instruction Formats

	op	rs	rt	rd	sh	fn
R	6 bits	5 bits	5 bits	5 bits	5 bits	6 bits
	Opcode	Source register 1	Source register 2	Destination register	Shift amount	Opcode extension

	op	rs	rt	operand / offset
I	6 bits	5 bits	5 bits	16 bits
	Opcode	Source or base	Destination or data	Immediate operand or address offset

	op	jump target address
J	6 bits	26 bits
	Opcode	Memory word address (byte address divided by 4)

Figure 5.4   MicroMIPS instructions come in only three formats: register (R), immediate (I), and jump (J).

The MicroMIPS Instruction Set

Instruction	Usage	op	fn
Copy			
Load upper immediate	`lui    rt,imm`	15	
Arithmetic			
Add	`add    rd,rs,rt`	0	32
Subtract	`sub    rd,rs,rt`	0	34
Set less than	`slt    rd,rs,rt`	0	42
Add immediate	`addi   rt,rs,imm`	8	
Set less than immediate	`slti   rt,rs,imm`	10	
Logic			
AND	`and    rd,rs,rt`	0	36
OR	`or     rd,rs,rt`	0	37
XOR	`xor    rd,rs,rt`	0	38
NOR	`nor    rd,rs,rt`	0	39
AND immediate	`andi   rt,rs,imm`	12	
OR immediate	`ori    rt,rs,imm`	13	
XOR immediate	`xori   rt,rs,imm`	14	
Memory access			
Load word	`lw     rt,imm(rs)`	35	
Store word	`sw     rt,imm(rs)`	43	
Control transfer			
Jump	`j      L`	2	
Jump register	`jr     rs`	0	8
Branch less than 0	`bltz   rs,L`	1	
Branch equal	`beq    rs,rt,L`	4	
Branch not equal	`bne    rs,rt,L`	5	
Jump and link	`jal    L`	3	
System call	`syscall`	0	12

Table 13.1

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