MOSFET Physical Effects and Models

from

Device Electronics for Integrated Circuits, 3rd Edition, Muller, et al,

ELCT 424

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Pre-MOSFET History

- MOS theory pre-dates bipolar transistors
  - Patents issued in the early 1930s
  - Did not include Silicon as a material
  - Otherwise, strikingly similar to today's MOSFETs
- In the 1940s, Schockley writes "With the metal plate positive, then the additional charge on the semiconductor will be represented by an increased number of electrons" which "should be free to move and should contribute to the conductivity of the semiconductor."
- Created the bipolar transistor in 1948, and only later produced the first operating MOS transistors.

4 Decades of MOSFETS

The most extensively used solid state device

- Relatively simple to fabricate
- Scalable
  - 200X reduction over ~30 years
- Totally displaced bipolar in memory devices
- Dominates logic circuits
  - Especially high performance microprocessors

Scaling

Constant-Field Scaling Rules

- Dennard (1974)
- Not really rules, but guidelines

Parameter	Scaling Factor
Surface dimensions, L	1/K
Vertical dimensions, x_{ox}, x_j	1/K
Impurity concentrations	K
Currents, Voltages	1/K
Current densities	K
Capacitance/area	K
Transconductance	1
Circuit delay time	1/K
Power dissipation	$1/K^2$
Power density	1
Power-delay product	$1/K^3$

Past and Predicted Scaling

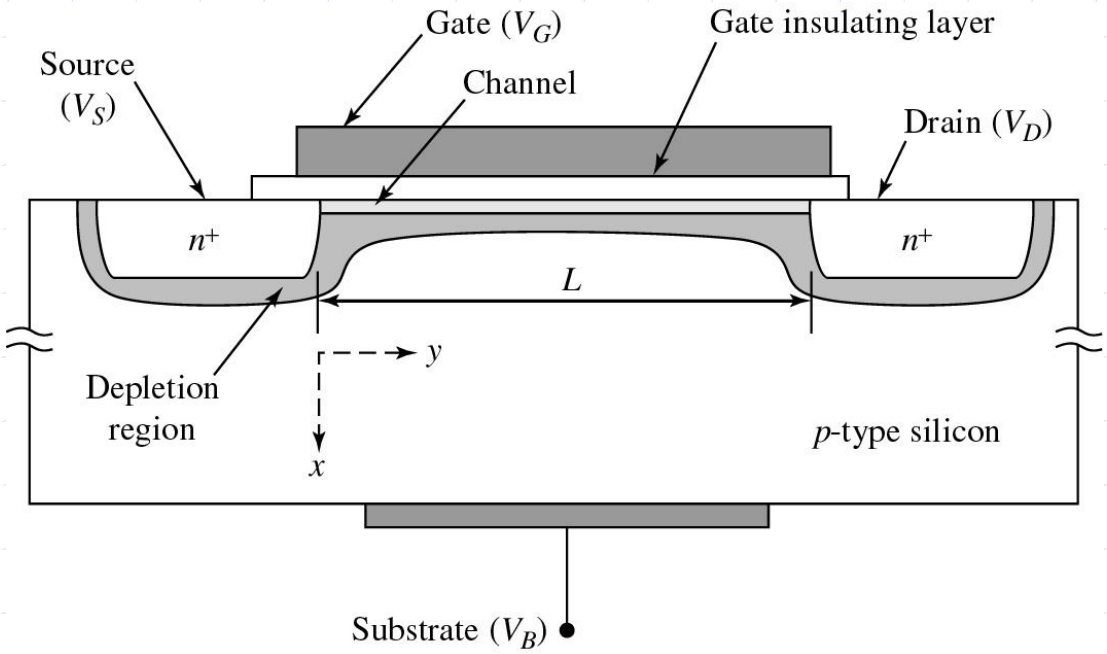
TABLE 9.2 Past and Predicted Technology Scaling Trends for MOS Technology, from *International Technology Roadmap for Semiconductors* (*1997–2001 editions*) [3]

Year of Production	1997	1999	2001	2003	2006	2010	2016
Min. dim. L (μm)	0.25	0.18	0.13	0.1	0.07	0.045	0.022
DRAM density (Gbits/cm^2)	0.18	0.38	0.42	0.91	1.85	4.75	28.85
Logic V_{DD} (V)	2.5–1.8	1.8–1.5	1.2	1.0	0.9	0.6	0.4
Equivalent x_{ox} (nm)	4–5	1.9–2.5	2.3	2.0	1.9	1.2	0.9
Junction depth x_j (nm)	50–100	45–70	30–60	26–52	20–40	15–30	10–20
Local wire pitch (nm)	600	500	350	245	130	105	30
Metal aspect ratio	1.8	2	1.6*	1.6	1.7	1.8	2.0
max. I_{Dsat} NMOS	600	750	900	900	900	900	900
(μA/μm) PMOS	280	350	420	420	420	420	420

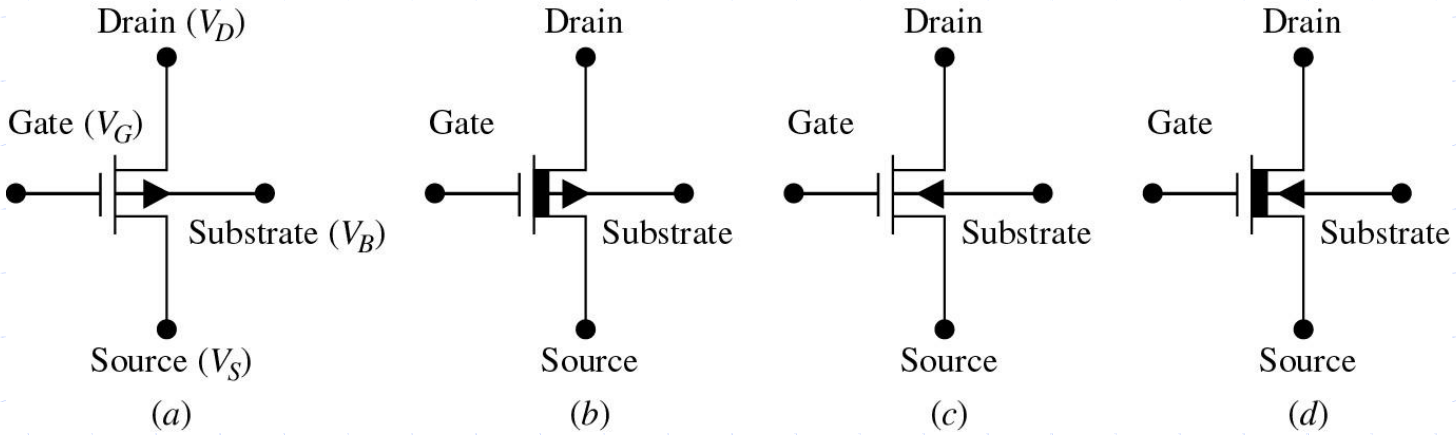
* Switching to copper Manufacturable solution yet to be found.

Basic MOSFET Behavior

Channel length, *L*, extends along *y*-axis
Depth into the silicon is *x*-axis
Width extends along the *z*-axis into the drawing



Types of MOSFETs



a) Enhancement mode, p-channel
b) Depletion mode p-channel
c) Enhancement mode, n-channel
d) Depletion mode, n-channel

Basic Drain Current Equation

$$I_D = WQ_n(y)\upsilon(y) = WQ_n(y)\mu_n \partial V(y)/\partial y$$

V_G = gate voltage
V_S = source voltage
V_D = drain voltage
V_B = bulk voltage (sometimes tied to source)

$$Q_n(y) = -C_{ox}[V_G - V_T - V(y)]$$

Substitute $Q_n(y)$ into the I_D equation and integrate across L

$$I_D = \mu_n C_{ox} \frac{W}{L}\left[\left(V_G - V_T - \frac{1}{2}V_D\right)V_D\right] \qquad (9.1.5)$$

$V(y)$ goes from V_S at y=0, to V_D at y=L

NOTE: (9.1.5) valid only for $V_D <$ or= $V_G - V_T$

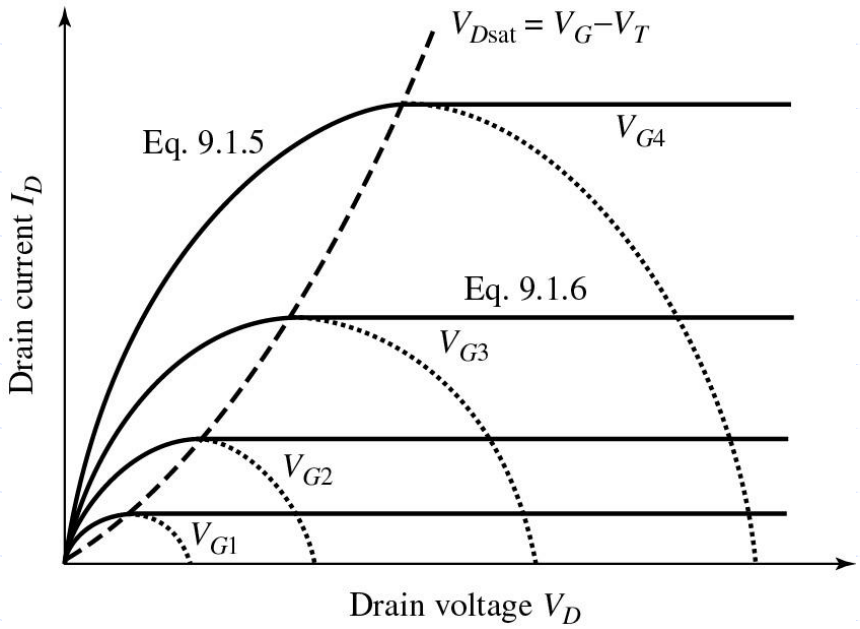
Characteristic Curves

Channel "pinch-off"

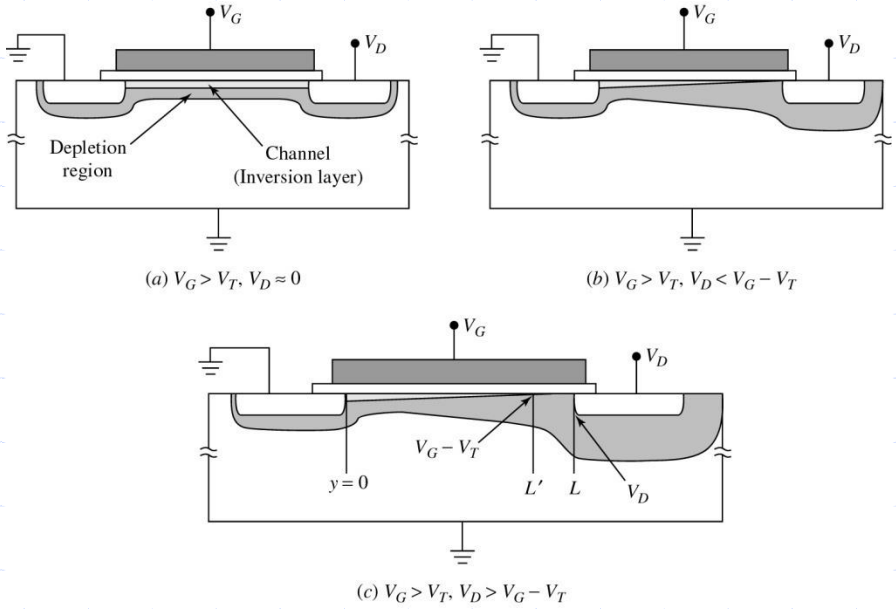
$V_D = V_G - V_T$

Operating in saturation region is per $I_{D_{sat}} = \mu_n C_{ox}(V_G - V_T)^2$

Derived by substituting $V_D = V_G - V_T$ into (9.1.5)

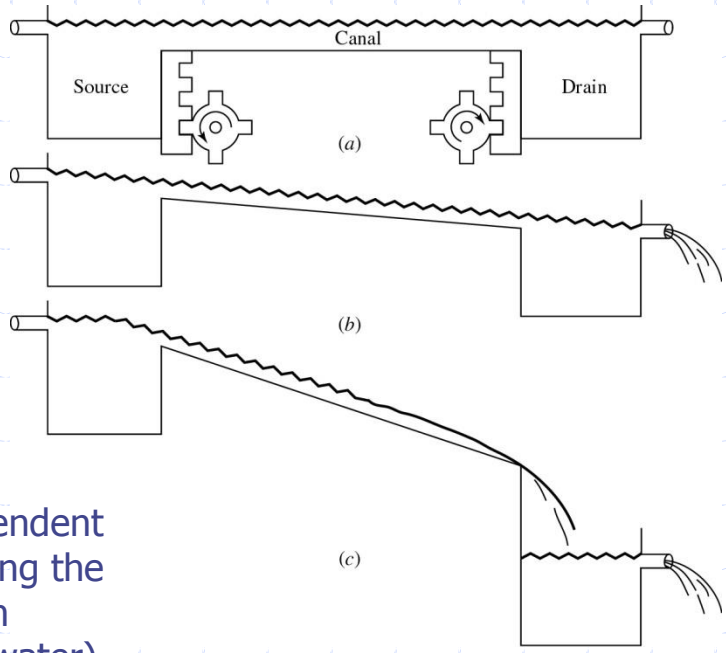


Gate and Drain Bias Effects



V_D modulates depletion region

$I_D = I_S$ = charge*velocity and depends on channel geometry



Saturation results when flow is dependent only on the rate of charge leaving the source, no longer dependent on channel geometry (free falling water)

Channel Length Modulation

(9.1.5) Predicts Long Channel MOSFET Behavior Well

Channel lengths are constantly scaled down

- Increase drive current (faster switching)
- Device density

I_D continues to increase with large V_D in short channel devices

Because of *Channel Length Modulation*

So called because of the effects of pinchoff

I_{Dsat} for short channel devices

$$I_{Dsat} = \frac{\mu W C_{ox}}{2L}(V_G - V_T)^2\left(1 + \frac{V_D}{V_A}\right)$$

Chapter 6 "Things to Know" for Test #2

- History of FETs.
- Types of FETs (know what the acronyms mean).
- Load line analysis of a simple circuit as shown in these slides.
- Qualitative explanation of MOSFET operation.
- How the source and drained are defined in terms of carriers.
- The FET operating regions and their relation to the characteristic curves.
- The band diagram details associated with channel formation.
- What is scaling?
- How is a scaling factor applied, and how are physical parameters (length, width, thickness, doping, etc.) adjusted to accommodate a scaling factor?
- How is performance (current density, power, power delay product, etc.) related to the scaling factor?
- What are three reliability concerns arise from scaling?