

NAND and NOR Gates

ELEC 311

Digital Logic and Circuits

Dr. Ron Hayne

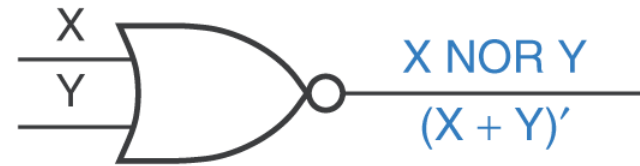
Images Courtesy of Cengage Learning



NAND and NOR Gates



X	Y	X NAND Y
0	0	1
0	1	1
1	0	1
1	1	0



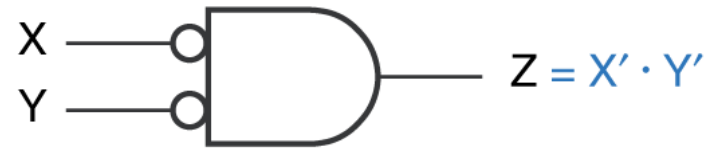
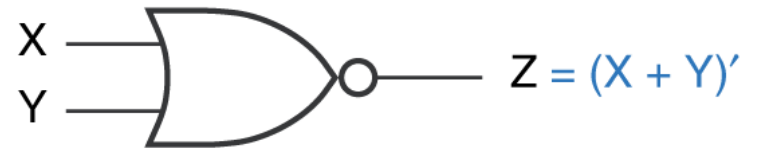
X	Y	X NOR Y
0	0	1
0	1	0
1	0	0
1	1	0

DeMorgan's Laws

◆ $(X \cdot Y)' = X' + Y'$

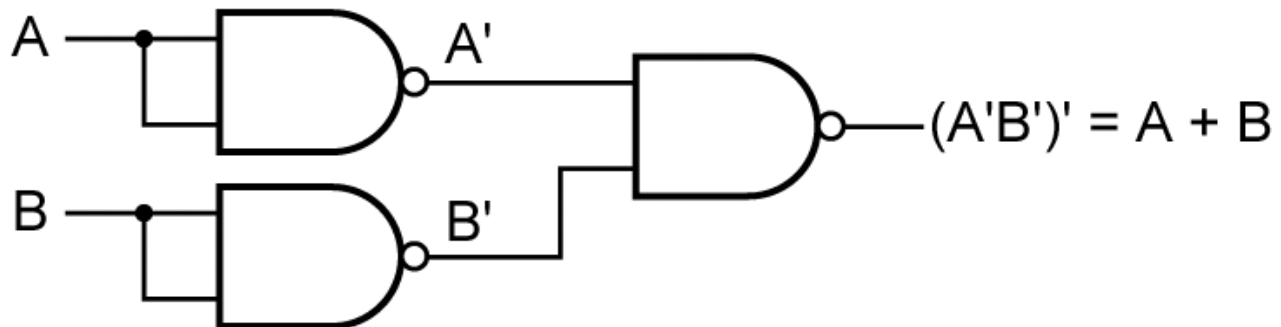
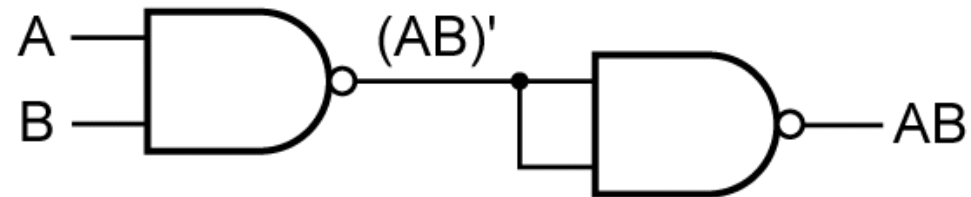
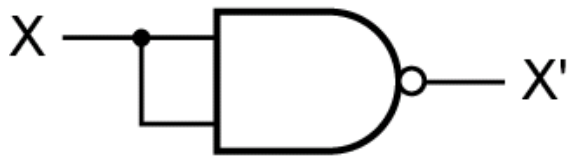


◆ $(X + Y)' = X' \cdot Y'$

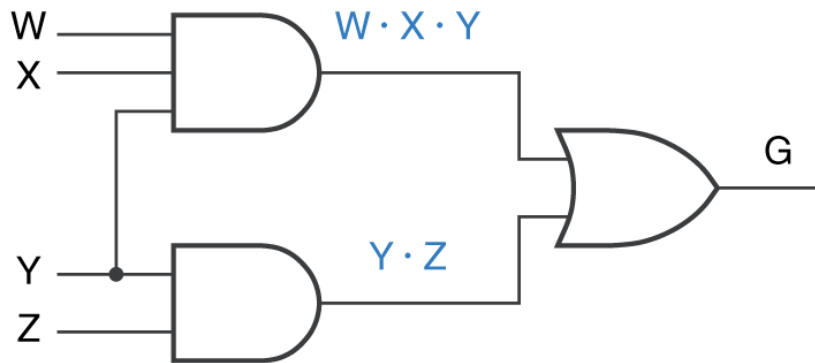


Functionally Complete Set

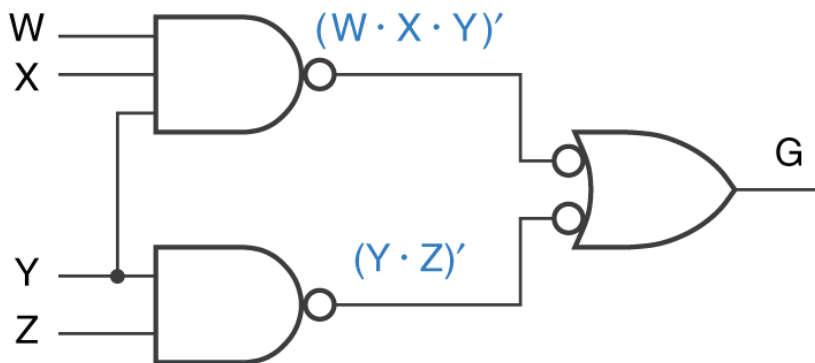
- ◆ Any function can be realized using only NAND gates



SOP to NAND-NAND

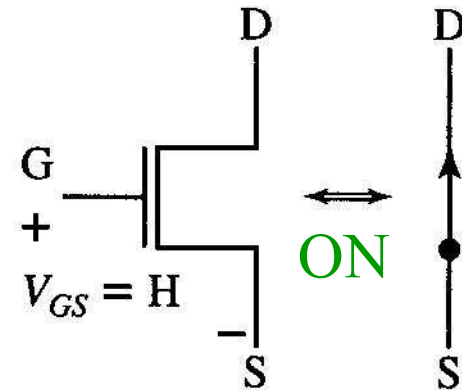
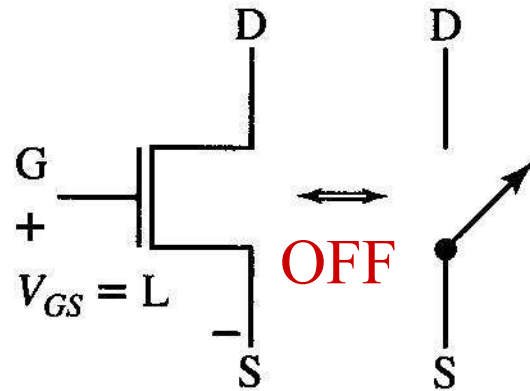


$$G = WXY + YZ$$

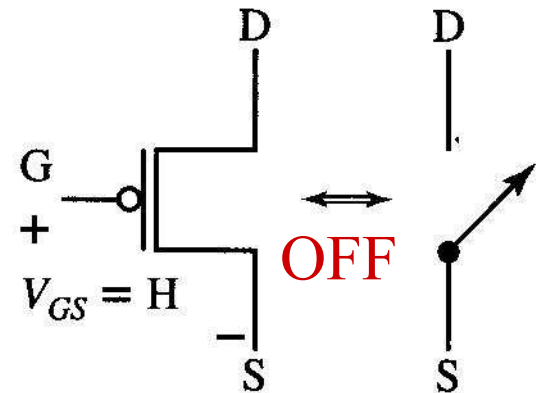
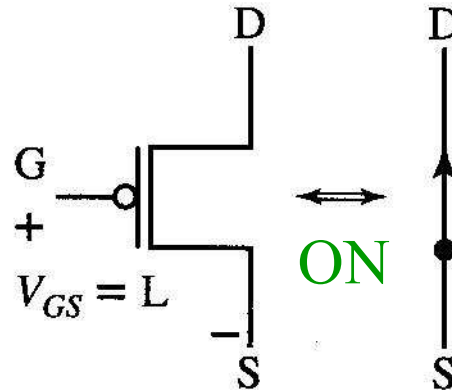


MOSFETs

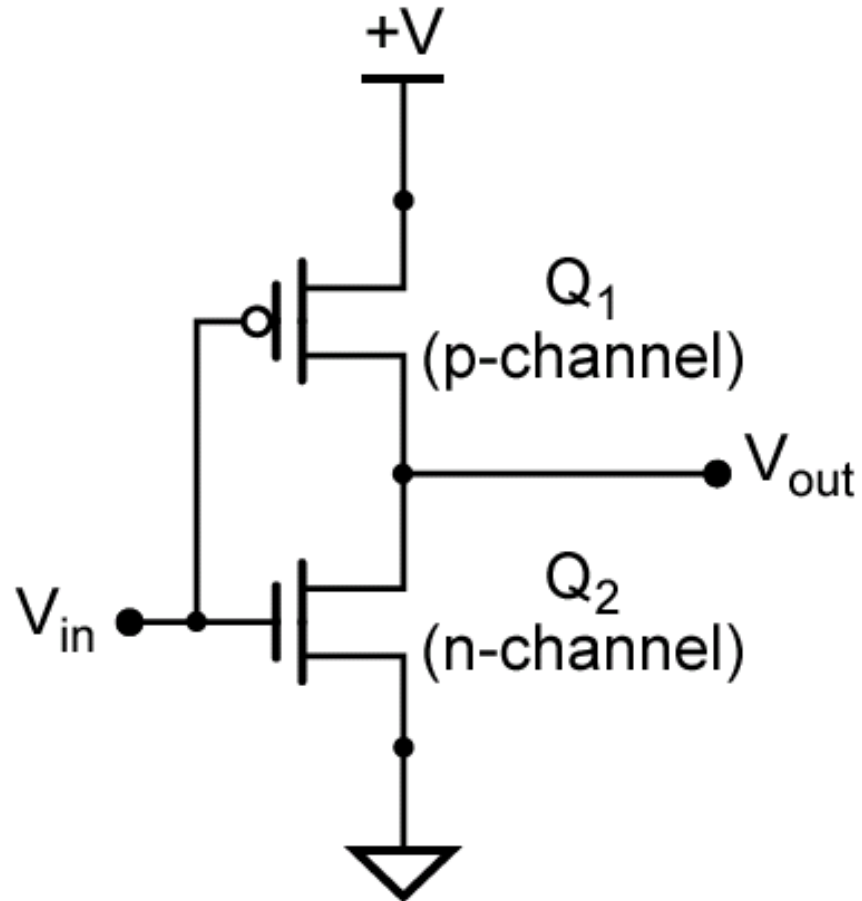
NMOS
(*n*-channel)



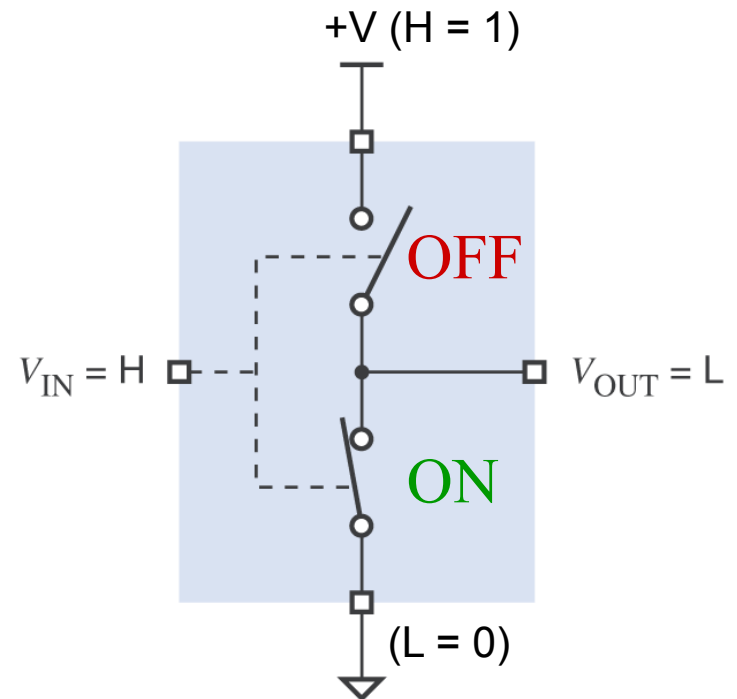
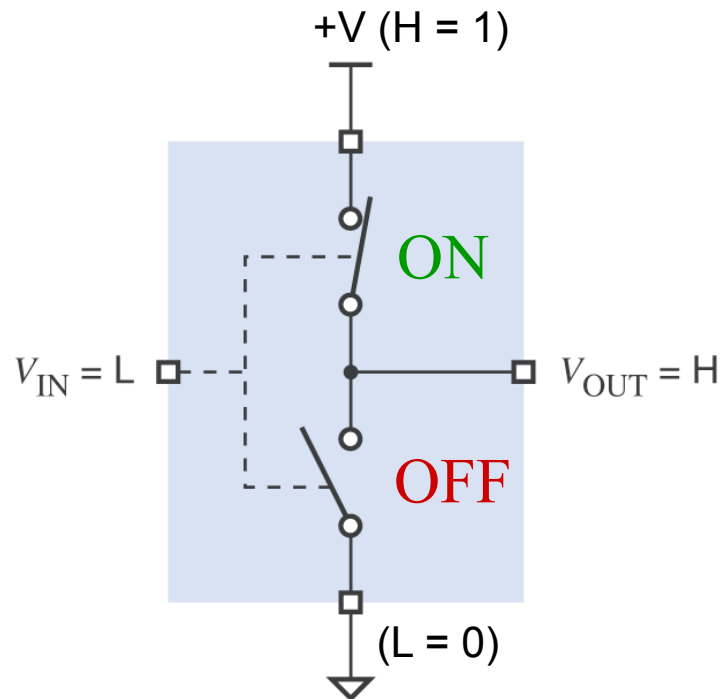
PMOS
(*p*-channel)



CMOS Inverter

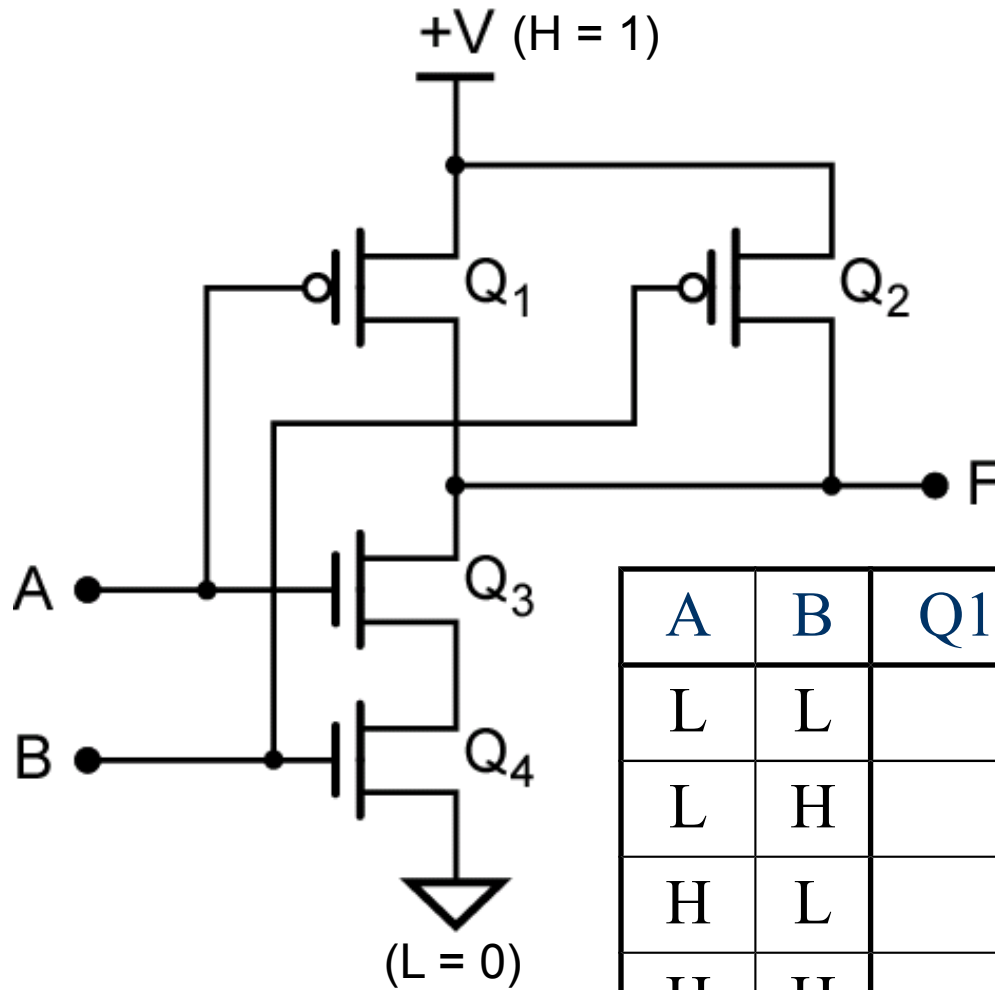


CMOS Inverter



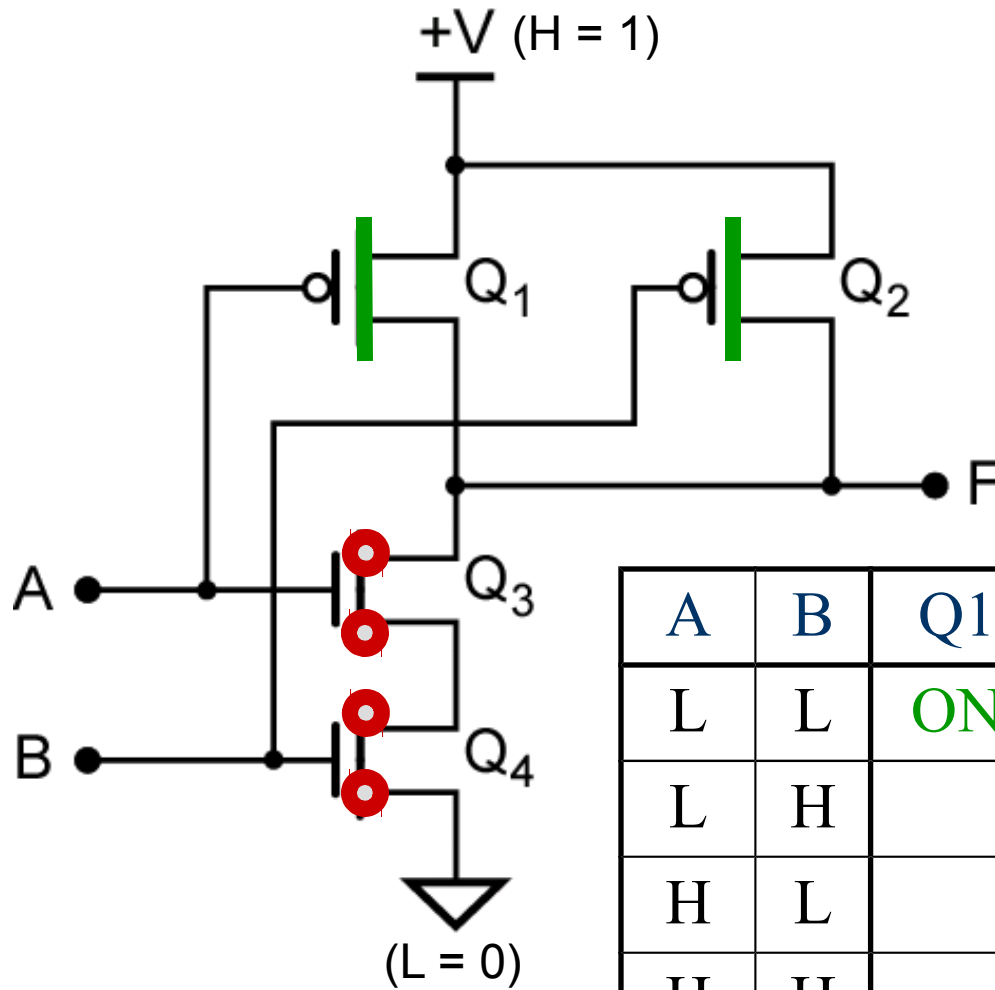
V_{in}	Q1	Q2	V_{out}
0 (L)	ON	OFF	1 (H)
1 (H)	OFF	ON	0 (L)

CMOS NAND Gate



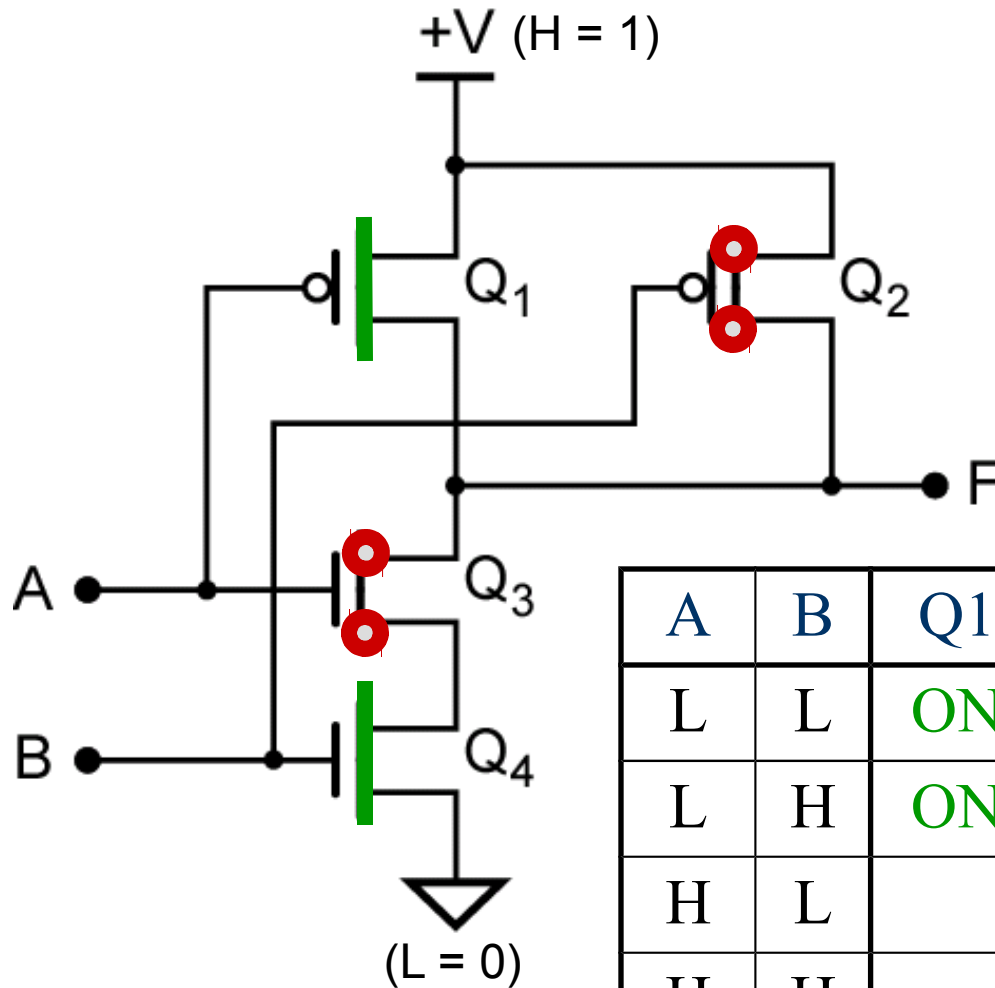
A	B	Q1	Q2	Q3	Q4	F
L	L					
L	H					
H	L					
H	H					

CMOS NAND Gate



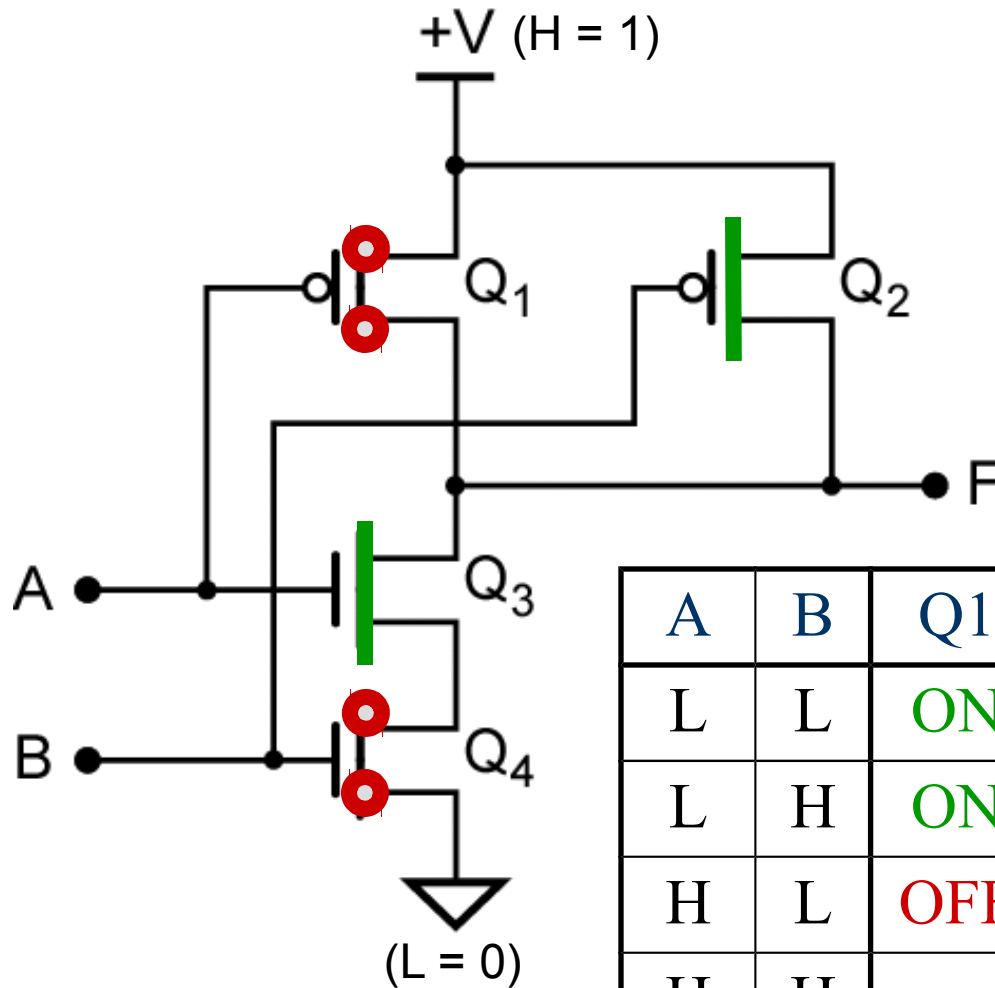
A	B	Q1	Q2	Q3	Q4	F
L	L	ON	ON	OFF	OFF	H
L	H					
H	L					
H	H					

CMOS NAND Gate



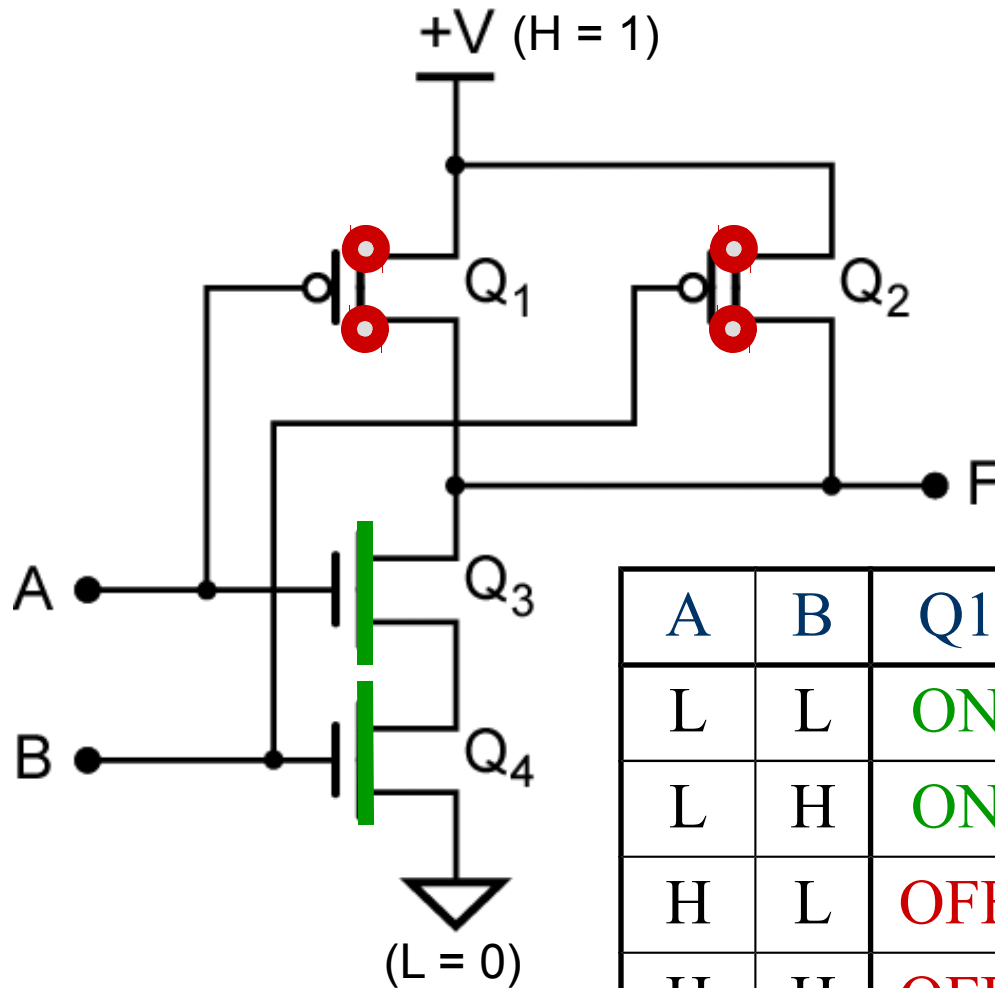
A	B	Q1	Q2	Q3	Q4	F
L	L	ON	ON	OFF	OFF	H
L	H	ON	OFF	OFF	ON	H
H	L					
H	H					

CMOS NAND Gate



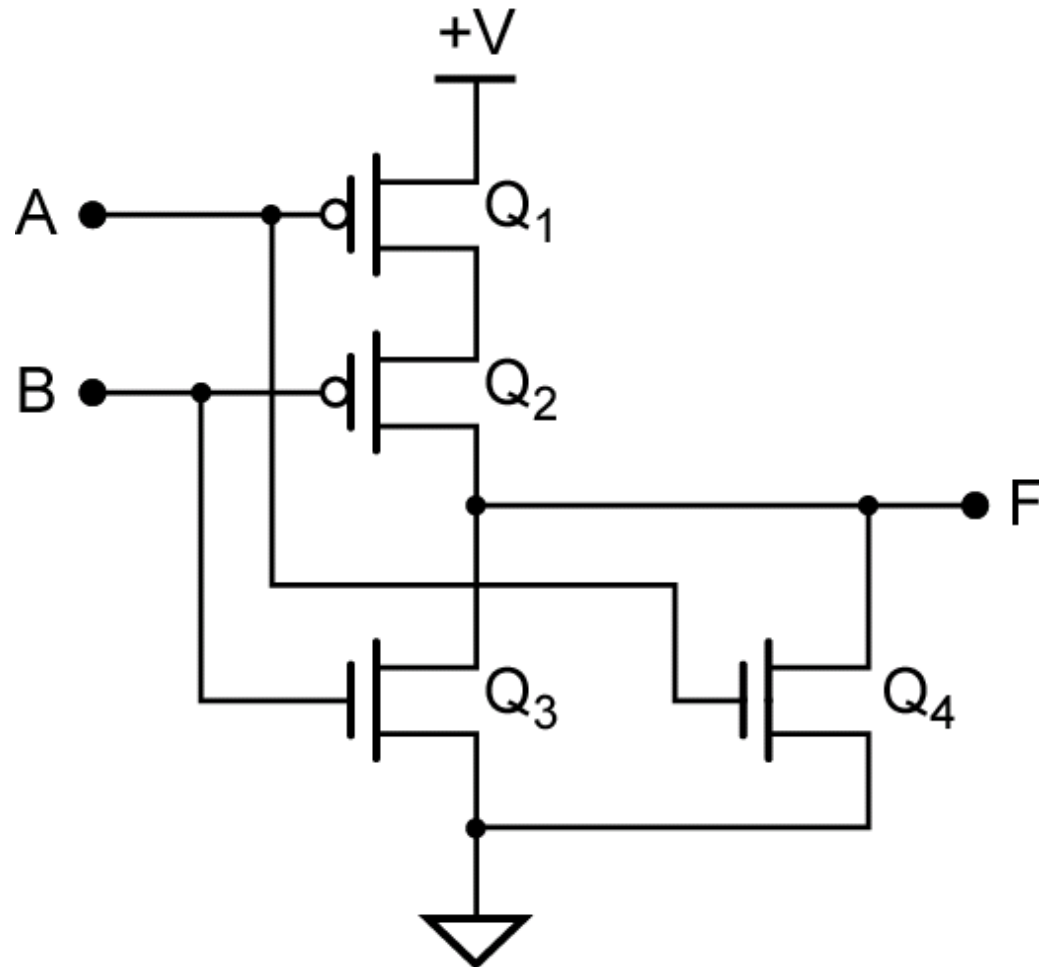
A	B	Q1	Q2	Q3	Q4	F
L	L	ON	ON	OFF	OFF	H
L	H	ON	OFF	OFF	ON	H
H	L	OFF	ON	ON	OFF	H
H	H					

CMOS NAND Gate

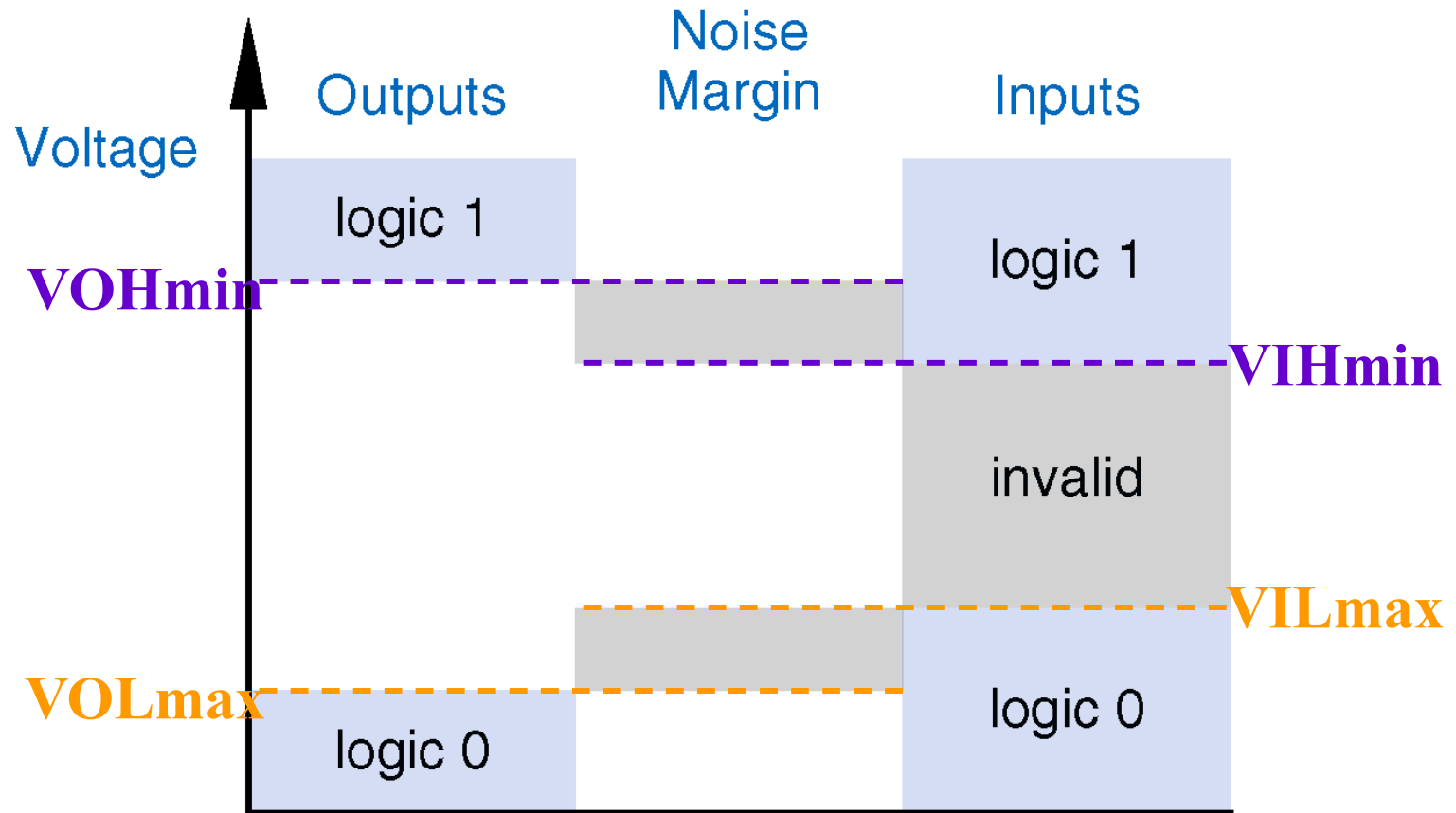


A	B	Q1	Q2	Q3	Q4	F
L	L	ON	ON	OFF	OFF	H
L	H	ON	OFF	OFF	ON	H
H	L	OFF	ON	ON	OFF	H
H	H	OFF	OFF	ON	ON	L

CMOS NOR Gate



Noise Margin



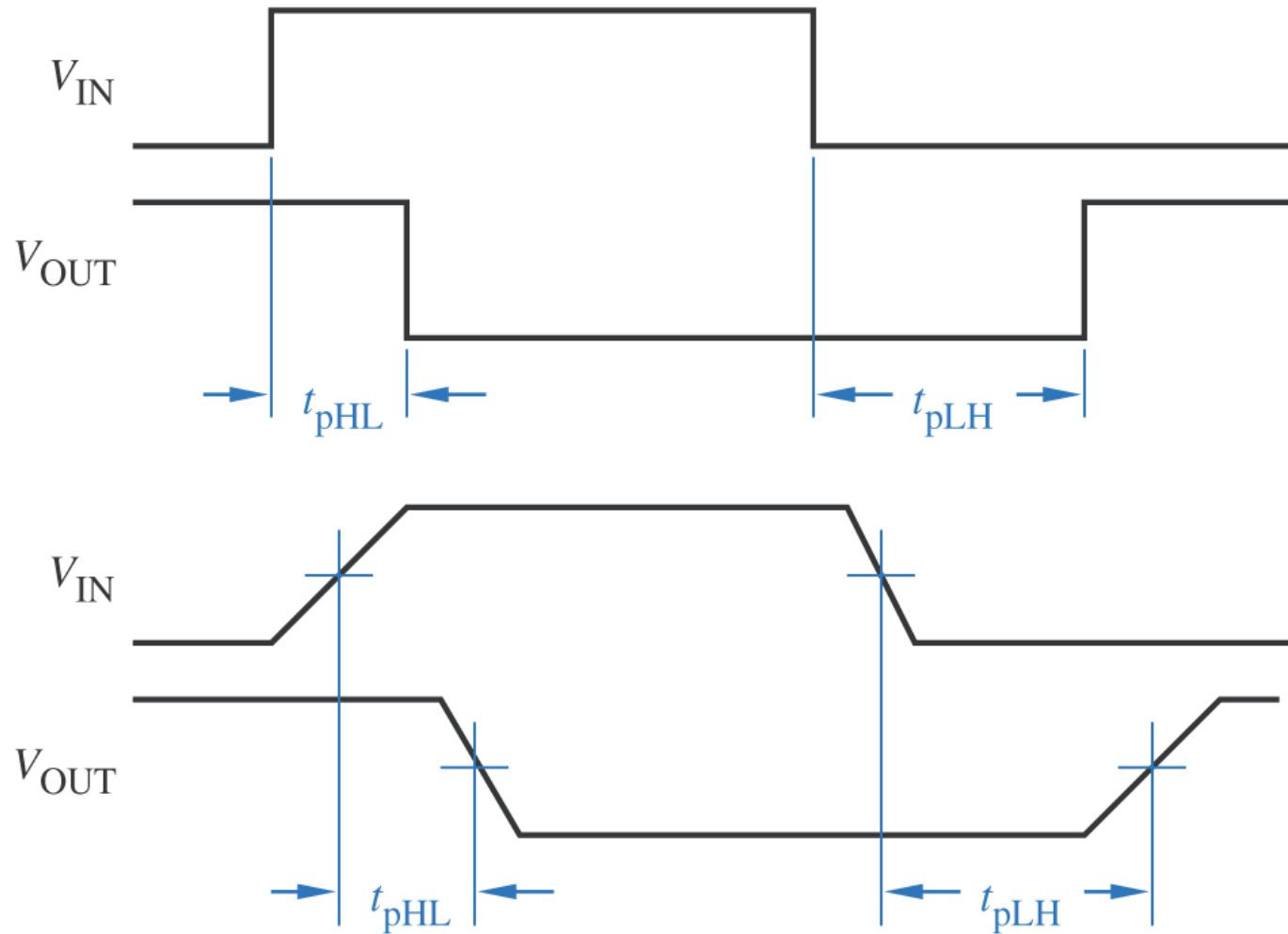
Electrical Characteristics

Sym.	Parameter	Test Conditions⁽¹⁾		Min.	Typ.⁽²⁾	Max.	Unit
V_{IH}	Input HIGH level	Guaranteed logic HIGH level		3.15	—	—	V
V_{IL}	Input LOW level	Guaranteed logic LOW level		—	—	1.35	V
I_{IH}	Input HIGH current	$V_{CC} = \text{Max.}, V_I = V_{CC}$		—	—	1	μA
I_{IL}	Input LOW current	$V_{CC} = \text{Max.}, V_I = 0 \text{ V}$		—	—	-1	μA
V_{IK}	Clamp diode voltage	$V_{CC} = \text{Min.}, I_N = -18 \text{ mA}$		—	-0.7	-1.2	V
I_{IOS}	Short-circuit current	$V_{CC} = \text{Max.}, ^{(3)} V_O = \text{GND}$		—	—	-35	mA
V_{OH}	Output HIGH voltage	$V_{CC} = \text{Min.}, V_{IN} = V_{IL}$	$I_{OH} = -20 \mu\text{A}$	4.4	4.499	—	V
			$I_{OH} = -4 \text{ mA}$	3.84	4.3	—	V
V_{OL}	Output LOW voltage	$V_{CC} = \text{Min.}, V_{IN} = V_{IH}$	$I_{OL} = 20 \mu\text{A}$	—	.001	0.1	V
			$I_{OL} = 4 \text{ mA}$		0.17	0.33	V

$$\text{NMH} = V_{OH\text{min}} - V_{IH\text{min}} = 4.4 \text{ V} - 3.15 \text{ V} = 1.25 \text{ V}$$

$$\text{NML} = V_{IL\text{max}} - V_{OL\text{max}} = 1.35 \text{ V} - 0.1 \text{ V} = 1.25 \text{ V}$$

Propagation Delay



Propagation Delay

SWITCHING CHARACTERISTICS OVER OPERATING RANGE, C _L = 50 pF							
Sym.	Parameter ⁽⁴⁾	Test Conditions		Min.	Typ.	Max.	Unit
t _{PD}	Propagation delay	A or B to Y		—	9	19	ns
C _I	Input capacitance	V _{IN} = 0 V		—	3	10	pF
C _{pd}	Power dissipation capacitance per gate	No load		—	22	—	pF

Summary

- ◆ NAND and NOR Gates
- ◆ DeMorgan's Laws
- ◆ SOP to NAND-NAND
- ◆ MOSFETs
- ◆ CMOS Logic Gates
 - Inverter, NAND, NOR
- ◆ Electrical Characteristics
 - Noise Margin
 - Propagation Delay