

Multiplexers, Decoders, and PLDs

ELEC 311

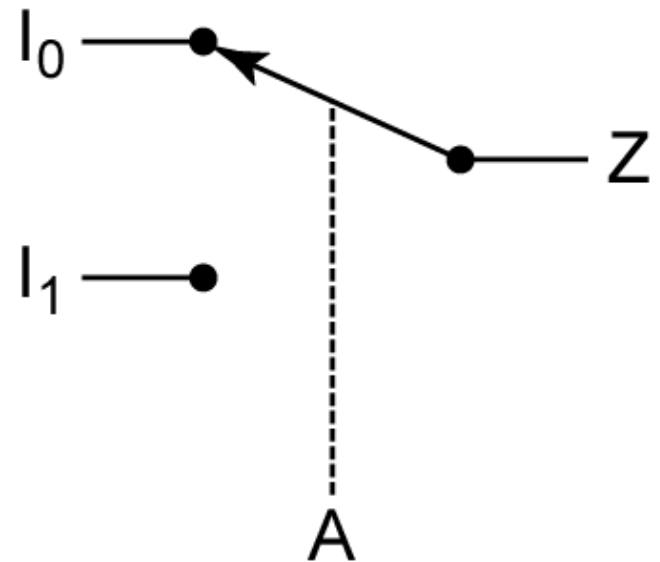
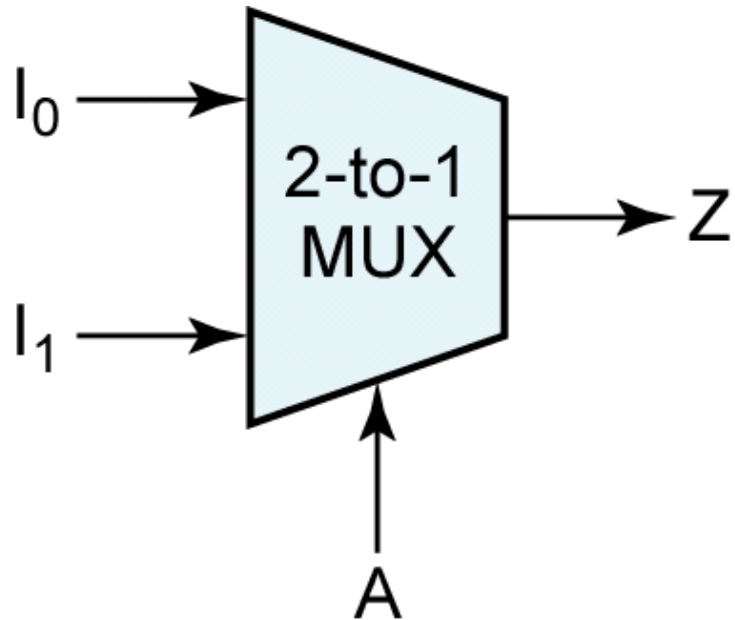
Digital Logic and Circuits

Dr. Ron Hayne

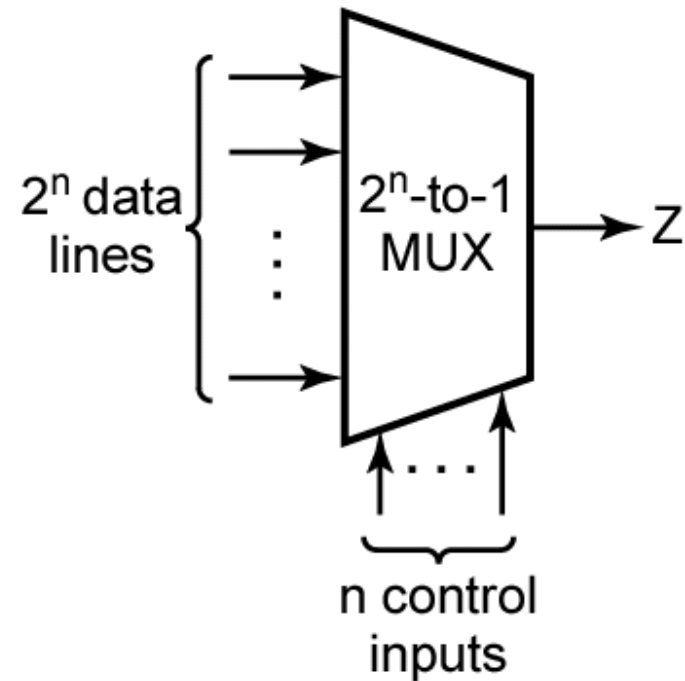
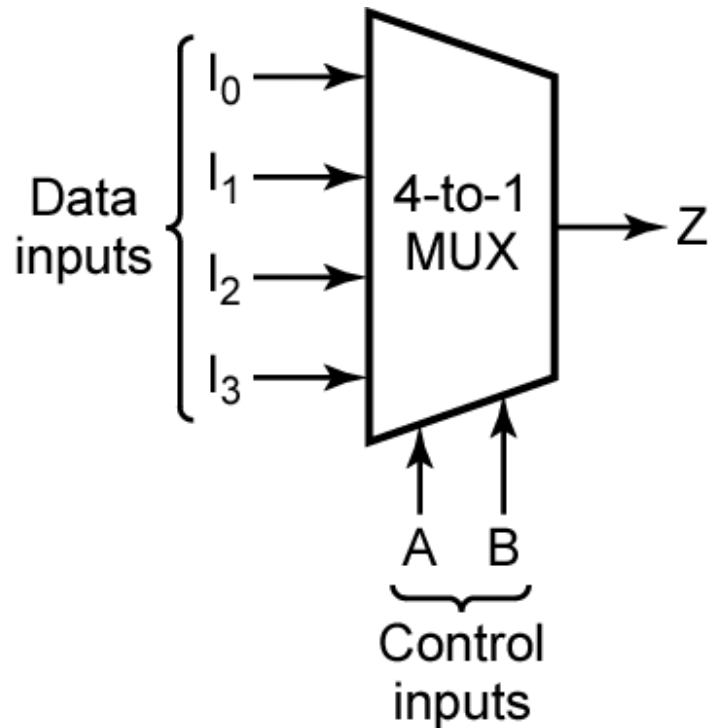
Images Courtesy of Cengage Learning



Multiplexers



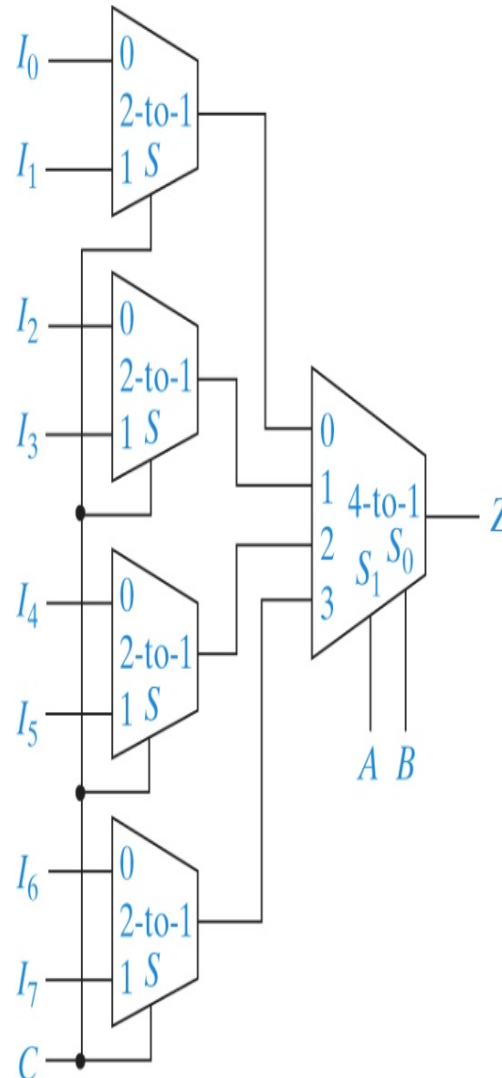
Larger Multiplexers



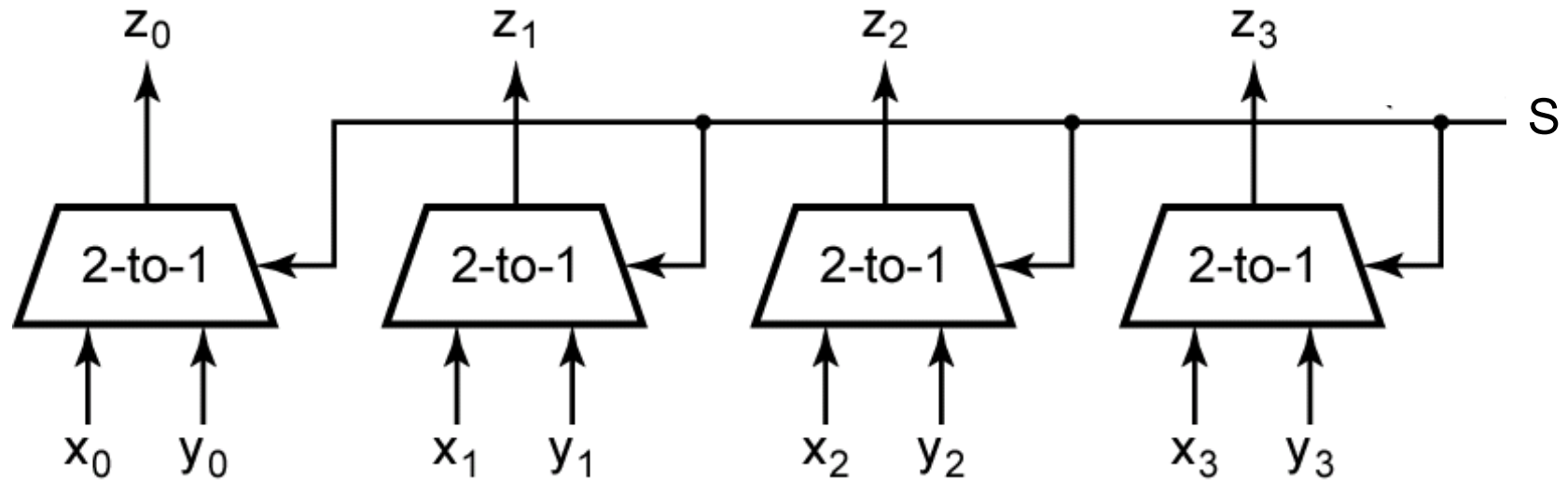
Cascading Multiplexers

FIGURE 9-5
Component MUXs
of Figure 9-4

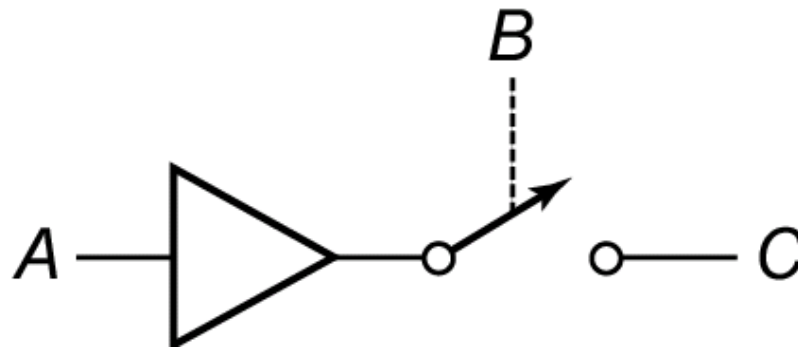
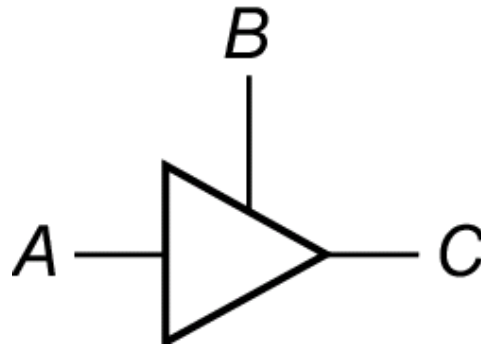
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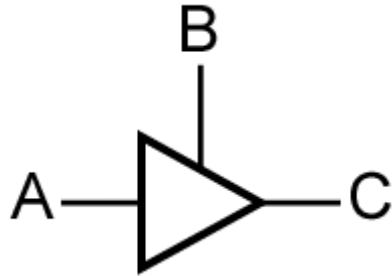
Multiple-Bit Data



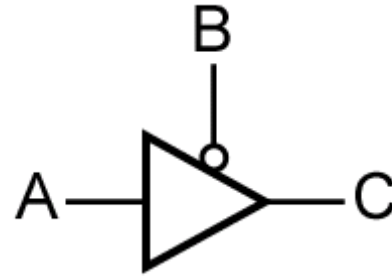
Tri-State Buffer



Tri-State Buffers

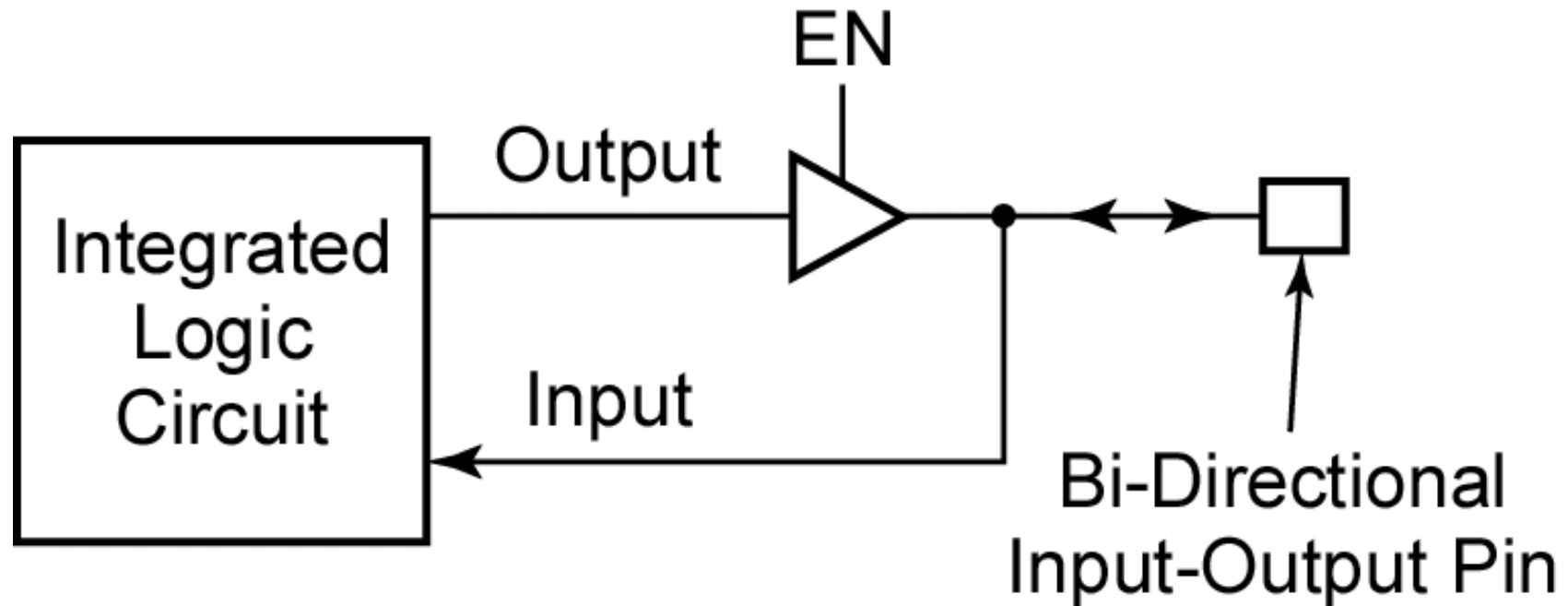


B	A	C
0	0	Z
0	1	Z
1	0	0
1	1	1

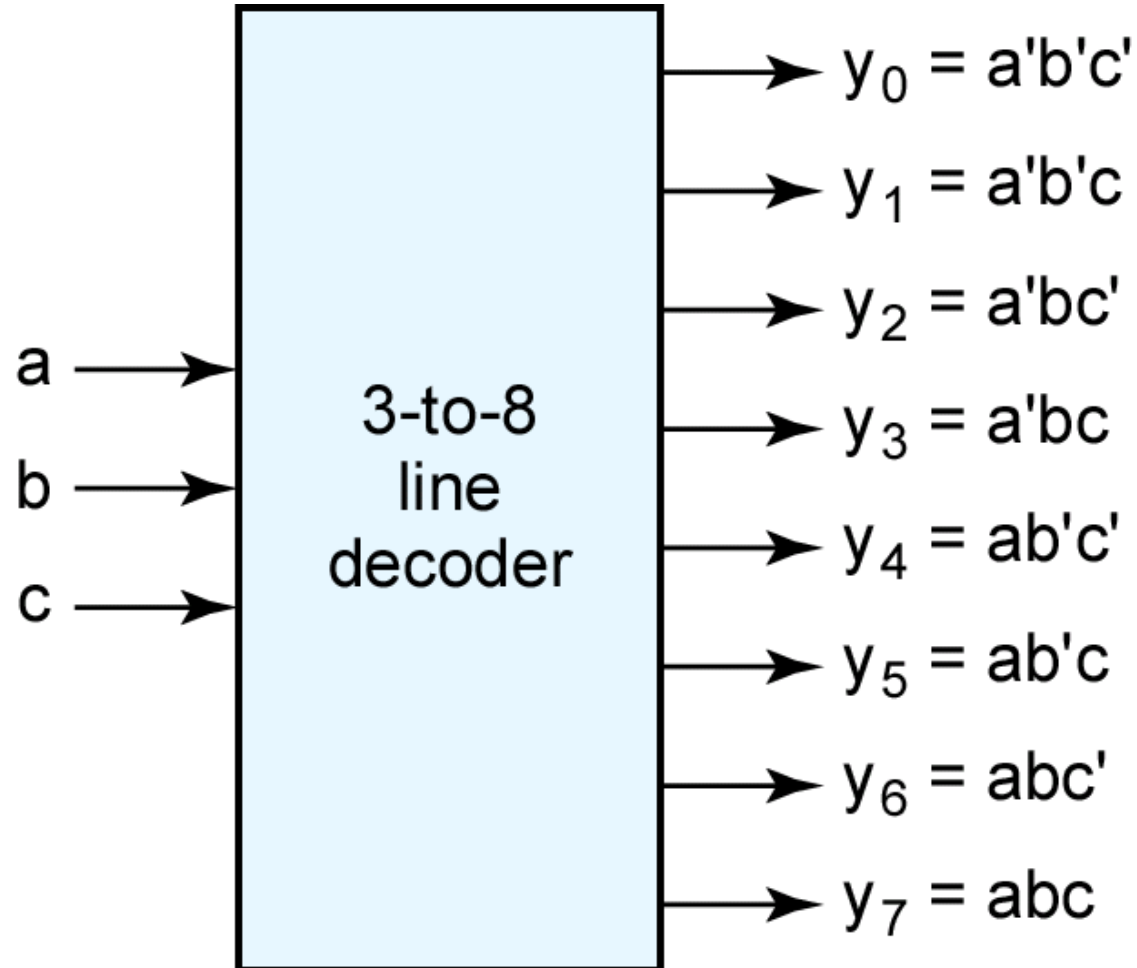


B	A	C
0	0	0
0	1	1
1	0	Z
1	1	Z

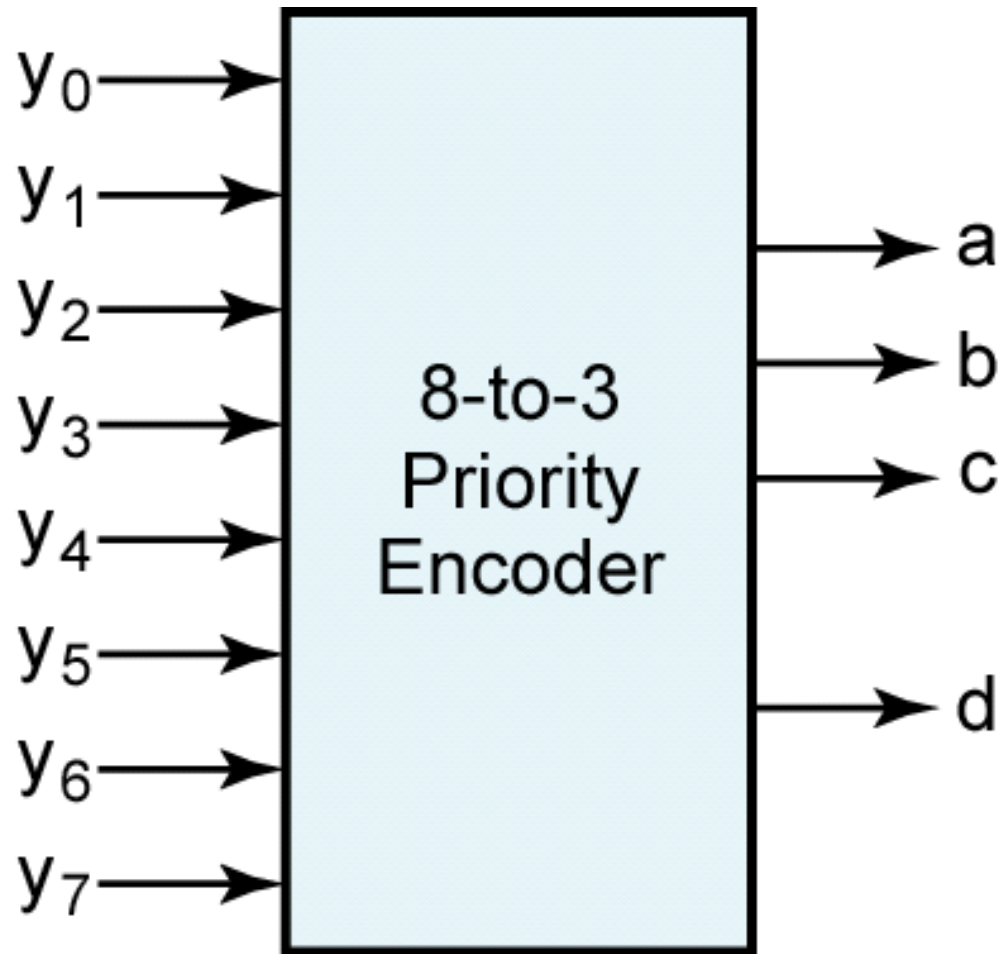
Bi-Directional I/O Pins



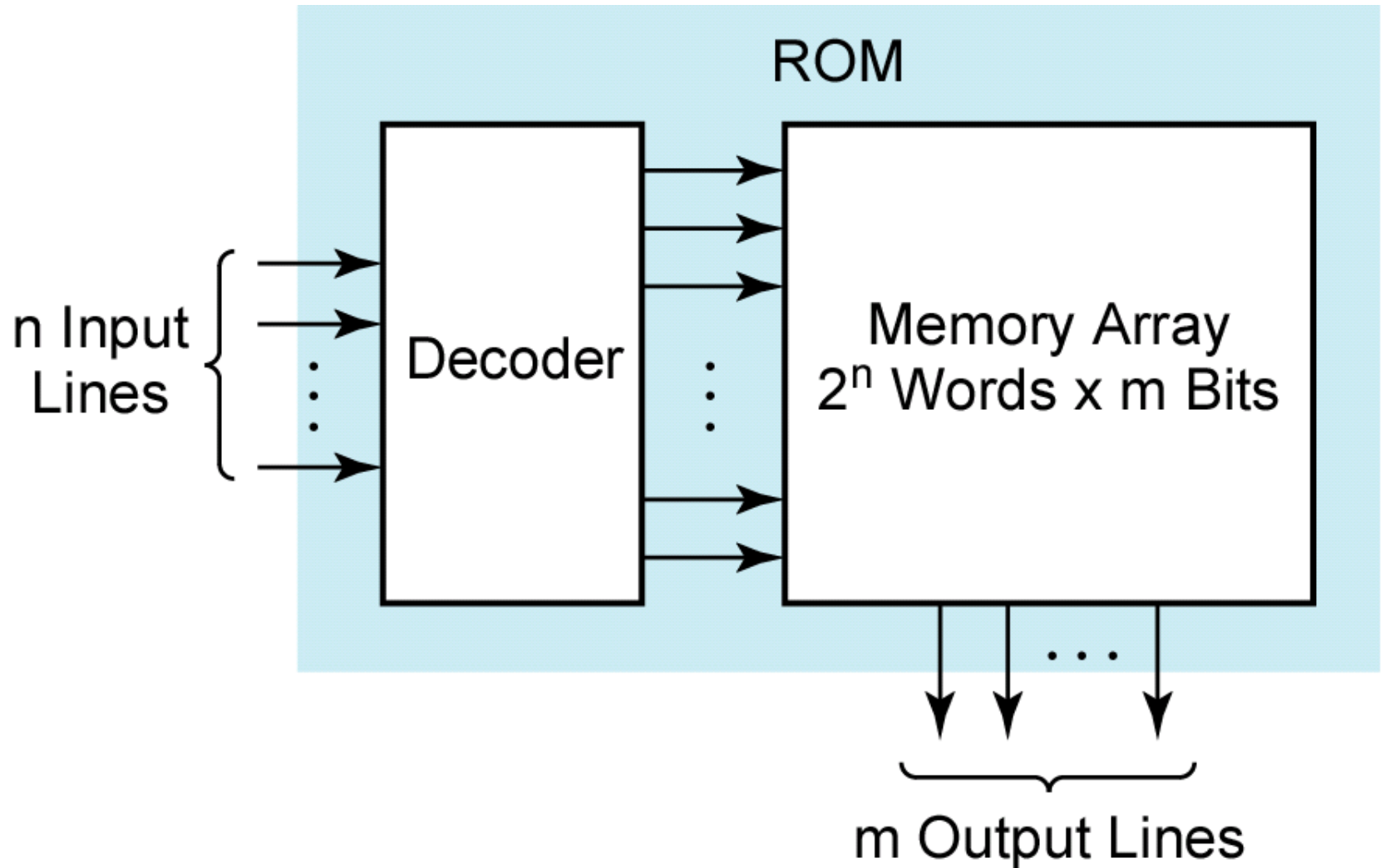
Decoders



Priority Encoders



Read-Only Memory



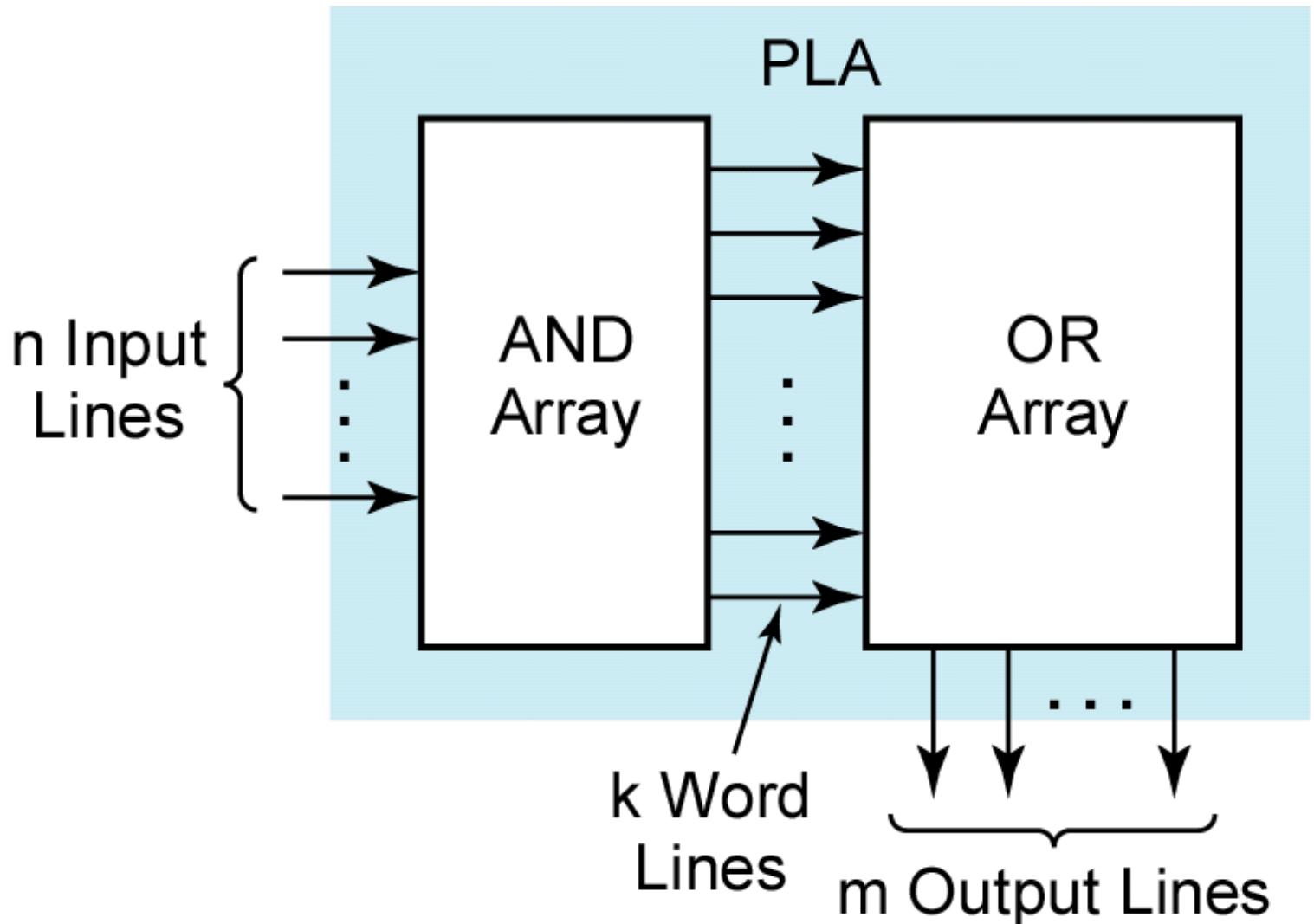
Hex to ASCII Converter

Input				Hex Digit	ASCII Code for Hex Digit						
W	X	Y	Z		A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀
0	0	0	0	0	0	1	1	0	0	0	0
0	0	0	1	1	0	1	1	0	0	0	1
0	0	1	0	2	0	1	1	0	0	1	0
0	0	1	1	3	0	1	1	0	0	1	1
0	1	0	0	4	0	1	1	0	1	0	0
0	1	0	1	5	0	1	1	0	1	0	1
0	1	1	0	6	0	1	1	0	1	1	0
0	1	1	1	7	0	1	1	0	1	1	1
1	0	0	0	8	0	1	1	1	0	0	0
1	0	0	1	9	0	1	1	1	0	0	1
1	0	1	0	A	1	0	0	0	0	0	1
1	0	1	1	B	1	0	0	0	0	1	0
1	1	0	0	C	1	0	0	0	0	1	1
1	1	0	1	D	1	0	0	0	1	0	0
1	1	1	0	E	1	0	0	0	1	0	1
1	1	1	1	F	1	0	0	0	1	1	0

Programmable Logic Devices

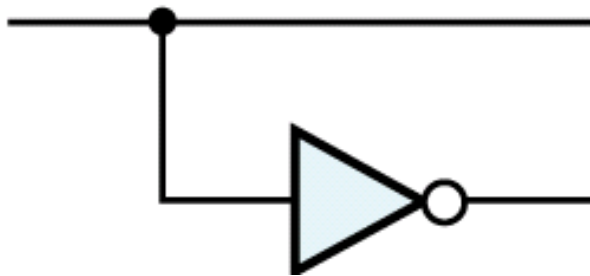
- ◆ Programmable Logic Array (PLA)
- ◆ Programmable Array Logic (PAL)
- ◆ Complex Programmable Logic Device (CPLD)
- ◆ Field Programmable Gate Array (FPGA)

Programmable Logic Arrays

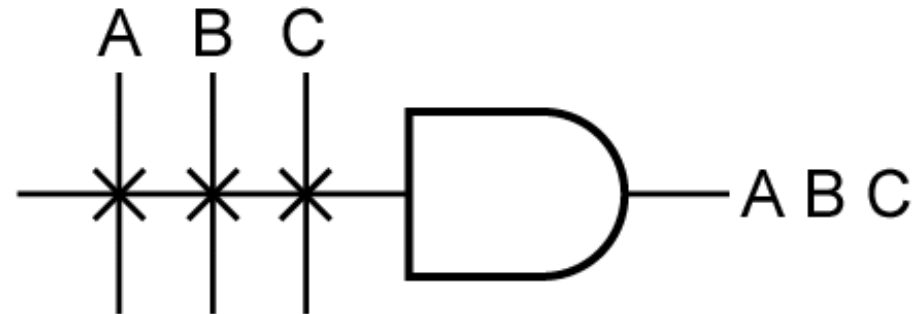
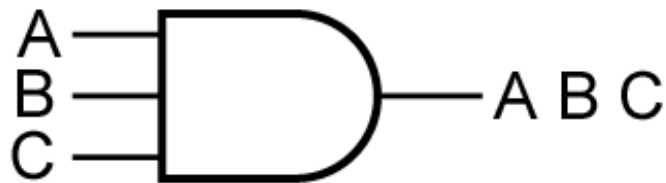
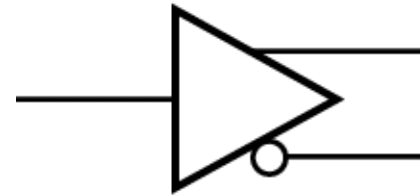


Programmable Array Logic

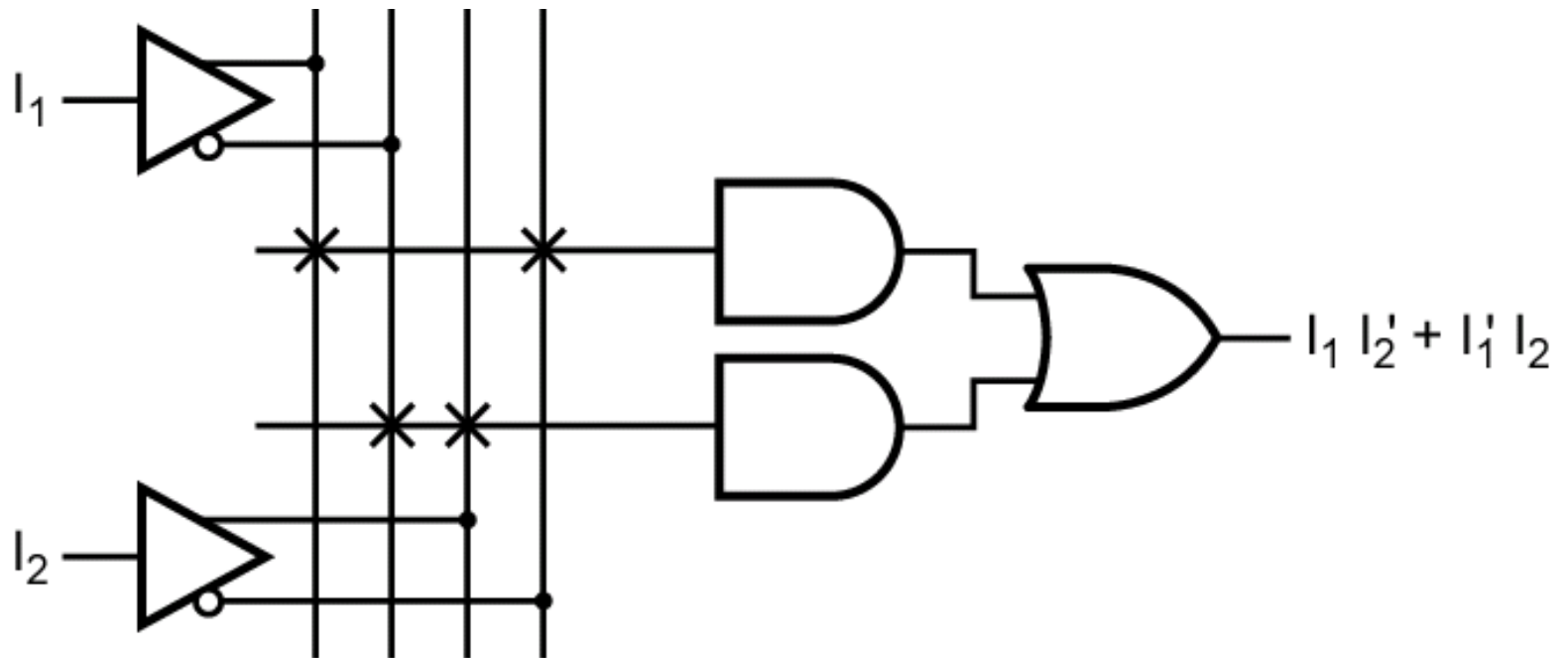
◆ Logic Symbol



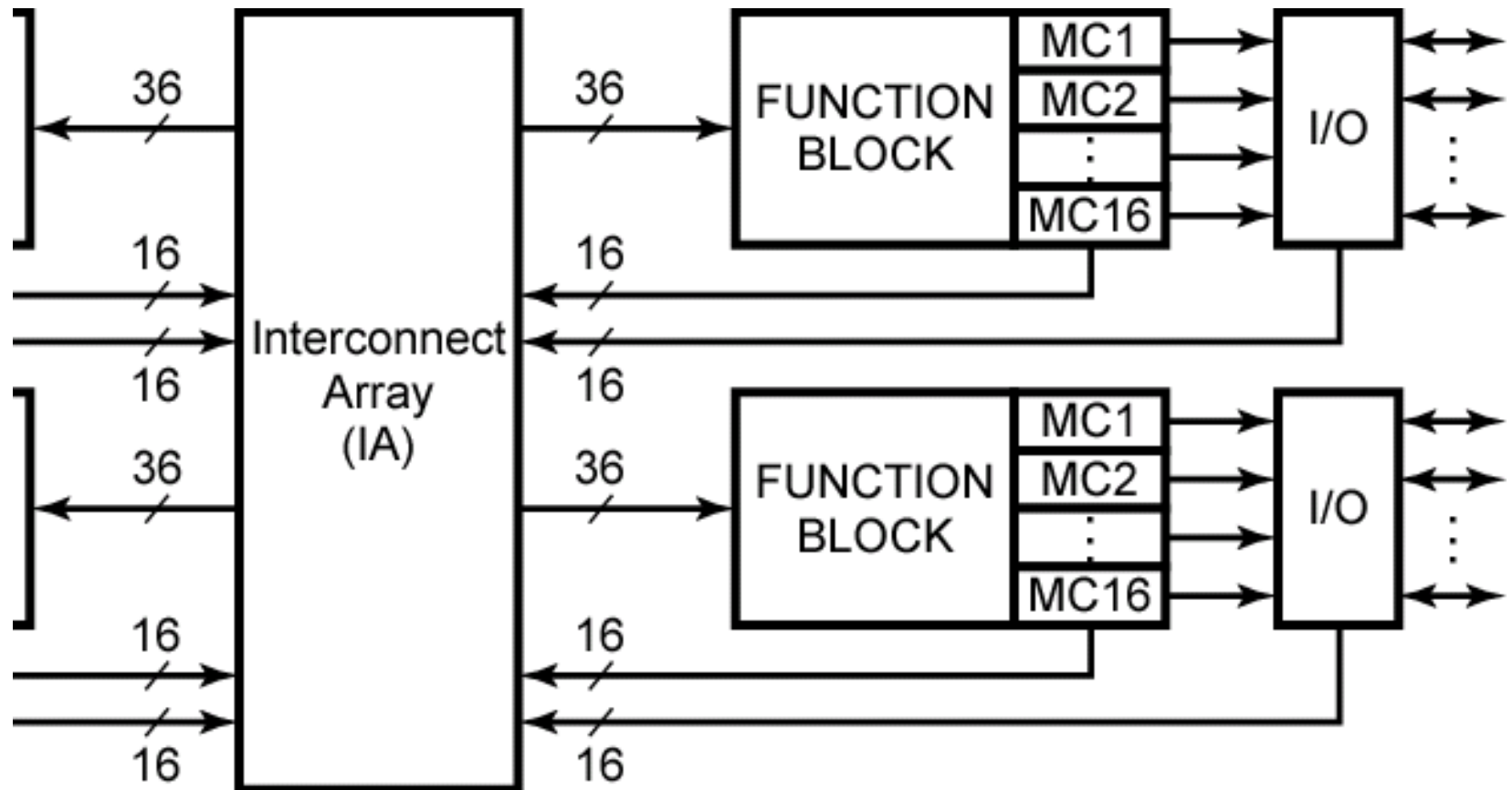
◆ PAL Symbol



Programmed PAL

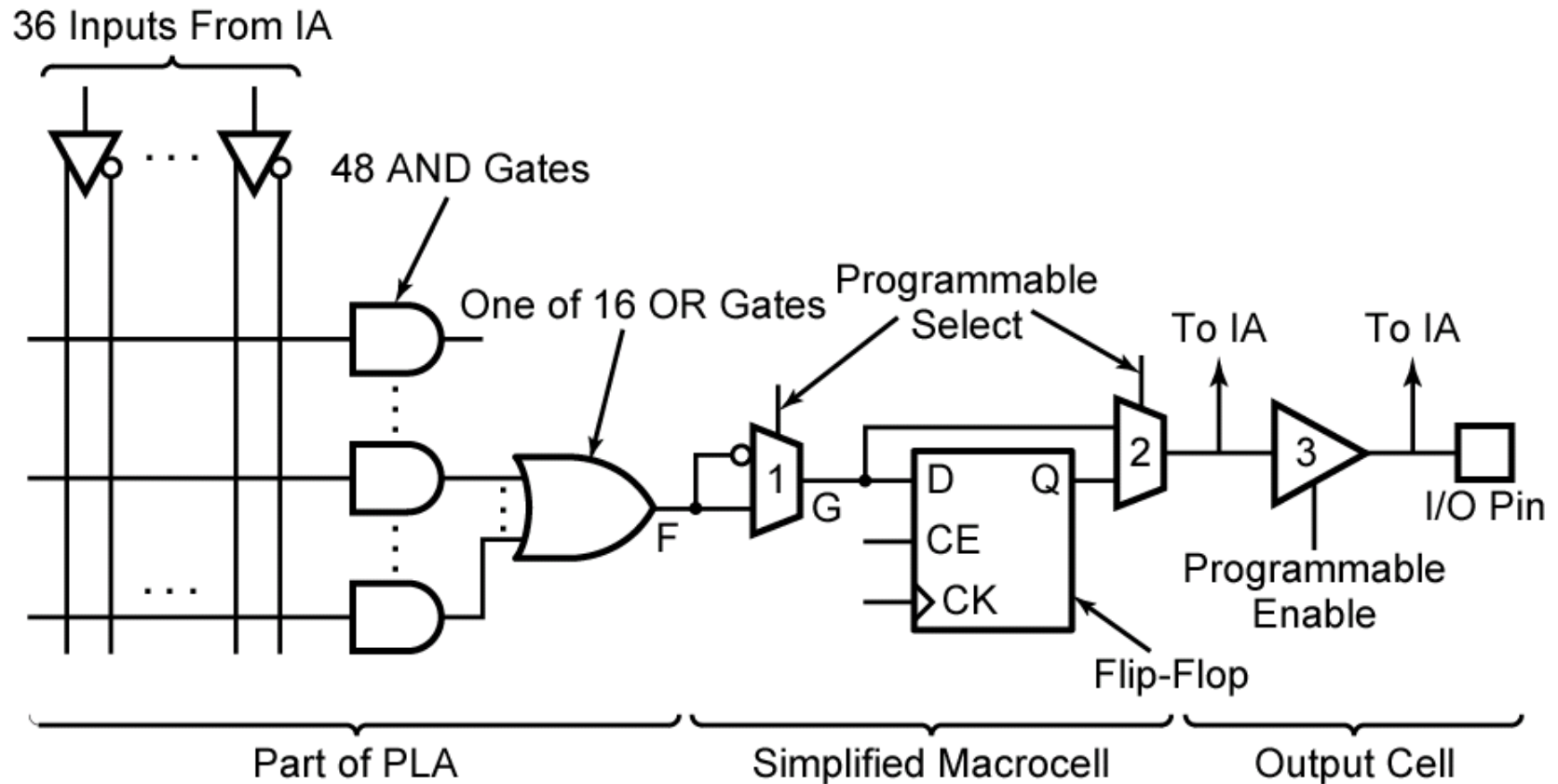


Complex PLD

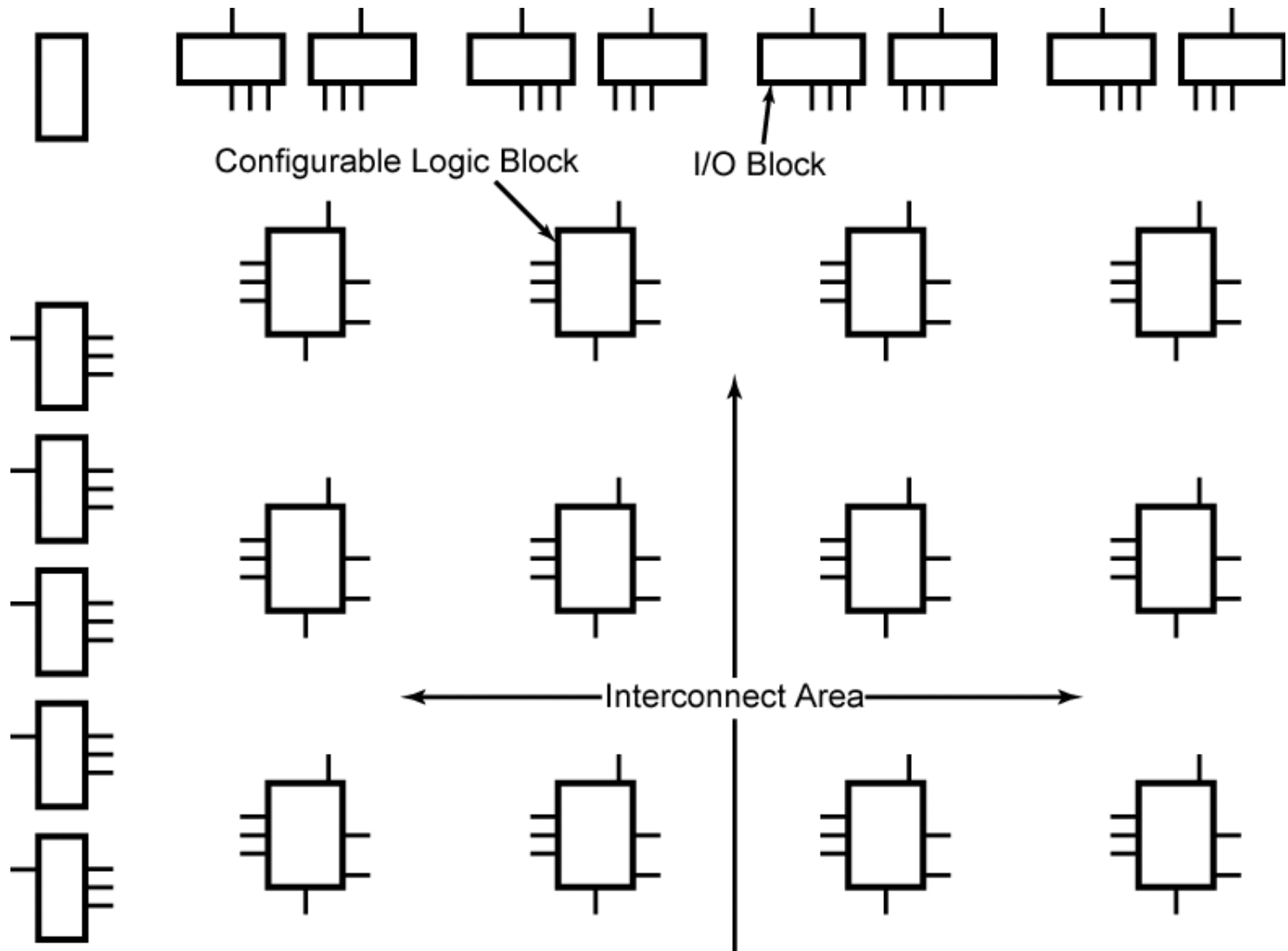


Architecture of Xilinx XCR3064XL CPLD (© Xilinx, Inc.)

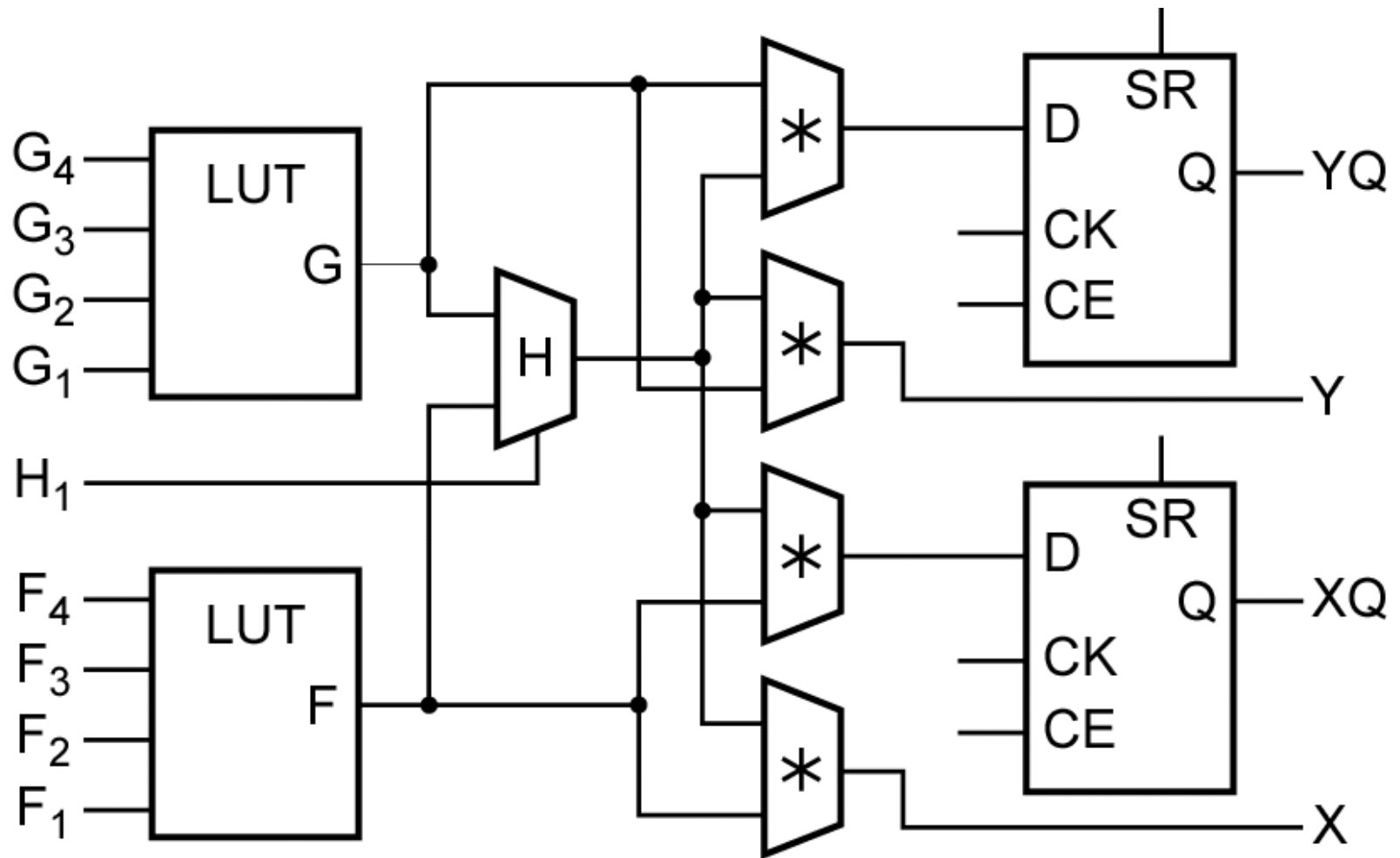
Xilinx CPLD



Field Programmable Gate Array



Configurable Logic Block



* = Programmable MUX

Summary

- ◆ Multiplexers
- ◆ Three-State Buffers
- ◆ Decoders
- ◆ Priority Encoders
- ◆ Read-Only Memory
- ◆ Complex Programmable Logic Devices
- ◆ Field Programmable Gate Arrays