1. Design a shift register, which uses a counter to rotate a variable number of bits. When St = 1, D is loaded into the 8-bit register and N is loaded into the 3-bit down counter. The register then rotates left until the counter reaches 0, when Done is signaled.

a) Illustrate the results for the following sample data:
   - D = 11011011, N = 4
   - D = 00111100, N = 6

b) Draw a block diagram of the variable shift register circuit and define any necessary control signals.

c) Draw the state graph for the control circuit.

d) Write a complete VHDL model (entity and behavioral architecture) for the variable shift register. Use two processes: one to generate the control signals and one to update the registers based on those signals.

e) Simulate the circuit using the sample data from part a) above.