1. Design a 4-bit shift register with the following specifications:
   - A falling-edge triggered clock (CLK)
   - An active-low clear (ClrN)
   - An active-low load signal (LdN) with parallel data input (D)
   - A function select signal (S)
     - When S = 0, the register shifts right with sign extension (copy the sign bit)
     - When S = 1, the register shifts right with a serial data input (SI)

a) Draw the logic symbol and a truth table for the 4-bit shift register.
b) Write a complete VHDL model (entity and behavioral architecture) for the 4-bit shift register.
c) Draw a schematic diagram using two 4-bit shift registers to create an 8-bit shift register.
d) Write a complete VHDL model (entity and structural architecture) for the 8-bit shift register.
e) Simulate the 8-bit shift register for the following test sequence:
   - Load 11101110, shift right 4 times with S = 0
   - Clear
   - Load 01110111, shift right 2 times with S = 1 and SI = 0