Multiplexers, Decoders, and PLDs

ELEC 311

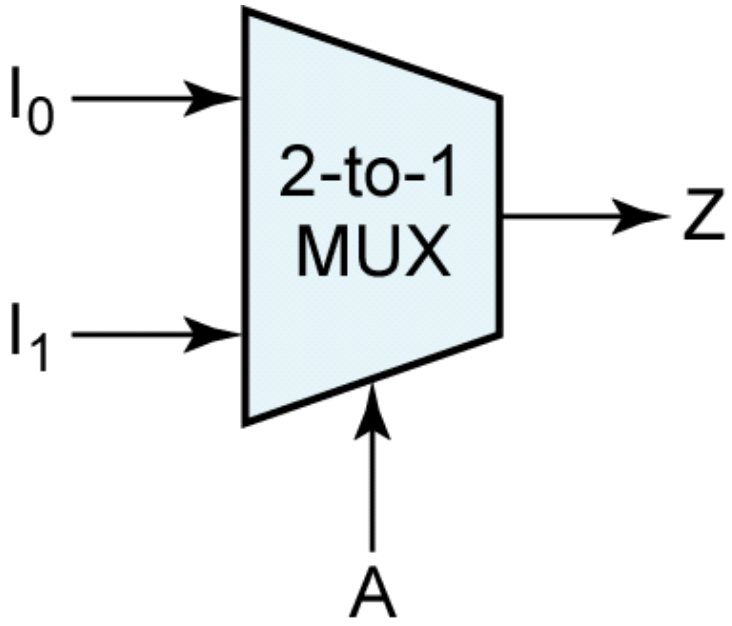
Digital Logic and Circuits

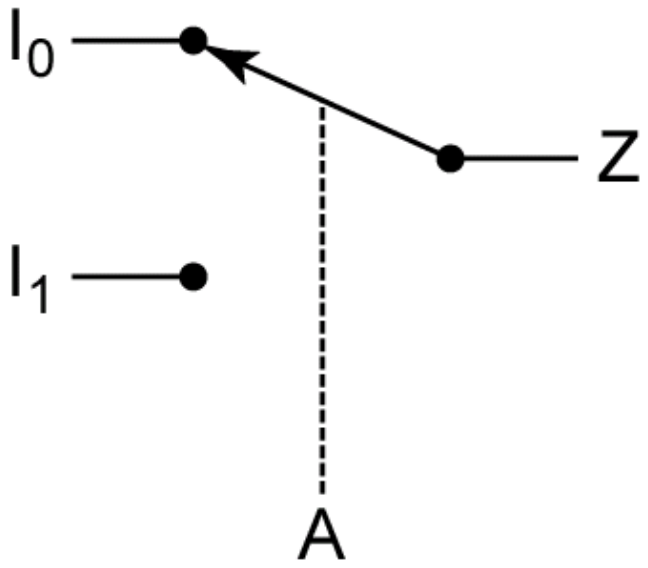
Dr. Ron Hayne

Images Courtesy of Cengage Learning

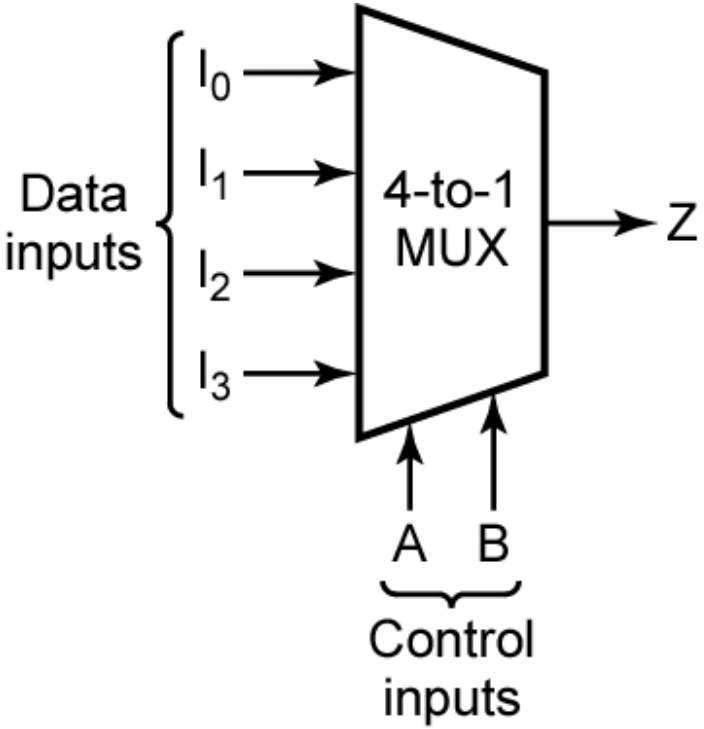
THE CITADEL
DEPARTMENT OF ELECTRICAL & COMPUTER ENGINEERING

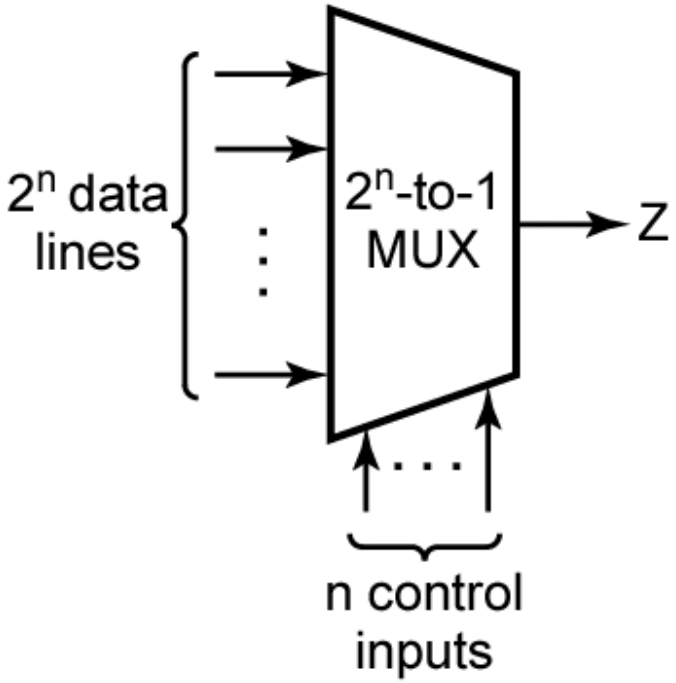
Multiplexers





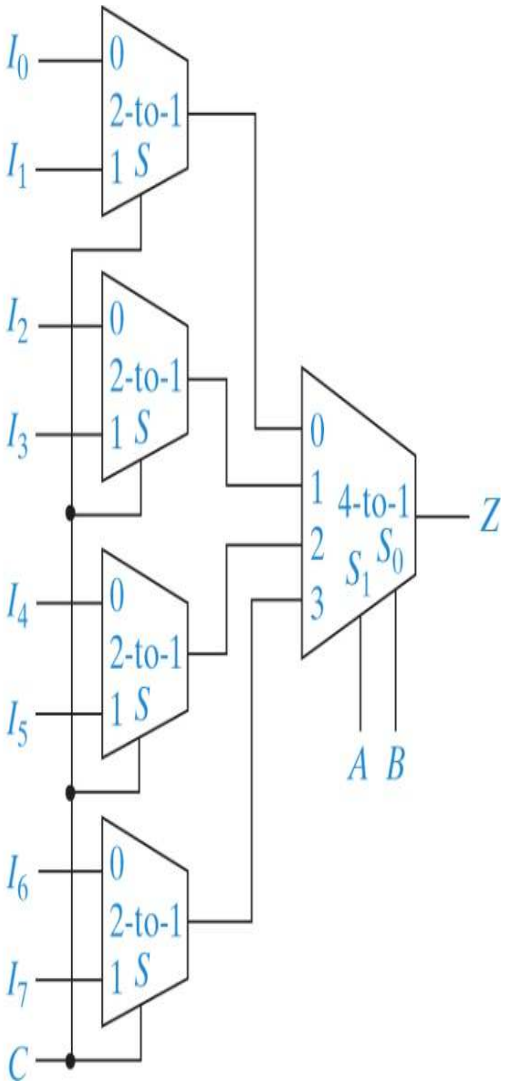
Larger Multiplexers



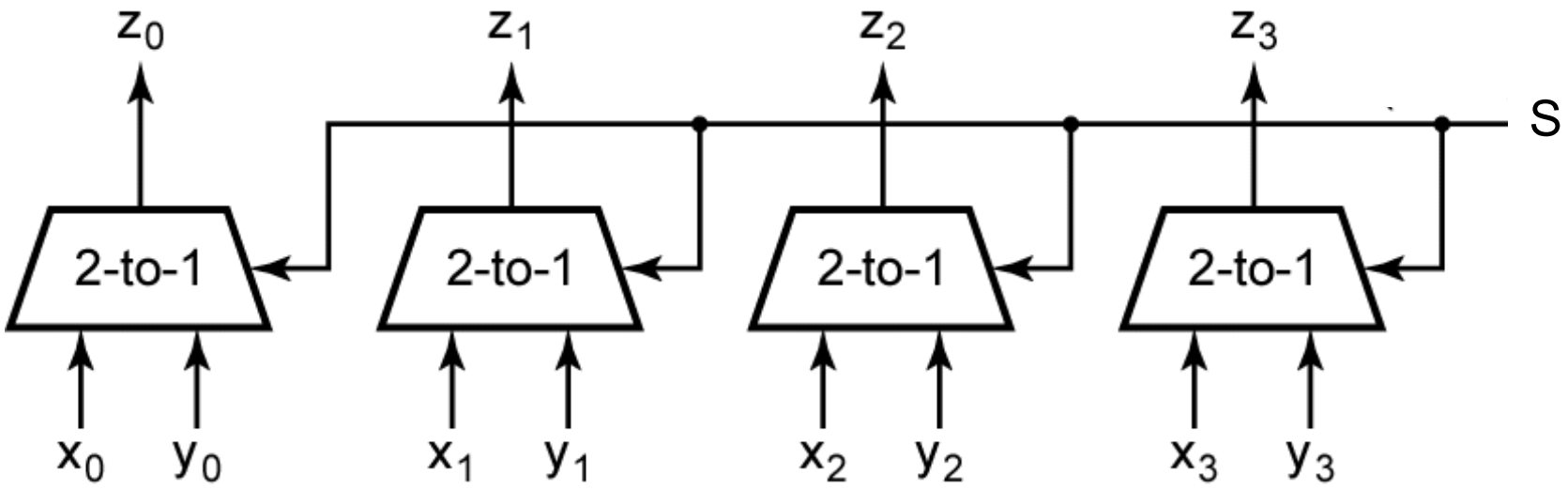


Cascading Multiplexers

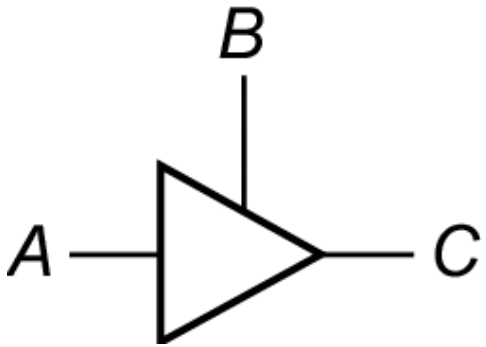
FIGURE 9-5
Component MUXs of Figure 9-4

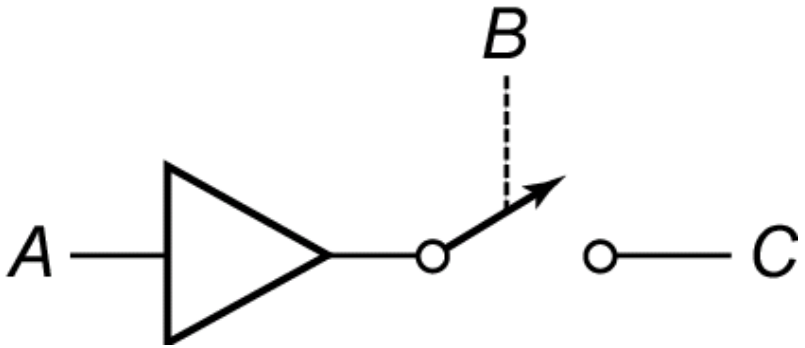


Multiple-Bit Data

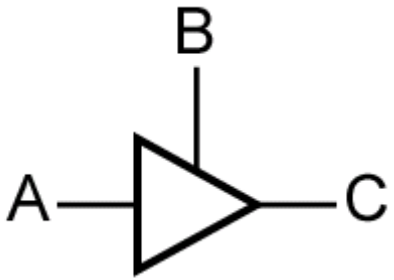


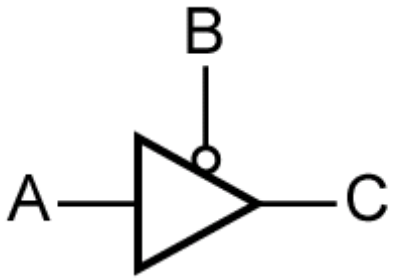
Tri-State Buffer





Tri-State Buffers

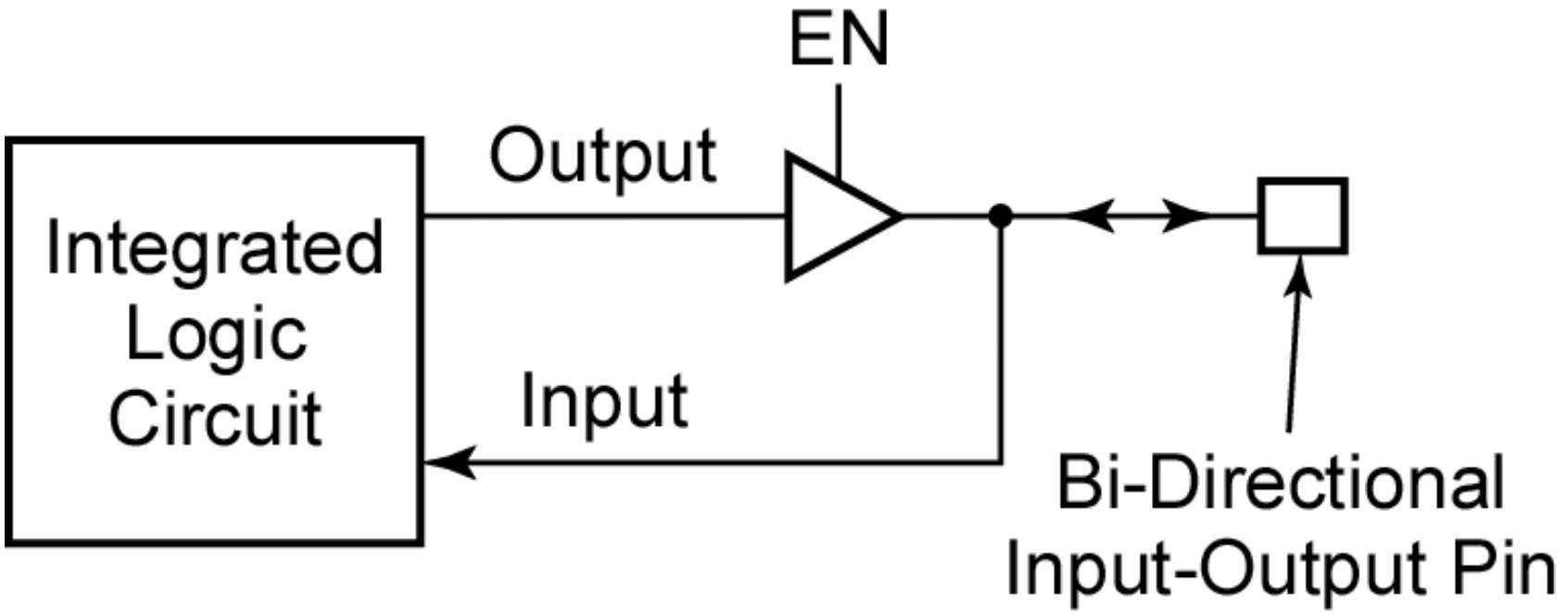




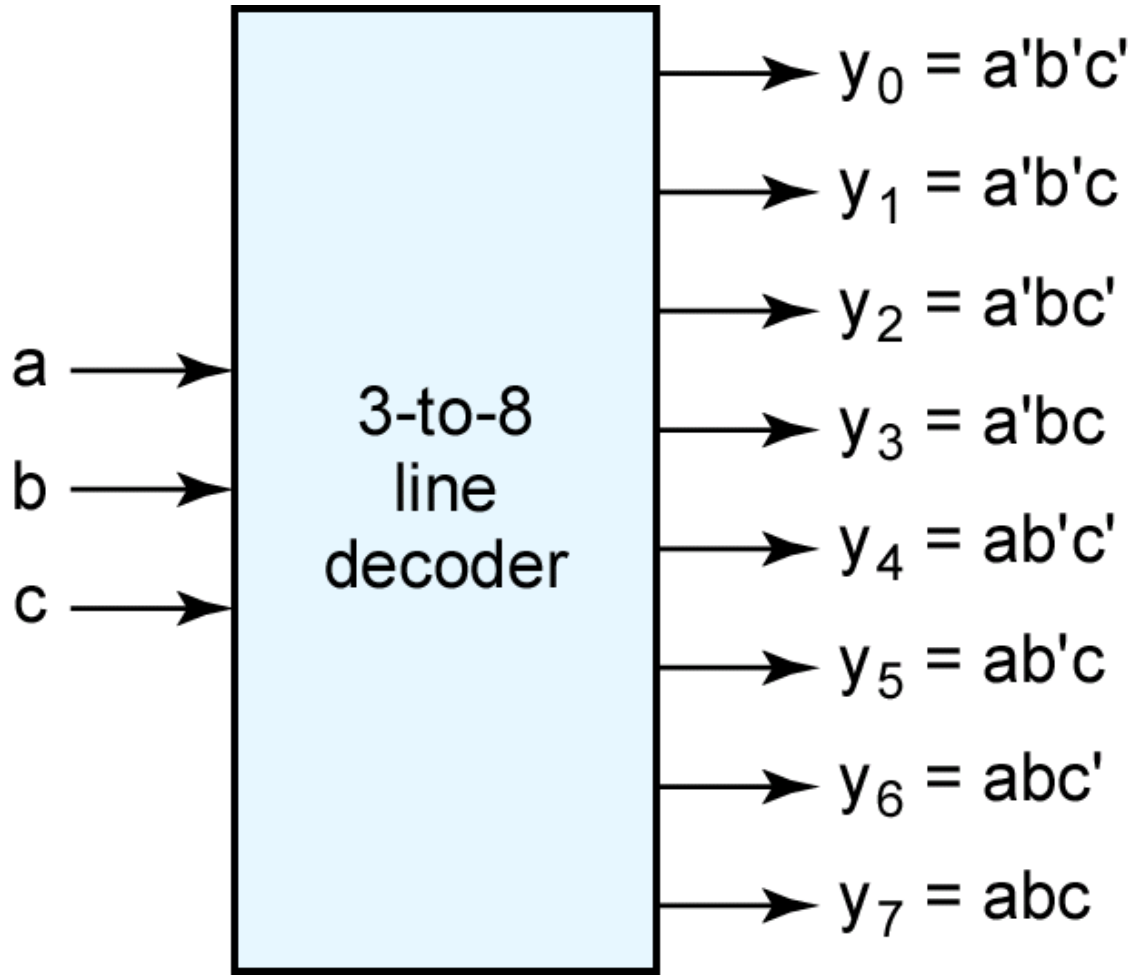
B	A	C
0	0	Z
0	1	Z
1	0	0
1	1	1

B	A	C
0	0	0
0	1	1
1	0	Z
1	1	Z

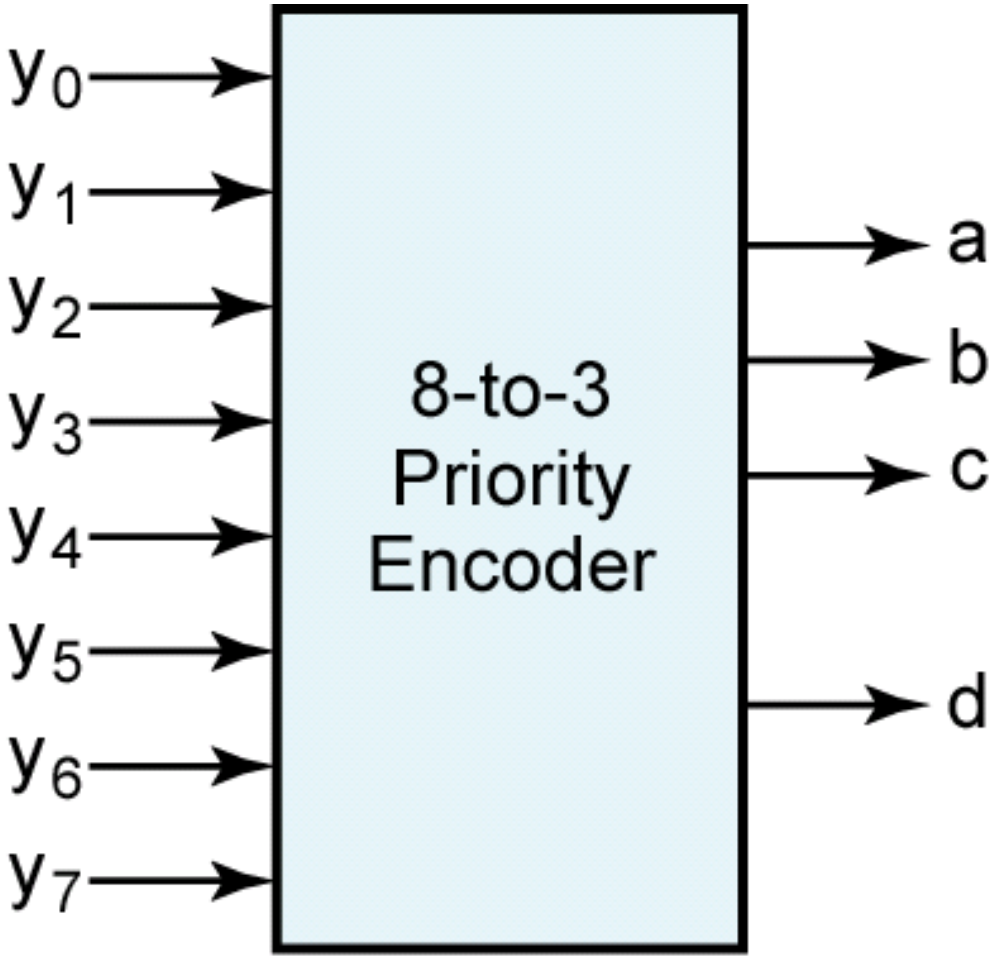
Bi-Directional I/O Pins



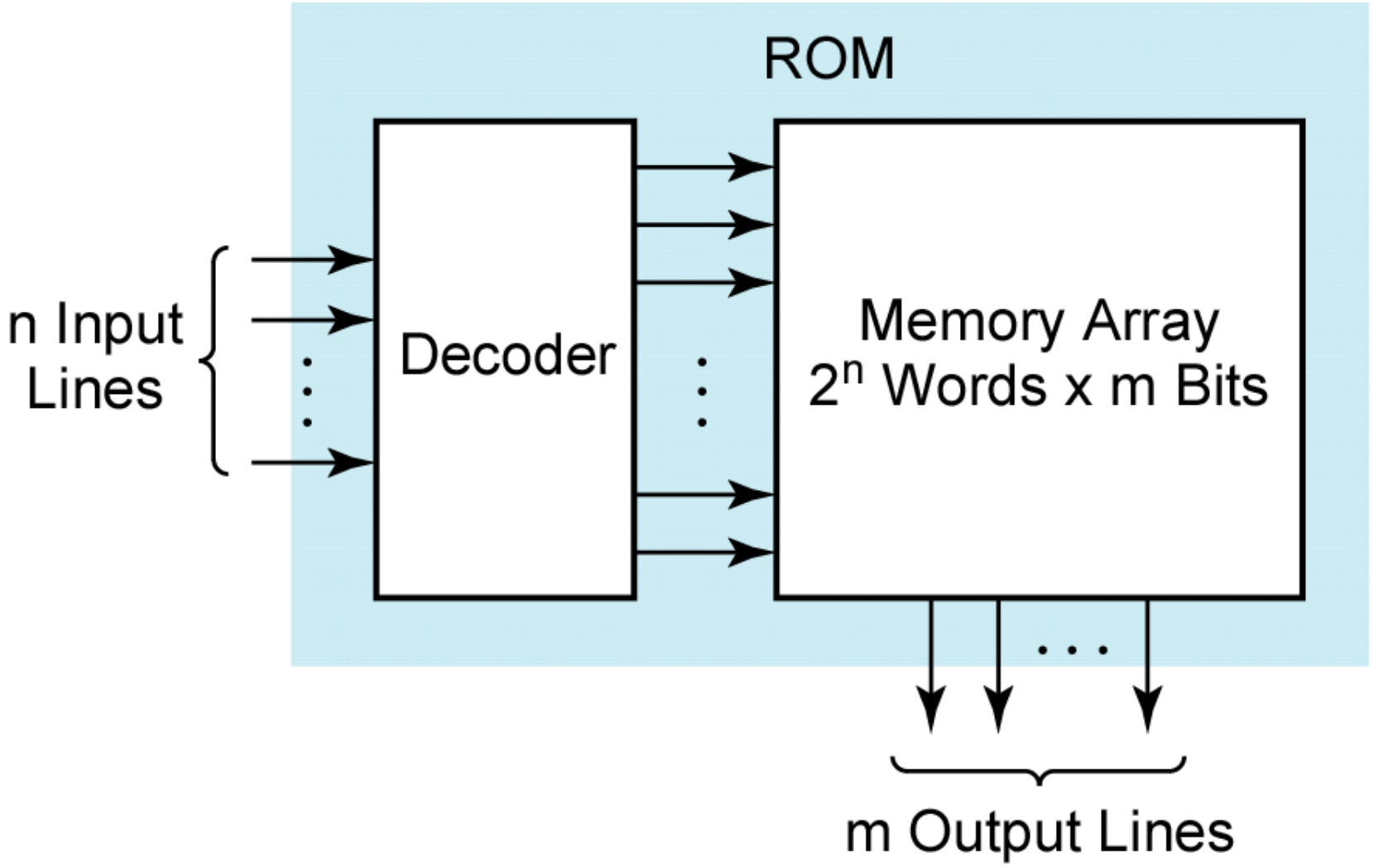
Decoders


a
b
c
3-to-8
line
decoder
y0 = a'b'c'
y1 = a'b'c
y2 = a'bc'
y3 = a'bc
y4 = ab'c'
y5 = ab'c
y6 = abc'
y7 = abc

Priority Encoders



Read-Only Memory



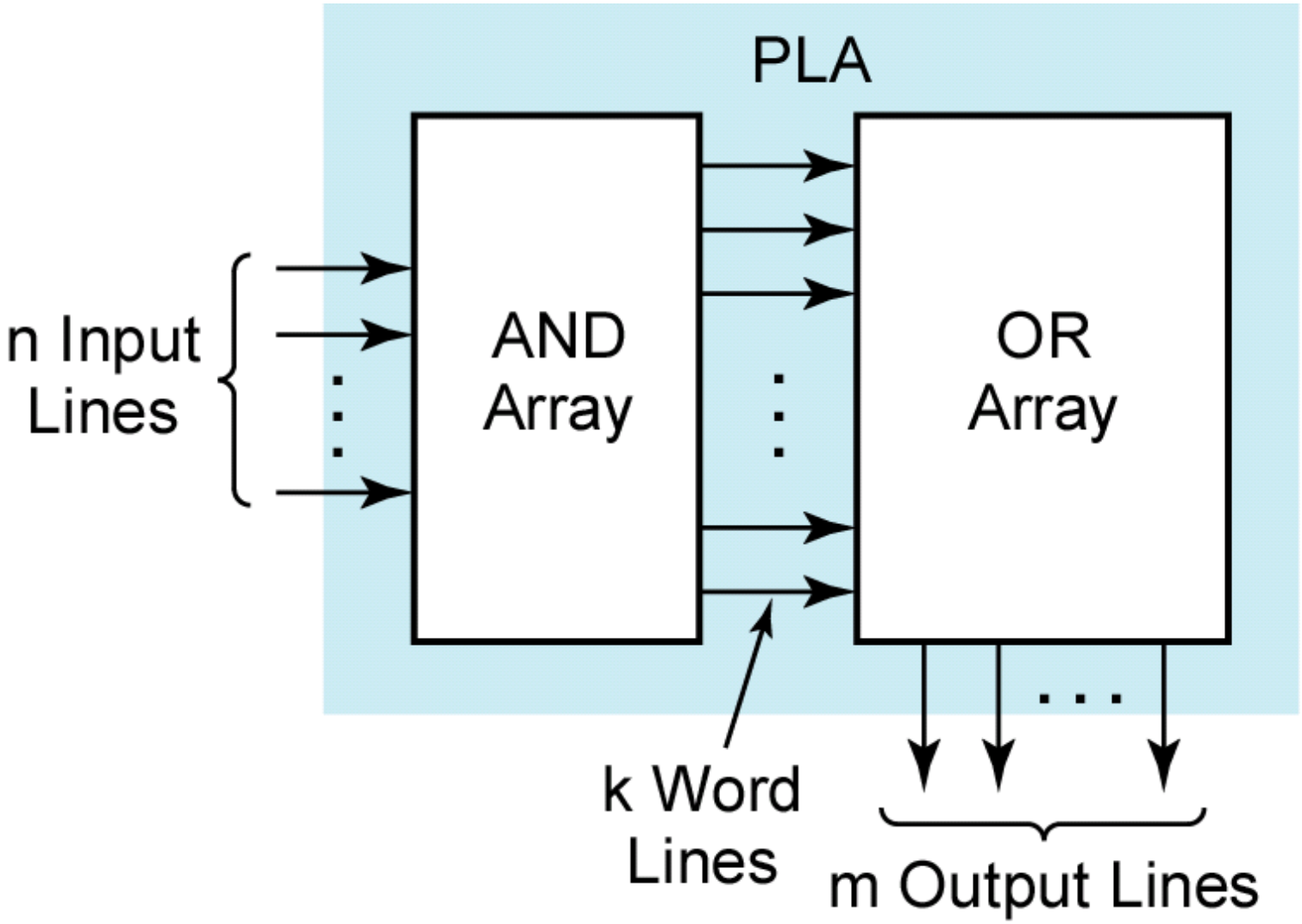
Hex to ASCII Converter

Input				Hex	ASCII Code for Hex Digit						
W	*X*	*Y*	*Z*	Digit	A_6	A_5	A_4	A_3	A_2	A_1	A_0
0	0	0	0	0	0	1	1	0	0	0	0
0	0	0	1	1	0	1	1	0	0	0	1
0	0	1	0	2	0	1	1	0	0	1	0
0	0	1	1	3	0	1	1	0	0	1	1
0	1	0	0	4	0	1	1	0	1	0	0
0	1	0	1	5	0	1	1	0	1	0	1
0	1	1	0	6	0	1	1	0	1	1	0
0	1	1	1	7	0	1	1	0	1	1	1
1	0	0	0	8	0	1	1	1	0	0	0
1	0	0	1	9	0	1	1	1	0	0	1
1	0	1	0	A	1	0	0	0	0	0	1
1	0	1	1	B	1	0	0	0	0	1	0
1	1	0	0	C	1	0	0	0	0	1	1
1	1	0	1	D	1	0	0	0	1	0	0
1	1	1	0	E	1	0	0	0	1	0	1
1	1	1	1	F	1	0	0	0	1	1	0

Programmable Logic Devices

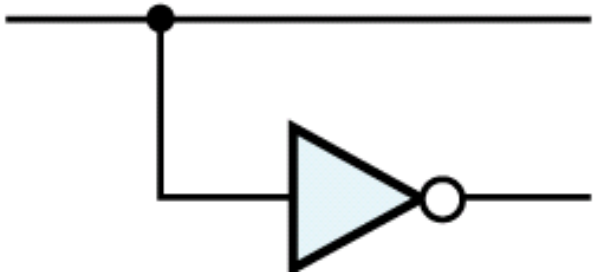
- Programmable Logic Array (PLA)
- Programmable Array Logic (PAL)
- Complex Programmable Logic Device (CPLD)
- Field Programmable Gate Array (FPGA)

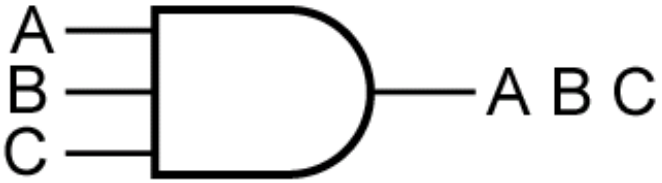
Programmable Logic Arrays



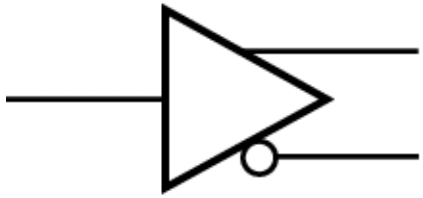
Programmable Array Logic

- Logic Symbol

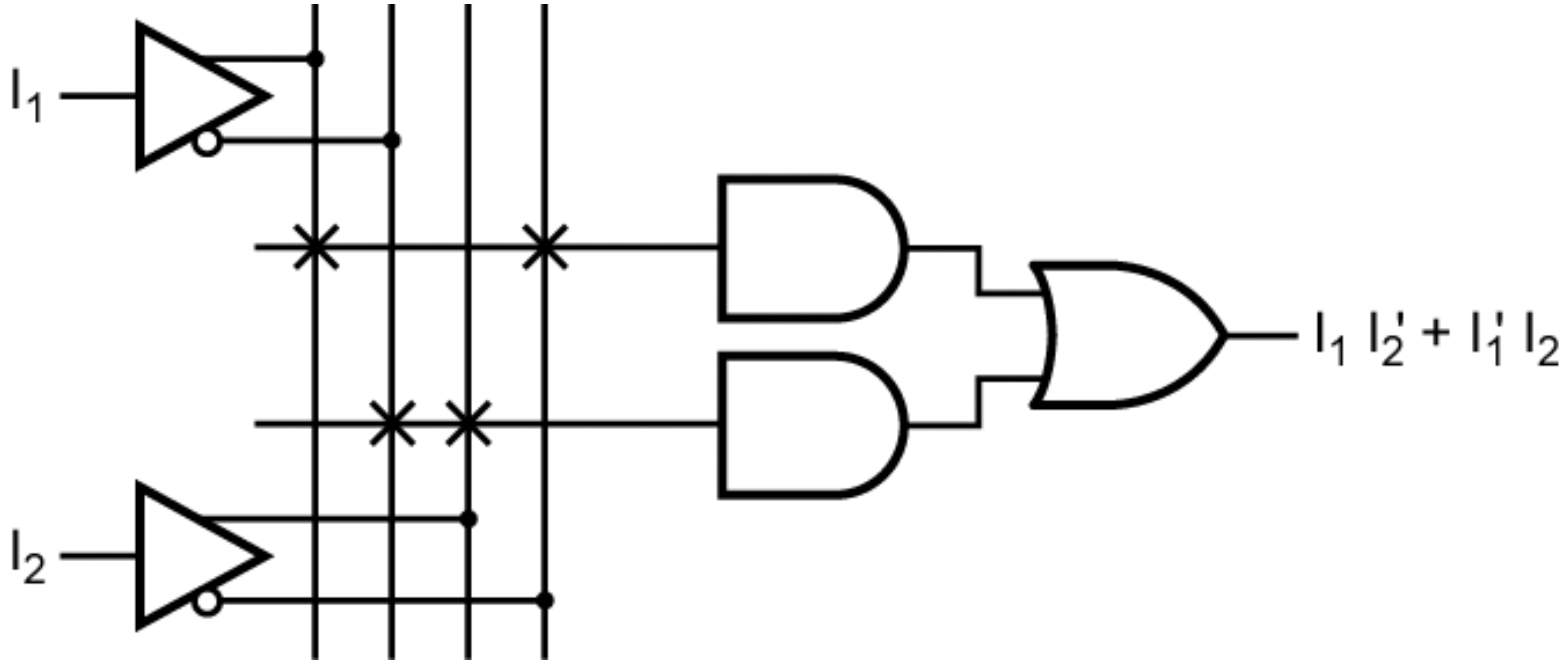




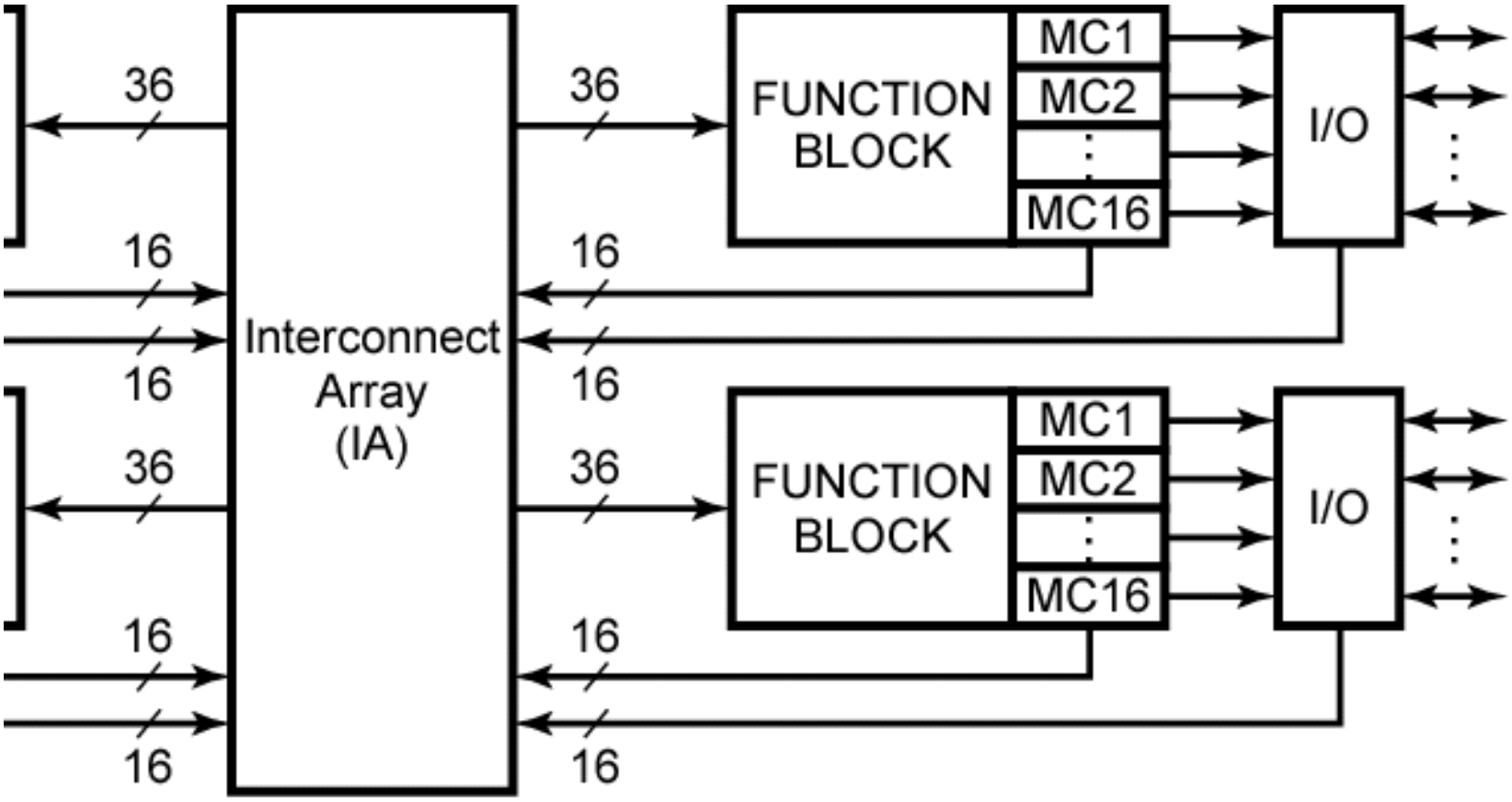
- PAL Symbol



Programmed PAL

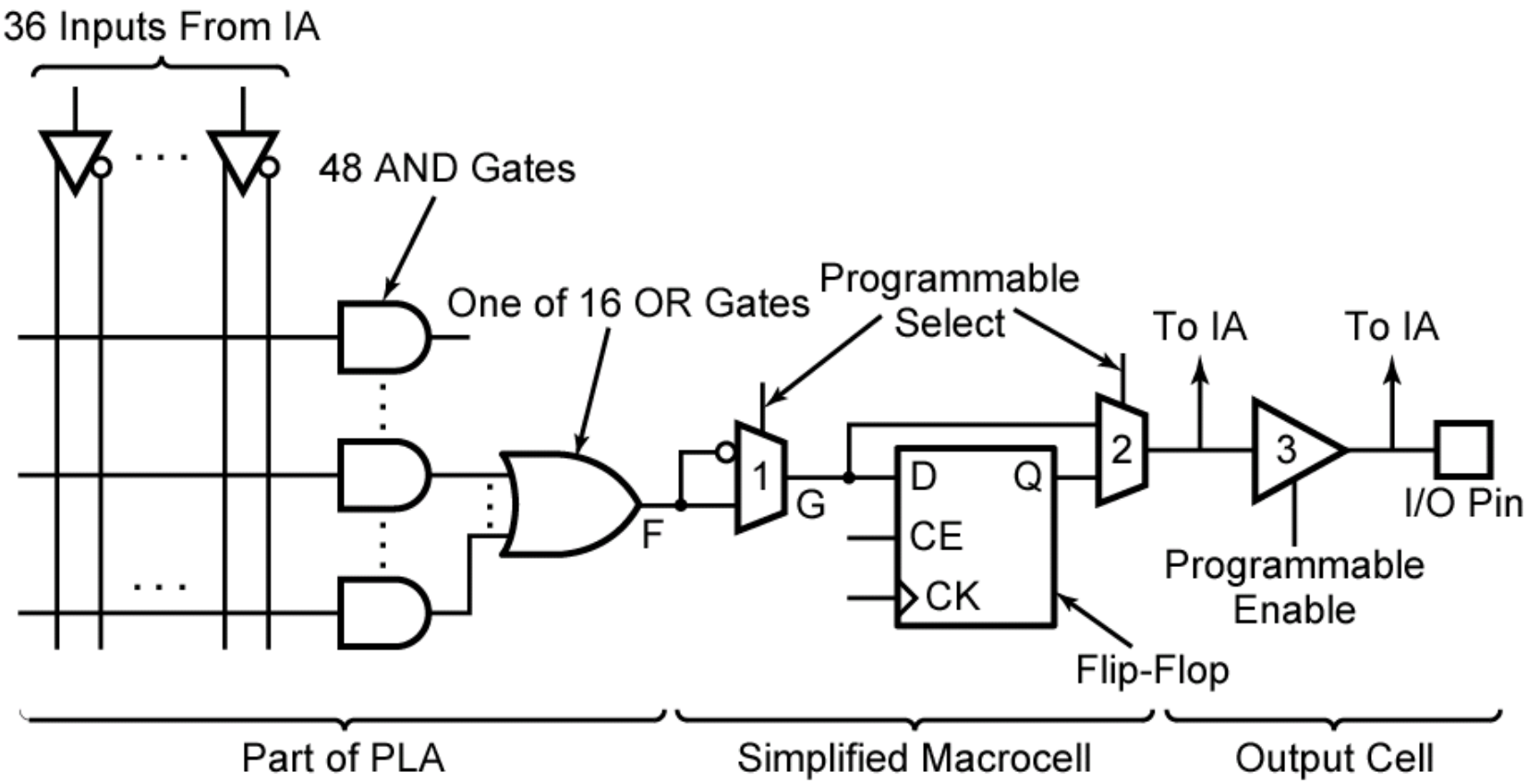


Complex PLD

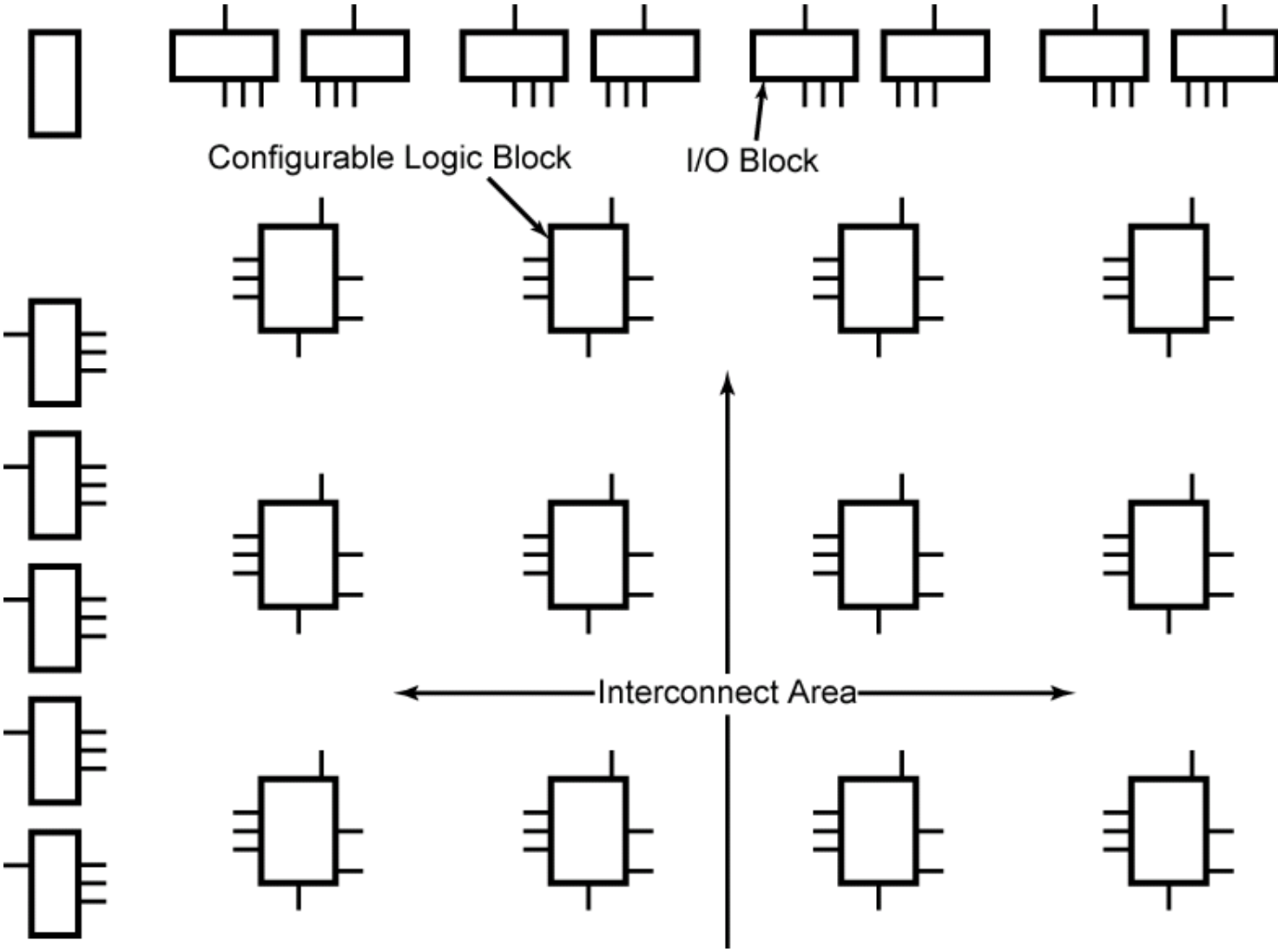


Architecture of Xilinx XCR3064XL CPLD (© Xilinx, Inc.)

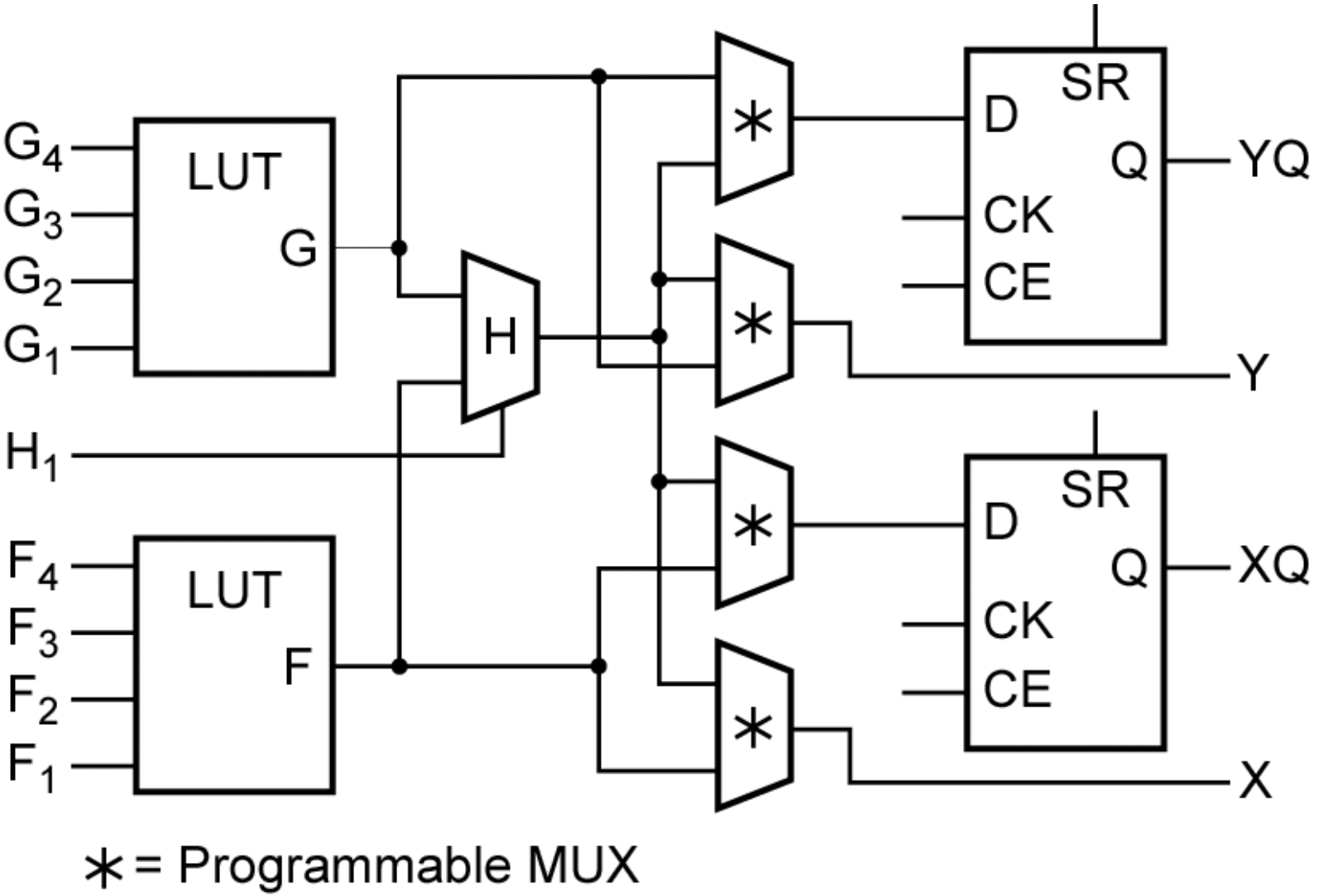
Xilinx CPLD


36 Inputs From IA
48 AND Gates
One of 16 OR Gates
Programmable
Select
To IA
To IA
1
G
F
D
Q
CE
CK
2
3
I/O Pin
Programmable
Enable
Flip-Flop
Part of PLA
Simplified Macrocell
Output Cell

Field Programmable Gate Array



Configurable Logic Block



Summary

- Multiplexers
- Three-State Buffers
- Decoders
- Priority Encoders
- Read-Only Memory
- Complex Programmable Logic Devices
- Field Programmable Gate Arrays