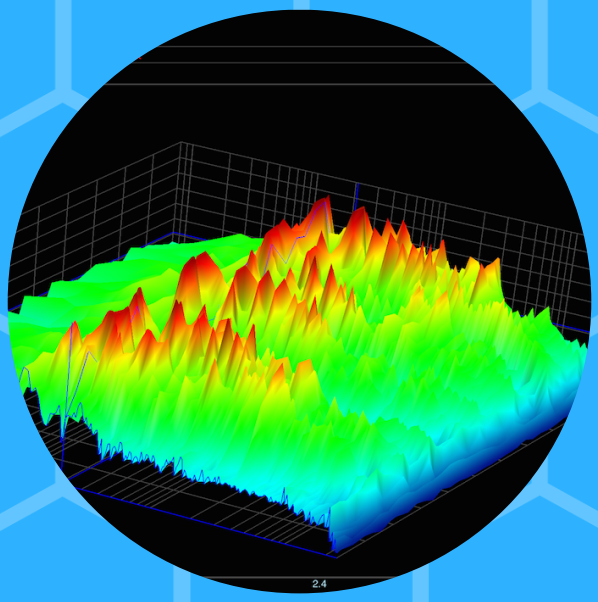
MASTER 1 SESI - UPMC - May 2017

UE PROJET SESI

Design of a multi standard Delta Sigma digital analog converter



Charles PAULAS VICTOR

Tutors :
Hassan Aboushady
Islam Eshra

UPMC
SORBONNE UNIVERSITÉS

Contents

1. Abstract

4G is currently settling down around the world, meanwhile 5G is still in development and will replace 4G in a few years. One of the requirements for this new generation of mobile networks is the ability to provide reliable infrastructure for massive communication between many devices (smartphone, IoT, cars, etc.).

With this project, I had the opportunity to work with researchers from LIP6 including Hassan Aboushady and Islam Eshra who are working on a larger research project called "An RF Front-End For a Cognitive Radio Transmitter" in order to tackle 5G requirements. They offered me the opportunity to design a multi standard Digital-Analog Converter (DAC) using Delta Sigma Modulation which will be a part of the transmitter.

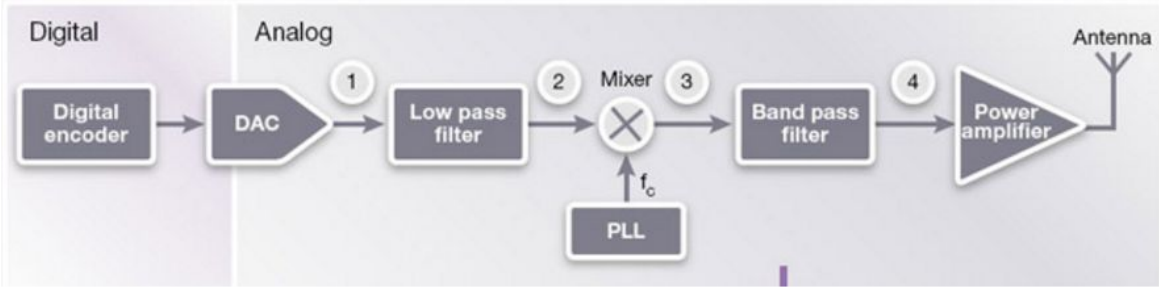


Figure 1. Example of a RF transmitter

The main objective of this project is to design a Matlab model of a DAC by using a Delta Sigma Modulator for two standards: UMTS and WiFi. The DAC must be implemented in a QPSK transmitter and reconfigured for various wireless communication standards. In the following subpart, we will see different concepts that provide a framework for this project.

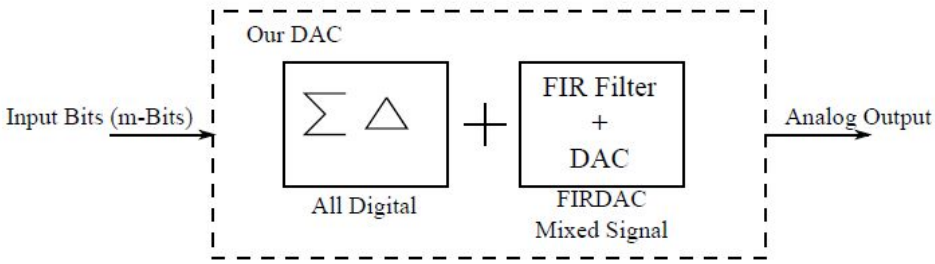


Figure 2. Block representation of the converter made in this project

2. Digital Analog Converter

2.1. Conventional Converter

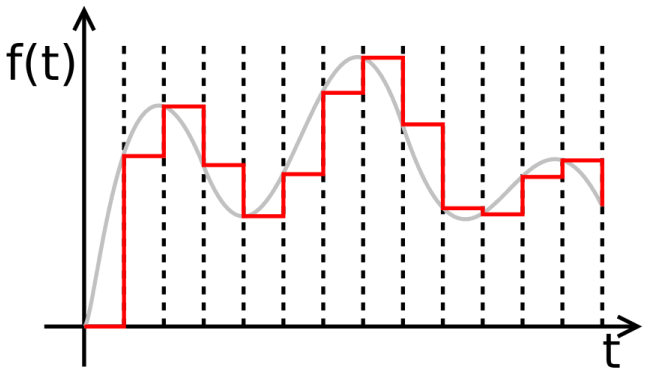


Figure 3. Digital Analog Conversation

In electronics a digital/analog converter (DAC) is a system that convert a digital signal, such as an audio file, into a analog signal. An ideal DAC should transform, at a certain frequency, a serie of binary word (a word represent the quantized amplitude of a sample taken from the signal), into a constant current level.[3] Then it will be processed by a reconstruction filter to smooth out the step response into a continuous signal.
Quantization noise is the error induced by the discretization of the amplitude of signal, also known as resolution.

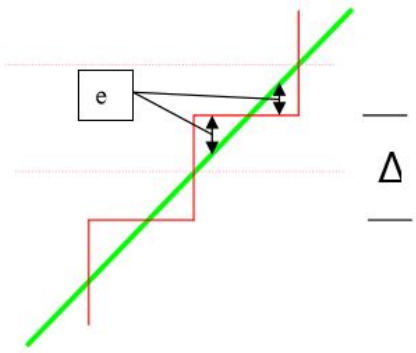


Figure 4. Black arrows show the quantization error for 2 points [3]

As soon as we convert a signal, there will be always quantization noise. So, we have to choose specific DAC architecture which corresponds to our requirements, such as Delta Sigma.

2.2. Delta Sigma Modulation

Delta Sigma converters are very attractive for our purpose because they are able to trade bandwidth for resolution thanks to oversampling and quantization noise shaping.

To explain the Delta Sigma modulation concept, we will suppose that we are in a case where we need to design an Analog-Digital Converter (ADC). Consequently, input signals will be continuous and will be sampled in order to be processed by discrete transfer function.

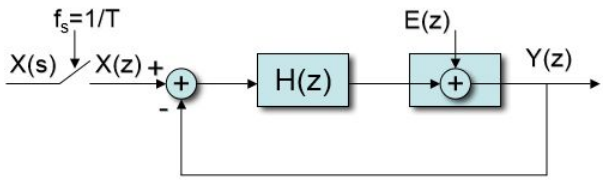


Figure 5. Block diagram of the Noise Shaping loop (1st order). H(z) is function transfer of low pass filter (Integrator) and E(z) is function transfer of the quantization error [4]

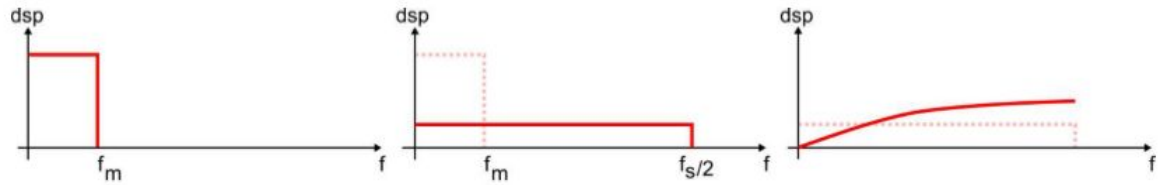


Figure 6. *Left* : Spectral density of quantized signal, with Fm as sampling frequency. The rectangle represents quantization noise density. *Middle* : The same signal but oversampled. *Right* : The oversampled signal injected into a noise shaping loop (1st order) [5]

We notice on the last figure that oversampling reduces the amplitude and spreads the noise across zero to fs/2. The noise shaping loop pushes the noise to high frequencies. The spectrum of our information signal should be at the lowest level of noise.

In some case, the Nyquist rate is very high, so we would, of course, put the oversampling frequency higher than Nyquist rate. But it is very difficult to realise hardware system that would operate at such a high frequency. Consequently, we have to relax the oversampling ratio and that will generate more quantization noise. In order to keep our bandwidth from the noise, we should increase the order of the Delta Sigma modulation to have a better noise rejection, but we have to be careful about the stability of the system.

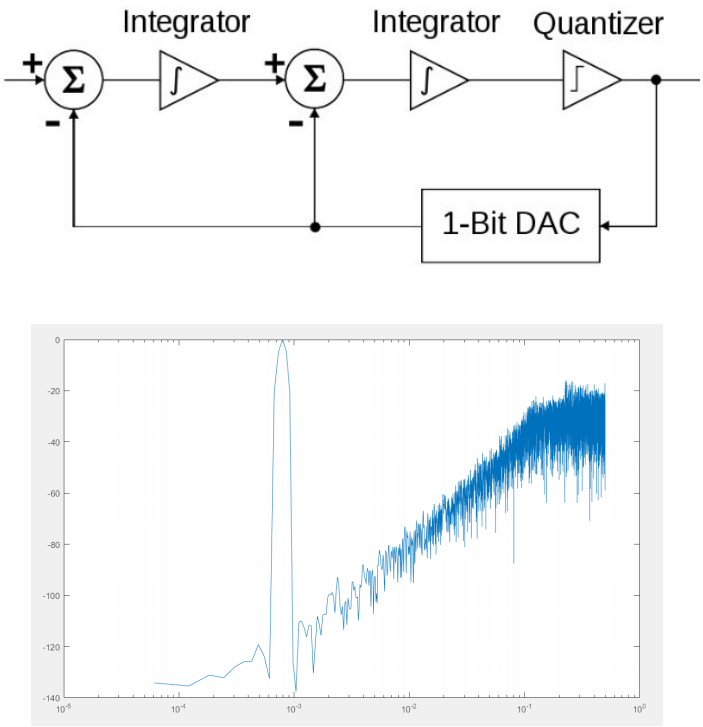


Figure 7. 2nd order Delta Sigma modulation block diagram and a FFT from the output of the quantizer, made from Matlab (Y axis : power in dB; X axis :Normalized Frequency). We can see the input signal spectrum standing out from the noise.

A 1-Bit DAC is a block whose output will be two-level analog signal (V+ and V-, for instance) depending on if the input is higher or lower than the DAC quantization threshold [1]. At the output of the loop, the signal will be a one bit stream with modulated duty cycle. This signal has to be filtered (with a digital filter to delete the high frequency noises) and the oversampling ratio reduced (decimator) in order to make the result usable .[2]

2.3. Delta Sigma DAC

Our project is to build a DAC and this converter has a different block diagram:

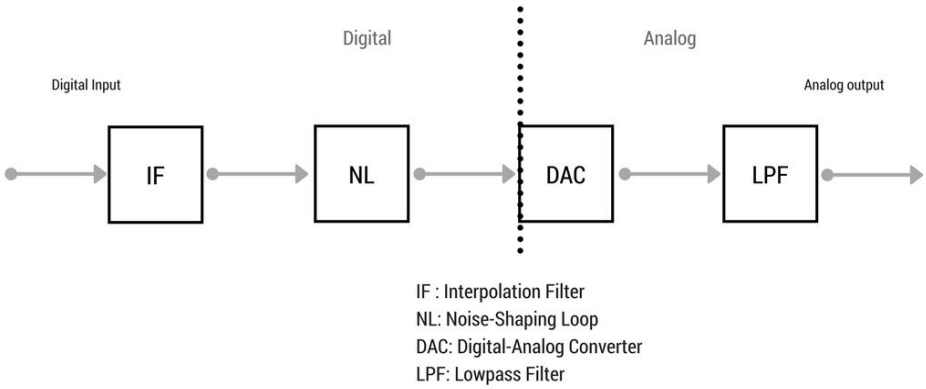


Figure 8. Block Diagram of Delta Sigma DAC[2]

The one bit DAC is not in the noiseshaper loop anymore and it needs an analog low pass filter (LPF) in order to smooth the output of the DAC (reconstruction filter). However, designing a analog LPF for this case is a difficult task (expensive, high power consumption …).

In the next part, we will explain how to tackle this problem with Finite Impulse Response Filter (FIR filter) combined with single-bit DAC.

2.4. FIRDAC

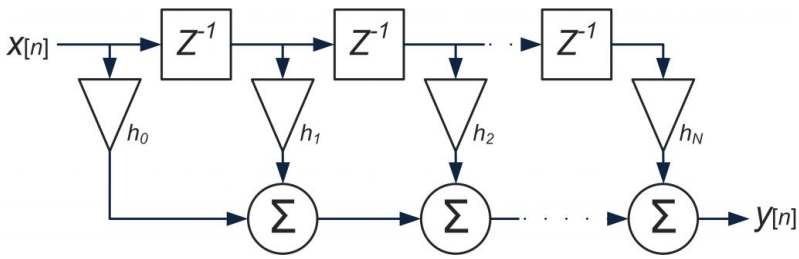


Figure 9. FIR filter architecture

Since the signal coming from the noiseshaper loop still is digital, we can replace the DAC by an digital filter. In this case, we choose an FIR filter because of its phase linearity. Also, we embed a 1 Bit-DAC in the FIR architecture unit instead of the gain blocks of the FIR architecture as shown in the next figure. However, the high level of each DAC will be multiplied by the corresponding coefficient.

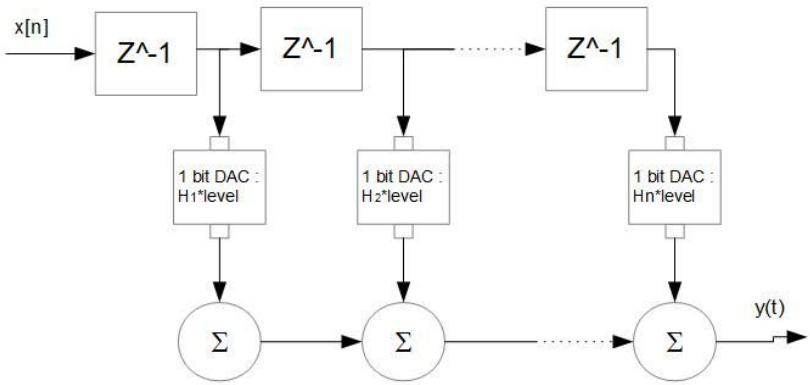


Figure 10. FIRDAC architecture

After the 1 Bit DACs, signals will be analog and they will be naturally summed together towards the output.

Since the FIRDAC will be made as hardware components, there will be some limitations to respect during the design:

- Maximum order of the filter : 63
- All the coefficient must be positives
- The difference between the smallest coefficient and the biggest coefficient has to be equal or lower than 153

3. QPSK Transceiver

3.1. Transmitter

In this project, we will limit the scope of RF transmitters to Quadrature Phase-Shift Keying (QPSK) based transmitter.

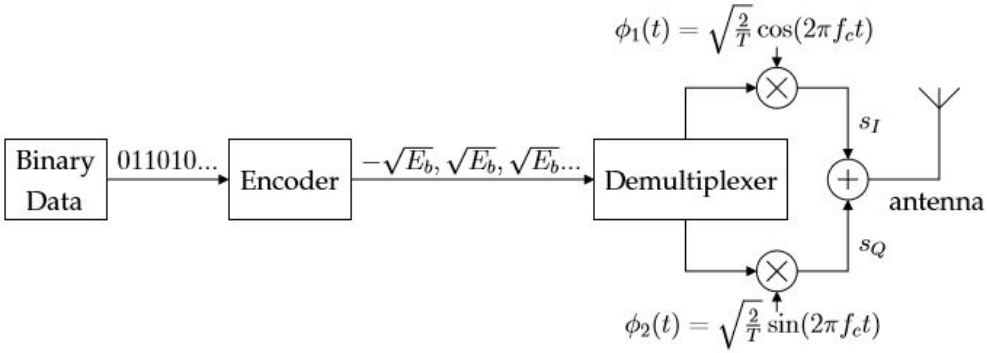


Figure 11. Coherent QPSK transmitter block diagram

This digital modulation system is able to convey binary data by changing the phase of a carrier wave. The phase can have four different values: $\pi/4$, $3\pi/4$, $5\pi/4$, $7\pi/4$, and each phase value is associated to a binary value of two bits: 11, 10, 00, or 01 (in Gray code). The Encoder will associate each bit to a non-return-to-zero level (symbol), after which the signal is distributed by the Demultiplexer into two branches called the 'In-phase branch (I)' and 'Quadrature-phase branch'. The distribution is based on odd and even bits. For instance, odd bits are sent to the I branch and even bits to the Q branch. Then, each branch signal is multiplied by its own carrier signal (Carrier signals' phase have $\pi/2$ difference). This is where the phase shift actually happens. Then, the two signals are added together towards the antenna.

In Figure 11, the signals result from the demultiplexer have to be analog since these signals have to be multiplied by carrier signals, which are analog signals. It is for this reason that we need to implement a DAC between the demultiplexer and the mixer.

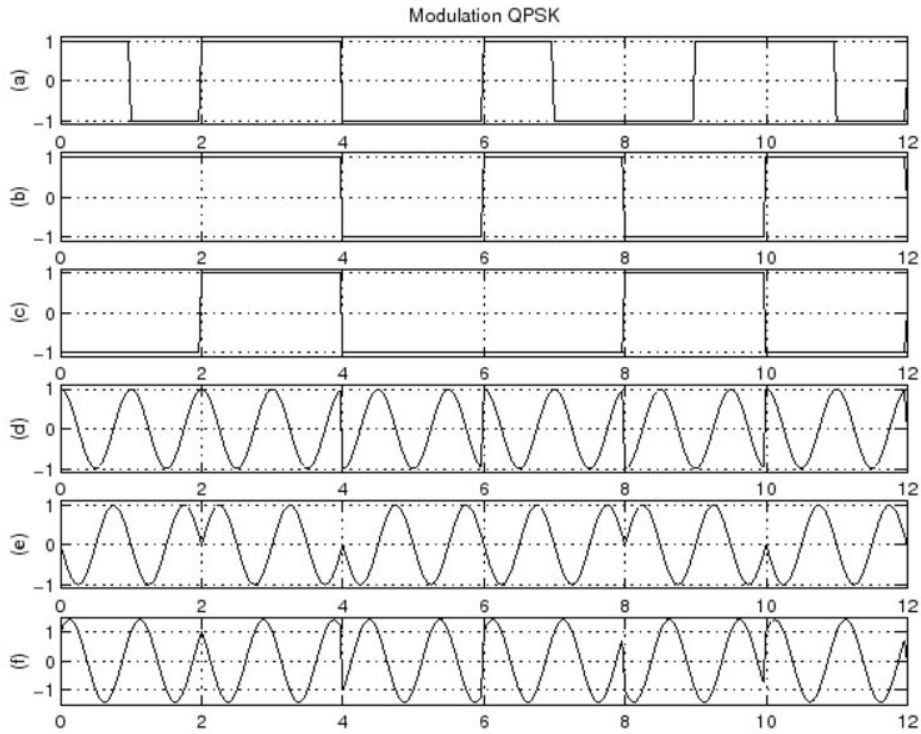


Figure 12. QPSK transmitter signals chronogram [6]
a) Binary data, input signal b) Binary signal in I branch c) Binary signal in Q branch d) I branch signal after multiplication by carrier e) Q branch signal after multiplication by carrier f) Signal after the sum, output signal

Pulse Shaping and bitrate

Our initial data signal is represented as rectangular signal. This kind of signal has a very large spectrum that will generate some leakage in the Out-Of Band. Moreover if we keep rectangular signal, symbols can interfere other symbols causing less reliable signal.

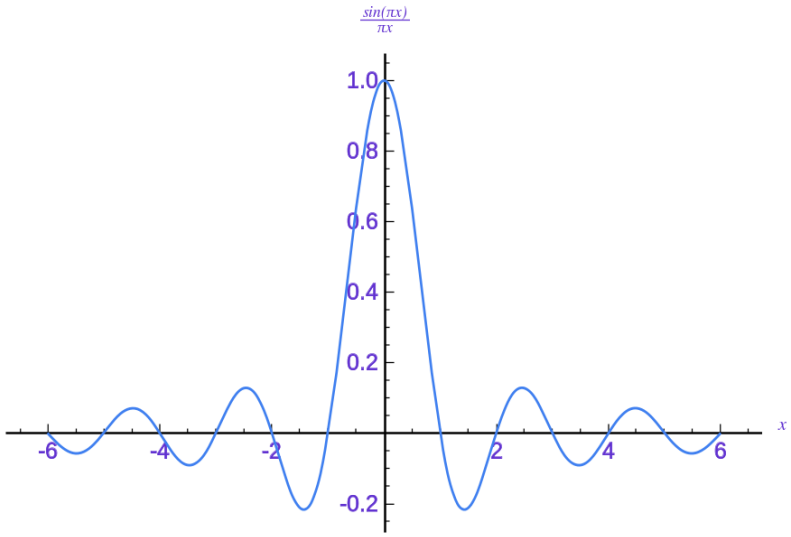


Figure 13. Rectangular signal spectrum

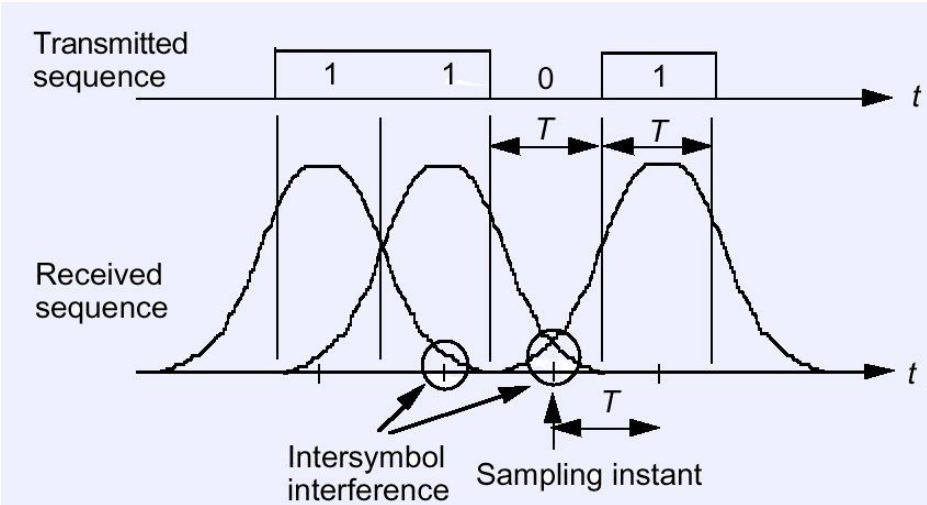


Figure 14. Intersymbol Interference illustration [13]

In order to avoid this problem, we put filter for shaping the waveform of transmitted pulses. It is called Pulse Shaping and we will use a Raised Cosine filter.

For instance, with a rectangular spectrum, we can adjust the shape of the pulse with the Bêta parameter, also called the Roll off. The value of bêta parameter is defined by the Standards.

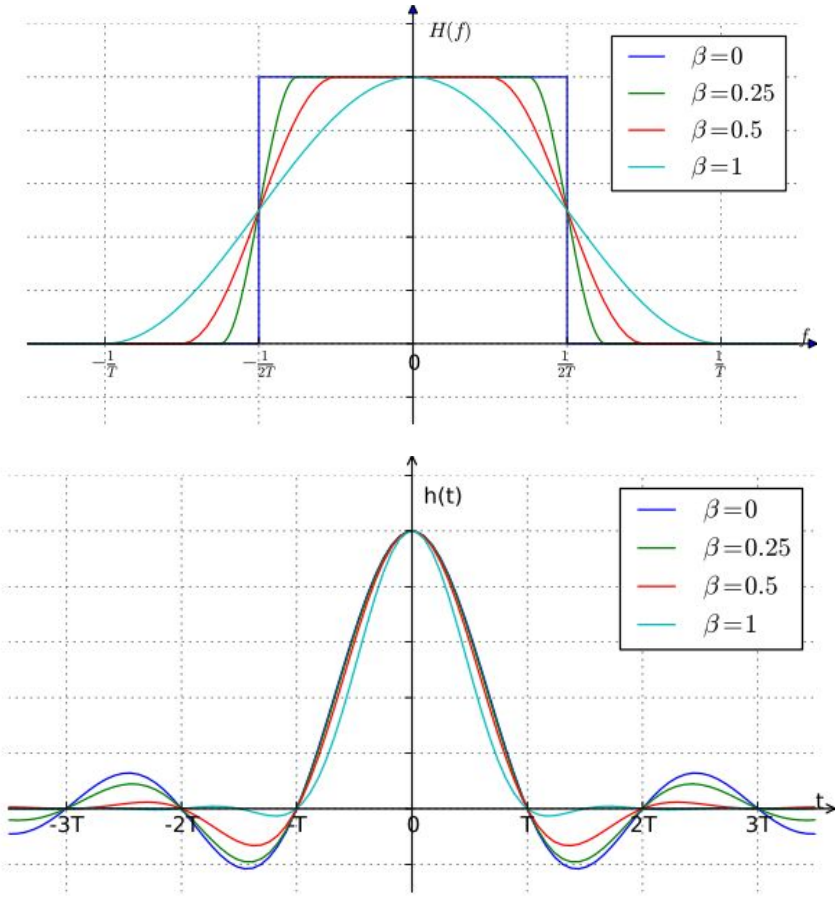


Figure 15. Frequency and Impulse response for different Bêta [14]

Besides, we have to make sure that the period of the bitrate is suitable for our system. For instance, a system without pulse shaping and its bandwidth is 5 MHz :

$$Bandwidth = \frac{1}{Tsymbol}$$

where Tsymbol is the period of one symbol

With the pulse shaping, the formula will be :

$$Bandwidth = \frac{1}{Tsymbol}(\beta + 1)$$

As we are using oversampling, bandwidth can be written as :

$$Bandwidth = \frac{Fs}{2 \times OSR}$$

where Fs is the oversampling frequency, OSR the oversampling ratio. Fs = 1 because we are working with normalized frequencies

Finally, the formula of Tsymbol is :

$$Tsymbol = \frac{2 \times OSR \times (\beta+1)}{Fs} = 2 \times OSR \times (\beta + 1)$$

3.2. Receiver

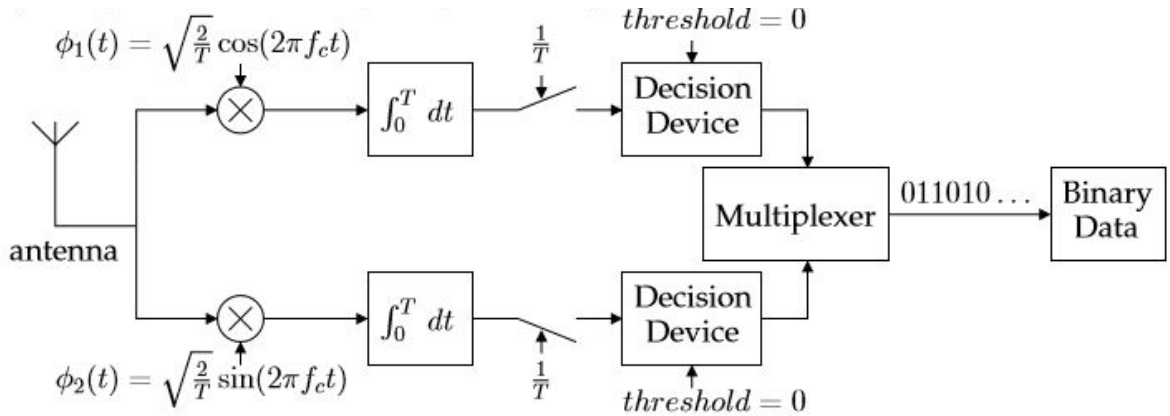


Figure 16. QPSK receiver block diagram

The signal from the antenna will be multiplied by the two carrier signals (same as in the transmitter), in order to have the in-phase signal in one branch and the quadrature-phase signal in the other.Following this, the signals are filtered by an integrator to avoid the replicated spectrum made by the modulation. The decision devices (a comparator for instance) translate each branch signal into binary data that will be gathered and organized by the multiplexer. At the end of this stage, we have the initial binary data back.

Based on the received signal, we can plot a constellation diagram. This diagram shows us how the receiver demodulates the signal from the transmitter. We will discuss later how to interpret this kind of diagram.

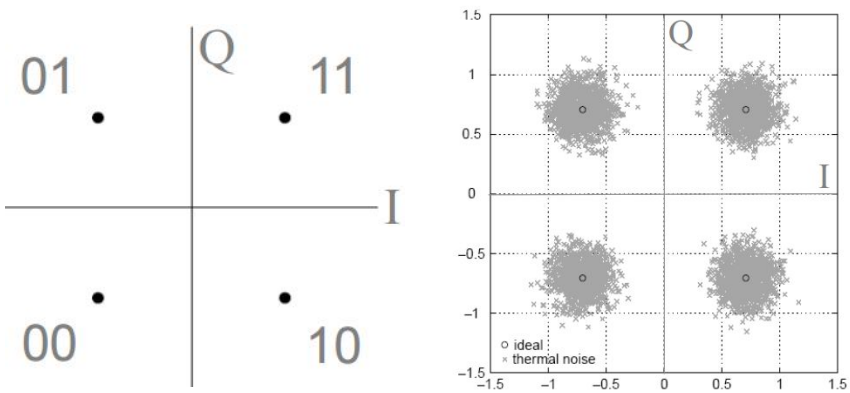


Figure 17. A theoretical QPSK constellation diagram and a constellation diagram of a signal with noise (SNR = 10). Plotted in Matlab.

4. Project Organization

4.1. Objectives

The goal of this project is to design a processing block which is composed of Delta Sigma modulator and FIRDAC and also suitable for UMTS and WiFi, then run various test in a QPSK transmitter in order to measure its performances.

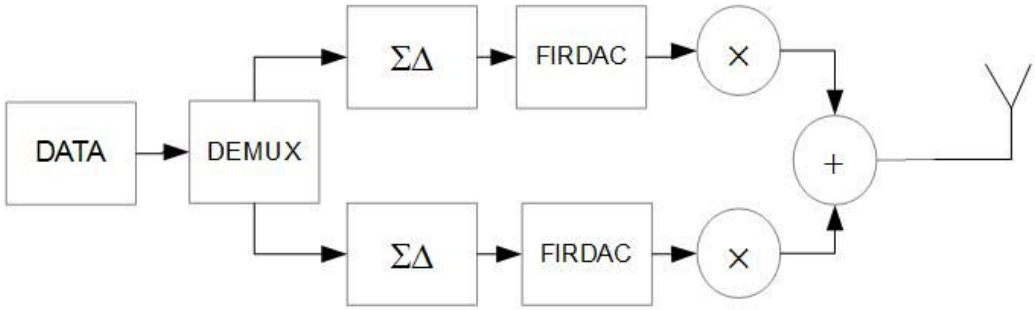


Figure 18. QSPK transmitter with the Delta Sigma modulator and FIRDAC implemented

This figure summarizes the whole project in block diagrams. The converter part is important since it is based on digital components which are able to adapt to different kinds of standards.

4.2. Task list

- ❏ Understand Delta Sigma Modulator and run a simulation on Simulink

  We will go through the book *Understanding Delta-Sigma Data Converters,* by Richard Schreier, Gabor C. Temes to completely understand how the Delta Sigma modulator works. A simulink model of a discrete time Delta Sigma modulator will be designed and used for a better understanding.

- ❏ Understand QPSK and build a matlab model for the single arm Transmitter, then modifying the parameters for the QPSK modulation scheme

  Using *Circuit RF pour les communications numériques,* M2 course by Hassan Aboushady, we will study QPSK digital modulation and design a matlab model.

- ❏ Understand the metrics upon which transmitter performance is measured (SNR, EVM, BER, spectrum mask …)

To verify the abilities of the system, we have to observe and analyze measurements. Some matlab script have to be written in order to systematically challenge our system.

- ❏ Study the specification of UMTS and WiFi and determine their Bandwidth, their desired SNR, desired Mask

  We have to make sure that our system's features are matching with the standard we have chosen. This is why we have to understand and pick standardized values

- ❏ Implement Delta Sigma based on Schreier's Toolbox

  The Schreier's book provides a matlab Toolbox to efficiently design y a Delta Sigma modulator.

- ❏ Understand FIR, FIRDAC, Filter Toolbox

  In order to implement the digital lowpass filter after the Delta Sigma modulator, we must know how to design a FIRDAC and how to simulate it, using the matlab Filter Toolbox.

- ❏ Build matlab model of Delta Sigma Modulator and FIRDAC

  Since the modulator and the filter are ready, we need to make them work together in a matlab simulation.

- ❏ Embed the Delta Sigma Modulator + FIRDAC in the QPSK transmitter model

  If the previous task is validated, we will do the last implementation. This will permit us to test if the multiplication with the carrier is done correctly.

- ❏ Adjust Delta Sigma modulator and FIR DAC for different standards like UMTS and WiFi

  At the end, we will configure the system with various coefficients in order to generate signals corresponding to the requirement of different standards.

The planning is in the appendix.

4.3. Development Environment

In this project, we will mainly use the language and software Matlab do our design. Matlab is as numerical computing environment developed by MathWorks. Matlab allows matrix manipulations, plotting data. Optional tool can be used, like Simulink which is very convenient to design signal processing systems.
Besides, we will use some tools provided by the book "Understanding Delta-Sigma Data Converters" by Schreier and Temes [2]. This book provides Delta Sigma architectures and some matlab script to help us calculate coefficient for the Delta Sigma block.

Architecture

We will work with the Cascade of Integrators with Distributed Feedback (CIFB) architecture, in the second and third order.

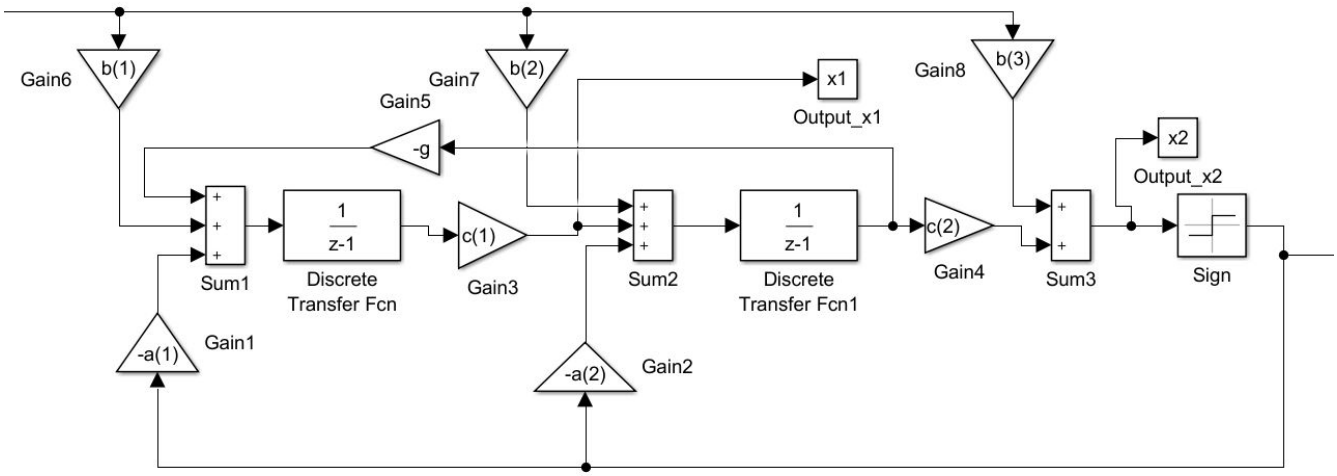


Figure 19. Second Order CIFB Delta Sigma [2]

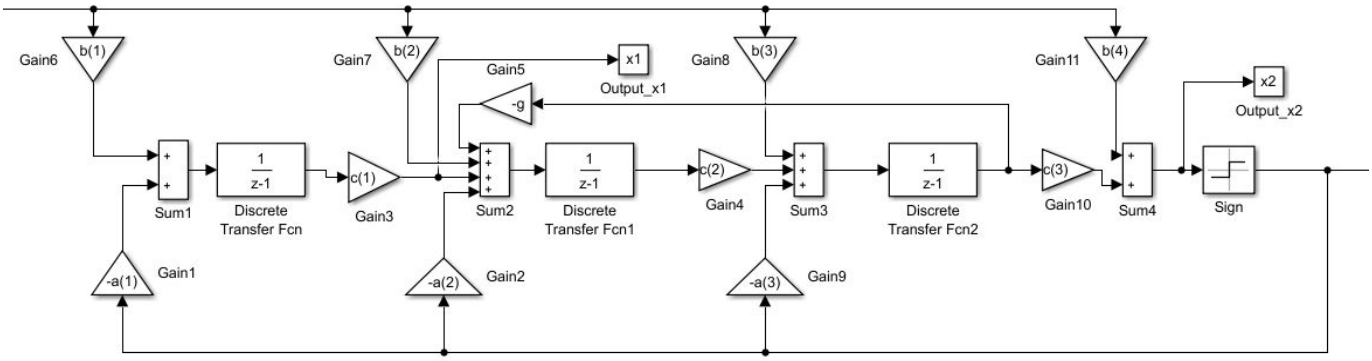


Figure 20. Third Order CIFB Delta Sigma [2]

These architectures have various gain components that refer to coefficients that are calculated by the matlab script provided by the Schreier's book.

Filter Designer

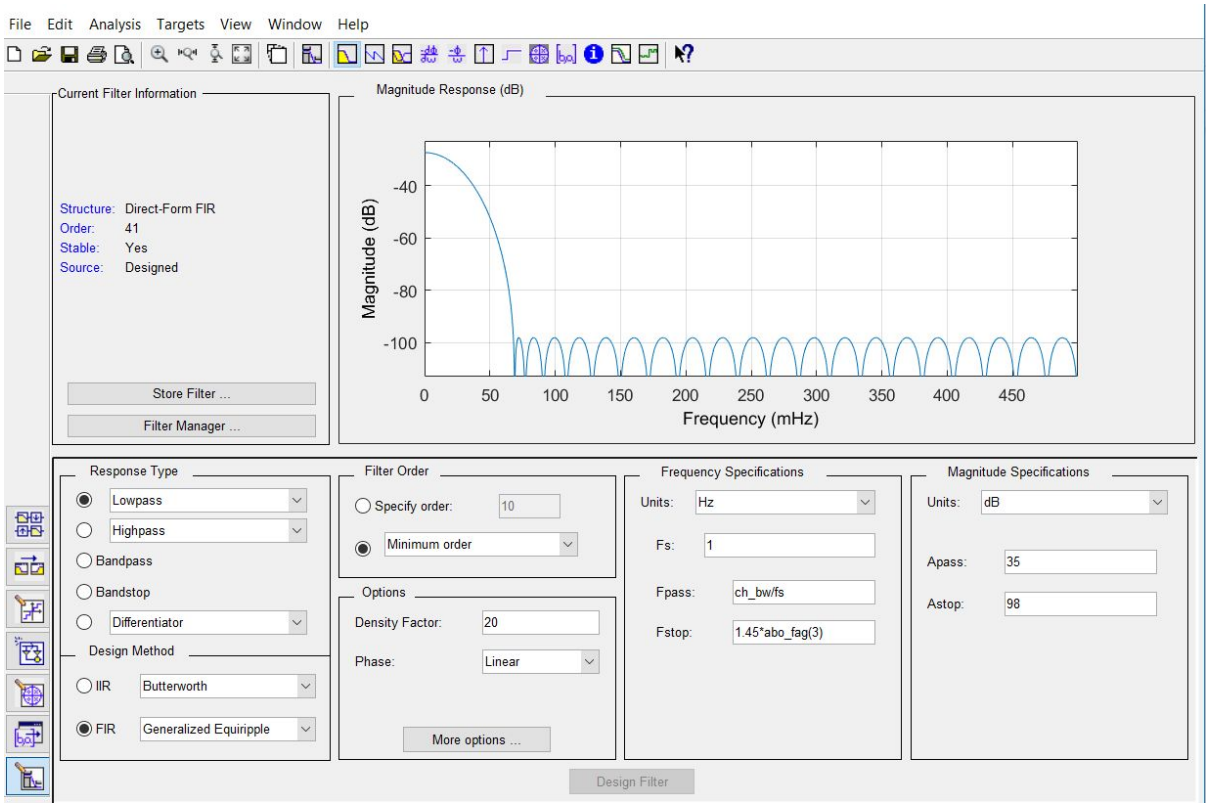


Figure 21. Parameters in Filter Designer for the UMTS standard

With this tool, we tune it in order to calculate the coefficient of a FIR Lowpass filter:

- Generalized Equiripple
- Sampling frequency Fs = 1 because we are working with a normalized Fs
- Fpass = the channel bandwidth (in UMTS it is 5 MHz)
- Fstop = the frequency at the interface between channel bandwidth and Out of Band
- Apass = amplitude for the channel bandwidth
- Astop = amplitude for the spectrum higher than Fstop

After multiple tweaking, we were able to have correct coefficients for each standard.

QPSK Transceiver architecture (see in the appendix)

4.4. Acceptance Testing

In this part, we will talk about how to analyze the results from our models and compare them to the standards. These standard are related to UMTS and WiFi.

- Spectrum Mask

Moreover, in wireless communication, each standard has its own spectrum emission mask. We have to make sure that the transmitted signal is not interfering with an another standard's spectrum.

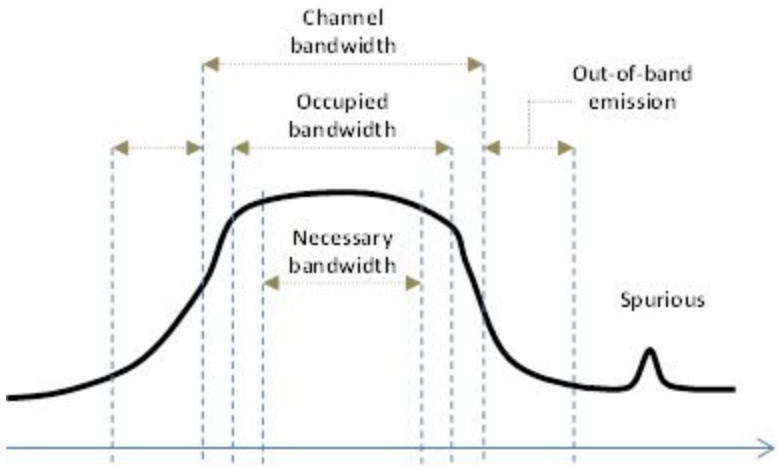


Figure 22. Illustration of a spectrum emission

As we can see in Figure 22, the spectrum is divided into different sections:

- "*Necessary bandwidth is the width of the frequency band which is theoretically just sufficient to ensure the transmission of information.*
- *Occupied bandwidth is the width of the frequency band such that, below the lower and above the upper frequency limits, the mean powers emitted are each equal to a specified percentage B/2 oif the total mean transmitted power.*
- *Out of Band (OoB) : is the frequencies immediately outside the channel bandwidth which results from the modulation process and non-linearity in the transmitter, but excluding spurious emissions*
- *Spurious emission = emission on frequencies which are outside the channel bandwidth and the level of which may be reduced without affecting the corresponding transmission of information, thus excluding out-of-band emission.*"[1]

[1] Definitions are coming from the website SEAMCAT (Spectrum Engineering Advanced Monte Carlo Analysis Tool) Handbook, Edition 2, April 2016, European Communication Office

fs is the sampling frequency
OSR is the oversampling ratio

Spectrum Mask WIFI IEEE802.11a operating at 5 GHz ch_bw is the channel Bandwidth, it could be (10MHz, 20MHz, 50MHz, 90MHz) ch_bw = 50 MHz OSR = 64 fs = 2*OSR*ch_bw						
Frequency	0	(ch_bw-1)/fs	ch_bw+1)/fs	((2*ch_bw)/fs	(3*ch_bw)/fs	(4*ch_bw)/fs
Magnitude	0	0	-20	-28	-40	-40

Spectrum Mask UMTS 5MHz channel BW operating at 1.98GHz ch_bw is the channel Bandwidth ch_bw = 5 MHz OSR = 64 fs = 2*OSR*ch_bw							
Frequency	0	30E6/fs	30E6/fs	160E6/fs	160E6/fs	220E6/fs	0.5
Magnitude	0	0	-85	-85	-128	-128	-128

Spectrum Mask WiFi IEEE802.11g and ISM Band operating at 2.4GHz ch_bw is the channel Bandwidth ch_bw = 5 MHz OSR = 64 fs = 2*OSR*ch_bw							
Frequency	0	50E6/fs	50E6/fs	150E6/fs	150E6/fs	250E6/fs	0.5
Magnitude	0	0	-85	-85	-128	-128	-128

[9] [12]

- Error Vector Magnitude (EVM)

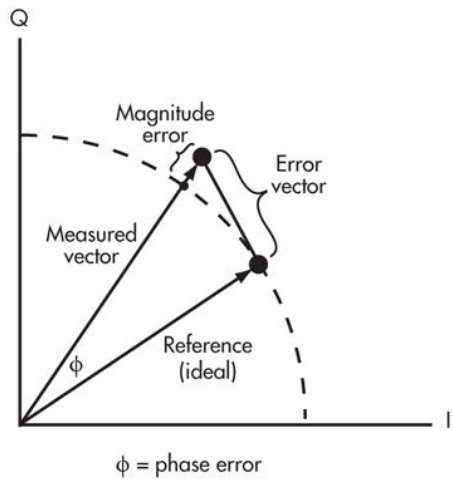


Figure 23. VIsual model of EVM [10]

Error vector magnitude determine impairments that affect signal in term of reliability of the modulated signal. In a constellation diagram, like figure 4, EVM illustrates the difference between a reference vector location and the actual measured vector. EVM must be as low as possible in order to obtain a reliable signal from our system. [8] [11]

- Signal to Noise Ratio (SNR)

The noise floor is the level of background noise. Below this level, the signal representing the information cannot be isolated from the noise.

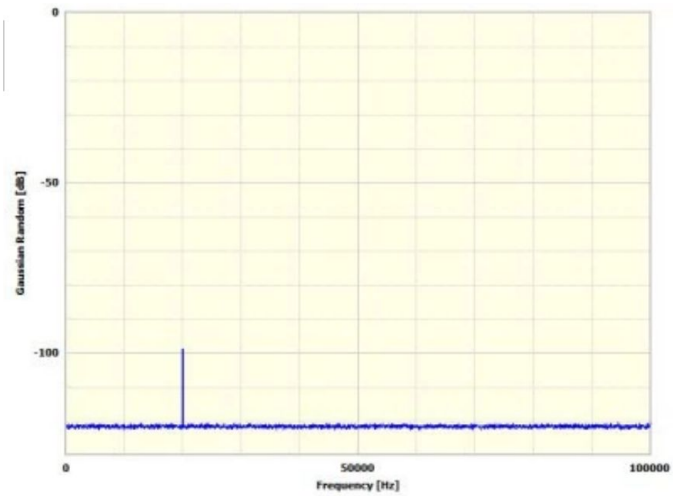


Figure 25. Representation of the noise floor in frequency domain

Signal to noise ratio is the ratio of the power of a signal and the of background noise (unwanted signal)[7]. It is usually measured in decibels (dB) :

$$\mathrm{SNR}_{\mathrm{dB}} = 10 \log_{10} \left(\frac{P_{\mathrm{signal}}}{P_{\mathrm{noise}}} \right)$$

After studying the standards for UMTS and WiFi, it appears that SNR is less relevant than EVM. Standards just ask the noise floor to be under -128 dB.

In a nutshell, these are the acceptance testing steps :

1. Generate a QPSK signal
2. Embed and adjust the Delta Sigma modulator and FIRDAC for a standard (UMTS for instance)
3. Verify that the system satisfy UMTS requirements in terms of noise floor, spectrum mask, SNR and EVM
4. Repeat steps 1, 2, 3 for WiFi standards

5. Results

5.1. Spectrum Mask

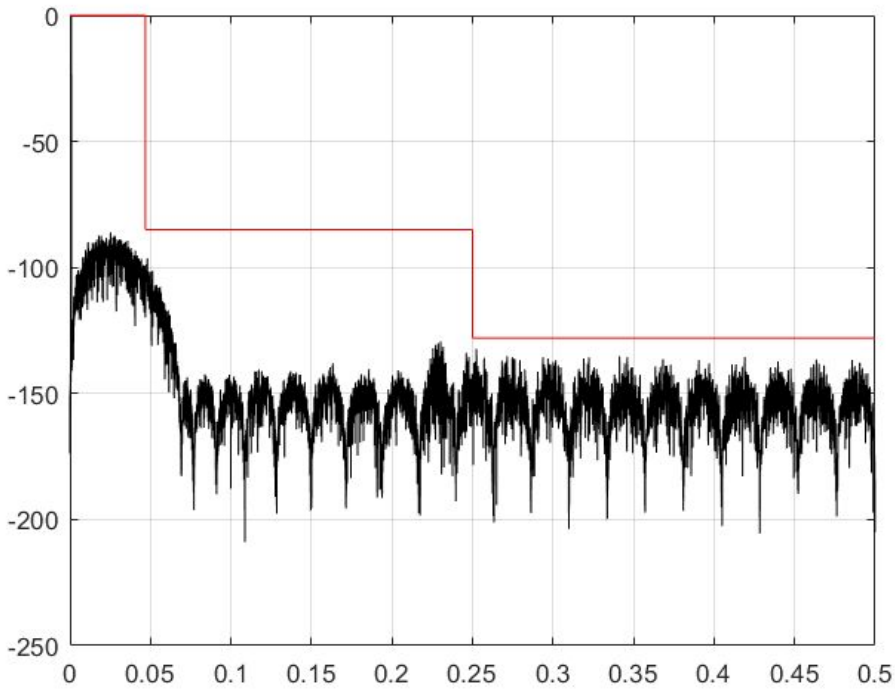
In this part, we will show the results concerning the spectrum mask for each standards. Those signals are measured after the Delta Sigma Block. There will be three kind of signal :

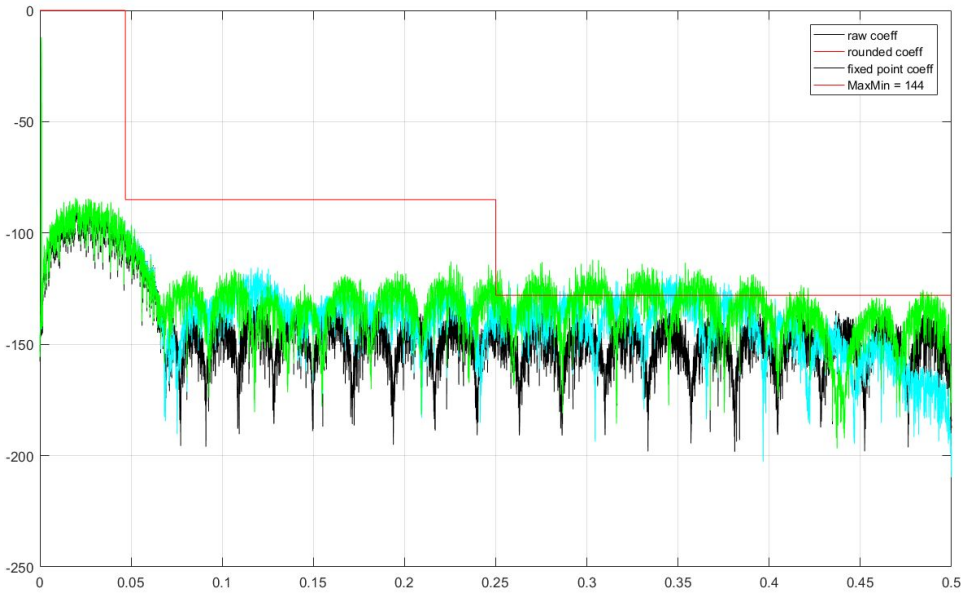
- based on raw coefficients taken straight from the Filter Designer : black spectrum
- based on rounded coefficient (the raw coefficients have been rounded) : cyan spectrum
- based on fixed point (raw coefficients have been quantized at 16 bit) : green spectrum

We will see that X axis is limited to 0.5. It's because we normalized the X axis by over sampling frequency Fs (Fs= 2*OSR*ChannelBandwidth). The Y axis is in dB.

Every spectrum based on raw coefficients respect the noise floor at -128 dB.

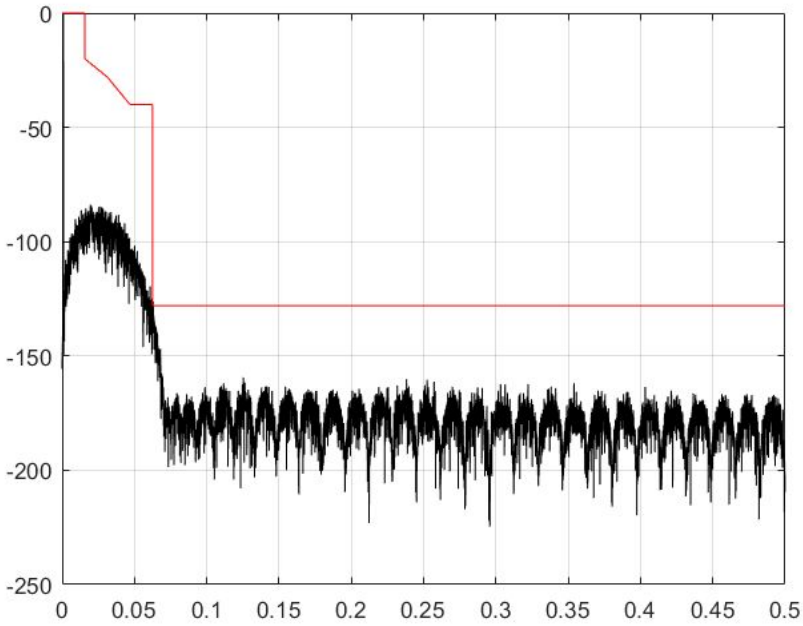
5.2. UMTS operating at 1.98GHz

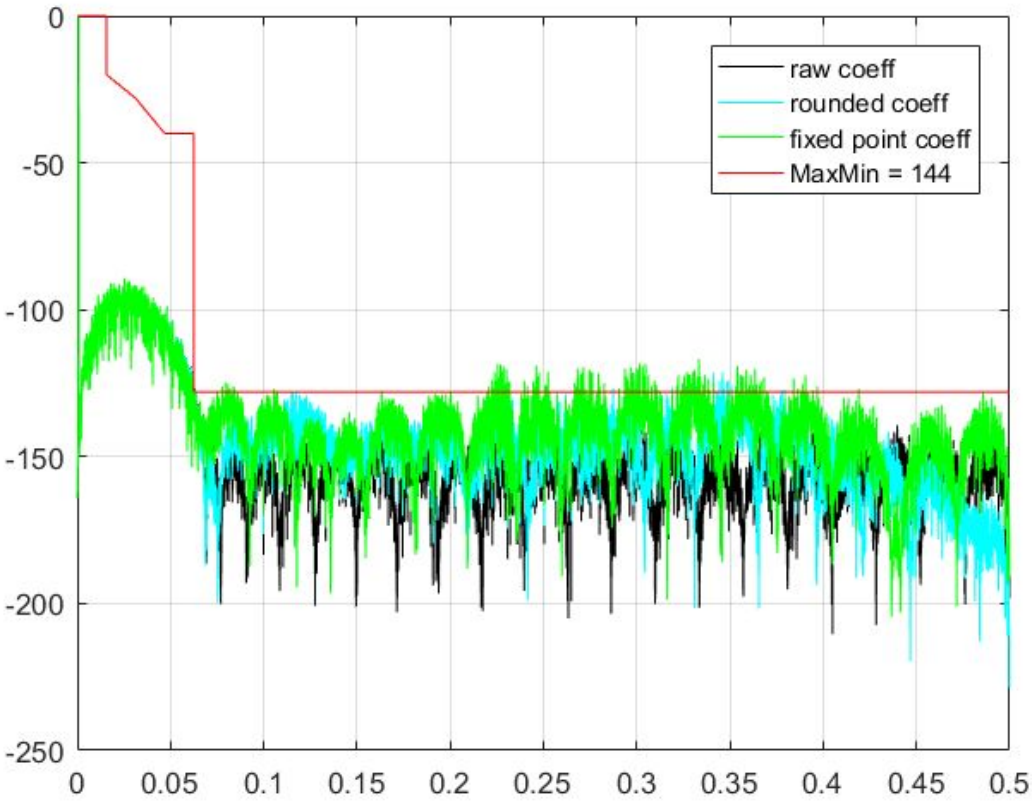




- Channel Bandwidth : 5 Mhz
- OSR : 64
- Order = 2
- Fs= 640 MHz

5.3. WiFi IEEE802.11a 5GHz

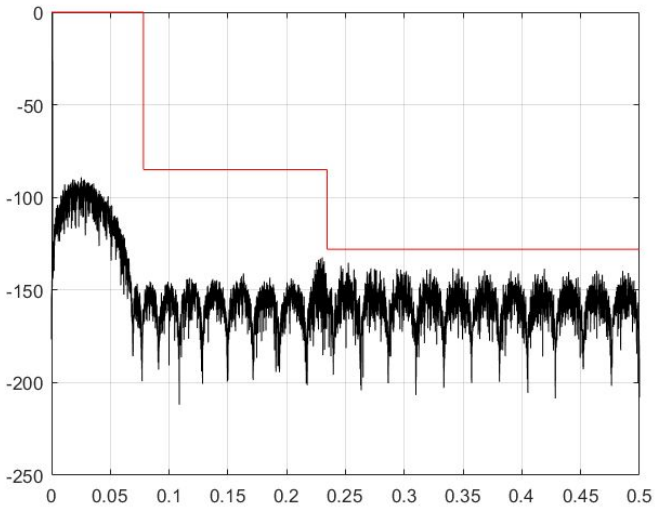


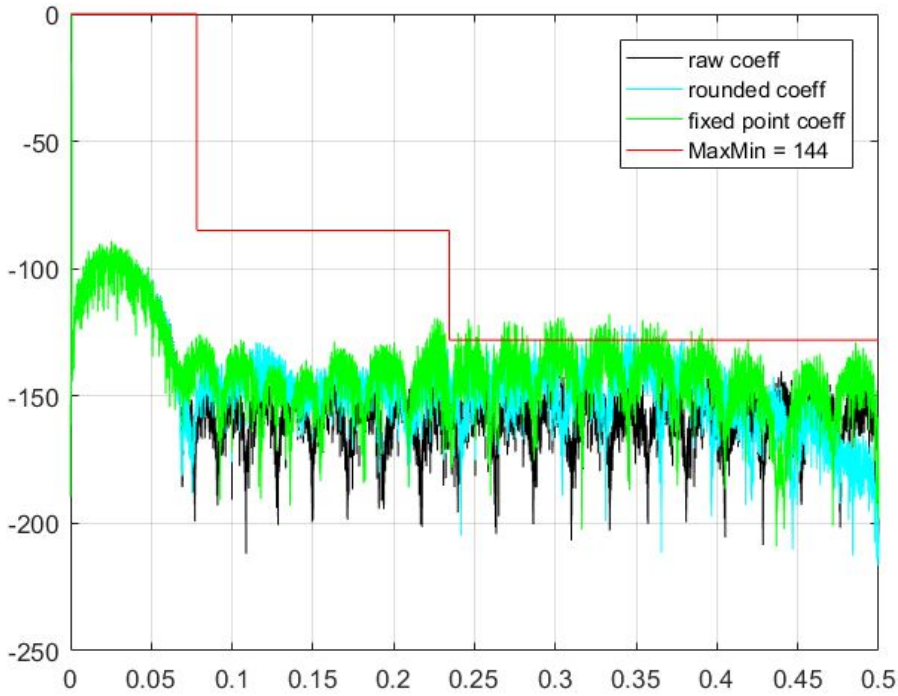


- Channel Bandwidth : 50 Mhz
- Fs= 6,4 GHz with an OSR of 64.

It’s too high for the hardware realization. So we need to decrease it: we defined OSR at 16
and the new Fs = 1,6 Ghz. In order to compensate this changement of OSR, we raise the order of Delta Sigma at 3 and this will produce a better noise rejection in the channel bandwidth.

5.4. WiFi IEEE802.11g operating at 2.4GHz





- Channel Bandwidth : 5 Mhz
- OSR : 64
- Order = 2

- Fs= 640 MHz

Comment

Unfortunately, the spectrum based on fixed point is not good enough with those spectrum mask. We have to consider it for the hardware realisation, since it is easier to work with fixed point value than float value in hardware domain.

5.5. EVM

In this part, we will show the results concerning the Error Vector Magnitude and show some Constellation Diagrams.

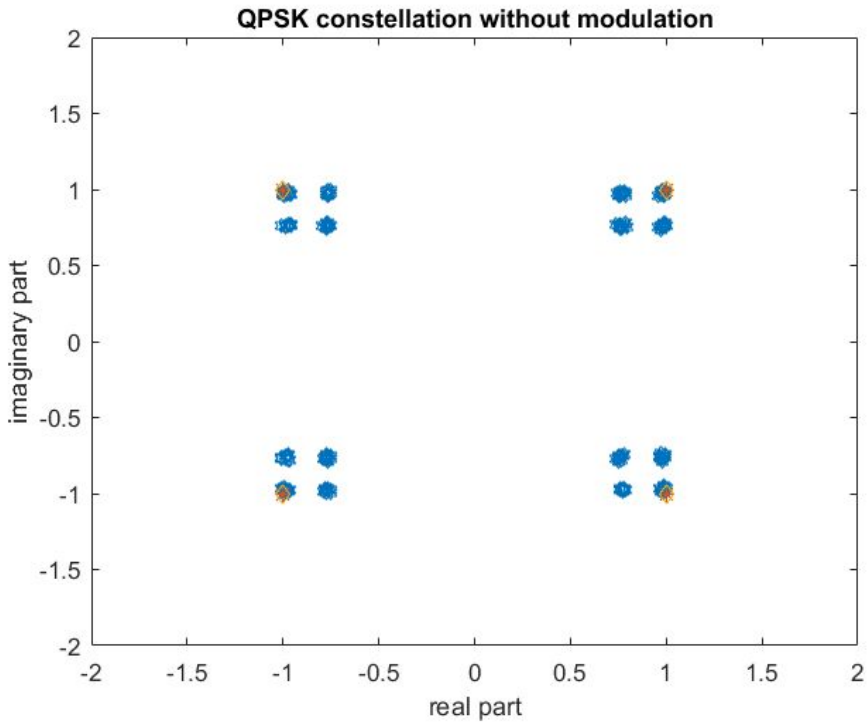
We measured at two different stage of the prototype:

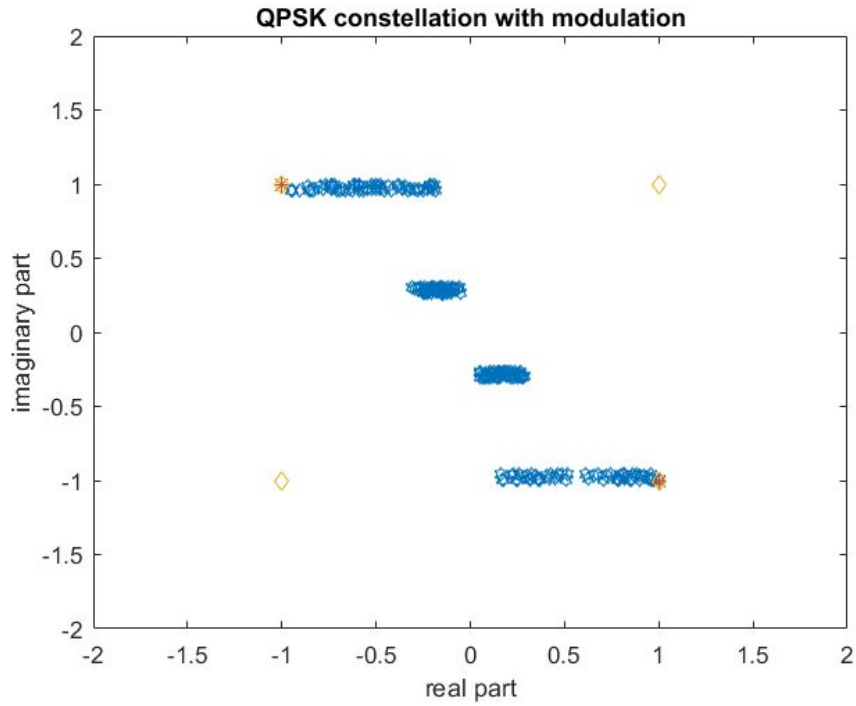
- Before the modulation
- After the demodulation

In the constellation diagram, the blue point are the signal coming from our system and the rhombus point are the reference point (goal)

WIFI IEEE802.11a operating at 5GHz

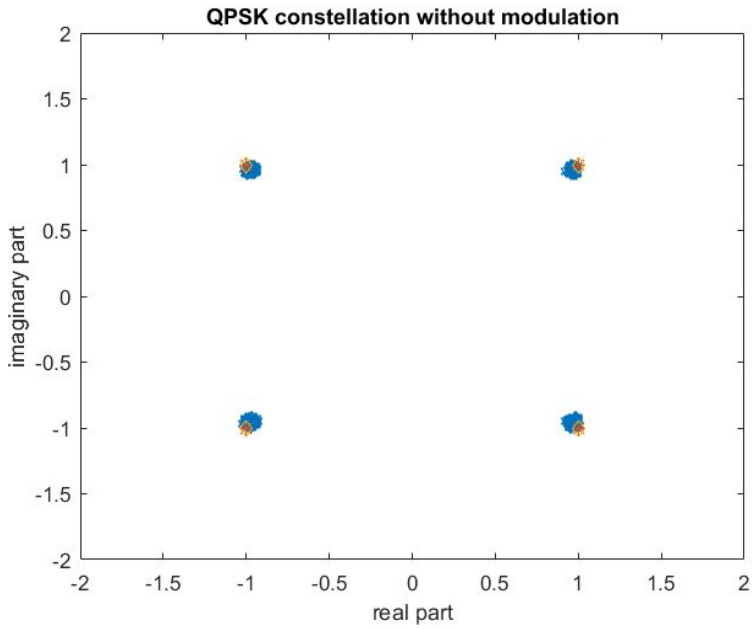
EVM before modulation : 16.25 %
EVM after the demodulation : 99.05 %

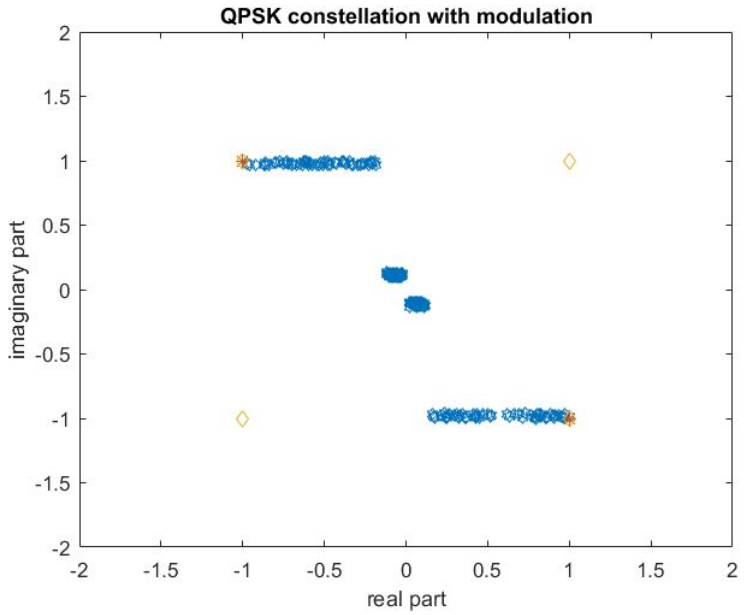




WiFi IEEE802.11g operating at 2.4GHz and UMTS operating at 1.98GHz

- EVM before modulation : 3,93 %
    - The constellation shows some motif, it could could be some sampling frequency error
- EVM after the demodulation : 88.62 %


QPSK constellation without modulation
imaginary part
real part
2
1.5
1
0.5
0
-0.5
-1
-1.5
-2
-2
-1.5
-1
-0.5
0
0.5
1
1.5
2


QPSK constellation with modulation
imaginary part
real part
2
1.5
1
0.5
0
-0.5
-1
-1.5
-2
-2
-1.5
-1
-0.5
0
0.5
1
1.5
2

Comment

Before the modulation, EVM is good for WiFi IEEE802.11g operating at 2.4GHz and UMTS operating at 1.98GHz. We can try to decrease more the value and try to get 0 %
WIFI IEEE802.11a operating at 5GHz doesn't operate very well (16%).

The EVM results show us that modulation stage doesn't work well and need to be fixed. There is too much error. The whole modulation stage should be investigated.

6. Conclusion

We achieved to design a QPSK transmitter with a Delta Sigma and FIRDAC stage. The results are not as good as we expected but there is some potential solution to make the results better. Because of a lack of time, we could have not investigate more.
Based on this work we could evolve it in order to work with other modulation type, such as 16 QAM.

This project was a great introduction for the research work. My tutors taught me very powerful methodology and expand my knowledge such as electronic and signal processing principles for telecommunication. It was a great experience to work with them.

7. References

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Appendix

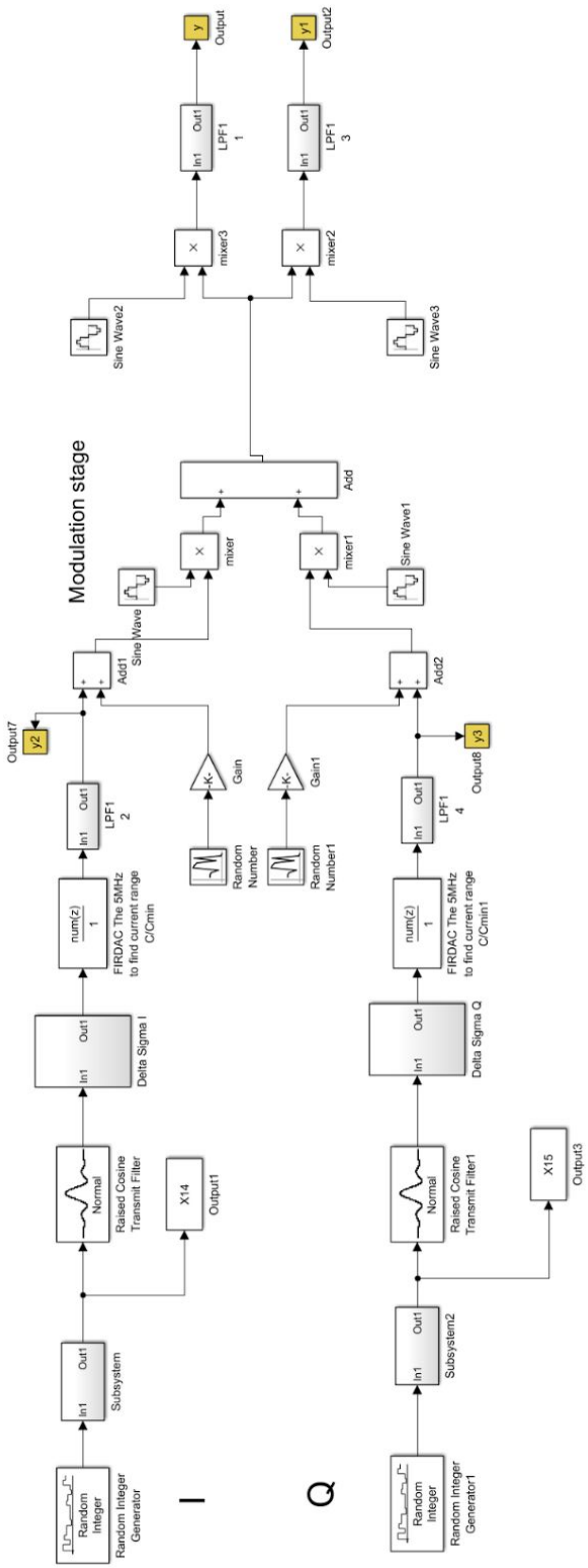
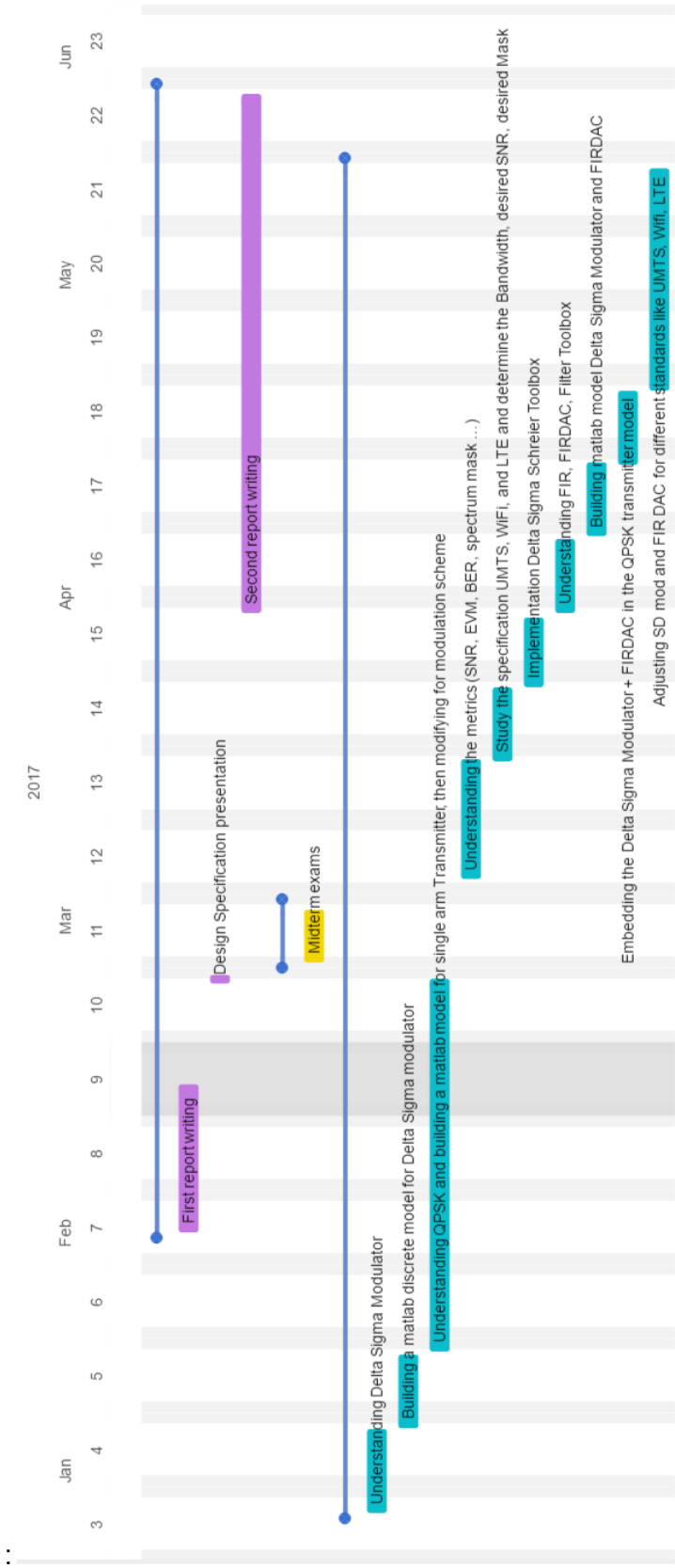


Figure 12. QPSK transmitter architecture (testbench)

Planning

The planning of this project is shown in this Gantt Diagram (made by Elegantt and Trello)



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