Low-Power LC-VCO-Based Chirp Signal Generator

Using Active Inductor

Full-Custom Design and Measurement on UMC 0.18 µm CMOS

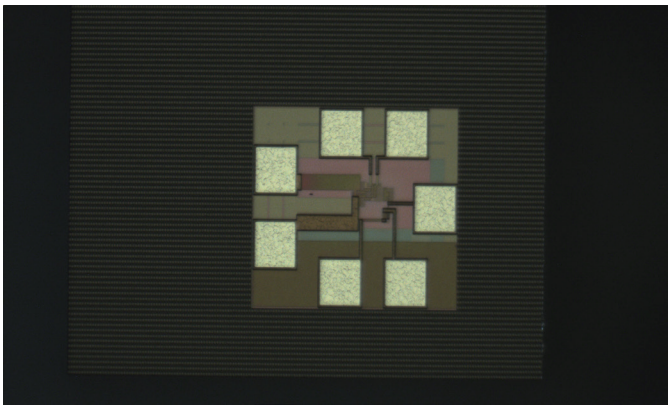
AWARDS & RESEARCH FUNDING

Outstanding Project Award

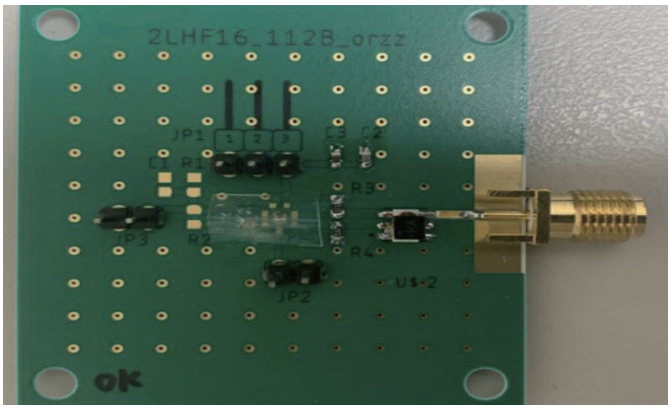
VLSI Design Contest, Department of Electrical Engineering, National Yunlin University of Science and Technology, Taiwan, Nov. 2023

Research Grant Recipient

Undergraduate Student Research Program, National Science and Technology Council (NSTC), Taiwan, Jun. 2023



Chip Micrograph – UMC 0.18 µm CMOS



RF Test PCB with SMA Output

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Portfolio for M.S. Application – Analog IC Design

Contents

Motivation

MOTIVATION & PROBLEM

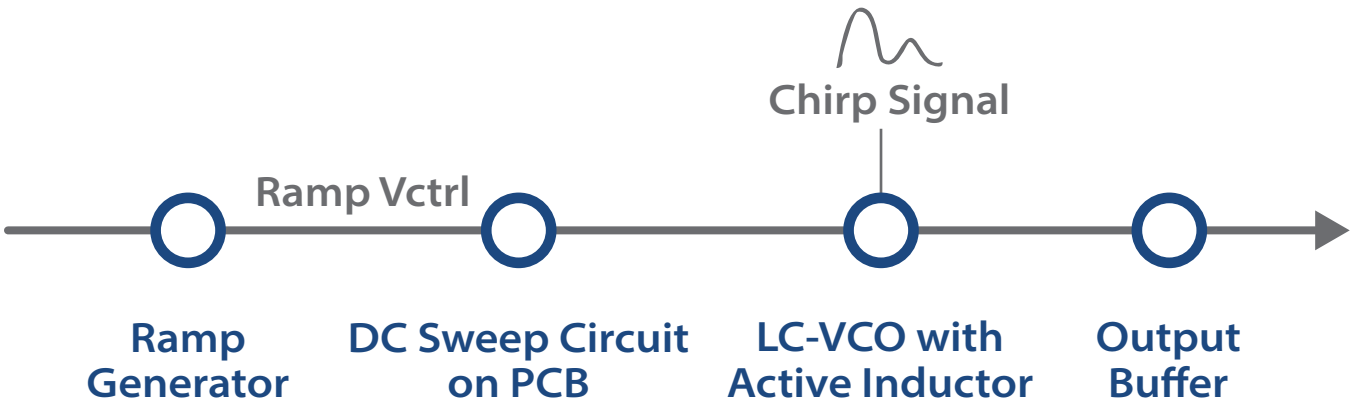
1. **Require** wideband frequency sweep for FMCW radar systems.
2. **F a c e** limitations in analog VCO : narrow tuning and high phase noise.
3. **A v o i d** high-power and complex digital architectures.

DESIGN OBJECTIVES

1. **Generate** chirp signals with low power and continuous sweep.
2. **Optimize** spectral purity, tuning linearity, and integration size.
3. **T a r g e t** 3.0 – 3.5 GHz range for embedded radar use.

PROPOSED SOLUTION

1. **Implement** LC-tank VCO with tunable active inductor.
2. **C o n t r o l** oscillation frequency via ramp voltage from PCB circuit.
3. **Fabricate** full-custom layout in UMC 0.18 µm CMOS with RO4003C PCB.



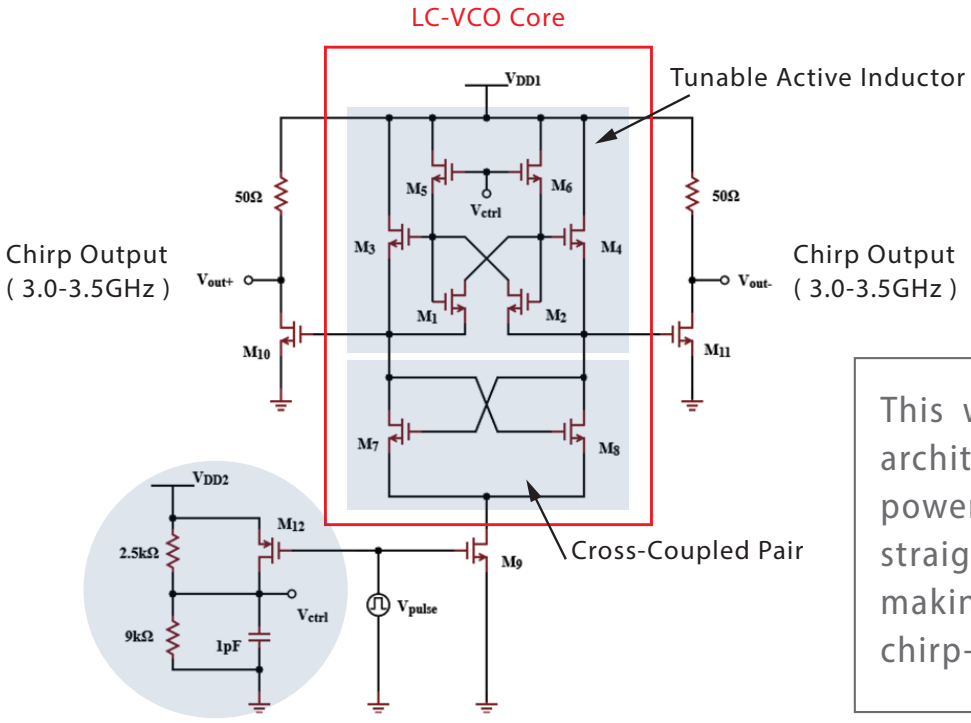
Design Overview & Key Techniques

SYSTEM DESIGN HIGHLIGHTS

1. **Designed** LC-VCO with active inductor for linear sweep.
2. **Achieved** chirp range of **3.0–3.5 GHz** with ramp control.
3. **Completed** full-custom layout in **UMC 0.18µm CMOS**, 0.122 mm^2.
4. **Integrated** external control via high-frequency **RO4003C PCB**.
5. **Verified** spectral purity and frequency sweep in simulation.

COMPARISON OF CHIRP SIGNAL

Type	Pros	Cons
Analog	Low power, simple circuit	Limited accuracy, higher phase noise
Digital	High precision, clean output	High power, complex hardware
Mixed	Combines advantages of both	Costly, harder to implement



Ramp Control (Vctrl)
& External PCB Circuit (RO4003C)

This work adopts the analog architecture to achieve low power, compact layout, and straightforward integration, making it suitable for practical chirp-based RF applications.

Full-custom LC-VCO design with active inductor for chirp modulation

Simulation & Validation Results

SIMULATION SUMMARY

1. **Simulated** tuning range : **2.0–5.0 GHz**
2. **Applied** control voltage : **2.0–3.4V**
3. **Observed** nonlinear tuning characteristic
4. **Maintained** output power : **–30±5 dBm**
5. **Verified** continuous frequency sweep from ramp input
6. **Improved** output flatness by increasing output capacitor from 100 pF to 300 pF

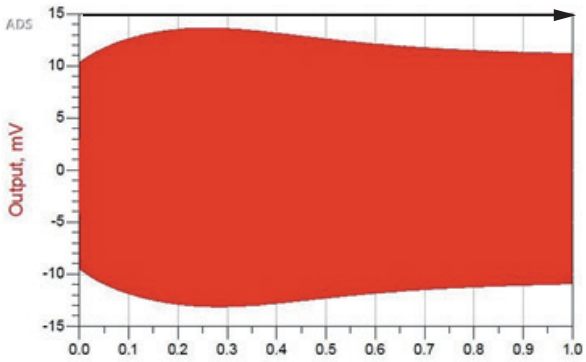
TECHNICAL OBSERVATION

Large output capacitor (**300 pF**) results in smoother power profile. Spectral output remains clean and monotonic — ideal for FMCW radar.

Control Voltage : 2.0 - 3.4 V

VCO Tuning Curve
(Vctrl–Frequency Response)

Reverse Chirp-Frequency Decreases Over Time



Ramp Input :
1MHz, 2.6 - 3.2V

Time-Domain
Simulation Result

Chirp Output
(Time Domain)

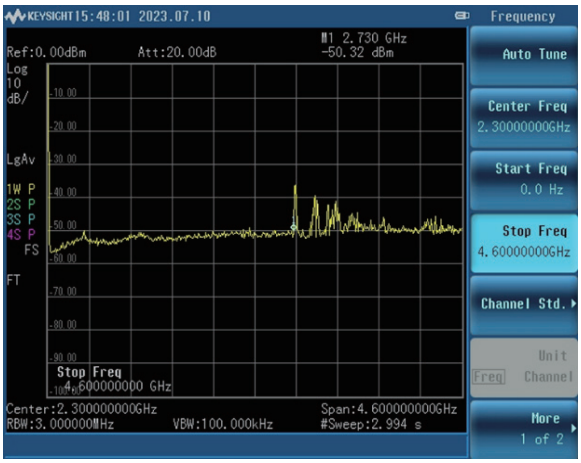
CONCLUSIONS

These results confirm the VCO's **wide tuning capability** and **power stability**, demonstrating its suitability for **clean, wideband** chirp generation in analog radar systems.

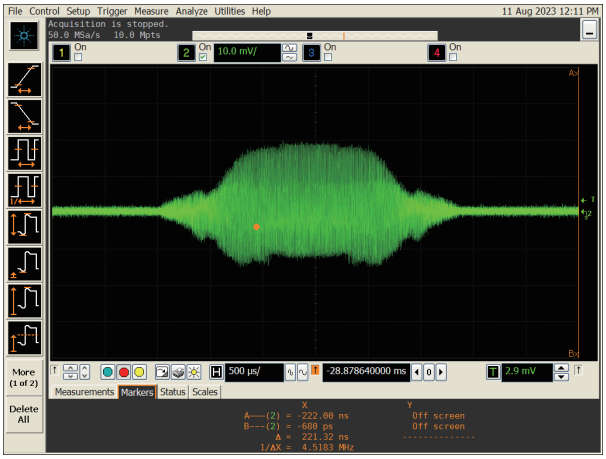
Measurement Results & Literature Comparison

MEASUREMENT SUMMARY

1. **Applied** ramp voltage (2.6 – 3.2 V @ 1 MHz) from PCB
2. **Measured** chirp output in **3.0 – 3.5 GHz range**
3. **Observed** power level of **–40 to –50 dBm**
4. **Matched** simulation result in bandwidth and waveform shape
5. **Verified** functional chirp generation using spectrum analyzer



Measured Spectrum Output
(3.0–3.5 GHz)



Time-Domain Output
(100 Hz Ramp)

This Design Outperforms Recent Cmos Chirp Generators In Both Bandwidth And Area Efficiency

Work	Technology	BW (Mhz)	Area (mm)	Center Freq (Ghz)
[1] APF (2020)	22 nm	140	0.25	0.08
[2] Mixer + VCO (2023)	65 nm	275	0.45	5.8
This Work	**0 . 1 8 µ m CMOS**	**500**	**0.122**	**3.25**

CONCLUSION HIGHLIGHT

These measurements confirm **successful** chirp generation with **clean spectrum** and **consistent bandwidth**, validating the full-custom analog design through both simulation and post-fabrication testing.

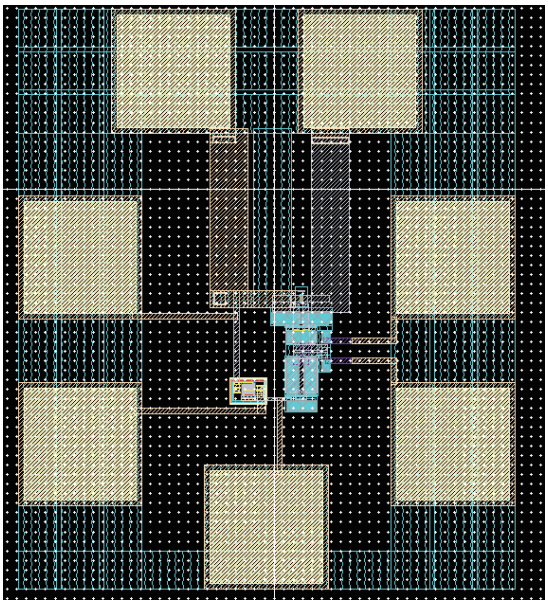
Layout & Hardware Implementation

LAYOUT SUMMARY

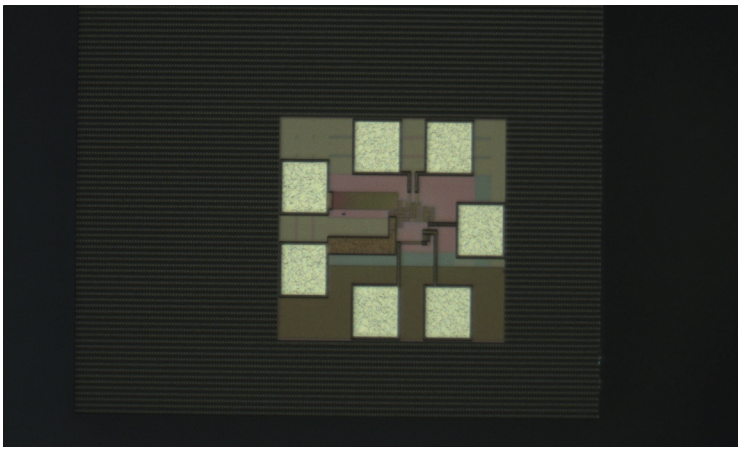
1. **Designed** full-custom LC-VCO in UMC 0.18 µm CMOS
2. **Integrated** active inductor, output buffer, and pad ring
3. **Achieved** compact layout : **0.122 mm**
4. **Verified** design via DRC, LVS, and post-layout simulation

HARDWARE INTEGRATION

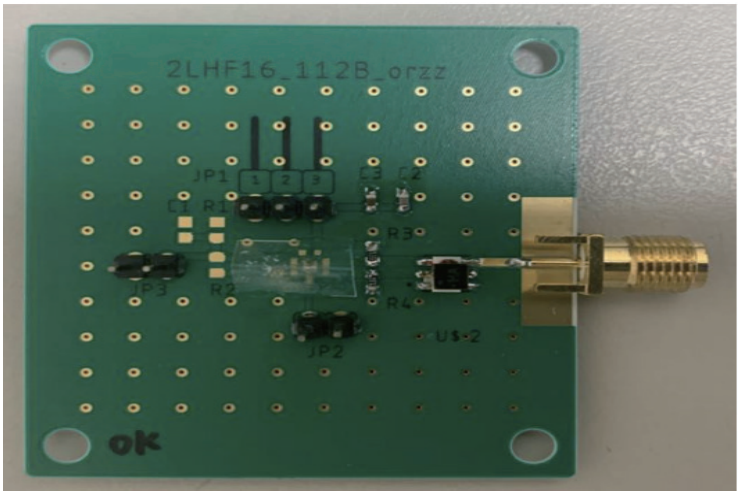
1. **Bonded** fabricated chip to RO4003C **PCB**
2. **Implemented** ramp control externally via PCB circuit
3. **Matched 50 Ω output** trace with SMA port for RF measurement



Full-Custom
Layout (0.122mm)



Fabricated Chip
(UMC 0.18µm CMOS)



Test PCB with Bonded
Chip (RO4003C)

Project Summary & References

This project presents a full-custom **analog chirp generator** based on an LC-VCO with a tunable active inductor, implemented in UMC 0.18 µm CMOS. From **schematic design** to **layout, tape-out,** and **hardware testing**, the complete system was validated through **simulation** and **measurement**.

SKILLS ACQUIRED

- Designed and verified wideband LC-VCO with active inductor
- Completed full-custom layout and physical verification
- Built high-frequency PCB and executed full-system measurement
- Acquired experience in **Cadence, ADS, PCB tools, and RF analysis**
- Conducted literature review and compared alternative VCO topologies, evaluating their advantages and limitations.
- Collaborated effectively to discuss technical challenges and implemented solutions through cross-functional communication.

FUTURE PLAN

I plan to pursue graduate research in analog and RF IC design, focusing on oscillator design, frequency synthesis, and mixed-signal systems.
I aim to further enhance my design skills and contribute to next-generation wireless and radar front-end technologies.

REFERENCES

[1] S. Kagita, S. George, and G. Fettweis, “Analog CMOS Non-Linear Chirp Generation Using All-Pass Filters,” IEEE MWSCAS, 2020.

[2] N. Naseh et al., “A Signal Generator and Down-Conversion Mixer for a 5.8-GHz FMCW Receiver,” IEEE RWS, 2023.

[3] B. Razavi, *Fundamentals of Microelectronics*, 2nd ed., Wiley, 2013.

[4] D. B. Leeson, “A simple model of feedback oscillator noise spectrum,” Proc. IEEE, vol. 54, no. 2, pp. 329–330, 1966.

“This work demonstrates competitive performance in bandwidth and area compared to recent CMOS-based chirp generation circuits.”