Equations for Exam #3

General:

$$\phi_F = \frac{kT}{q}\ln\frac{N_a}{n_i}$$

$$V_T = V_P - V_0, \quad V_0 = \frac{kT}{q}\ln\frac{N_a N_d}{n_i^2}$$

JFETs:

$$V_P = \frac{qa^2 N_d}{2\varepsilon}$$

$$|V_D(\text{sat.})| = |V_P| - |V_{GS}| - |V_0|$$

$$I_D = G_0 V_P\left[\frac{V_D}{V_P} + \tfrac{2}{3}\left(-\frac{V_G}{V_P}\right)^{\frac{3}{2}} - \tfrac{2}{3}\left(\frac{V_D - V_G}{V_P}\right)^{\frac{3}{2}}\right]$$

$$I_D(\text{sat.}) = G_0 V_P\left[\frac{V_D}{V_P} + \tfrac{2}{3}\left(-\frac{V_G}{V_P}\right)^{3/2} - \tfrac{2}{3}\right]$$

$$= G_0 V_P\left[\frac{V_G}{V_P} + \tfrac{2}{3}\left(-\frac{V_G}{V_P}\right)^{3/2} + \tfrac{1}{3}\right]$$

$$\frac{V_D}{V_P} = 1 + \frac{V_G}{V_P}$$

$$G_0 = 2aq\mu_n n\frac{Z}{L}$$

$$g_m(\text{sat.}) = G_0\left[1 - \left(-\frac{V_G}{V_P}\right)^{1/2}\right]$$

Metal-Semiconductor FET:

$$v_d = \frac{\mu\mathcal{E}}{1 + \mu\mathcal{E}/v_s}$$

$$I_D = qnv_s A = qN_d v_s Z h$$

Metal-Insulator-Semiconductor FET:

$$\phi_s(\text{inverted}) = 2\phi_F = 2\frac{kT}{q}\ln\frac{N_a}{n_i}$$

$$L_D = \sqrt{\frac{\epsilon_s kT}{q^2 p_0}}$$

$$V_i = \frac{-Q_s}{C_i}$$

$$W = \left[\frac{2\varepsilon_s\phi_s}{qN_a}\right]^{1/2}$$

$$W_m = 2\left[\frac{\epsilon_s\phi_F}{q^2 N_a}\right]^{1/2}$$

$$Q_d = -qN_a W_m = -2(\epsilon_s qN_a\phi_F)^{1/2}$$

$$C_i = \frac{\varepsilon_i}{d}, \quad C_d = \frac{\epsilon_s}{W}$$

$$C_{min} = \frac{C_i C_d}{C_i + C_d}$$

$$V_{FB} = \Phi_{ms} - \frac{Q_i}{C_i}$$

$$V_T = -\frac{Q_d}{C_i} + 2\phi_F = V_{FB} - \frac{Q_d}{C_i} + 2h_f$$

$$= \Phi_{ms} - \frac{Q_i}{C_i} - \frac{Q_d}{C_i} + 2\phi_F$$

$$V_T = \left|\begin{array}{c|c|c|c} \Phi_{ms} & -\dfrac{Q_i}{C_i} & -\dfrac{Q_d}{C_i} & +2\phi_F \\ (-) & (-) & \begin{array}{c}(+)\text{ n channel}\\(-)\text{ p channel}\end{array} & \begin{array}{c}(+)\text{ n channel}\\(-)\text{ p channel}\end{array}\end{array}\right.$$

$$V_D(\text{sat.}) \approx V_G - V_T$$

$$C_{debye} = \frac{\varepsilon_s}{L_D}$$

$$D_{it} = \tfrac{1}{q}\left(\frac{C_i C_{LF}}{Ci - C_{LF}} - \frac{C_i C_{HF}}{C_i - C_{HF}}\right)\text{cm}^{-2}\text{eV}^{-1}$$

MOSFET:

$$Q_s = Q_n + Q_d$$

$$Q_n = -C_i\left[V_G - \left(V_{FB} + \phi_s - \frac{Q_d}{C_i}\right)\right]$$

$$V_G = V_{FB} - \frac{Q_s}{C_i} + \phi_s$$

$$V_D(\text{sat.}) = |V_G| - |V_T|$$

$$I_D = \frac{\overline{\mu_n} Z C_i}{L}\left[(V_G - V_T)V_D - \tfrac{1}{2}V_D^2\right]$$

$$g = g_m(\text{sat.}) \approx \frac{Z}{L}\overline{\mu_n} C_i\,(V_G - V_T)$$

$$I_D(\text{sat.}) \approx \tfrac{1}{2}\overline{\mu_n} C_i\frac{Z}{L}(V_G - V_T)^2 = \frac{Z}{2L}\overline{\mu_n} C_i V_D^2(\text{sat.})$$

$$I_D = \frac{\overline{\mu_n} Z C_i}{L\{1 + \theta(V_G - V_T)\}}\left[(V_G - V_T)V_D - \tfrac{1}{2}V_D^2\right]$$

$$I_D = \frac{\overline{\mu_n} Z C_i}{L}\left\{(V_G - V_{FB} - 2\phi_F - \frac{1}{2}V_D)V_D - \frac{2}{3}\frac{\sqrt{2\epsilon_s qN_a}}{C_i}[(V_D + 2\phi_F)^{3/2} - (2\phi_F)^{3/2}]\right\}$$

$v = \mu\mathcal{E}$ for $\mathcal{E} < \mathcal{E}_{sat}$
and $v = v_s$ for $\mathcal{E} > \mathcal{E}_{sat}$

Short Channel Characteristics:

$$I_D(\text{sat.}) \approx ZC_i(V_G - V_T)v_s$$

$$\approx \left\{\frac{1-r}{1+r}\right\} ZC_i(V_G - V_T)v_{inj}$$

Subthreshold Characteristics:

$$I_D = \mu(C_d + C_{it})\frac{Z}{L}\left(\frac{kT}{q}\right)^2\left(1 - e^{\frac{-qV_n}{kT}}\right)\left(e^{\frac{q(V_G - V_T)}{c_r kT}}\right)$$

$$c_r = \left[1 + \frac{C_d + C_{it}}{C_i}\right]$$

Drain Induced Barrier Lowering:

$$I_D = \frac{Z}{2L}\overline{\mu_n} C_i\,(V_G - V_T)^2\,(1 + \lambda V_D)$$

Constants:

$q = 1.6 \times 10^{-19}$C
$\epsilon_0 = 8.85 \times 10^{-14}$ Fm^{-1}, $\epsilon_{r_{Si}} = 11.8$
$\epsilon_r(SiO_2) = 3.9$
$h = 6.626 \times 10^{-34}$ m^{2}kg/s, $\quad \hbar = 1.055 \times 10^{-31}$ Js/rad
$m^* = 9.11 \times 10^{-31}$ kg
$kT|_{T=300K} \approx 0.026$ eV
$n_i(Si)|_{300K} = 1.5 \times 10^{10}$ cm^{-3}
v_{th} = Thermal Velocity $\approx 10^7$ cm/sec
$\vec{\varepsilon_c}$ = critical field $= 10^4$ V/cm

Old Figures

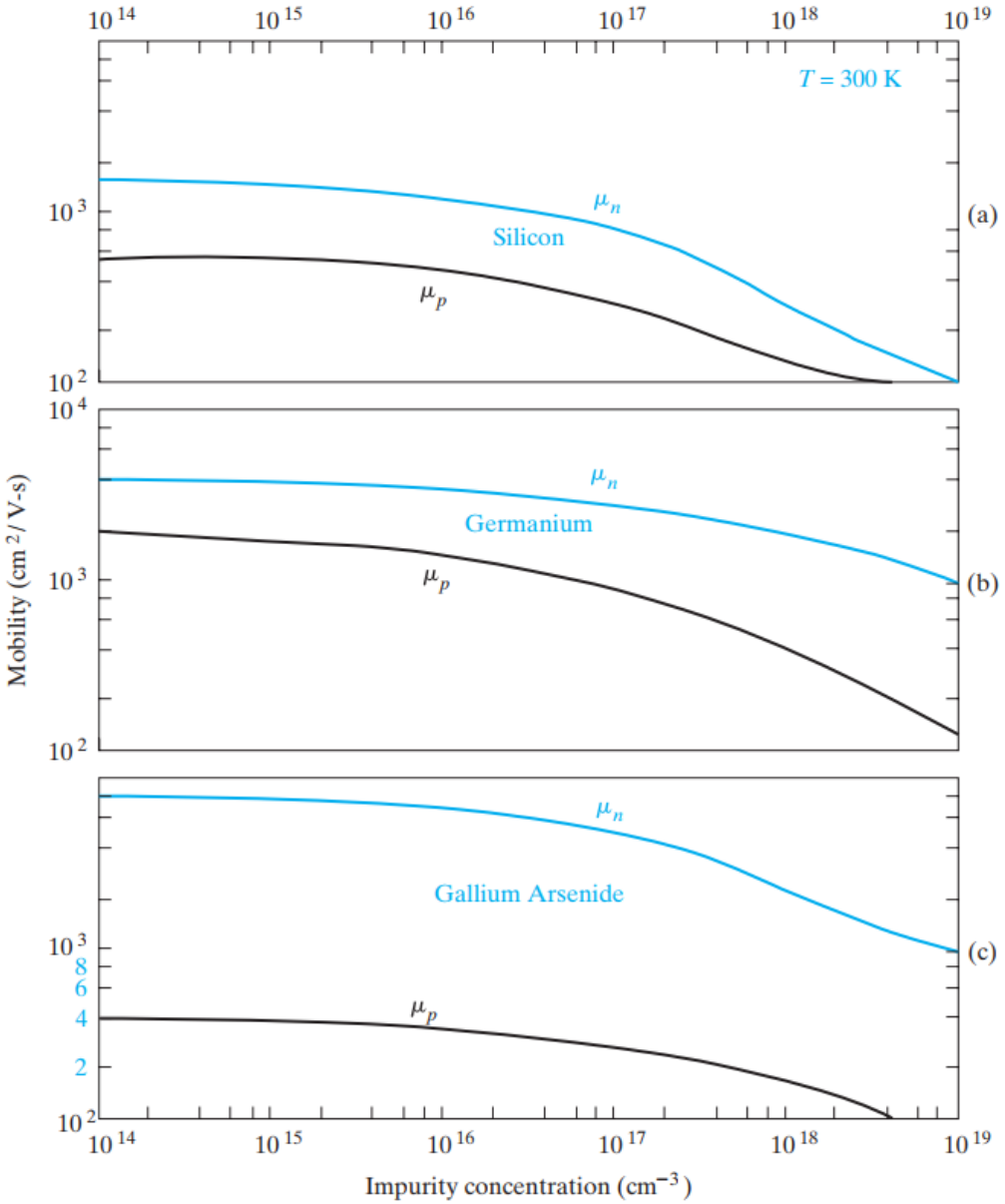
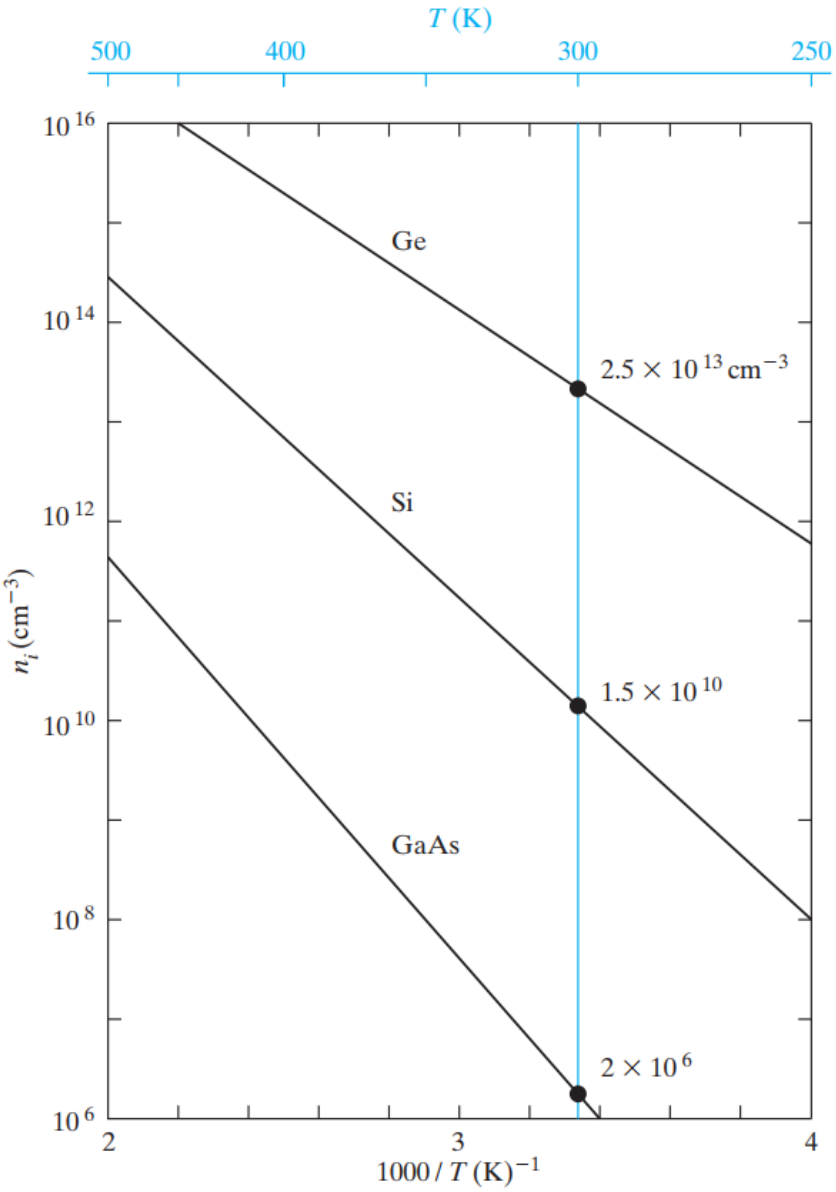
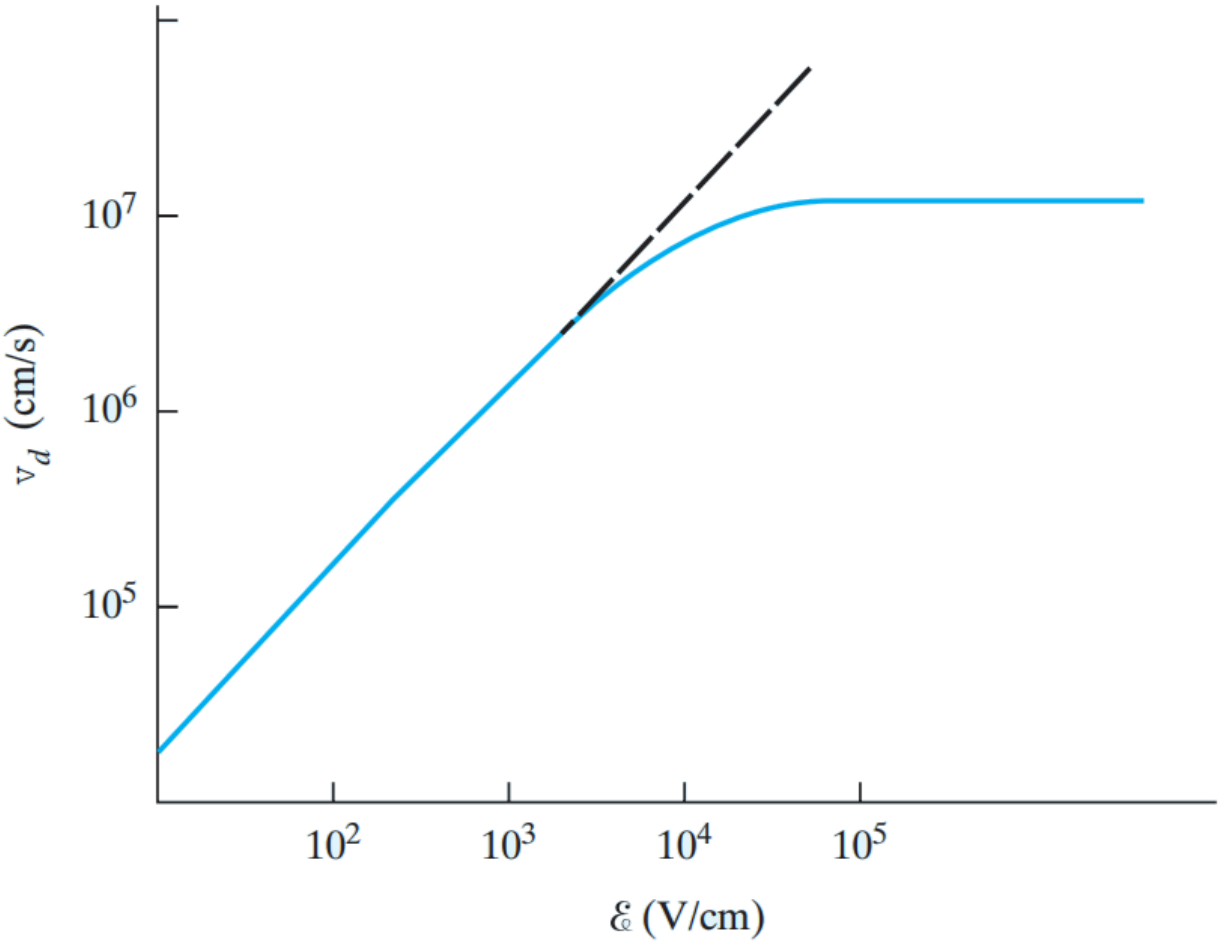


Figure 3–23
Variation of mobility with total doping impurity concentration ($N_a + N_d$) for Ge, Si, and GaAs at 300 K.

Figure 3–17
Intrinsic carrier concentration for Ge, Si, and GaAs as a function of inverse temperature. The room temperature values are marked for reference.





Transistor Operation

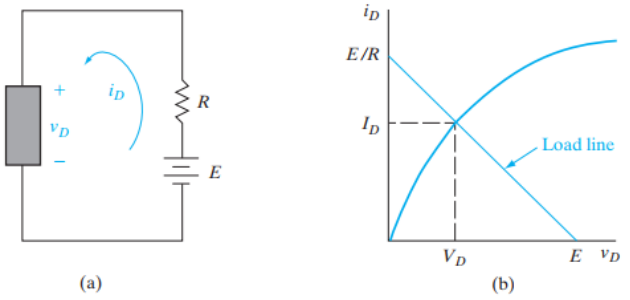


Figure 6–1
A two-terminal nonlinear device: (a) biasing circuit; (b) *I–V* characteristic and load line.

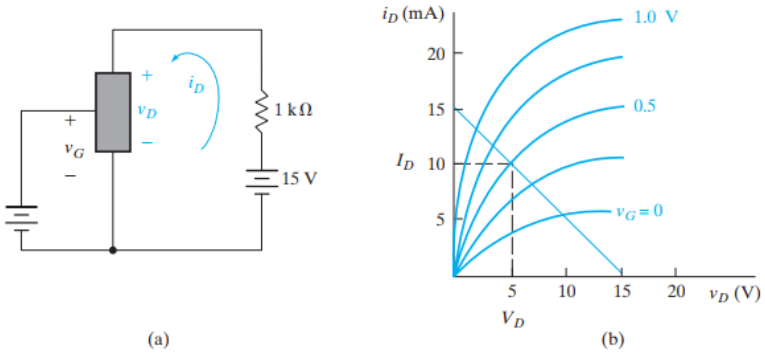


Figure 6–2
A three-terminal nonlinear device that can be controlled by the voltage at the third terminal v_G: (a) biasing circuit; (b) *I–V* characteristic and load line. If $V_G = 0.5$ V, the d-c values of I_D and V_D are as shown by the dashed lines.

The Junction FET

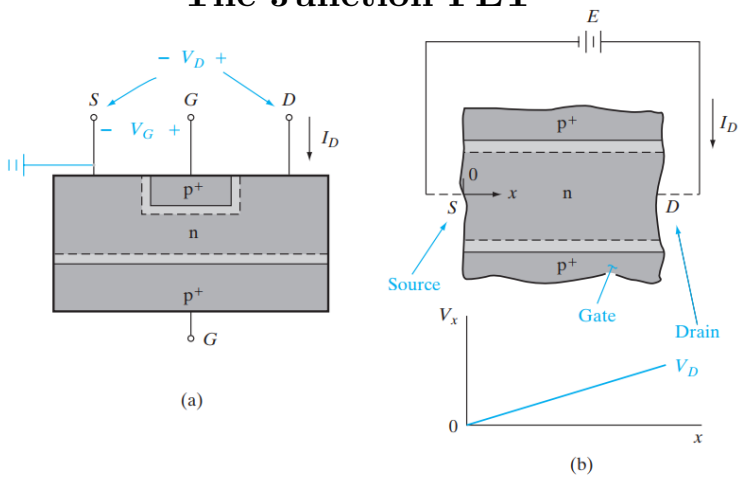


Figure 6–3
Simplified cross-sectional view of a junction FET: (a) transistor geometry; (b) detail of the channel and voltage variation along the channel with $V_G = 0$ and small I_D.

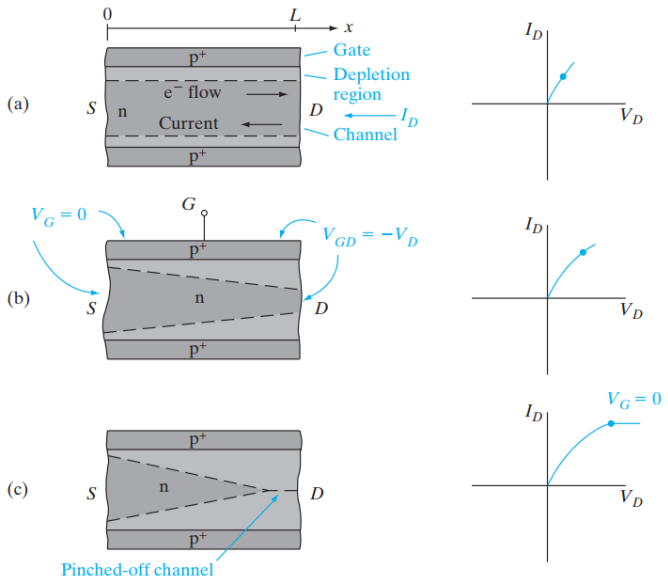


Figure 6–4
Depletion regions in the channel of a JFET with zero gate bias for several values of V_D: (a) linear range; (b) near pinch-off; (c) beyond pinch-off.

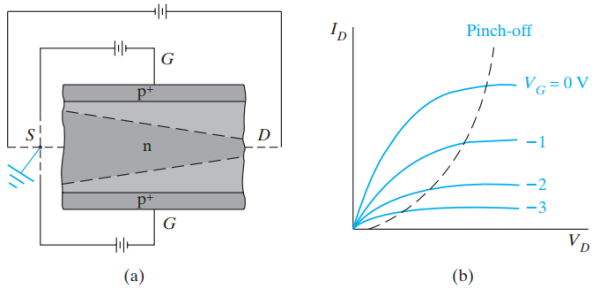


Figure 6–5
Effects of a negative gate bias: (a) increase of depletion region widths with V_G negative; (b) family of current–voltage curves for the channels as V_G is varied.

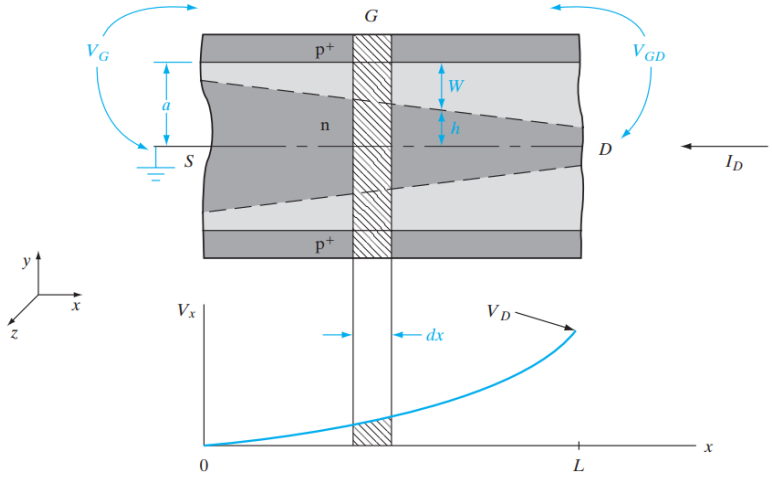


Figure 6–6
Simplified diagram of the channel with definitions of dimensions and differential volume for calculations.

The Metal-Semiconductor FET

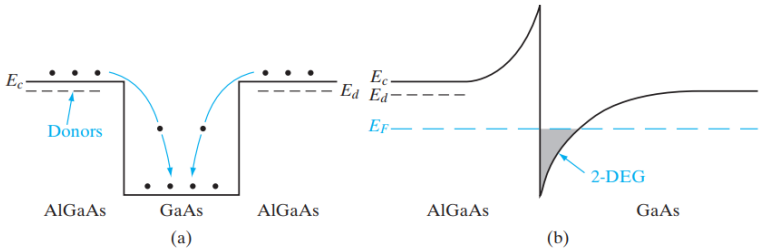


Figure 6–8
(a) Simplified view of modulation doping, showing only the conduction band. Electrons in the donor-doped AlGaAs fall into the GaAs potential well and become trapped. As a result, the undoped GaAs becomes n type, without the scattering by ionized donors which is typical of bulk n-type material. (b) Use of a single AlGaAs/GaAs heterojunction to trap electrons in the undoped GaAs. The thin sheet of charge due to free electrons at the interface forms a two-dimensional electron gas (2-DEG), which can be exploited in HEMT devices.

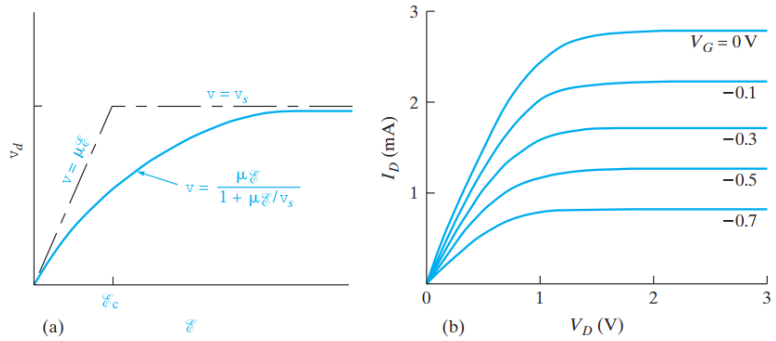


Figure 6–9
Effects of electron velocity saturation at high electric fields: (a) approximations to the saturation of drift velocity with increasing field; (b) drain current–voltage characteristics for the saturated velocity case, showing almost equally spaced curves with increasing gate voltage.

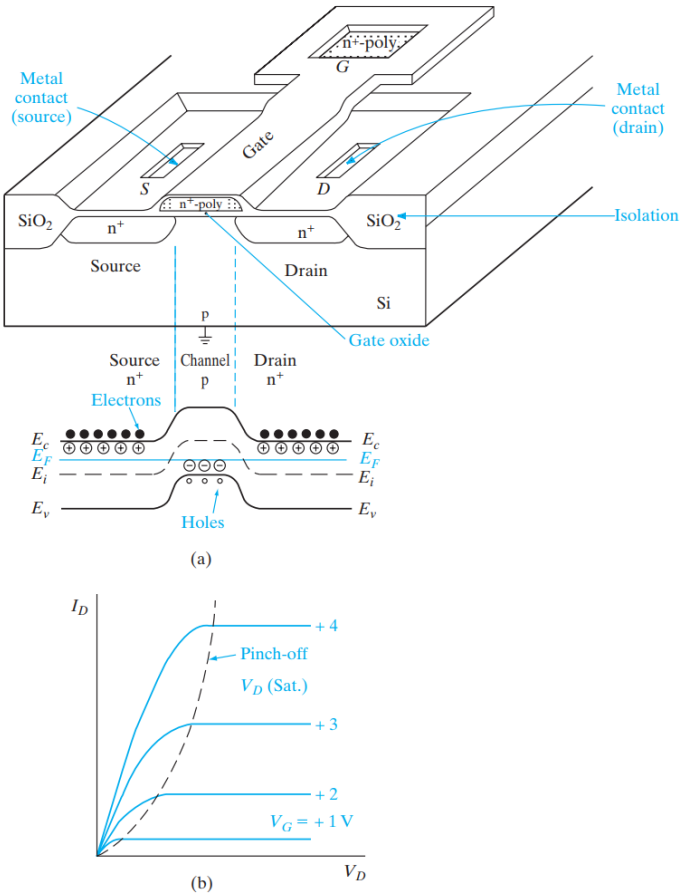


Figure 6–10
An enhancement-type n-channel MOSFET: (a) isometric view of device and equilibrium band diagram along channel; (b) drain current–voltage output characteristics as a function of gate voltage.

The Metal-Insulator-Semiconductor FET

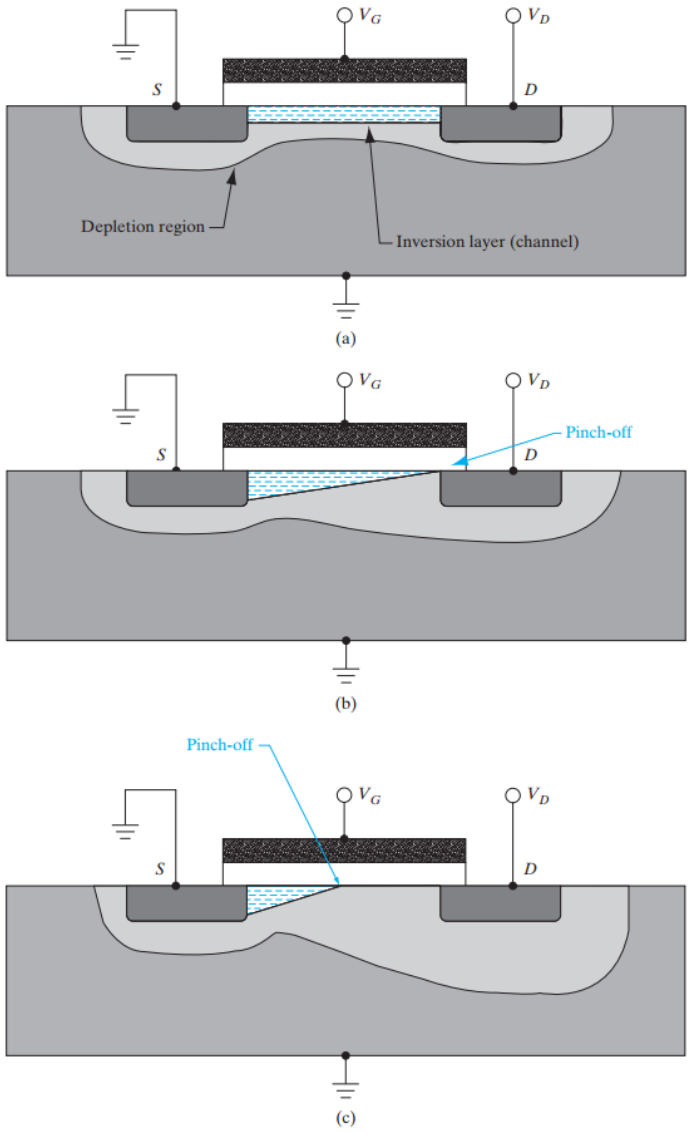


Figure 6–11
n-channel MOSFET cross sections under different operating conditions: (a) linear region for $V_G > V_T$ and $V_D < (V_G - V_T)$; (b) onset of saturation at pinch-off, $V_G > V_T$ and $V_D = (V_G - V_T)$; (c) strong saturation, $V_G > V_T$ and $V_D > (V_G - V_T)$.

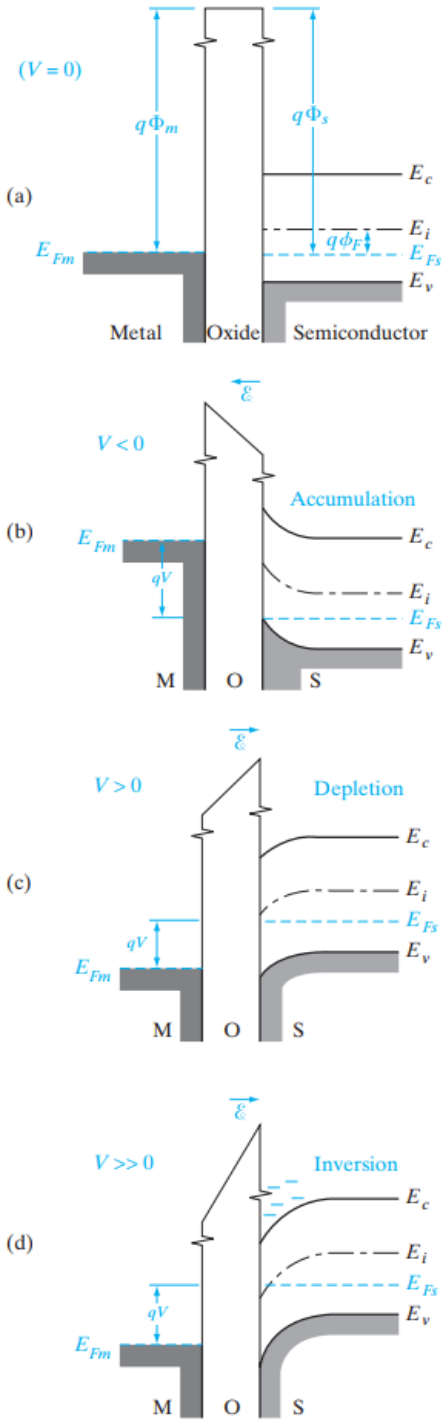


Figure 6–12
Band diagram for the ideal MOS structure at: (a) equilibrium; (b) negative voltage causes hole accumulation in the p-type semiconductor; (c) positive voltage depletes holes from the semiconductor surface; (d) a larger positive voltage causes inversion—an "n-type" layer at the semiconductor surface.

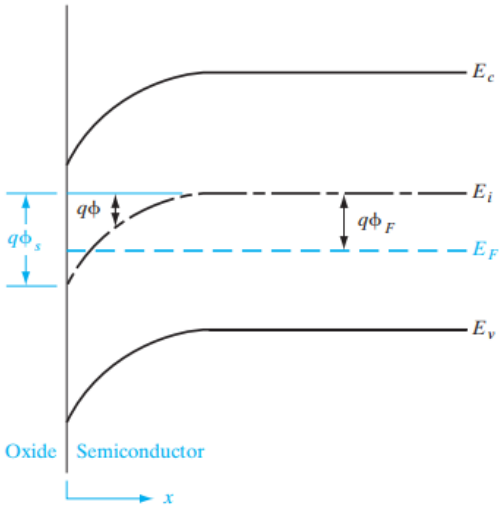


Figure 6–13
Bending of the semiconductor bands at the onset of strong inversion: The surface potential ϕ_s is twice the value of ϕ_F in the neutral p material.

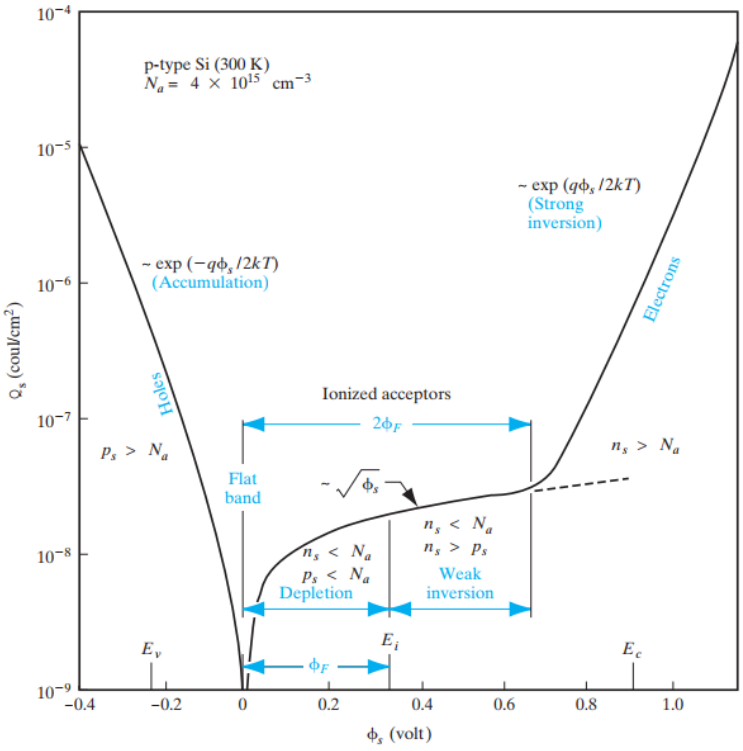


Figure 6–14
Variation of space-charge density in the semiconductor as a function of the surface potential ϕ_s for p-type silicon with $N_a = 4 \times 10^{15}$ cm^{-3} at room temperature. p_s and n_s are the hole and electron concentrations at the surface, ϕ_F is the potential difference between the Fermi level and the intrinsic level of the bulk. (Garrett and Brattain, Phys. Rev., 99, 376 (1955).)

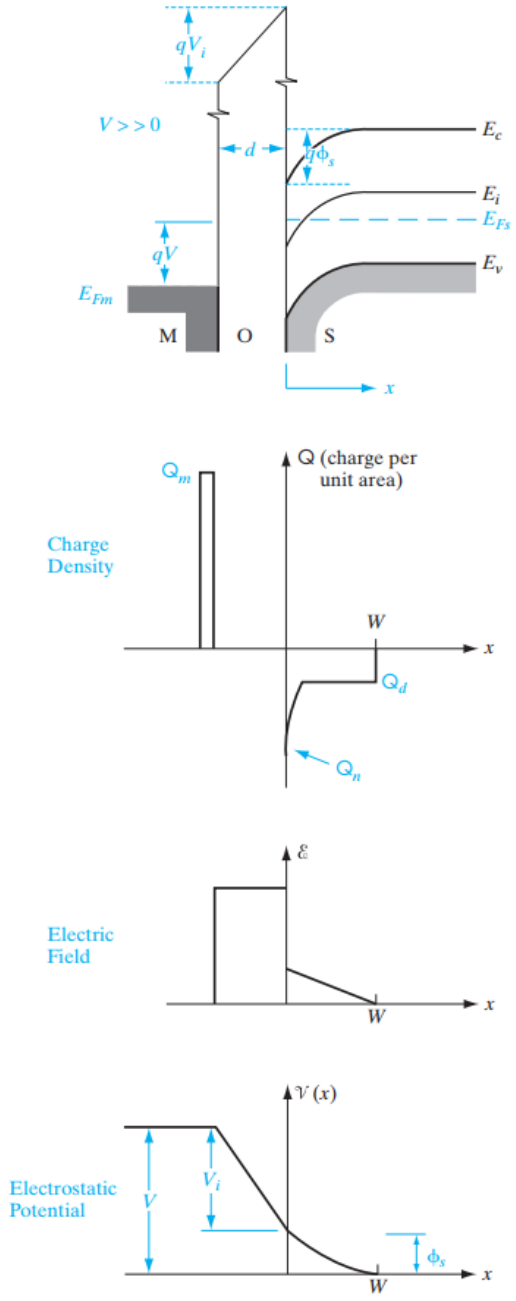


Figure 6–15
Approximate distributions of charge, electric field, and electrostatic potential in the ideal MOS capacitor in inversion. The relative width of the inverted region is exaggerated for illustrative purposes, but is neglected in the field and potential diagrams. The slopes of the band edges reflect the electric fields in the gate dielectric and the semiconductor channel. The product of the perpendicular electric field and dielectric constant (known as the displacement) is continuous across the dielectric–semiconductor interface if there are no charges at the interface, according to Maxwell's boundary conditions.

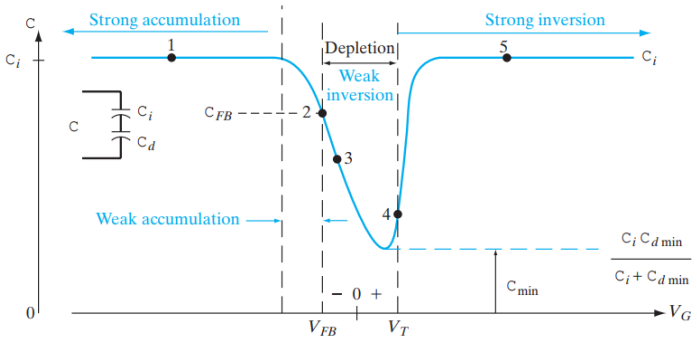


Figure 6–16
Capacitance–voltage relation for an n-channel (p-substrate) MOS capacitor. The dashed curve for $V > V_T$ is observed at high measurement frequencies. The flat band voltage V_{FB} will be discussed in Section 6.4.3. When the semiconductor is in depletion, the semiconductor capacitance C_s is denoted as C_d.

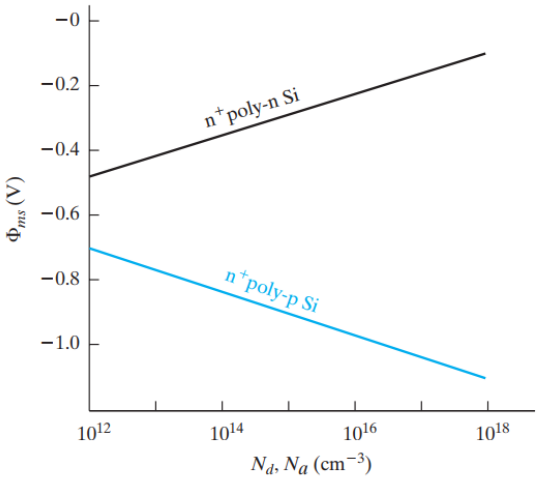
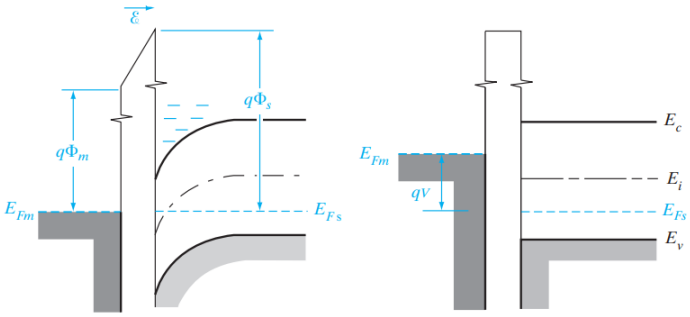


Figure 6–17
Variation of the metal–semiconductor work function potential difference Φ_{ms} with substrate doping concentration, for n^+ poly-Si.

Figure 6–18
Effect of a negative work function difference ($\Phi_{ms} < 0$): (a) band bending and formation of negative charge at the semiconductor surface; (b) achievement of the flat band condition by application of a negative voltage.



(a) Equilibrium
$V = 0$

(b) Flat band
$V = V_{FB} = \Phi_{ms}$

Figure 6–19
Effects of charges in the oxide and at the interface: (a) definitions of charge densities (C/cm^2) due to various sources; (b) representing these charges as an equivalent sheet of positive charge Q_i at the oxide–semiconductor interface. This positive charge induces an equivalent negative charge in the semiconductor, which requires a negative gate voltage to achieve the flat band condition.

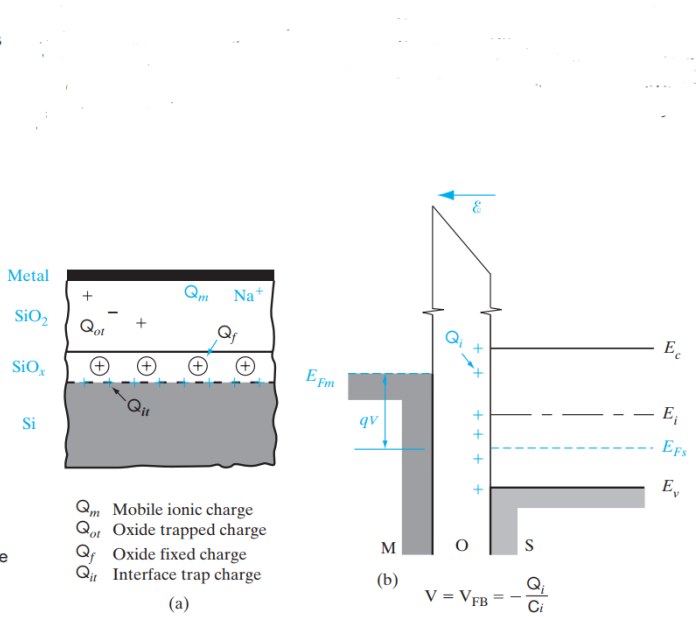


Figure 6–20
Influence of materials parameters on threshold voltage: (a) the threshold voltage equation indicating signs of the various contributions; (b) variation of V_T with substrate doping for n-channel and p-channel n^+ poly-SiO_2–Si devices.

(a)

$V_T =$	Φ_{ms}	$-\frac{Q_i}{C_i}$	$-\frac{Q_d}{C_i}$	$+ 2\phi_F$
	(−)	(−)	(+) n channel (−) p channel	(+) n channel (−) p channel

(b)

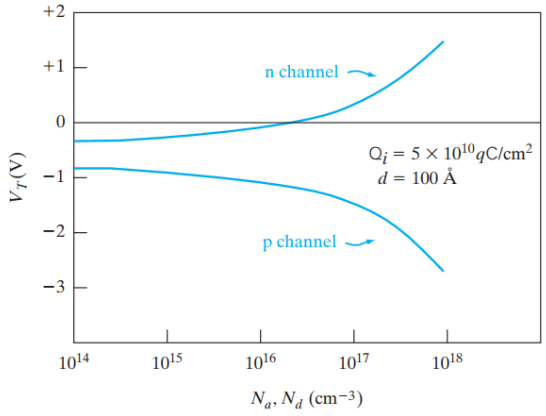
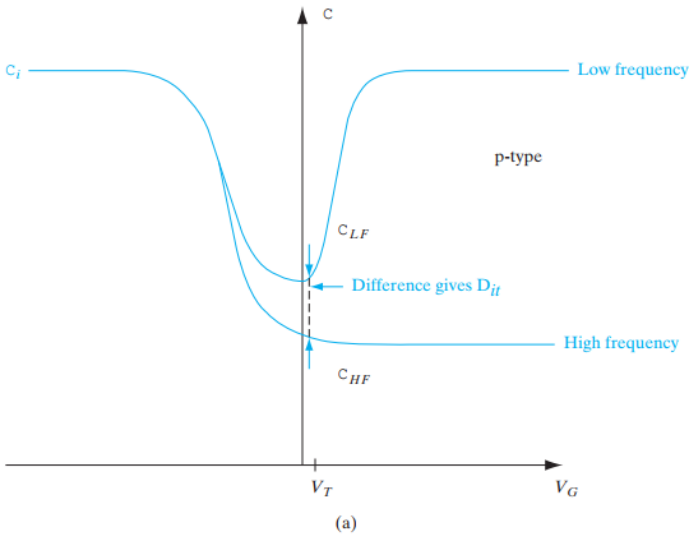
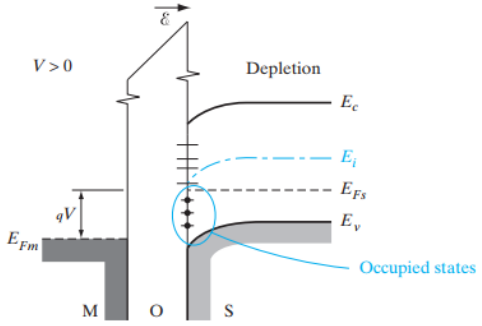


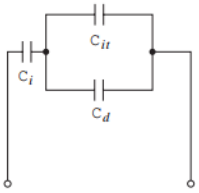
Figure 6–21
Fast interface state determination: (a) High-frequency and low-frequency *C–V* curves showing impact of fast interface states; (b) energy levels in the band gap due to fast interface states; (c) equivalent circuit of MOS structure showing capacitance components due to gate oxide (C_i), depletion layer in the channel (C_d), and fast interface states (C_{it}).



(a)



(b)



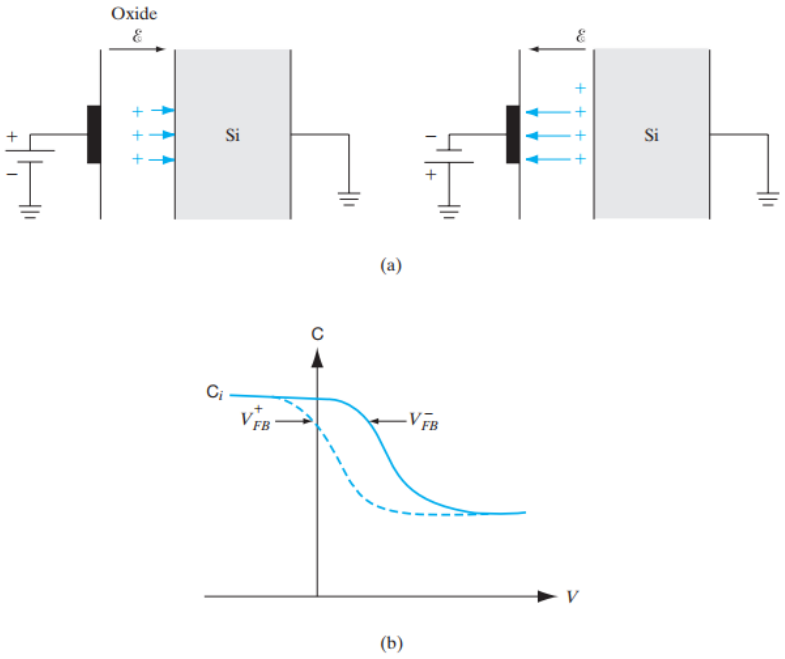


Figure 6–22
Mobile ion determination: (a) movement of mobile ions due to positive and negative bias-temperature stress; (b) C–V characteristics under positive (dashed line) and negative (solid line) bias-temperature.

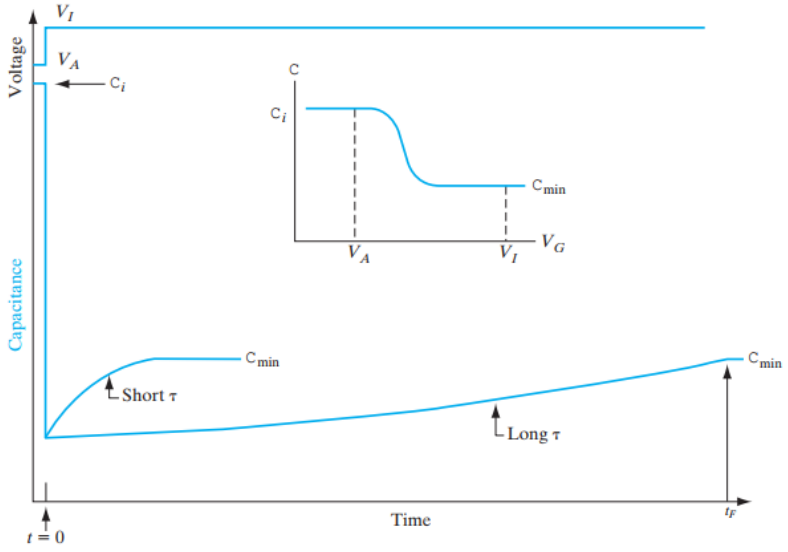


Figure 6–23
Time-dependent MOS capacitance (C_{HF}) due to the application of a step voltage V_A (which puts the capacitor in accumulation) to V_I (which puts the capacitor in inversion).

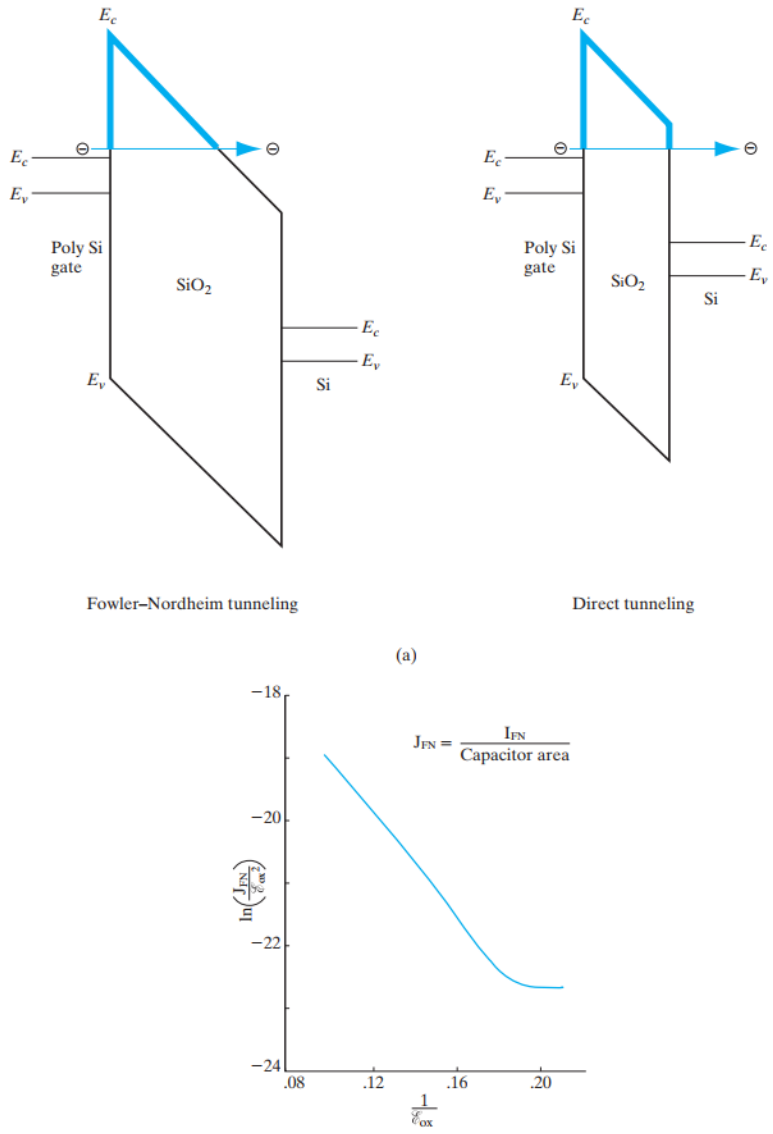


Figure 6–24
Current–voltage characteristics of gate oxides: (a) Fowler–Nordheim and direct tunneling through thin gate oxides; (b) plot of Fowler–Nordheim tunneling leakage current as a function of electric field across the oxide.

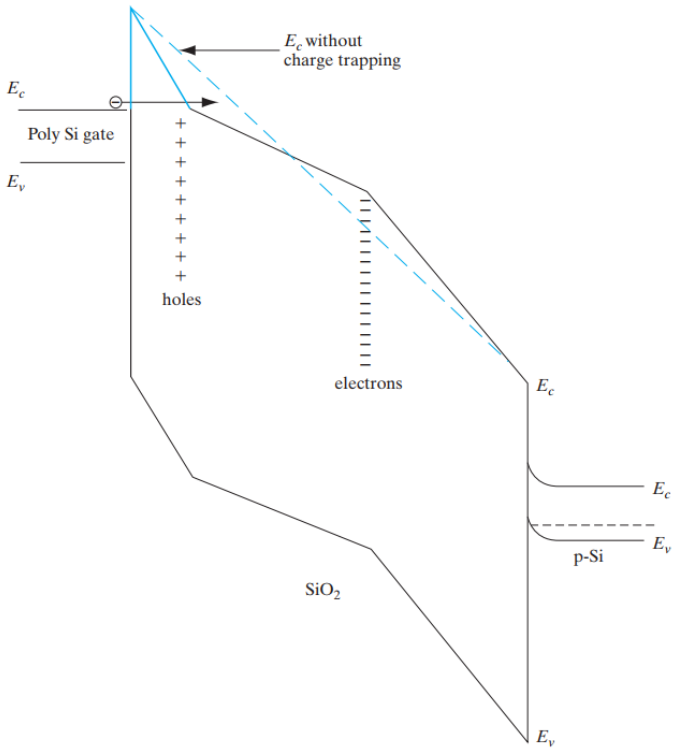


Figure 6–25
Time-dependent dielectric breakdown of oxides: Band diagram of a MOS device showing the band edges in the polysilicon gate, oxide, and Si substrate. Trapped holes and electrons in the oxide distort the band edges, and increase the electric field in the oxide near the gate. The tunneling barrier width is seen to be less than if there were no charge trapping (dashed line).

The MOS Field-Effect Transistor

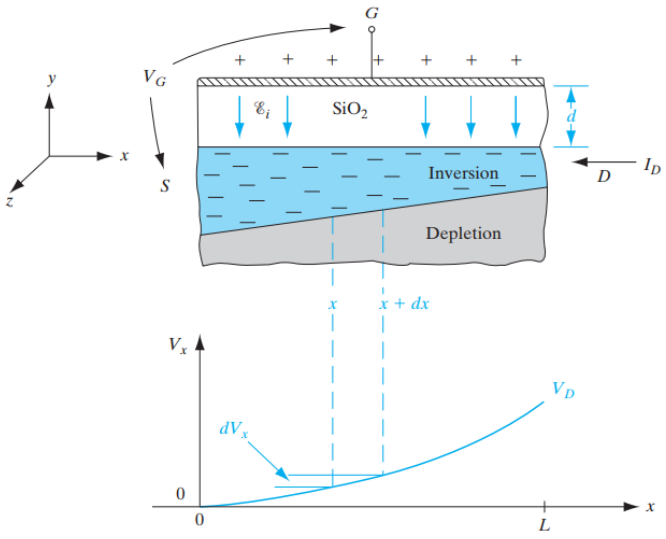


Figure 6–26
Schematic view of the n-channel region of a MOS transistor under bias below pinch-off, and the variation of voltage V_x along the conducting channel.

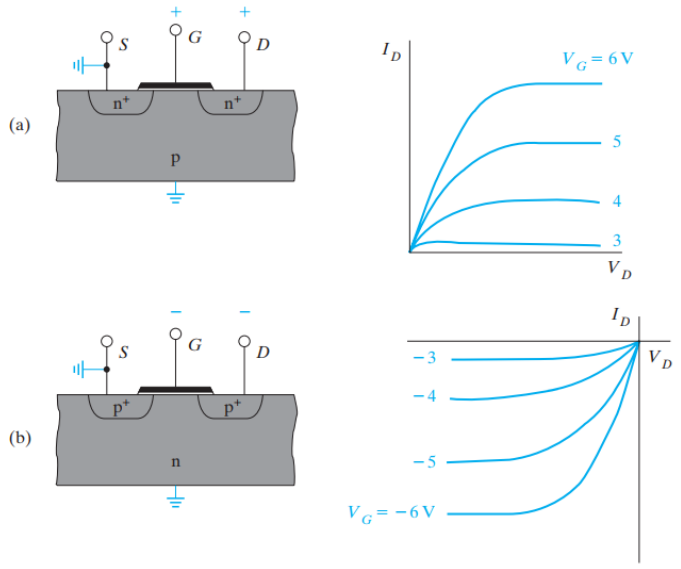


Figure 6–27
Drain current–voltage characteristics for enhancement transistors: (a) for n-channel V_D, V_G, V_T, and I_D are positive; (b) for p-channel all these quantities are negative.

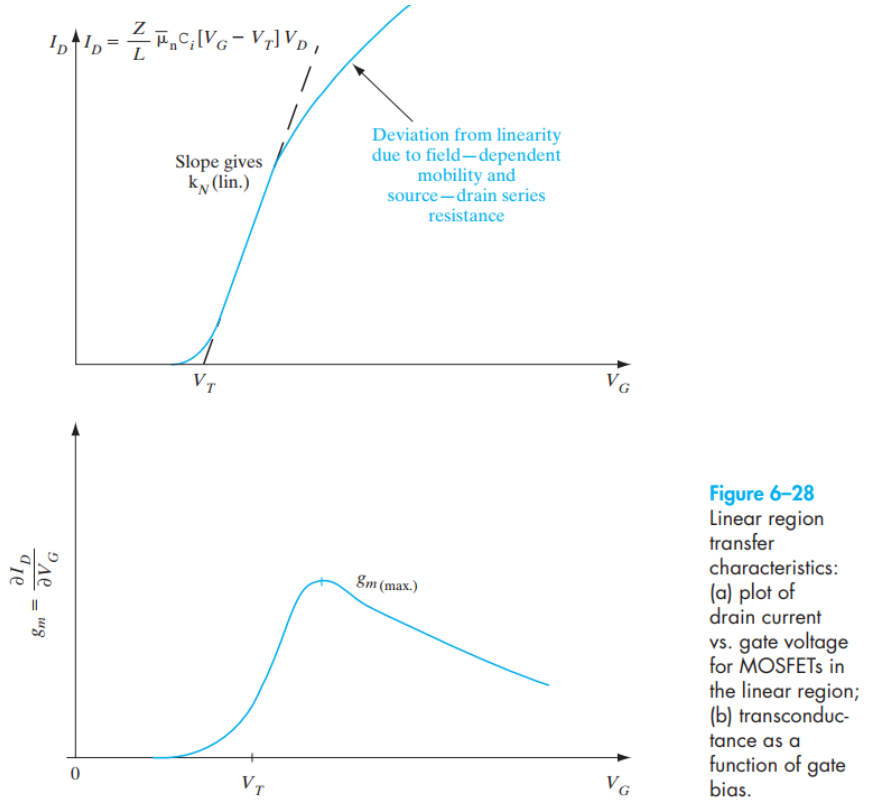


Figure 6–28
Linear region transfer characteristics: (a) plot of drain current vs. gate voltage for MOSFETs in the linear region; (b) transconductance as a function of gate bias.

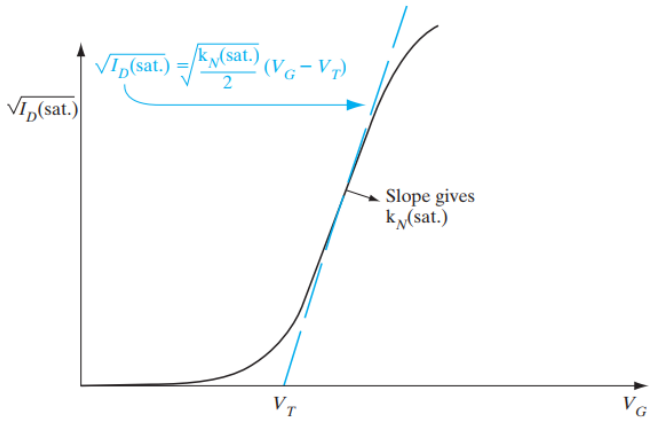


Figure 6–29
Saturation region transfer characteristics: plot of square root of the drain current vs. gate voltage for MOSFETs.

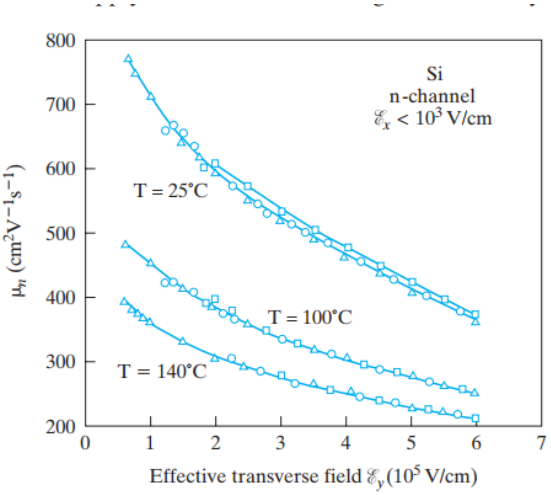


Figure 6–30
Inversion layer electron mobility vs. effective transverse field, at various temperatures. The triangles, circles, and squares refer to different MOSFETs with different gate oxide thicknesses and channel dopings. (After Sabnis and Clemens, *IEEE IEDM*, 1979.)

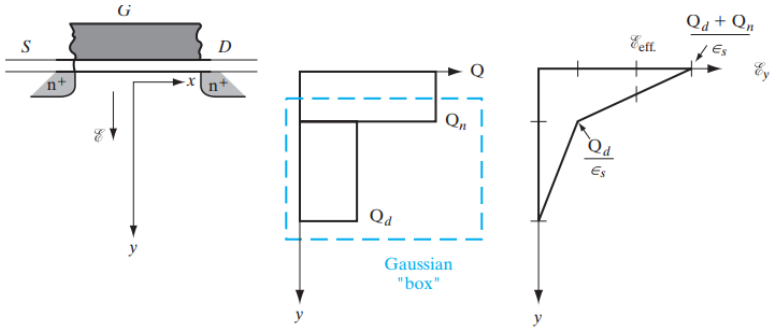


Figure 6–31
Determination of effective transverse field. Idealized charge distribution and transverse electric field in the inversion layer and depletion layer, as a function of depth in the channel of a MOSFET. The region to which we apply Gauss's law is shown in color.

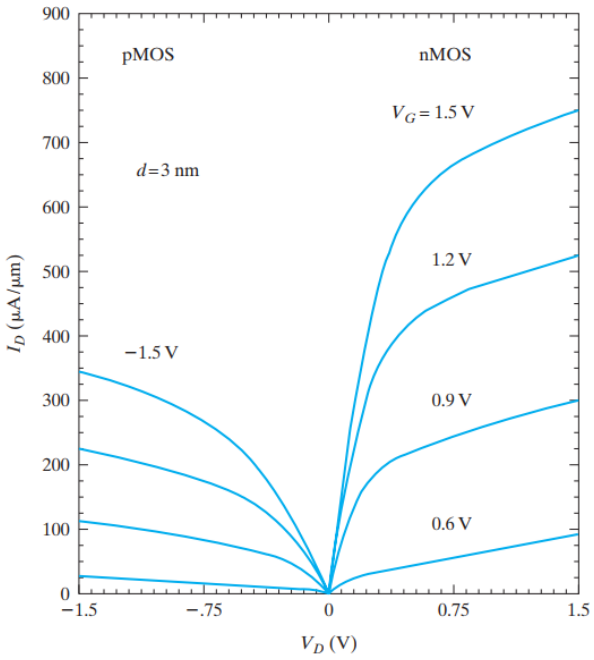


Figure 6–32
Experimental output characteristics of n-channel and p-channel MOSFETs with 0.1-μm channel lengths. The curves exhibit almost equal spacing, indicating a linear dependence of I_D on V_G, rather than a quadratic dependence. We also see that I_D is not constant but increases somewhat with V_D in the saturation region. The p-channel devices have lower currents because hole mobilities are lower than electron mobilities.

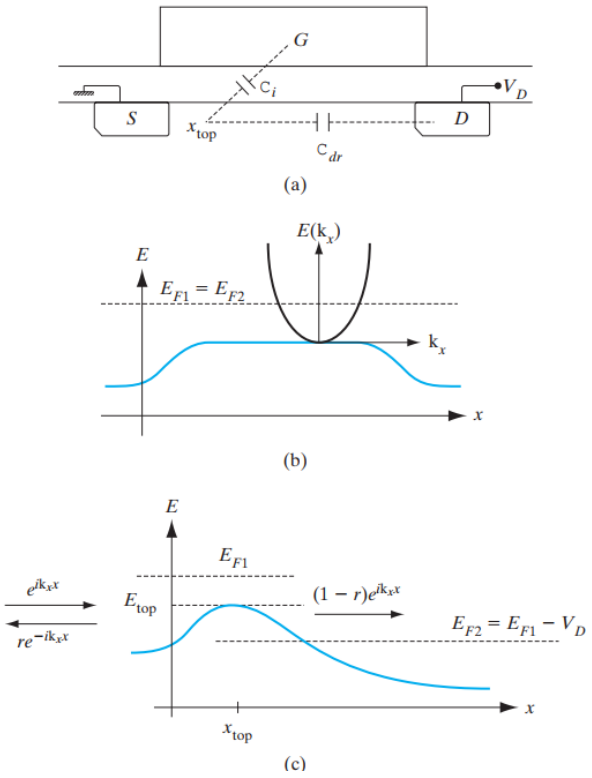


Figure 6–33
(a) Source-injection-limited quasi-ballistic MOSFET. The gate capacitance and drain-to-channel capacitance compete from control of the potential barrier near the source end of the channel at x_{top}. (b) Channel potential profile for MOSFET in equilibrium, and superimposed parabolic $E(k)$ band structure; (c) Channel potential profile with drain at V_D showing partial transmission of electron waves over "top of barrier."

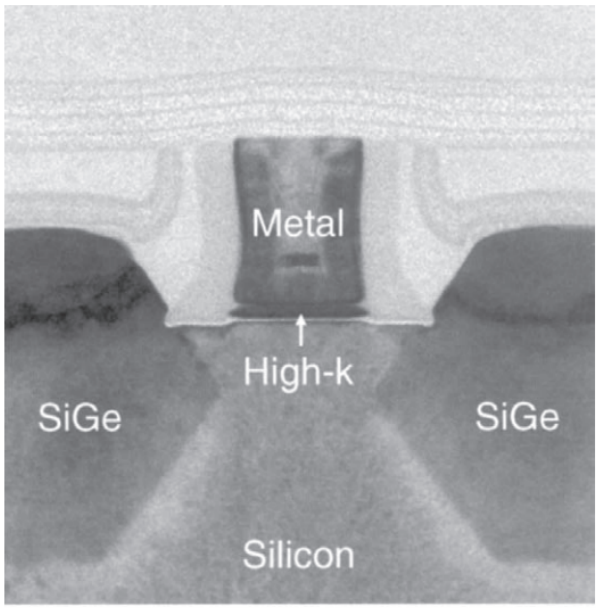


Figure 6–34
Cross section of a MOSFET. This high resolution transmission electron micrograph of a silicon Metal–Oxide Semiconductor Field Effect Transistor shows the silicon channel and metal gate separated by a thin silicon high-k gate dielectric. This 45nm PMOS metal gate transistor was made using gate-last or replacement metal gate process flow. (Photograph courtesy of Intel.)

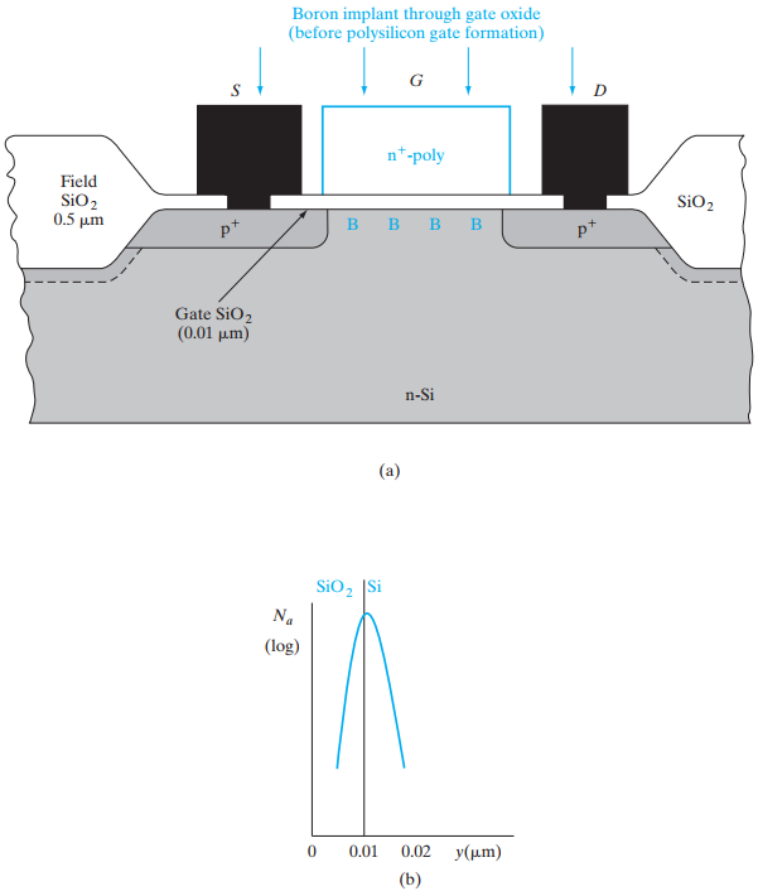


Figure 6–35
Thin oxide in the gate region and thick oxide in the field between transistors for V_T control (not to scale).

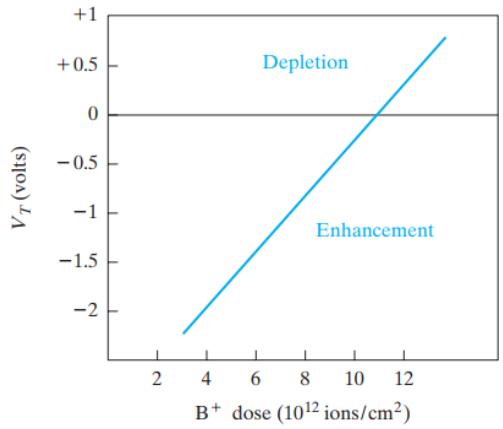


Figure 6–36
Typical variation of V_T for a p-channel device with increased implanted boron dose. The originally enhancement p-channel transistor becomes a depletion-mode device ($V_T > 0$) by sufficient B implantation.

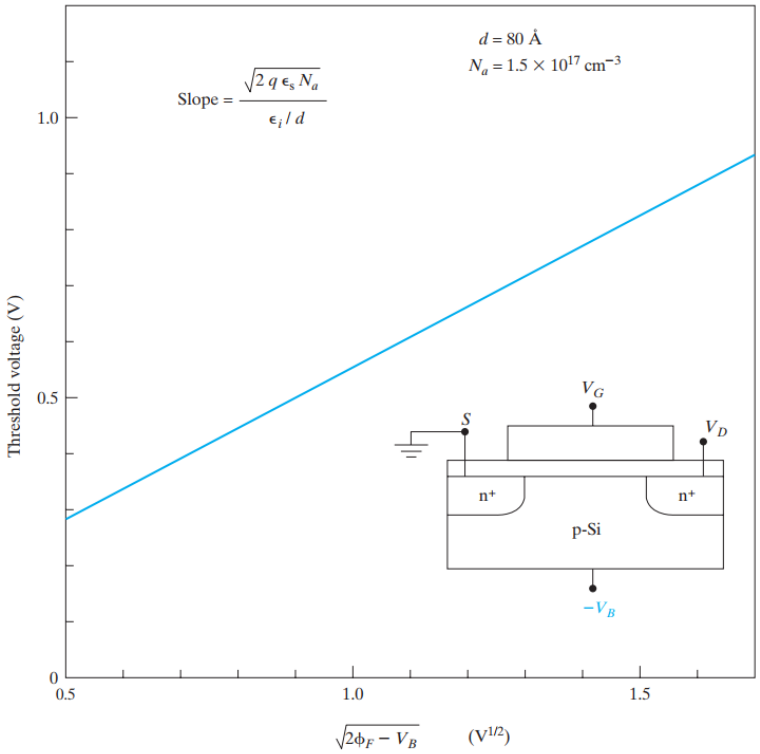


Figure 6–37
Threshold voltage dependence on substrate bias resulting from application of a voltage V_B from the substrate (i.e., bulk) to the source. For n channel, V_B must be zero or negative to avoid forward bias of the source junction. For p channel, V_B must be zero or positive.

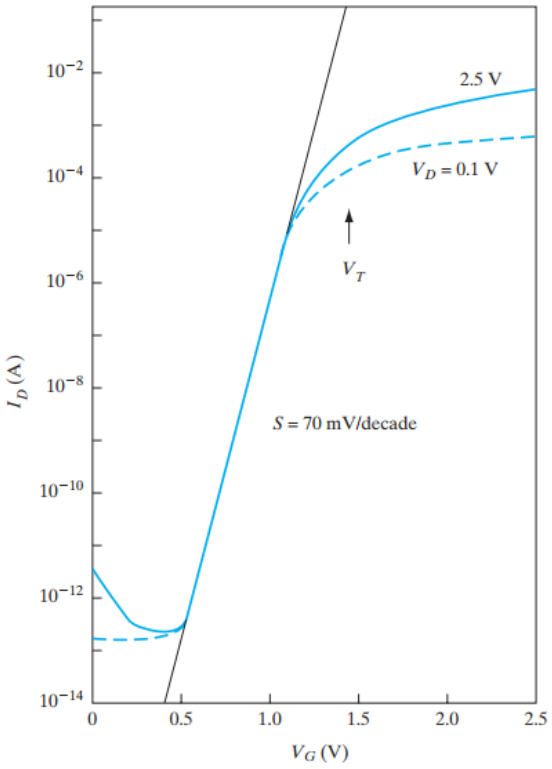


Figure 6–38
Subthreshold conduction in MOSFETs: (a) semilog plot of I_D vs. V_G; (b) equivalent circuit showing capacitor divider which determines subthreshold slope.

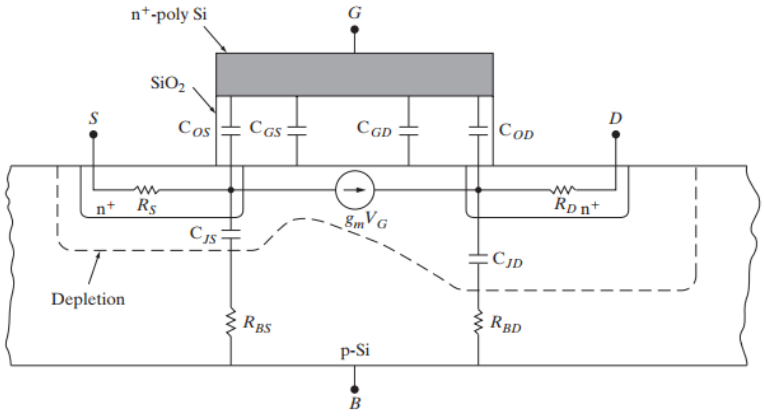


Figure 6–39
Equivalent circuit of a MOSFET, showing the passive capacitive and resistive components. The gate capacitance C_i is the sum of the distributed capacitances from the gate to the source end of the channel (C_{GS}) and the drain end (C_{GD}). In addition, we have an overlap capacitance (where the gate electrode overlaps the source/drain junctions) from the gate-to-source (C_{OS}) and gate-to-drain (C_{OD}). C_{OD} is also known as the Miller overlap capacitance. We also have p-n junction depletion capacitances associated with the source (C_{JS}) and drain (C_{JD}). The parasitic resistances include the source/drain series resistances (R_S and R_D), and the resistances in the substrate between the bulk contact and the source and drain (R_{BS} and R_{BD}). The drain current can be modeled as a (gate) voltage-controlled constant-current source.

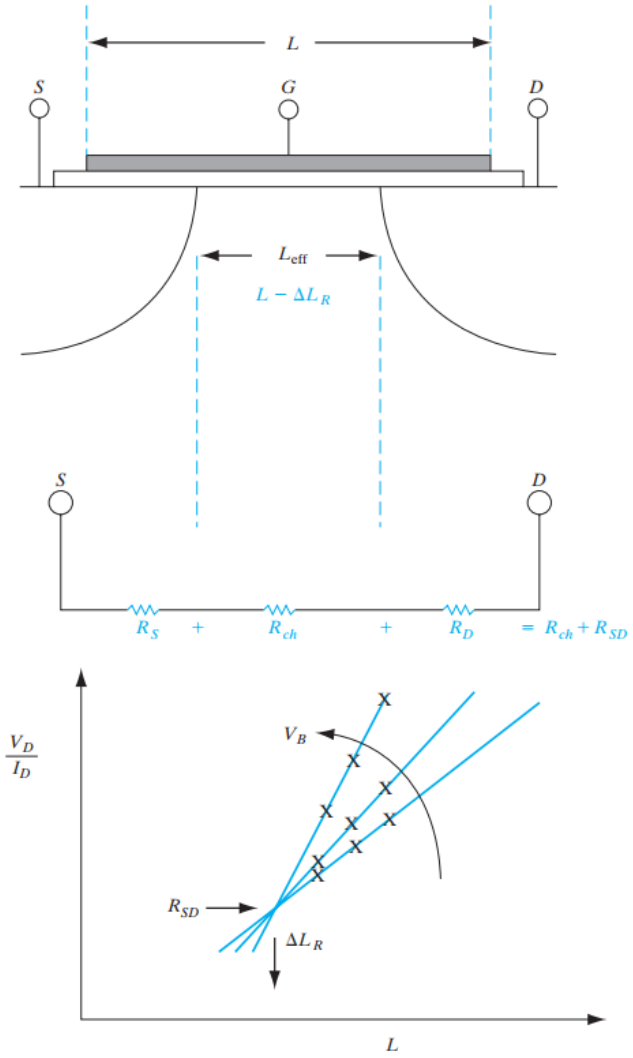


Figure 6–40
Determination of length reduction and source/drain series resistance in a MOSFET. The overall resistance of a MOSFET in the linear region is plotted as a function of channel length, for various substrate biases. The X's mark data points for three different physical gate lengths *L*.

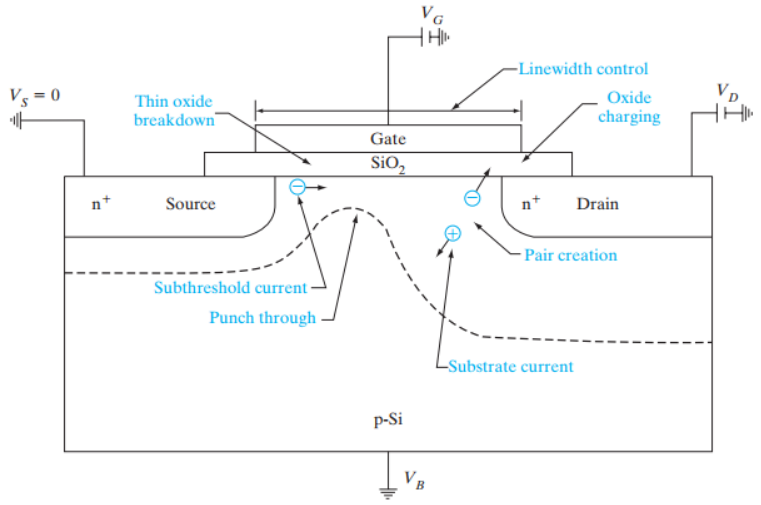


Figure 6–41
Short channel effects in MOSFETs. As MOSFETs are scaled down, potential problems due to short channel effects include hot carrier generation (electron–hole pair creation) in the pinch-off region, punch-through breakdown between source and drain, and thin gate oxide breakdown.

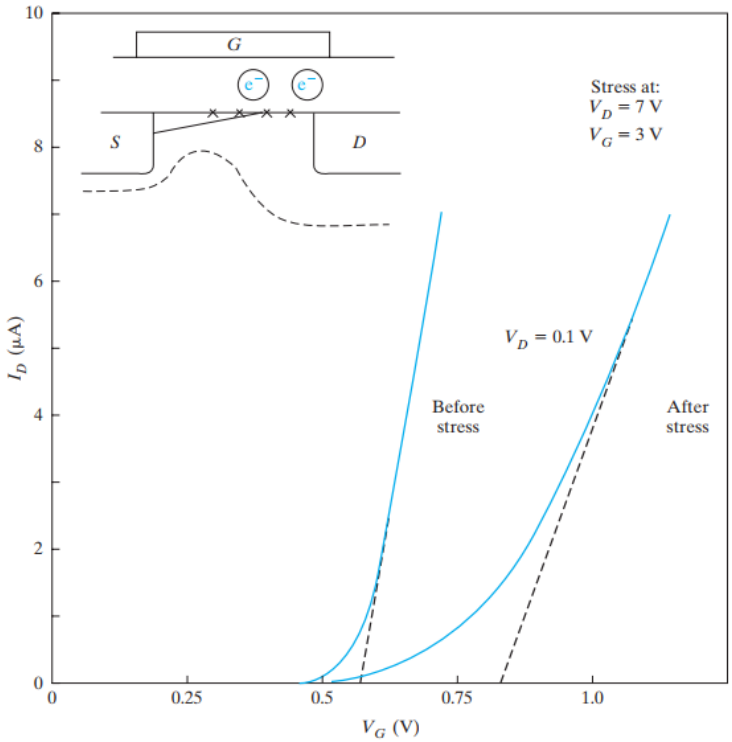


Figure 6–42
Hot carrier degradation in MOSFETs. The linear region transfer characteristics before and after hot carrier stress indicate an increase of V_T and decrease of transconductance (or channel mobility) due to hot electron damage. The damage can be due to hot electron injection into the gate oxide which increases the fixed oxide charge, and increasing fast interface state densities at the oxide–silicon interface (indicated by x).

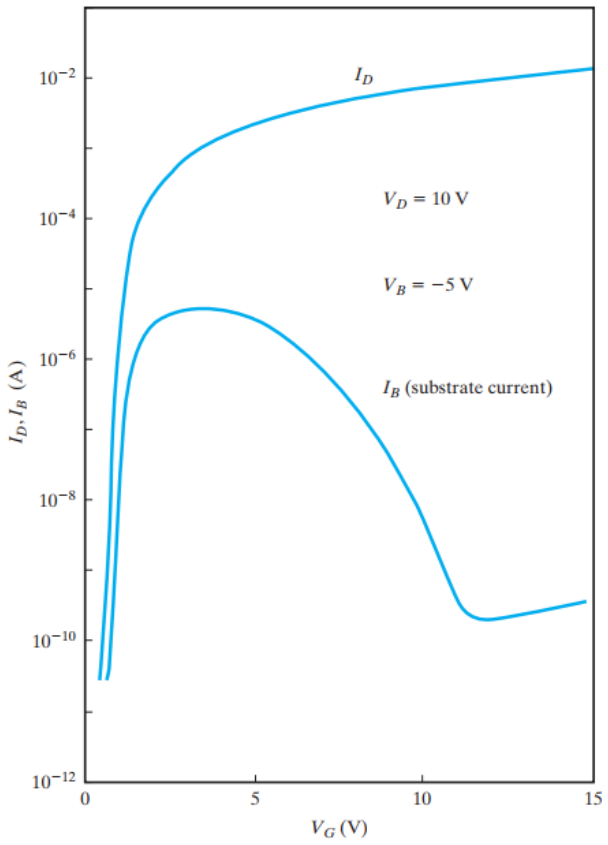


Figure 6–43
Substrate current in a MOSFET. The substrate current in n-channel MOSFETs due to impact-generated holes in the pinch-off region, as a function of gate bias. The substrate current initially increases with V_G, because of the corresponding increase of I_D. However, for even higher V_G the MOSFET goes from the saturation to the linear region, and the high electric fields in the pinch-off region decrease, causing less impact ionization. (After Kamata, et al., *Jpn. J. Appl. Phys.*, 15 (1976), 1127.)

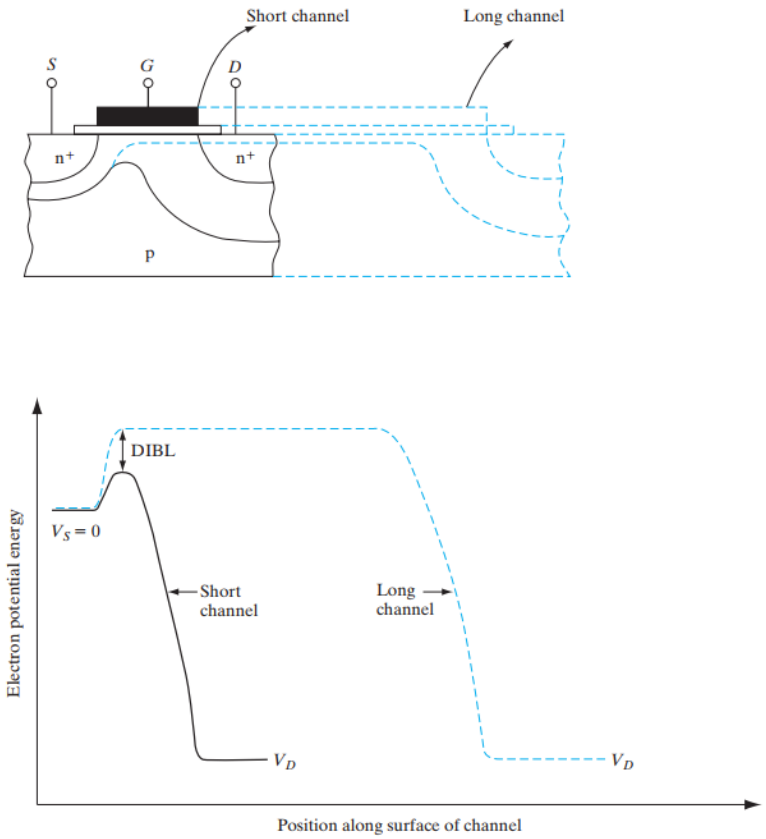


Figure 6–44
Drain-induced barrier lowering in MOSFETs. Cross sections and potential distribution along the channel for a long channel and short channel MOSFET.

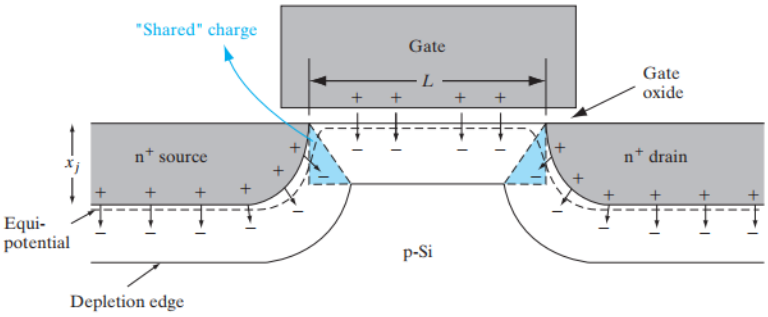


Figure 6–45
Short channel effect in a MOSFET. Cross-sectional view of MOSFET along the length showing depletion charge sharing (colored regions) between the gate, source, and drain.

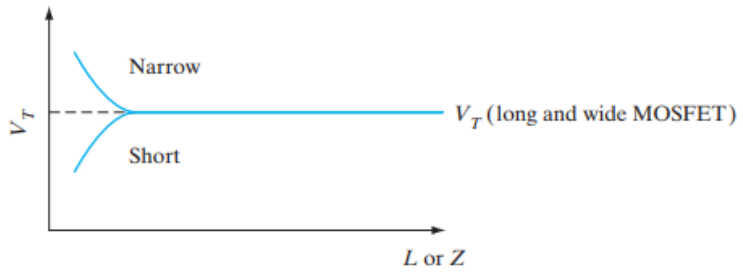


Figure 6–46
Roll-off of V_T with decreasing channel length, and increase of V_T with decreasing width.

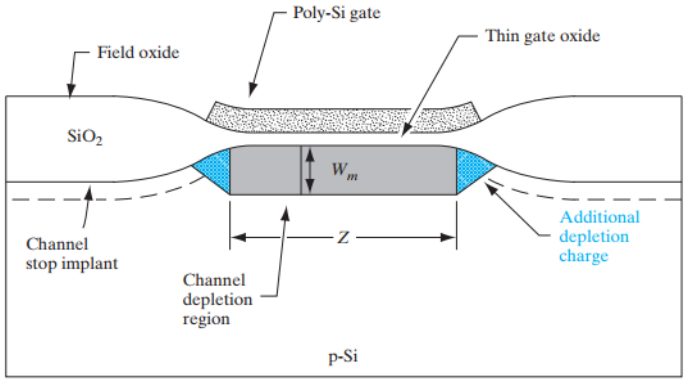


Figure 6–47
Narrow width effect in a MOSFET. Cross-sectional view of MOSFET along the width, showing additional depletion charge (colored regions) underneath the field or the LOCOS isolation regions.

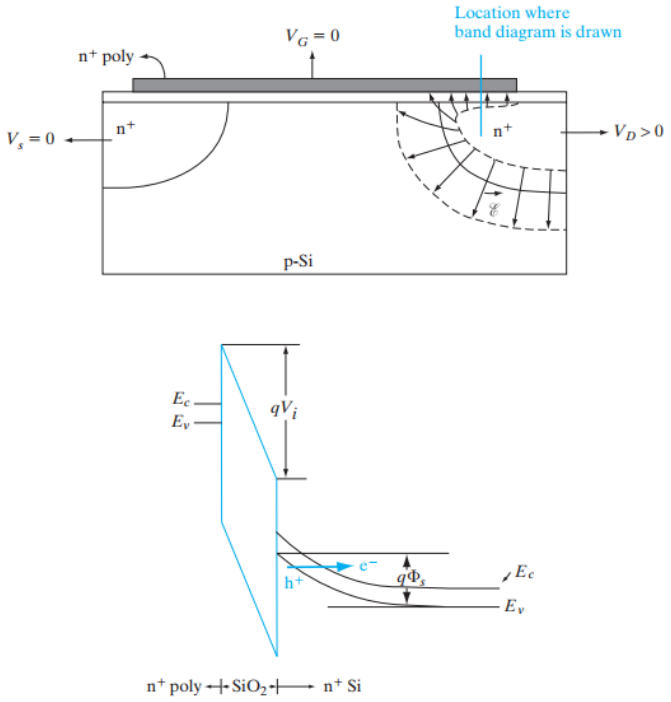


Figure 6–48
Gate-induced drain leakage in MOSFETs. The band diagram for the location shown in color is plotted as a function of depth in the gate–drain overlap region, indicating band-to-band tunneling and creation of electron–hole pairs in the drain region in the Si substrate.

the value E_g. GIDL is an important factor in limiting the off-state leakage current in state-of-the-art MOSFETs.

Advanced MOSFET Structures

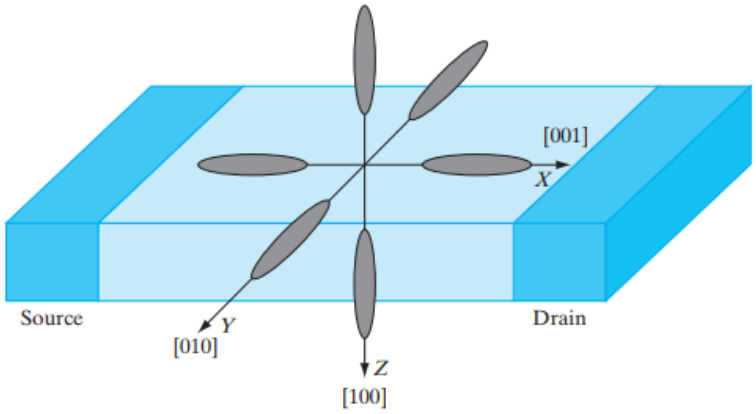


Figure 6–49
Energy ellipsoids in Si shown with respect to MOSFET made on (100) Si. Confinement by the inversion layer potential in the vertical direction lowers the two valleys in the *Z*-direction; tensile strain lowers them even more, reducing scattering between the valleys. Also, since these ellipsoids have the lower m_t in the transport direction from source-to-drain, there is enhancement of mobility and drain current.

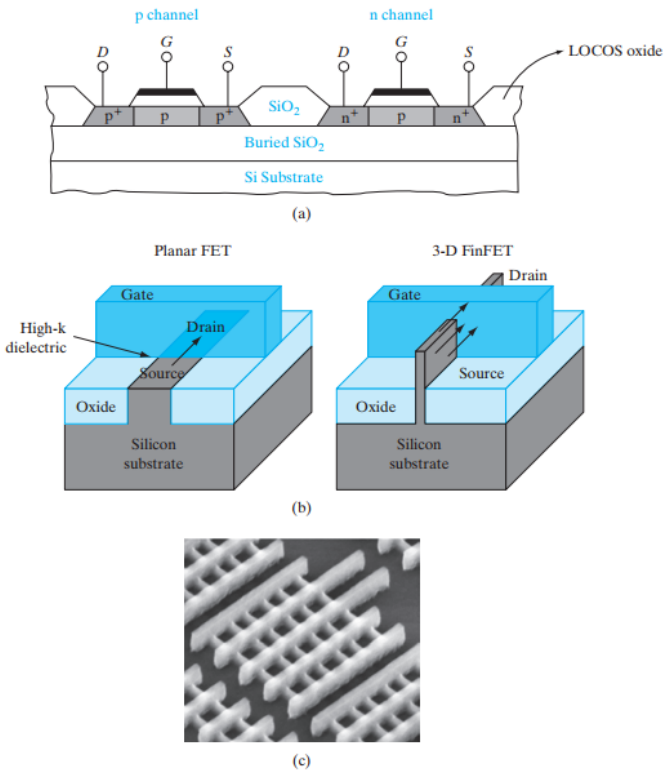


Figure 6–50
(a) Silicon on insulator. Both n-channel and p-channel enhancement transistors are made in islands of Si film on the insulating substrate. These devices can be interconnected for CMOS applications. (b) FinFET and comparison to planar MOSFET; (c) scanning electron micrograph of multiple fin 22 nm tri-gate FETs connected in parallel to increase the effective width (Photograph courtesy of Intel.).