Digital Design Prelab #8
Charlie Coleman
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1A)

D Flip Flop

```
entity DFlipFlop is
    Port ( D : in  STD_LOGIC;
           CLK : in  STD_LOGIC;
           Q : inout  STD_LOGIC);
end DFlipFlop;

architecture Behavioral of DFlipFlop is

begin
      ff : process(CLK, D)
      begin
            if(CLK = '1') then
                  Q <= D;
            end if;
      end process;

end Behavioral;
```

Edge Triggered D Flip Flop

```
entity EdgeTriggeredDFlipFlop is
    Port ( D : in  STD_LOGIC;
           CLK : in  STD_LOGIC;
           Q : inout  STD_LOGIC);
end EdgeTriggeredDFlipFlop;

architecture Behavioral of EdgeTriggeredDFlipFlop is

COMPONENT DFlipFlop
      PORT(
            D : IN std_logic;
            CLK : IN std_logic;
            Q : INOUT std_logic
            );
      END COMPONENT;
signal Qhold : STD_LOGIC;
signal Qfinal: STD_LOGIC;
begin

      DFlipFlop_1: DFlipFlop PORT MAP(
            D => D,
            CLK => "not"(CLK),
            Q => Qhold
      );
      DFlipFlop_2: DFlipFlop PORT MAP(
            D => Qhold,
            CLK => CLK,
            Q => Qfinal
      );
      Q <= Qfinal;
```

```
end Behavioral;
```

Four Bit Register

```
entity FourBitRegister is
    Port ( D1 : in  STD_LOGIC;
           D2 : in  STD_LOGIC;
           D3 : in  STD_LOGIC;
           D4 : in  STD_LOGIC;
           CLK : in  STD_LOGIC;
           Q1 : out  STD_LOGIC;
           Q2 : out  STD_LOGIC;
           Q3 : out  STD_LOGIC;
           Q4 : out  STD_LOGIC);
end FourBitRegister;

architecture Behavioral of FourBitRegister is

      COMPONENT EdgeTriggeredDFlipFlop
      PORT(
            D : IN std_logic;
            CLK : IN std_logic;
            Q : INOUT std_logic
            );
      END COMPONENT;
signal Q1temp : STD_LOGIC;
signal Q2temp : STD_LOGIC;
signal Q3temp : STD_LOGIC;
signal Q4temp : STD_LOGIC;
begin

      ETDFlipFlop1: EdgeTriggeredDFlipFlop PORT MAP(
            D => D1,
            CLK => CLK,
            Q => Q1temp
      );
      ETDFlipFlop2: EdgeTriggeredDFlipFlop PORT MAP (
            D => D2,
            CLK => CLK,
            Q => Q2temp
      );
      ETDFlipFlop3: EdgeTriggeredDFlipFlop PORT MAP (
            D => D3,
            CLK => CLK,
            Q => Q3temp
      );
      ETDFlipFlop4: EdgeTriggeredDFlipFlop PORT MAP (
            D => D3,
            CLK => CLK,
            Q => Q4temp
      );
      Q1 <= Q1temp;
      Q2 <= Q2temp;
      Q3 <= Q3temp;
      Q4 <= Q4temp;

end Behavioral;
```

2.A.a)

```
entity Decode2_4e is
    Port ( SØ : in  STD_LOGIC;
           S1 : in  STD_LOGIC;
           EN : in  STD_LOGIC;
           YØ : out  STD_LOGIC;
           Y1 : out  STD_LOGIC;
           Y2 : out  STD_LOGIC;
           Y3 : out  STD_LOGIC);
end Decode2_4e;

architecture Behavioral of Decode2_4e is

begin

      YØ <= not S1 and not SØ and EN;
      Y1 <= not S1 and SØ and EN;
      Y2 <= S1 and not SØ and EN;
      Y3 <= S1 and SØ and EN;

end Behavioral;
```