Computer System Design Lab # 7
ISA Read

Charlie Coleman
Lab Partner: Amy Guo

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Pre-Lab: Not applicable

Objective: Design a VHDL design to drive an A/D converter (ADC) and record the output through the IO space via a C program written in DOS.

Circuit Diagram: Not applicable

Outcome Predictions: We will be able to record the ADC and reconstruct the signal that is output.

Equipment:
- Xilinx Spartan 3 with MESA 4i38
- PC
- ADC0804
- Benchtop Power Supply
- Oscilloscope + Function Generator

Procedure:
1. Modify the VHDL design from Lab 6 to read 8 bit A-D conversions from IO pins.
2. Write the A-D conversions to the IO space.
3. Write a C script to fetch the A-D conversion from the IO space and print to the command line.
4. Using the ADC0804 Spec sheet, assemble the circuit to allow for A-D conversion.
5. Wire the 8 output pins of the ADC to the Spartan 3.

Recalculations and Predictions: N.A

Data and Observations:
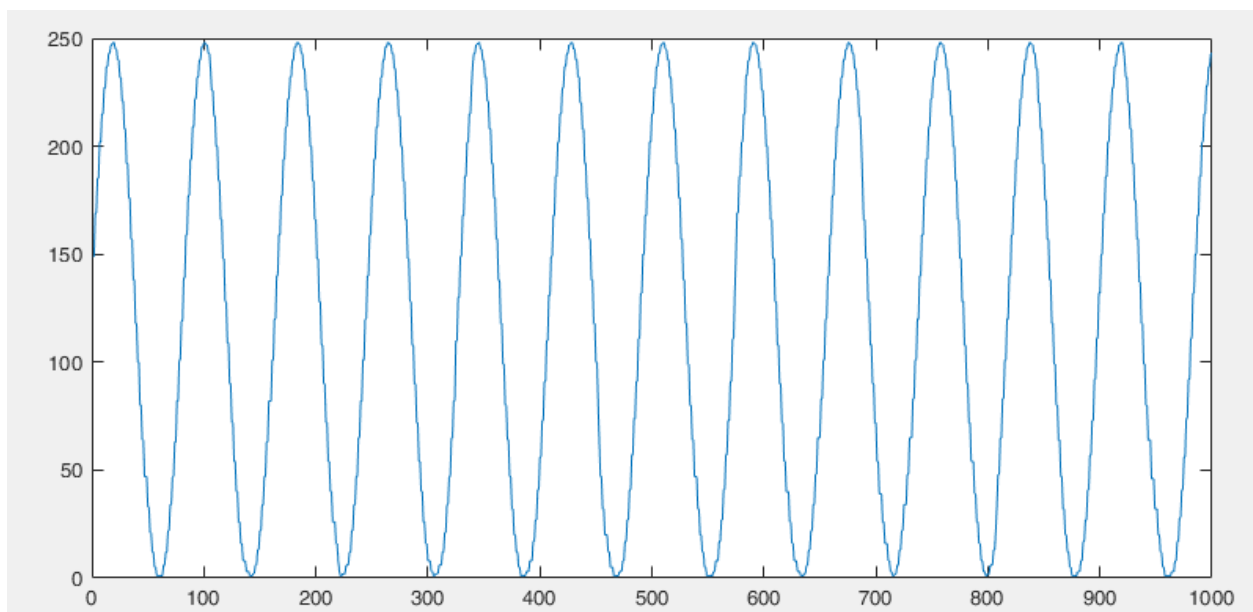
We were able to obtain the graph above from our C program coupled with the Xilinx Spartan 3 + ADC0804. This graph matches our expectations exactly, as we were using the oscilloscope to generate a sine wave from 0 to 5, the full range of the ADC.

Analysis & Discussion: The measurements are very similar to the expected outcome. Because V_{Ref} was 0-5V and our waveform went form 0-5V, we expected the values output by the ADC to go from close to 0 to close to 255. This matched the recorded output, as can be seen in the graph. These results were therefore good.

Lab Questions:

Q: What is the sample rate of your design?

A: The maximum sample rate achieved by our design was 2000 samples/second.

Q: What would be required to produce a variable sample rate design?

A: The sample rate is determined by the clock rate of the VHDL design (set by the user) and the capacitor/resistor pair in the circuit. The clock rate could be reset during execution via some extra code, but to change the hardware sample rate would require a potentiometer in place of the resistor or some form of variable capacitance capacitor.

Q: What voltage ranges can your design read?

A: 0 to 5V

Q: What changes would be required to be able to read wall voltage?

A: The reference voltages would need to be 0-120V, but the ADC0804 is not capable of such high voltages. The chip would need to be replaced with something capable of high power operation.

Results: This experiment worked as expected. The data output by our C program closely matched the expected range and waveform shape.

Conclusions: In this lab, we learned how to assemble a circuit based off of data sheets. This is useful because many times we will not have a circuit that we are reproducing, but will simply be tasked with creating our own that matches given specifications and works with the given hardware. We also learned not to name our files anything longer than 8 characters as this will confuse DOS and lead to prolonged periods of debugging.