Digital Design Lab #5: 7-segment Decoder Driver

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Objective: The objective of this lab was to create a seven segment decoder and use it to display the output of a three bit adder.

Design:

In this lab, a seven segment decoder was developed and tested using a three bit adder. Each segment of the seven segment decoder was developed separately and then combined into one schematic. The three bit adder from Lab #4 was used, with its outputs going into the seven segment decoder.

Truth Table 1:

A	B	C	D	Sa	Sb	Sc	Sd	Se	Sf	Sg
0	0	0	0	0	0	0	0	0	0	1
0	0	0	1	1	0	0	1	1	1	1
0	0	1	0	0	0	1	0	0	1	0
0	0	1	1	0	0	0	0	1	1	0
0	1	0	0	1	0	0	1	1	0	0
0	1	0	1	0	1	0	0	1	0	0
0	1	1	0	0	1	0	0	0	0	0
0	1	1	1	0	0	0	1	1	1	1
1	0	0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	1	1	0	0
1	0	1	0	0	0	0	1	0	0	0
1	0	1	1	1	1	0	0	0	0	0
1	1	0	0	0	1	1	0	0	0	1
1	1	0	1	1	0	0	0	0	1	0
1	1	1	0	0	1	1	0	0	0	0
1	1	1	1	0	1	1	1	0	0	0

Karnaugh Maps:

Sa	00	01	11	10
00	0	1	0	0
01	1	0	0	0
11	0	1	0	0
10	0	0	1	0

Sb	00	01	11	10
00	0	0	0	0
01	0	1	0	1
11	1	0	1	1
10	0	0	1	0

Sc	00	01	11	10
00	0	0	0	1
01	0	0	0	0
11	1	0	1	1
10	0	0	0	0

Sd	00	01	11	10
00	0	1	0	0
01	1	0	1	0
11	0	0	1	0
10	0	1	0	1

Se	00	01	11	10
00	0	1	1	0
01	1	1	1	0
11	0	0	0	0
10	0	1	0	0

Sf	00	01	11	10
00	0	1	1	1
01	0	0	1	0
11	0	1	0	0
10	0	0	0	0

Sg	00	01	11	10
00	1	1	0	0
01	0	0	1	0
11	1	0	0	0
10	0	0	0	0

Equations:

$$S_a = \bar{A}\bar{B}\bar{C}D + \bar{A}B\bar{C}\bar{D} + AB\bar{C}D + A\bar{B}CD$$

$S_b = \bar{A}B\bar{C}D + AB\bar{D} + ACD + BC\bar{D}$
$S_c = \bar{A}\bar{B}C\bar{D} + AB\bar{D} + ABC$
$S_d = \bar{B}\bar{C}D + \bar{A}B\bar{C}\bar{D} + BCD + A\bar{B}C\bar{D}$
$S_e = \bar{A}D + \bar{A}B\bar{C} + \bar{B}\bar{C}D$
$S_f = AB\bar{C}D + \bar{A}\bar{B}C + \bar{A}\bar{B}D + \bar{A}CD$
$S_g = \bar{A}\bar{B}\bar{C} + \bar{A}BCD + AB\bar{C}\bar{D}$

Procedure: To begin the lab, we created a new project in the Xilinx software. In this project, we created individual schematics for each segment of the decoder, Sa through Sg. Each schematic was given a symbol. Under a new schematic file, the schematic symbols were all added and the appropriate inputs were labeled with I/O markers. The software rearranged some of the input orders of the segments, so extra care was taken when connecting them. We then tested the 7-segment decoder for all input combinations using the clock simulation for 20 ns. We then tested the circuit with time delays using post-route simulation. The only inputs tested for using time delays were 1, 2, and 4, with A being the most significant bit. The decoder was then downloaded to a board and tested for all input combinations. We then created a schematic symbol for the seven segment decoder. We then pulled up our 3 bit adder from lab 4, and connected it to the seven bit decoder. This was done using Add Source to add the adder to the current project. We removed the 3 bit adder output markers, and connected the outputs of the adder to the inputs of the decoder. The schematic was then saved and synthesized. This schematic was then downloaded and tested with the following combinations.

CIN	A(2:0)	B(2:0)
0	000	000
0	001	010
0	011	011
0	011	100
0	011	101
0	001	110
0	110	101
0	111	111
1	111	111

Data: See attached diagrams and simulations.

Data Analysis:

Conclusion: