

Digital Design Lab 2: Simplifying Circuits

Charlie Coleman

Lab Partner: Luke Taylor

Objective: The objective of this lab was to look at the construction and performance of initial and simplified circuits, and to use that information to determine the benefits of circuit simplification.

Design:

Fig 2.1:

1A) $F = \bar{A} \wedge B \wedge C \vee A \vee B$

1B) Table 1:

A	B	C	F
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

1C) $F = B \wedge (\bar{A} \wedge C \vee 1) \vee A = A \vee B$

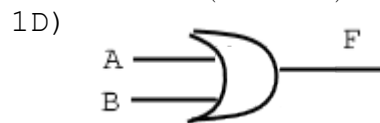


Fig 2.2:

1A) $F = (A \wedge B \vee C) \wedge (\bar{B} \vee \bar{C})$

1B) Table 2:

A	B	C	F
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

1C) $F = (A \wedge B \wedge \bar{B}) \vee (C \wedge \bar{B}) \vee (A \wedge B \wedge \bar{C}) \vee (C \wedge \bar{C}) = (A \wedge B \wedge \bar{C}) \vee (C \wedge \bar{B})$

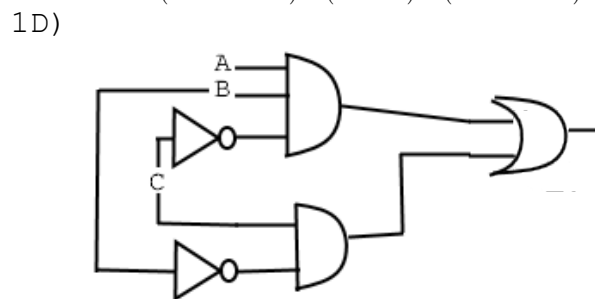


Fig 2.3:

1A) $F = (A \wedge C) \wedge (A \wedge B \vee \bar{C}) \wedge (C \wedge (B \vee D))$

1B) Table 3:

A	B	C	D	F
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	1
1	1	1	1	1

1C) $F = (A \wedge A \wedge B \wedge C \vee A \wedge C \wedge \bar{C}) \wedge (C \wedge (B \vee D)) = A \wedge B \wedge C \wedge (B \vee D) = A \wedge B \wedge C$

1D)

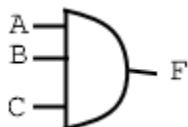


Fig 2.4:

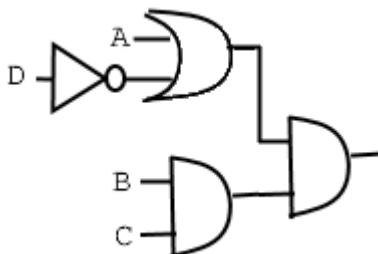
1A) $F = B \wedge C \wedge (A \wedge B \wedge (B \vee C) \vee (\bar{A} \wedge \bar{D}) \vee (A \wedge \bar{C}))$

1B) Table 4:

A	B	C	D	F
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	1
1	1	1	1	1

1C) $F = B \wedge C \wedge ((A \wedge B \wedge (B \vee C) \vee (\bar{A} \wedge \bar{D})) \vee A \wedge \bar{C})$
 $F = B \wedge C \wedge (((A \wedge B) \vee (A \wedge B \wedge C) \vee (\bar{A} \wedge \bar{D})) \vee (A \wedge \bar{C}))$
 $F = B \wedge C \wedge ((A \wedge B) \vee (\bar{A} \wedge \bar{D}) \vee (A \wedge \bar{C})) = B \wedge C \wedge (A \vee (\bar{A} \wedge \bar{D}))$
 $F = B \wedge C \wedge (A \vee \bar{D})$

1D)



Procedure: First, the logical expression for the circuit diagram is written. Next, the truth table is found. Then, the logical expression is simplified using Boolean algebra. Next, the simplified expression is drawn as a circuit diagram. After the diagram is drawn, the initial and simplified circuits are constructed and tested. Finally, the initial and simplified circuits are analyzed based on the number of input lines.

Data:

Fig 2.1:

Initial:
Truth Table: Table 1
Input Lines: 9
Simplified:
Truth Table: Table 1
Input Lines: 2

Fig 2.2:

Initial:
Truth Table: Table 2
Input Lines: 10
Simplified:
Truth Table: Table 2
Input Lines: 7

Fig 2.3:

Initial:
Truth Table: Table 3
Input Lines: 14
Simplified:
Truth Table: Table 3
Input Lines: 3

Fig 2.4:

Initial:
Truth Table: Table 4
Input Lines: 21
Simplified:
Truth Table: Table 4
Input Lines: 6

Data Analysis: All data measured in lab (truth tables) matched the calculated data.

Conclusion: In this lab, the concepts behind simplification using Boolean algebra were practiced and tested. All data calculated matched the data measured, and therefore the methods were validated. Some challenges were faced when constructing the fourth diagram. There were many wires going across the board, and it was difficult to keep things straight. These challenges were overcome by testing the circuit and comparing to the truth table.