ECE-2206 Digital Design Lab

EXPERIMENT #1

FAMILIARIZATION WITH LOGIC GATES

OBJECTIVES:

1) To construct circuits using pin diagrams.
2) To examine the characteristics of AND, OR, NAND and NOR gates.
3) Construct circuits using various types of gates.

COMPONENTS:

7400, 7402, 7408, 7420,7421,7427, 7432

NOTE: Please turn in the following parts as prelab.
Part 5A , 5B

PART 1) A) Using data manuals write the chip number and the pin numbers on the following gates.

B) Test a single gate on each chip to verify the truth table. Record you results.

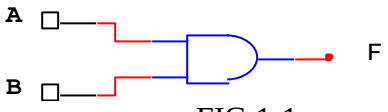

FIG 1-1

A	B	F
0	0	
0	1	
1	0	
1	1	

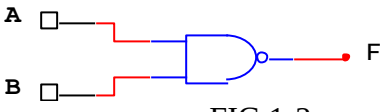

FIG 1-2

A	B	F
0	0	
0	1	
1	0	
1	1	

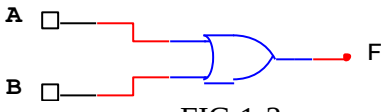

FIG 1-3

A	B	F
0	0	
0	1	
1	0	
1	1	

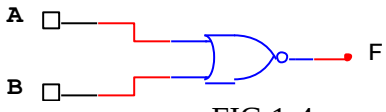

FIG 1-4

A	B	F
0	0	
0	1	
1	0	
1	1	

PART 2) A) For the following 4 input AND gate keep the input **A** at logic low and change the other inputs to different levels. Record your results in the following table.

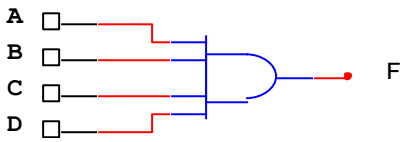

FIG 1-5

A	B	C	D	F
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	

B) Interpret the obtained results. (Make a general statement about AND gates.)

PART 3) A) Repeat part **2A** for a 4 input NAND gate.

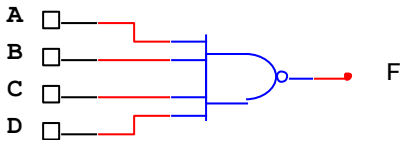

FIG 1-6

A	B	C	D	F
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	

B) Interpret the obtained results. (Make a general statement about NAND gates.)

PART 4) A) For the following 3 input NOR gate keep input **A** at logic high and change the other inputs to different levels. Record the results in the following table.

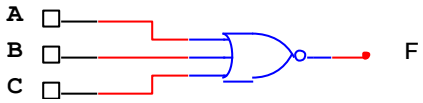

FIG 1-7

A	B	C	F
1	0	0	
1	0	1	
1	1	0	
1	1	1	

B) Interpret the obtained results. (Make a general statement about NOR gates.)

PART 5) A) Complete the truth table for the following circuit diagram and turn in a copy as a prelab.

B) Write the chip numbers and the pin numbers on the circuit diagram.

C) Construct and test the circuit for all possible input combinations. Compare the results with the truth table of part A.

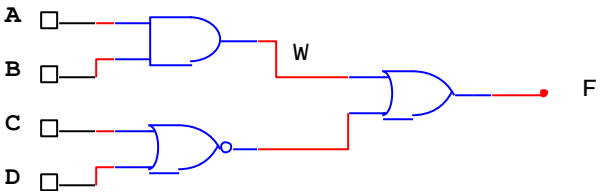

FIG 1-8

A	B	C	D	F
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

PART 5) CONTINUES

D) Break the connection at point **W** (by removing the connecting wire) and test the circuit for all possible input combinations.
Record the results in the following table.
Interpret the obtained results.

A	B	C	D	F
0	**0**	**0**	**0**	
0	**0**	**0**	**1**	
0	**0**	**1**	**0**	
0	**0**	**1**	**1**	
0	**1**	**0**	**0**	
0	**1**	**0**	**1**	
0	**1**	**1**	**0**	
0	**1**	**1**	**1**	
1	**0**	**0**	**0**	
1	**0**	**0**	**1**	
1	**0**	**1**	**0**	
1	**0**	**1**	**1**	
1	**1**	**0**	**0**	
1	**1**	**0**	**1**	
1	**1**	**1**	**0**	
1	**1**	**1**	**1**	

PART6) CONCLUSION: