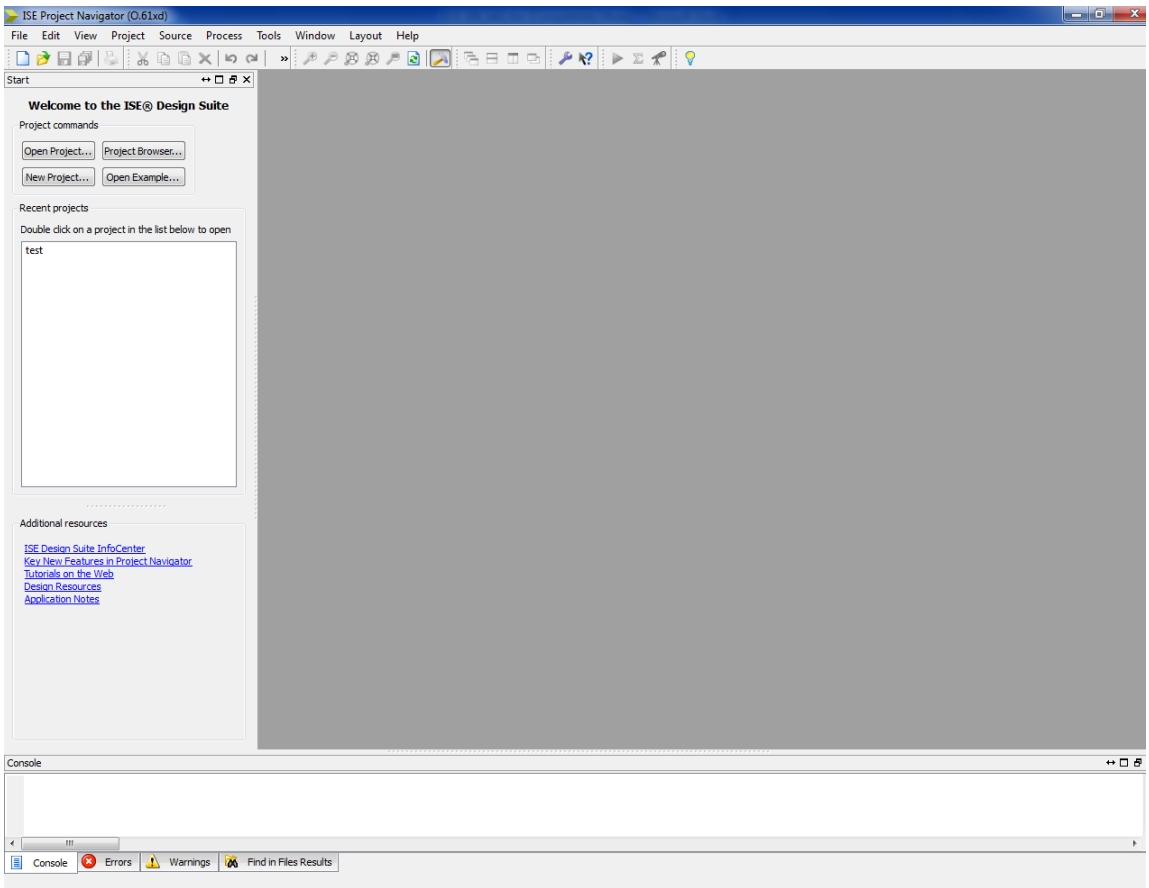
Experiment #3
Introduction to Xilinx ISE Software

Objective: To get familiar with the Xilinx ISE version 13.2_1 software.

Procedure:

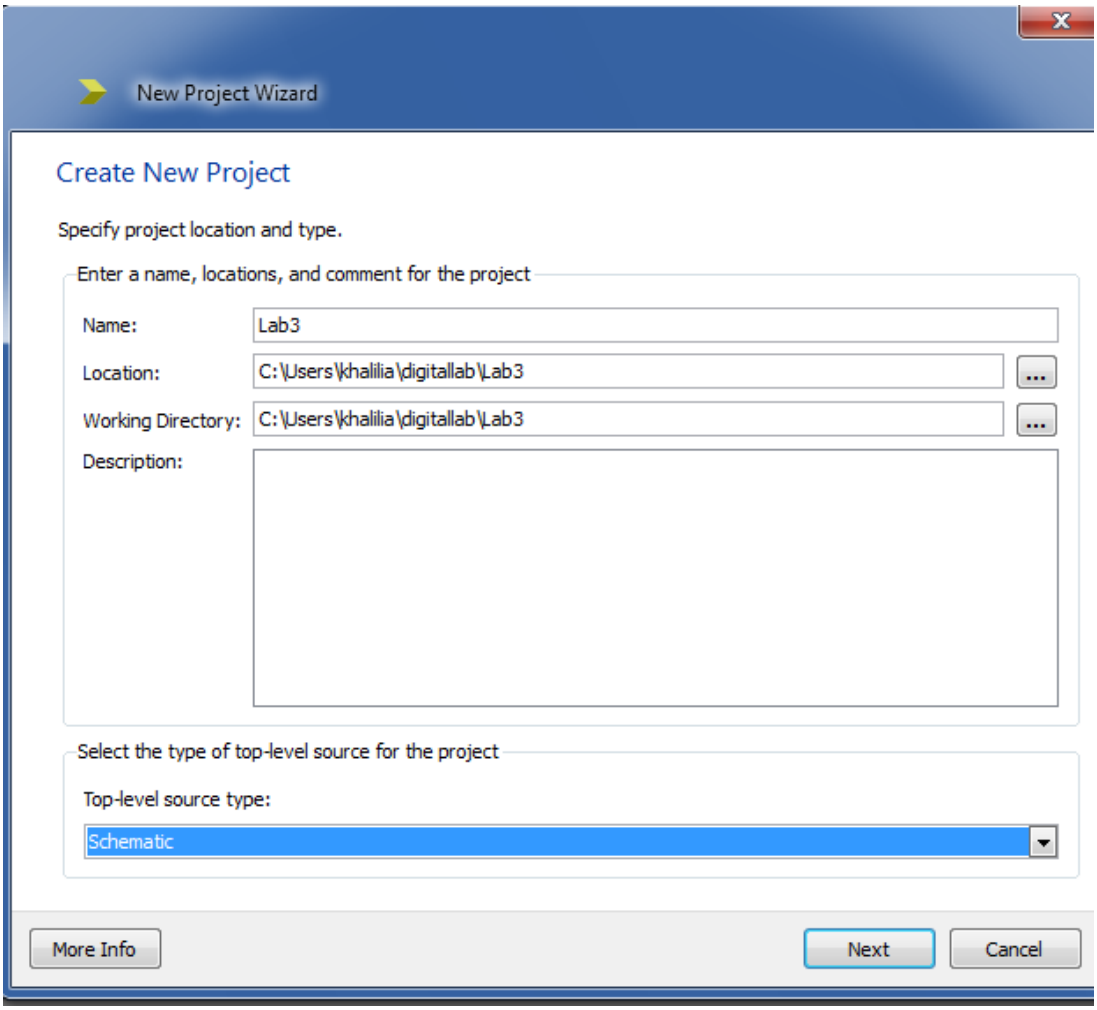
1) Access the **Xilinx ISE** program by: **Start → Programs → Xilinx ISE Design Suite 13.2_1 → ISE Design Tools → Project Navigator,** or click on the **Xilinx ISE Design Suite 13.2_1** icon on the screen.

2) Once the program has opened, create a new project by selecting **New Project** on upper left corner of the opened window, or by **File Menu → New Project…**



3) A) The **New Project** window will appear. Type in a project name, specify a location for your project (make sure you remember where it's going). Use the following as a template:

Project Name: **Lab3**
Project Location: **C:\Users\your-username\digitallab**
Top-Level Module Type: **Schematic**

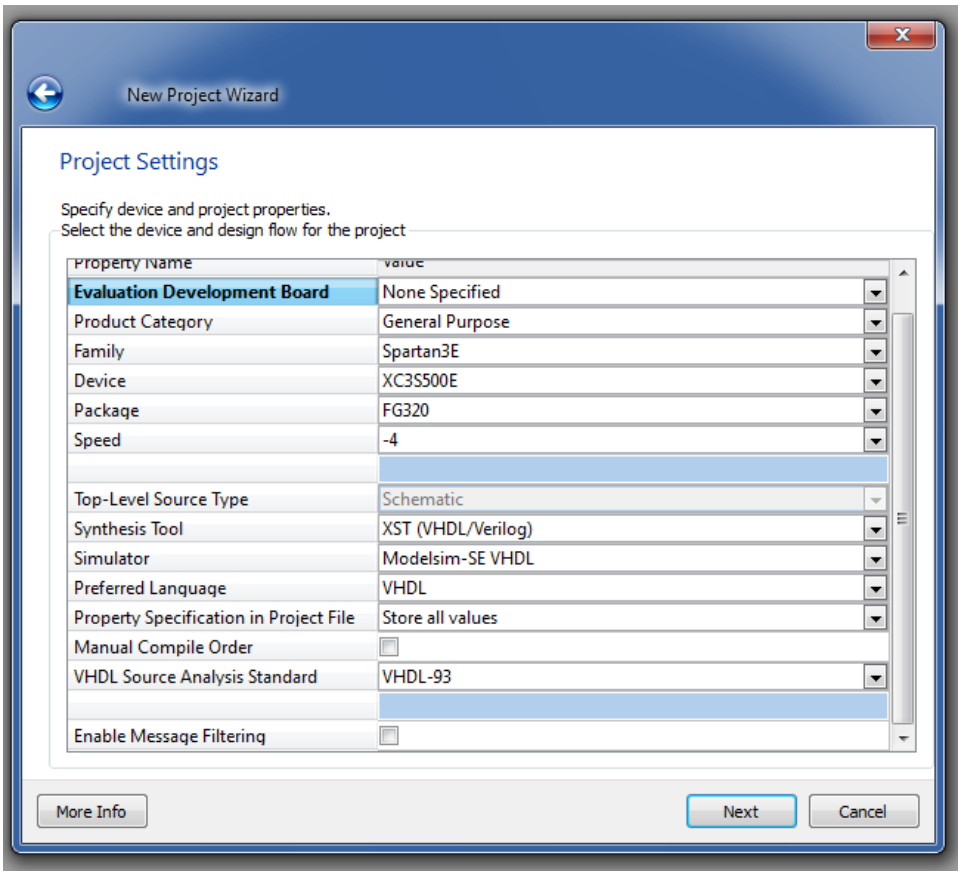


B) Click on next. You will get the window shown in step 4.

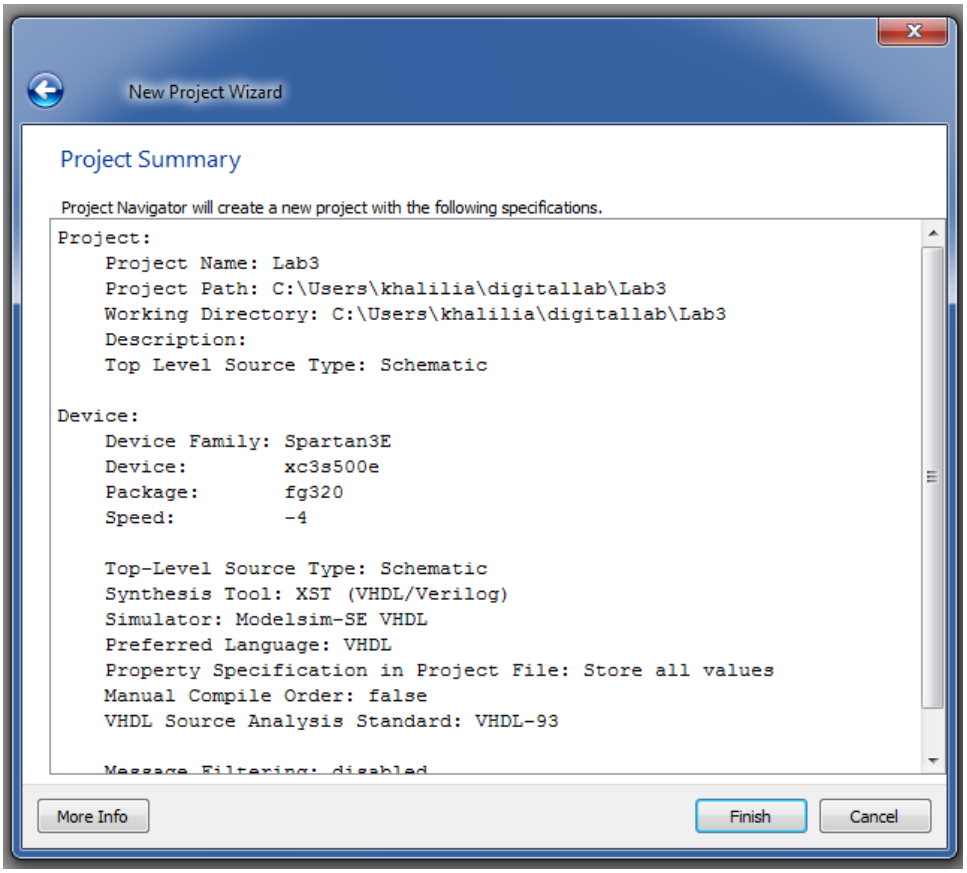
4) Make sure you have the following device specifications and simulator choice. Click on **Next**. You will get the window shown in step 5.

Device Family:	**Spartan3E**
Device:	**XC3S500E**
Package:	**FG320**
Speed Grade:	**-4**

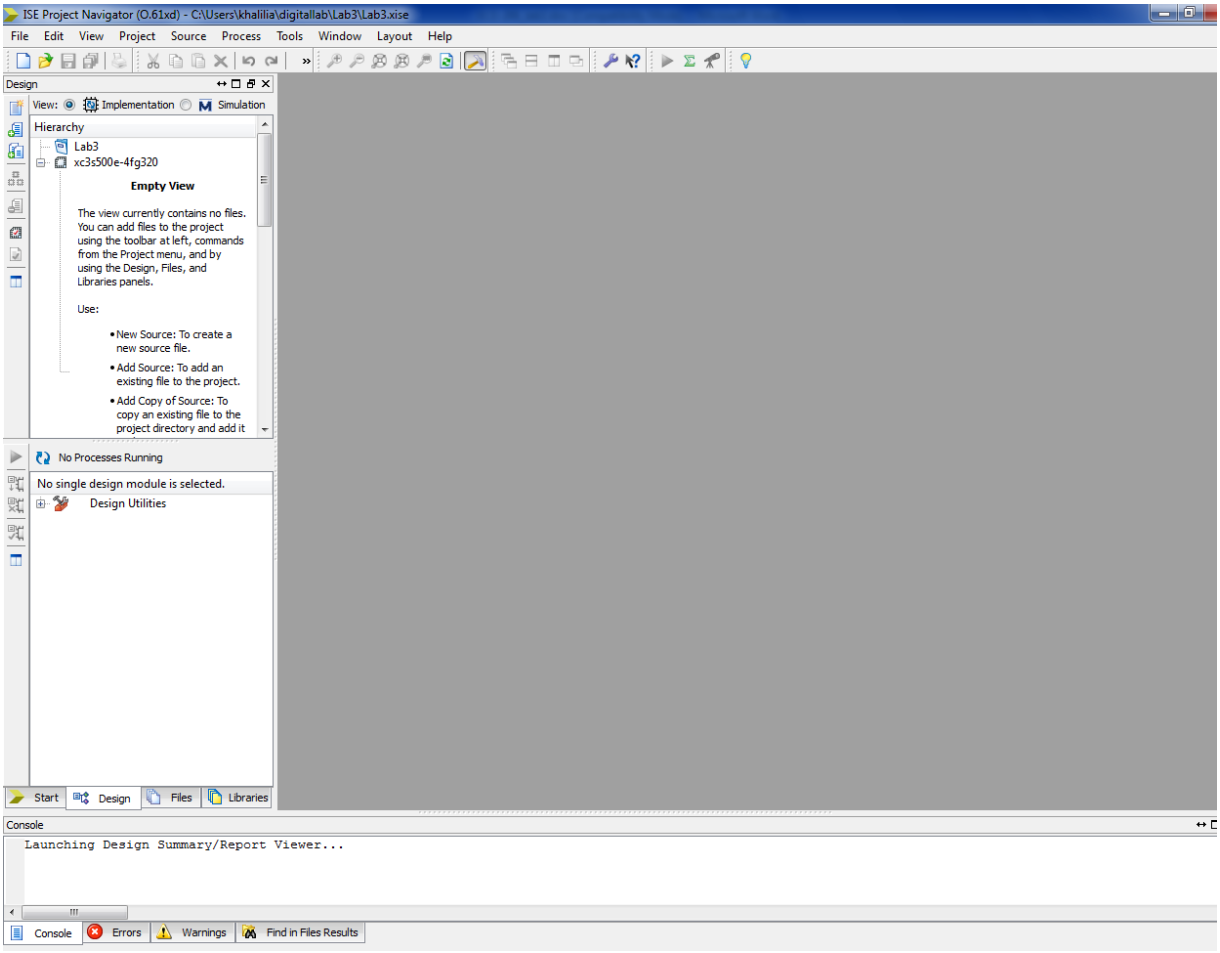
Simulator	**Modelsim-SE VHDL**



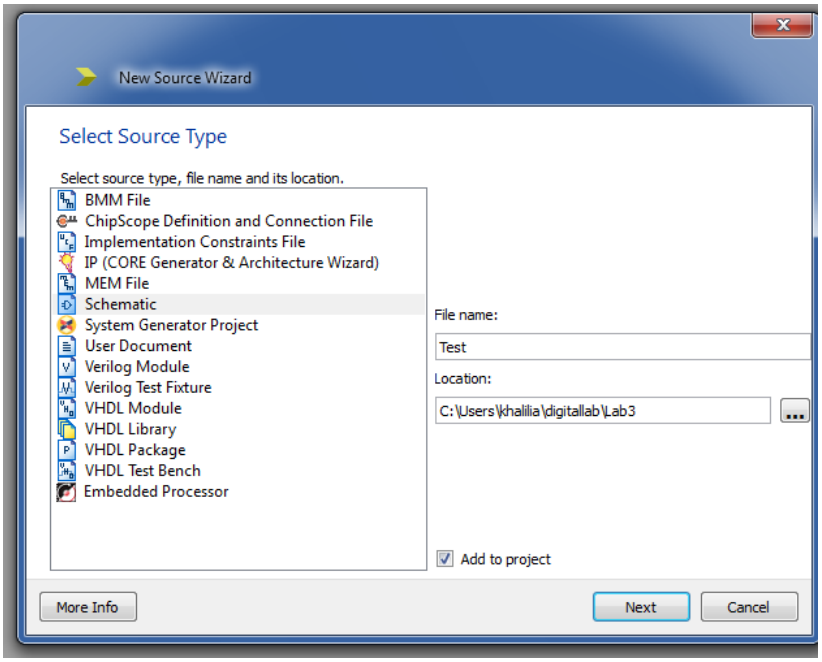
5) Click on **Finish**. You will get the window shown in step 6.



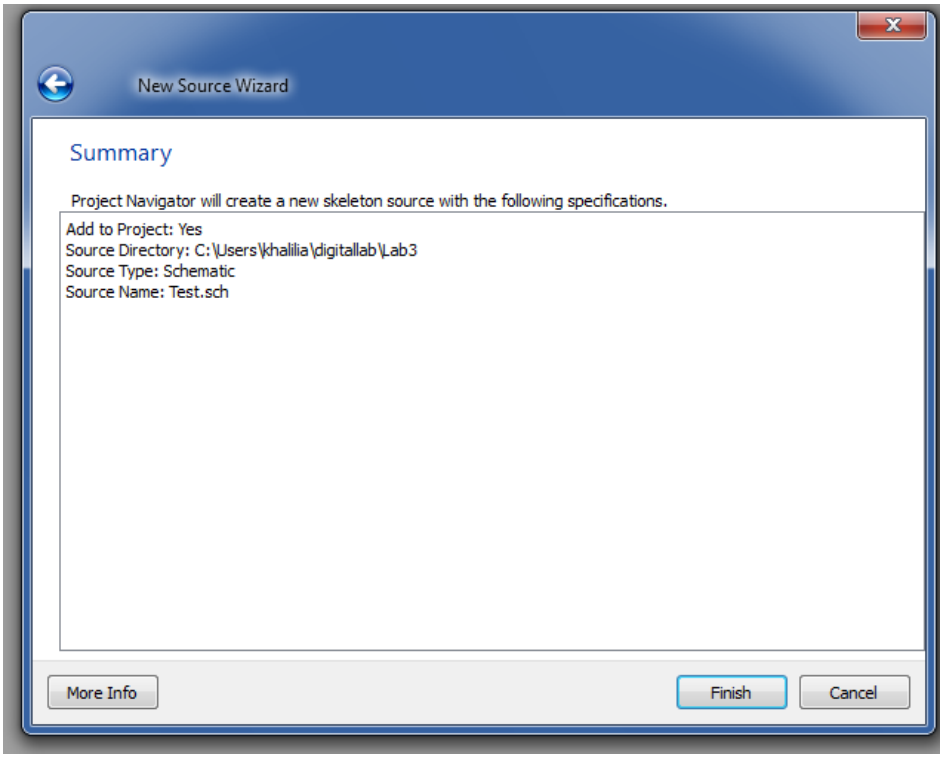
6) Create a new source, by **Project → New Source,** click on new source and you will get the window shown in step 7.



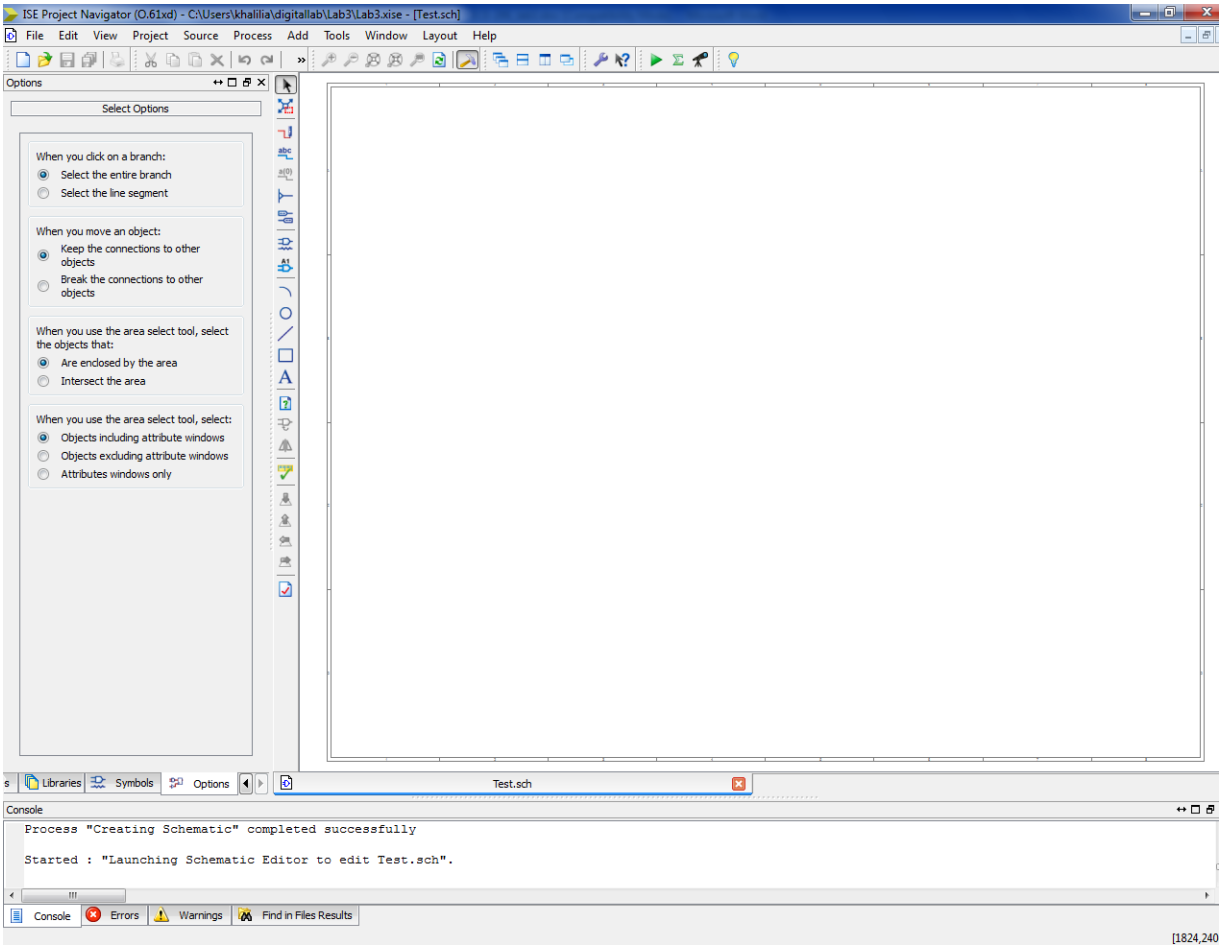
7) Highlight the **Schematic** option and type in your filename. The **Next** option will become available for you. Click on **Next**, you will have the window shown in step 8.



8) Click on finish. A schematic window will open up for you, shown in step 9.



9)



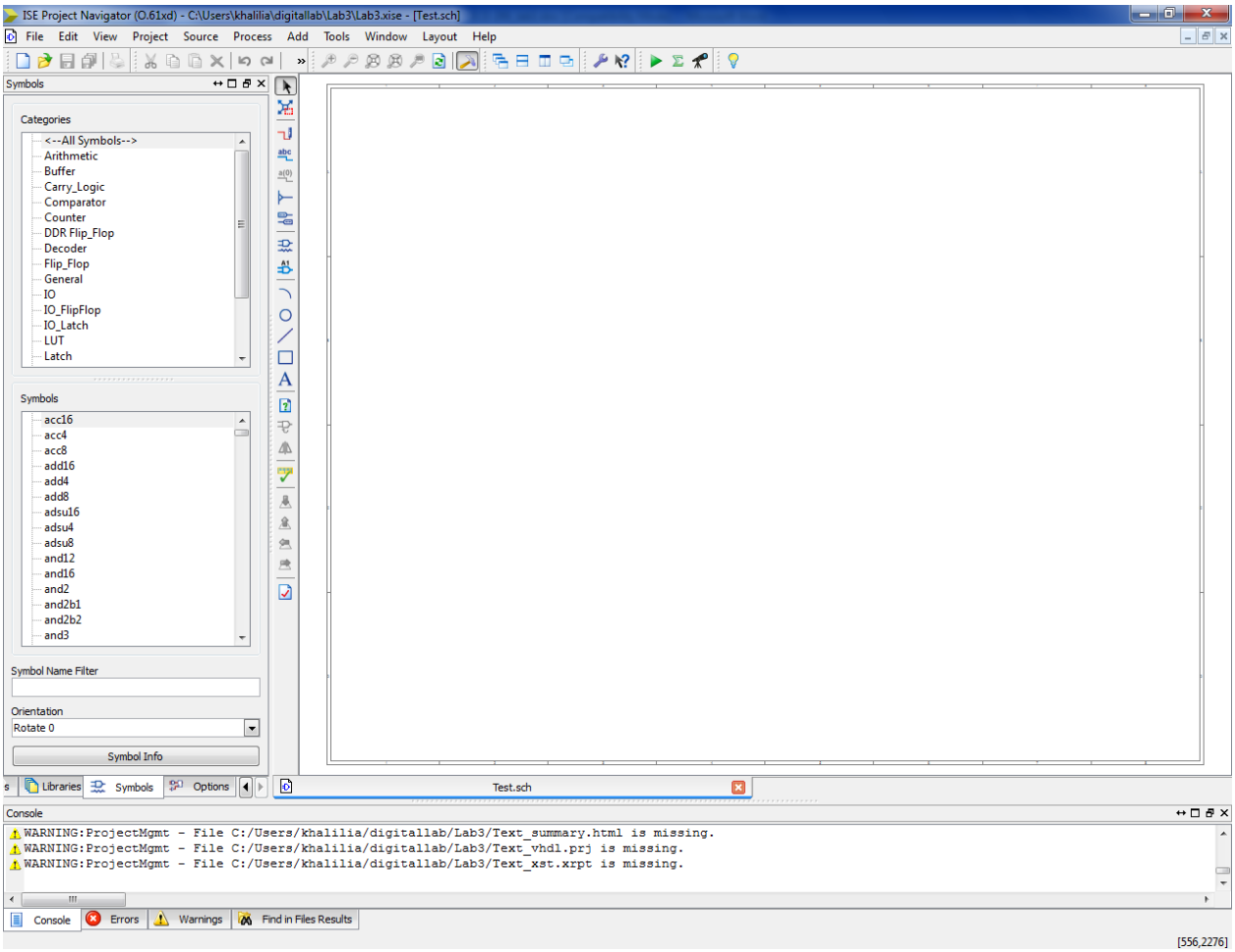
The following steps are :

. To implement a digital circuit diagram in the schematic window

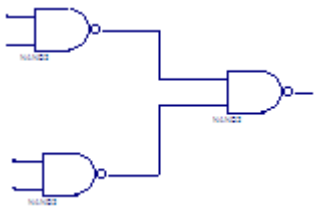
. Simulate the circuit for accuracy

. Downloading it onto the SPARTAN3E FPGA on the NEXYS2 board.

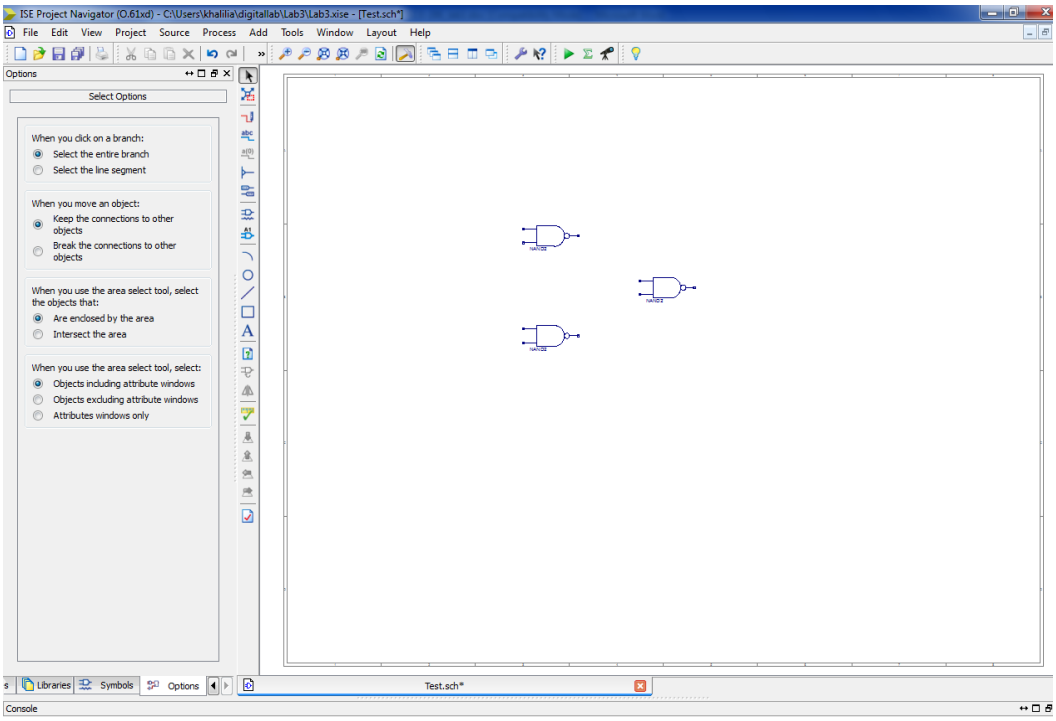
10) In order to access the standard logic gates and devices, click on the **Symbols** option in the lower left side of your schematic window. You should get the following window.



11) For quick access of the logic parts, type name of the part in the **Symbol Name Filter** field in the lower left side of the schematic window. Put three 2 input NAND gates on the schematic window to create the following circuit diagram.

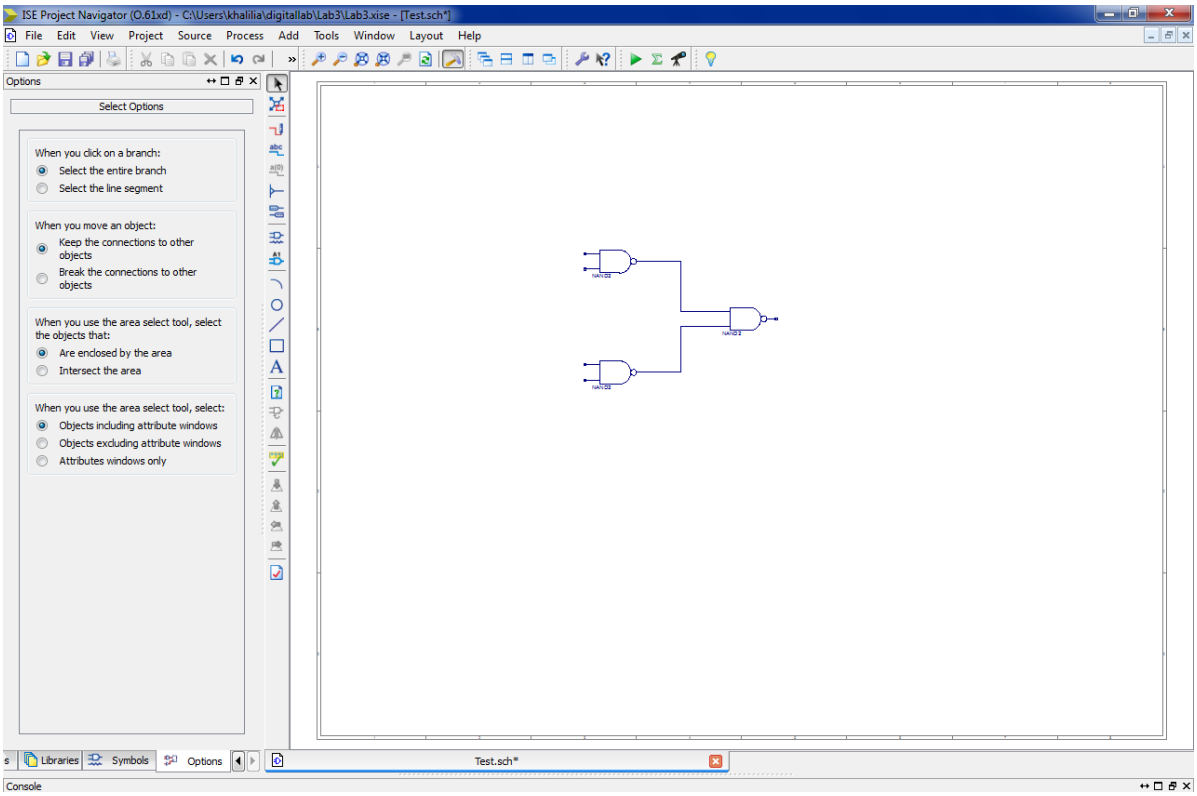


12) You should have the following schematic window.



13) To draw wire, click on the wire icon,  in the vertical tool bar, or select **Wire** from the **Add** menu. To place a wire, click on one part's lead and drag the cursor to the lead of another part. The program should then show a wire connecting the two parts.

NOTE: To get out of **Add Wire** mode (or nay other mode), click on the **Select** icon  on the vertical tool bar of the schematic window.

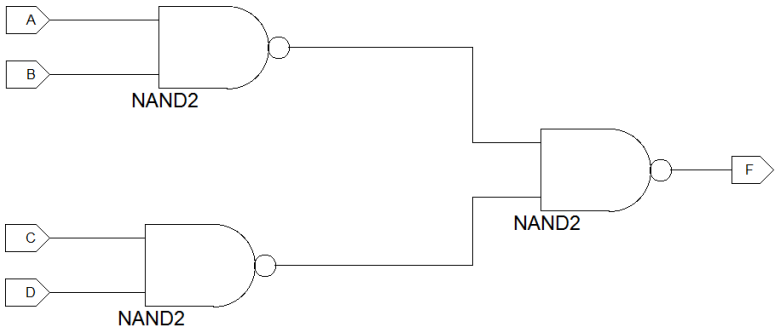


14) You need to add **I/O Markers** to assign signal names to the inputs and the output.

I) Add I/O markers to the schematic by clicking on the I/O marker icon in the vertical tool bar  , or by selecting **I/O Markers** from the **Add** menu.

II) On the left side of the window you will be given the option of choosing input or output markers. Choose accordingly. Click on the end of each wire to place an I/O marker. There should be one I/O marker on each lead (5 total).

III) Right-click on each marker, select **Rename Port** to rename the input/output. The result should look similar to the following diagram.



15) Save the schematic and check the circuit for errors either with the schematic checker, or the HDL compiler.

I) For schematic checker, in the schematic window click on **Tools => Check Schematic.**

II) For HDL compiler, highlight your schematic file in the **Design** window and click on **Synthesize** in the **Processes** window**.**

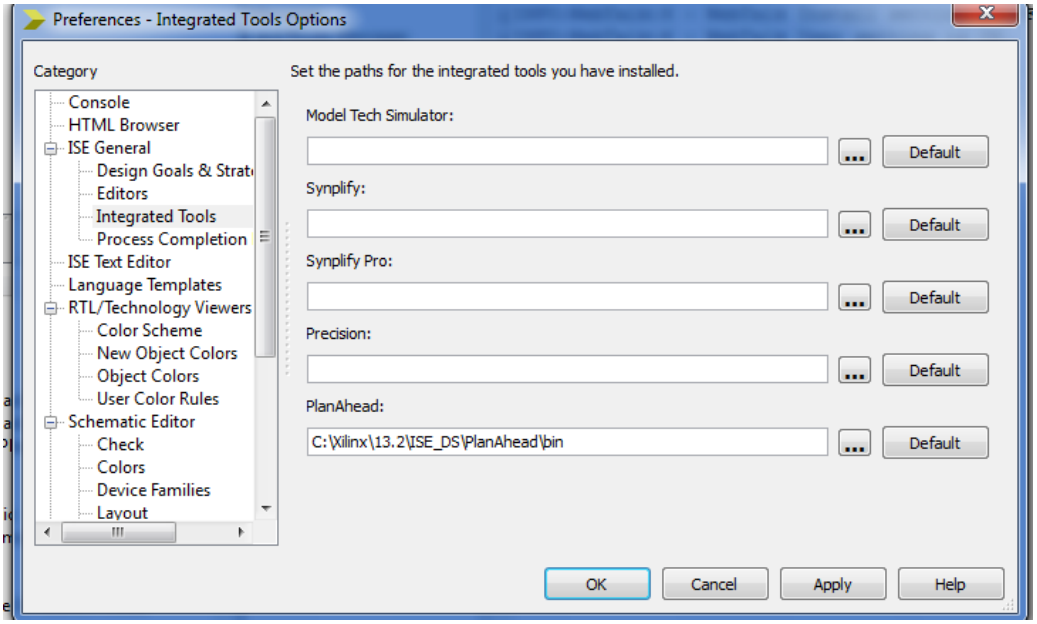
III) If there are any errors, correct them before proceeding to the next step.

NOTE: To access the **Design** window scroll the horizontal arrows in the lower left side of the schematic window and click on the **Design** option.

16) To simulate for logical accuracy, Xilinx ISE uses ModelSim's VHDL simulator to simulate all designs.

Note: First you need to set the path for the simulator.

a. From the top menu select **Edit → Preferences →Integrated Tools.**
You should have the following window.



b. Under **Model Tech Simulator,** click on search icon **(…)** and follow the follwing path to get to the modelsim simulator.
C → Modelteck64_10.0b → Win64 → Modelsim

To simulate a design (Behavioral simulation):

16.1 In the **Design** window, highlight your file and set the option to **Simulation**. In the **Processe** window expand the **ModelSim Simulator,** and double click on **Simulate Behavioral Model**.

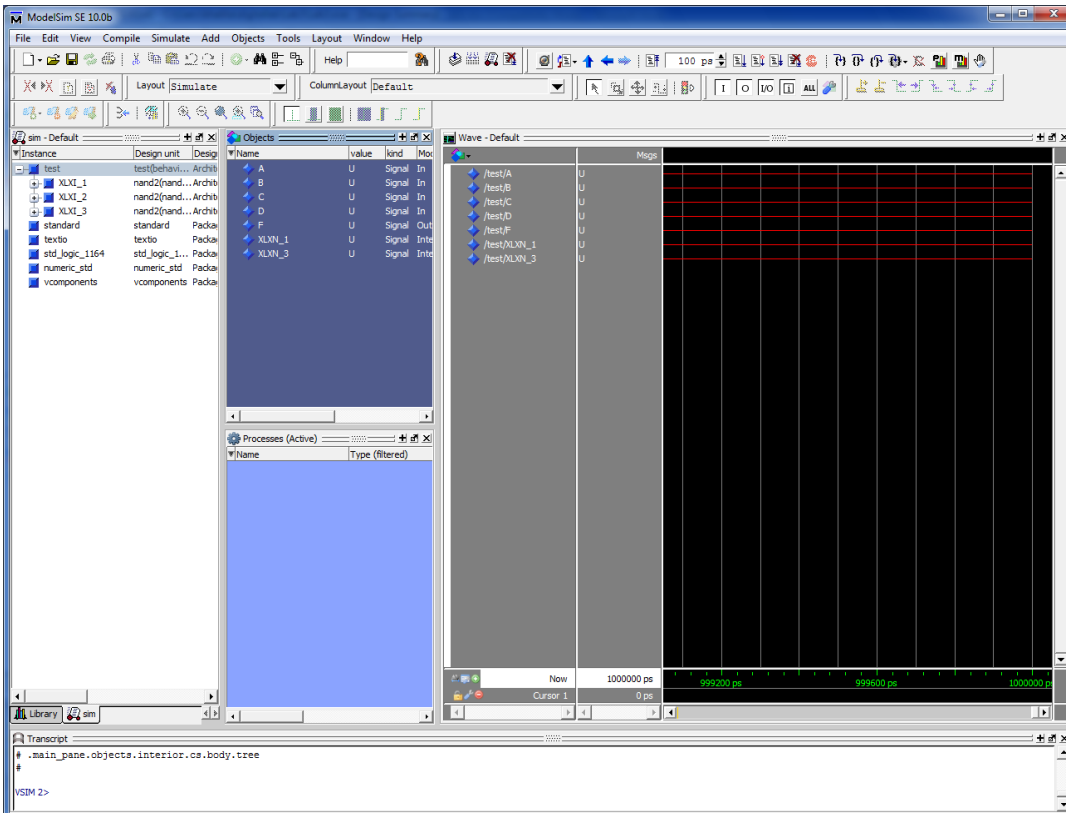
16.2 The ModelSim Simulator will launch. It may be behind the current windows.

16.3 The windows we are interested in are:

a. ModelSim SE 10.0b
b. Objects
c. Wave
d. Transcript

Make sure these are open.

16.4 In the **Transcript** window, type **restart** to erase the red lines in the **Wave** window.



16.5 To place driving patterns on your input lines using the **Force** option:

a. Select an input signal from the **objects** window by highlighting the signal

b. Right click and choose the **Modify → Force** option:
Fill in the values with 1 or 0.

c. Repeat steps a and b for all input signals

16.6 To run your simulation:

a. In the **Transcript** window

b. Type run 5ns

c. Pay attention to the length of time you run your simulation. This simulator will attempt to simulate gate delays, if you don't run long enough the signals may not have settled yet.

d. Simulate for all possible combinations by forcing each input combination and running the simulator for 5ns. Print out waves and list that demonstrate your circuit functioning correctly. Submit a copy of simulation results with your report.

16.7 To place driving patterns on your input lines using the **clock** option:

a. Select Signals from the **objects** window by highlighting the signals

b. Right click and choose the **Modify → clock** option:
In the **Period** field assign: 16ns for MSB (bit3)
8ns for (bit2)
4ns for (bit1)
2ns for (bit0)

c. Simulate for 20 ns.

d. Submit a copy of simulation results with your report.

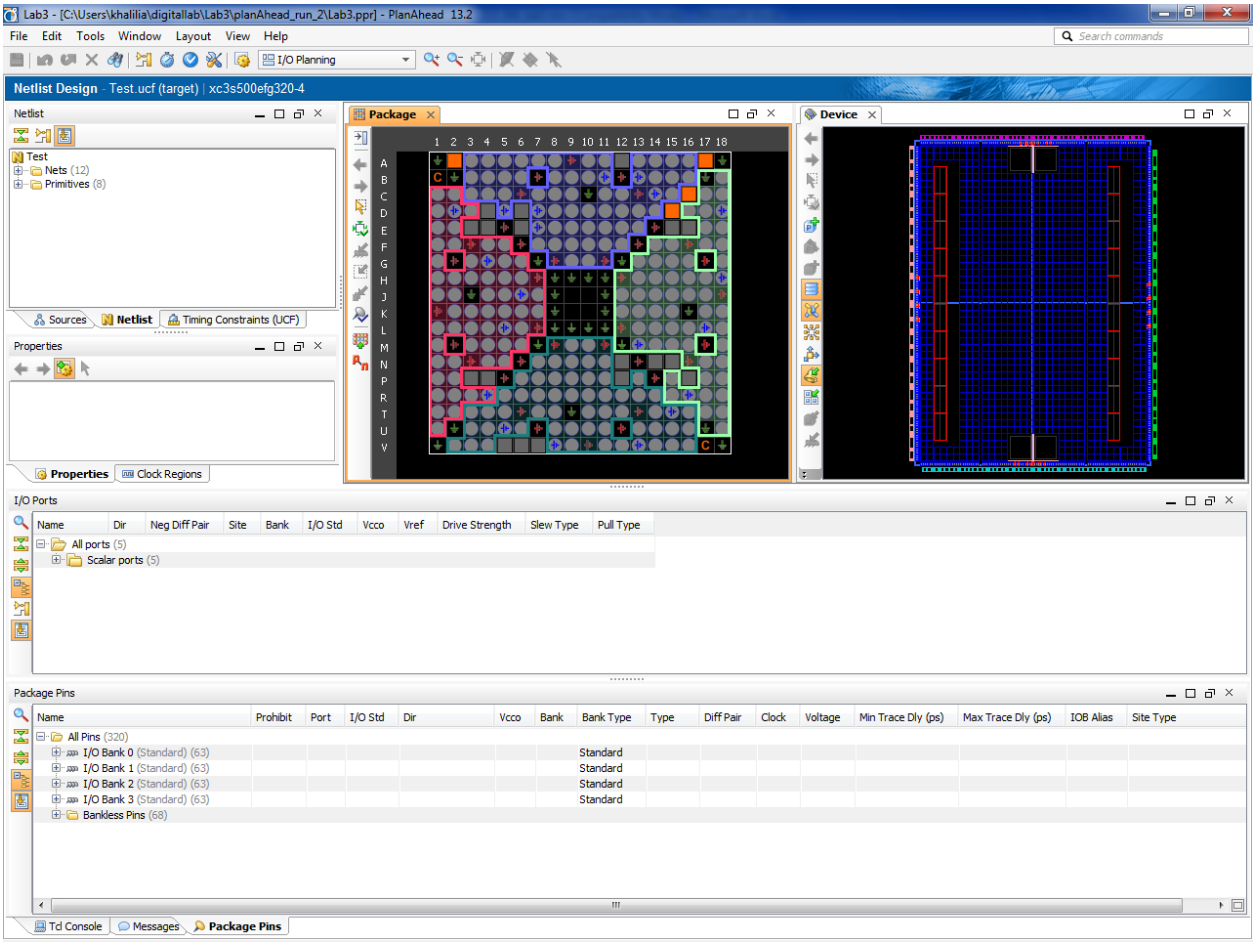
16.8 In the **Design** window, change the mode from **Simulation** to **Implementation**.

17) Before downloading the schematic to the board, we must assign the inputs and outputs from the schematic to certain pins on the chip itself so we can control the inputs and view the outputs. The inputs will be controlled by the push buttons and switches provided on the board and the output will be sent to one of the eight LEDs. For the I/O pin configuration of the Spartan3E FPGA, please use the handout that was provided for you at the beginning of the lab session. The pin assignments are implemented in a **Constraints file**.

For pin assignments:

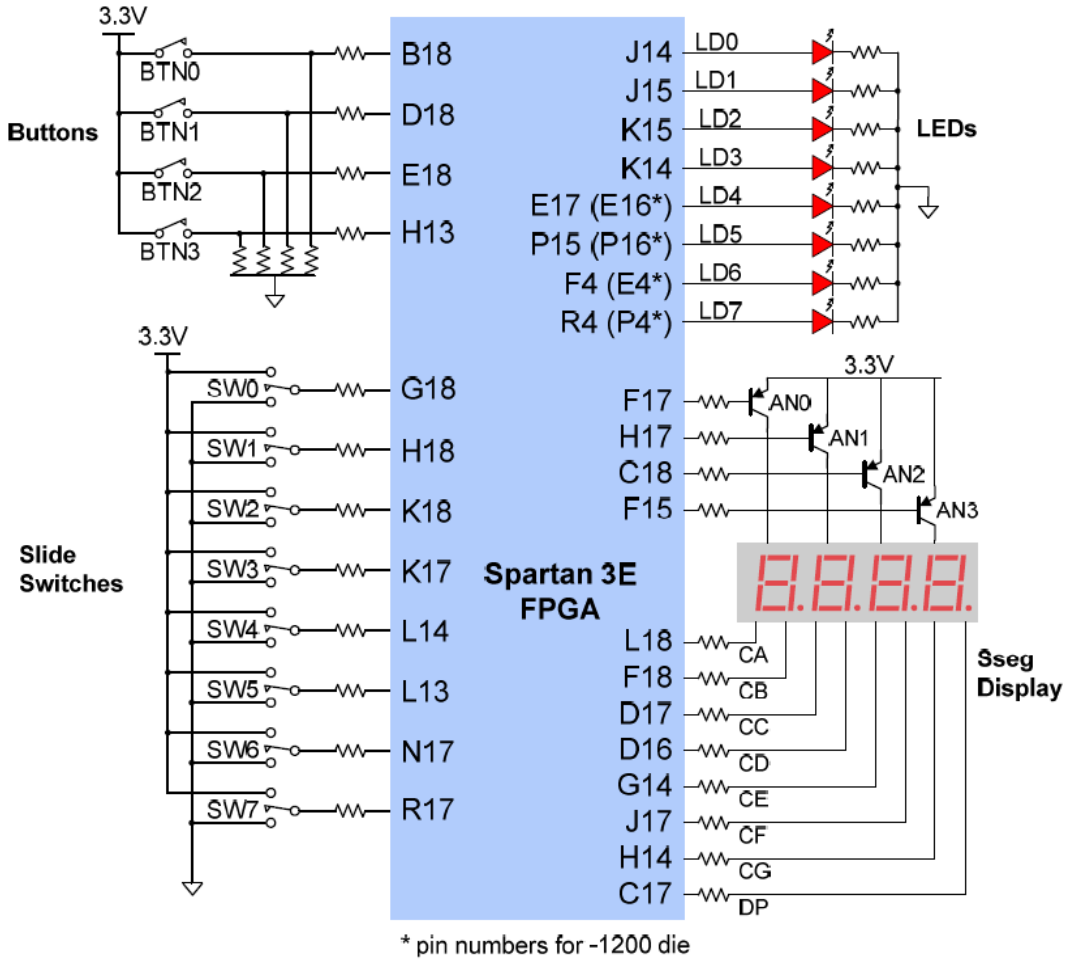
I) Highlight your top level design file.

II) To open the **Constraints Editor**, expand the **User Constraints** in the **Processes** window and double click on **I/O Pin Planning (PlanAhead) – Post-Synthesis**. You should get the following window.



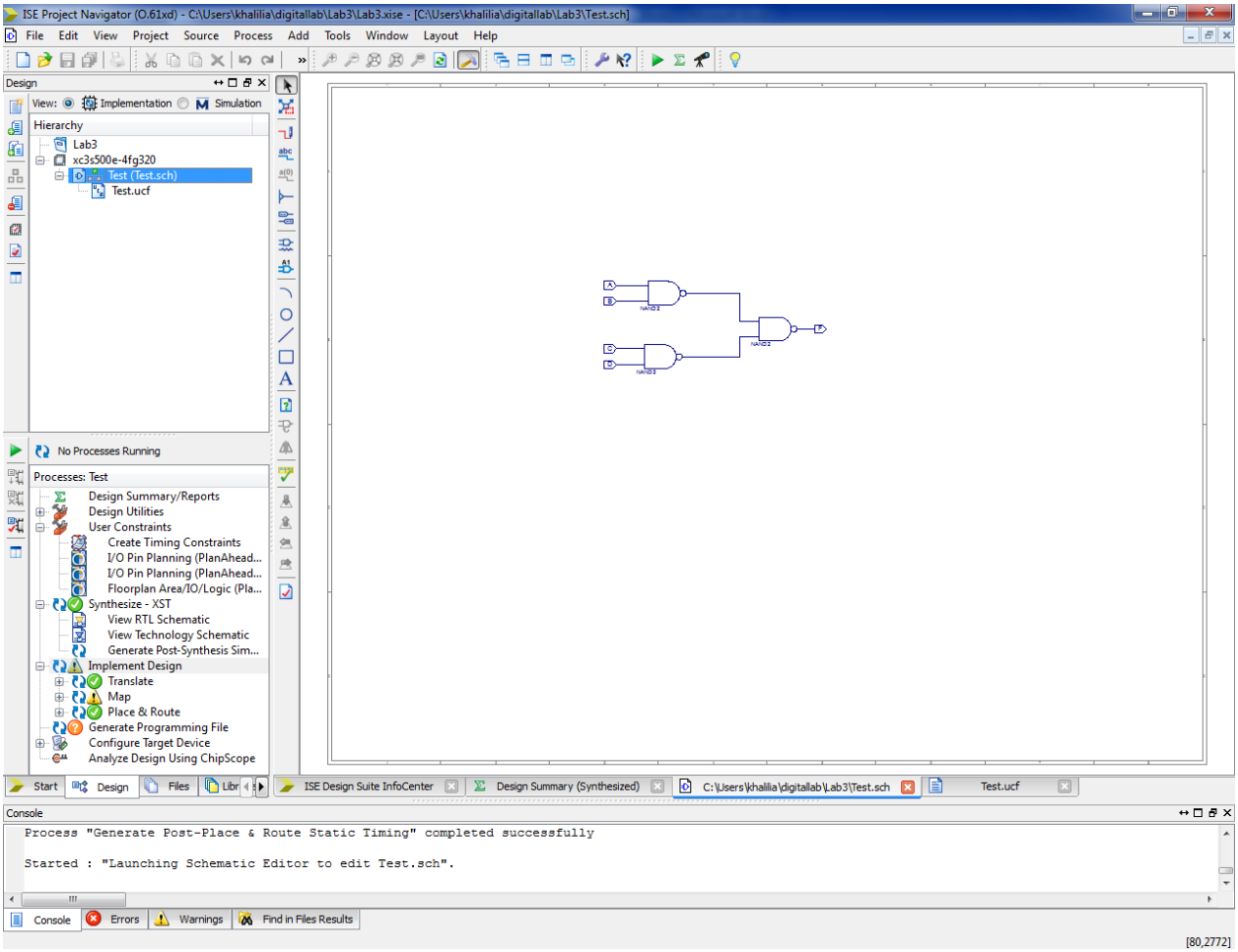
III) In the **I/O Ports** window, expand **Scalar ports,** there will be a list of all the input and output signals. These are the same as the I/O Markers in the schematic you created.

IV) Highlight an input and in the **I/O Port Properties** window assign a pin name in the empty box of the **Site** field (i.e. K17 is the input pin on the FPGA, which is connected to the SW3 of the **NEXYS2** board).



V) Repeat step **IV** for the rest of the inputs and output, when finished, hit the save icon and close the window. The pin assignments have been saved in a file with your schematic filename and .ucf extension. (Example: Test.ucf)

18) In the **Processes** window, Double-click on **Implement Design.** You should get the following window, with green check marks next to the **Implement Design** section.

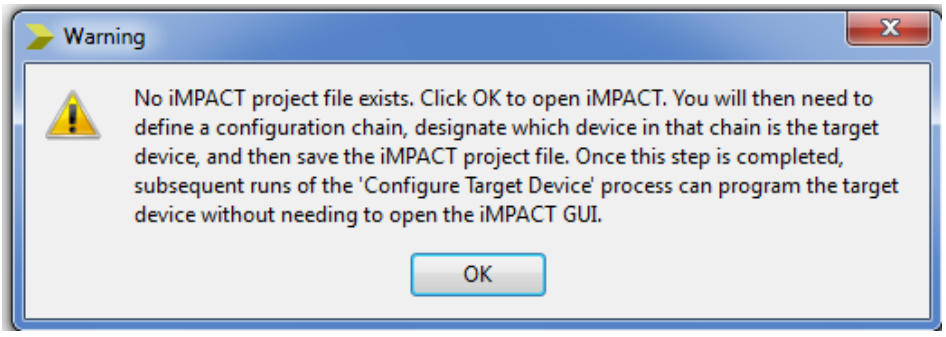


19) To download onto the FPGA on the NEXYS2 board:

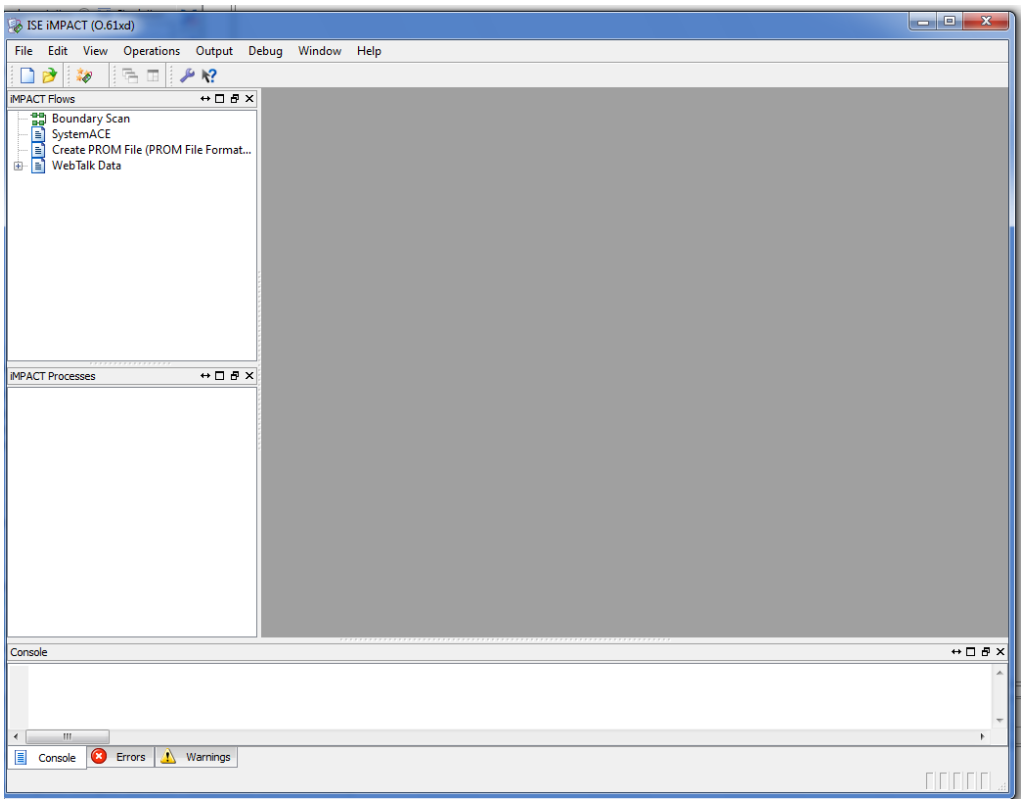
I) In the **Processes** window, double-click on **Generate Programming File** to generate the **Filename.bit** file. There should be a green check mark next to **Generate Programming File**.

II) Make sure your board is connected to the computer and it is turned on. Use the On/Off switch on the board.

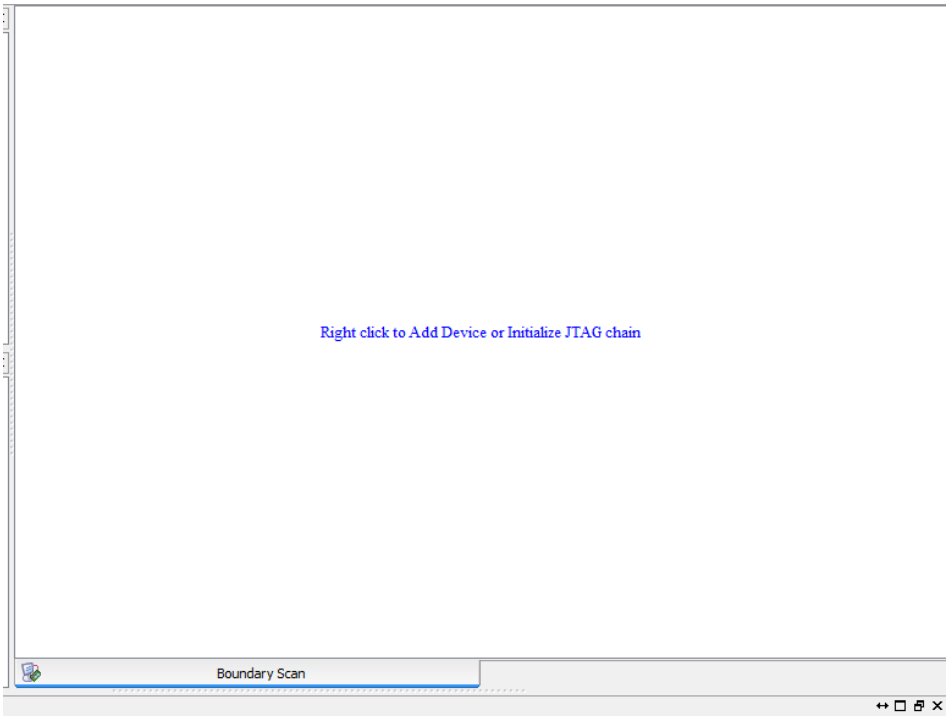
III) Double click on **Configure Target Device**. The following window will pop up**.**



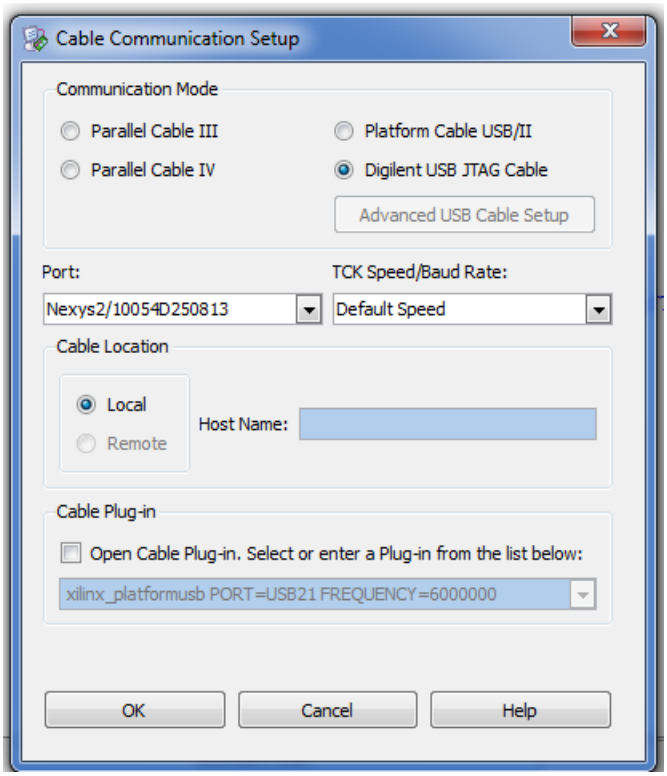
IV) Click on **OK**, you should have the following window. Double click on **Boundary Scan** in the **iMPACT Flows** window, the window in step **V** will pop up.



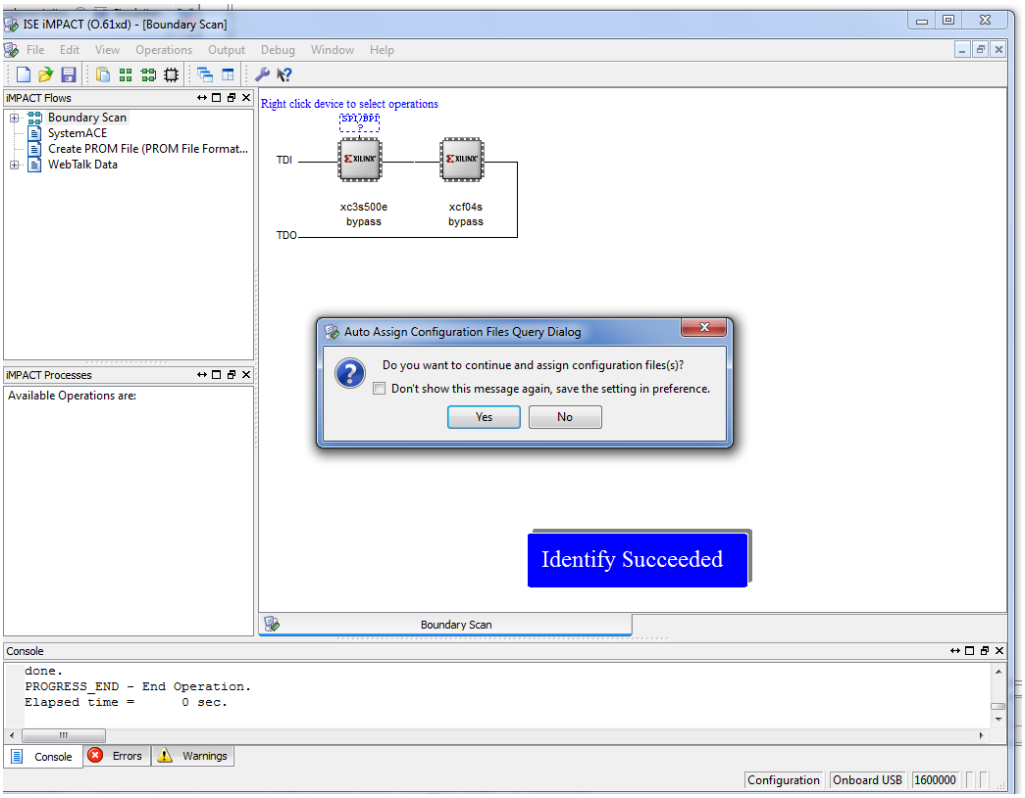
V) Right click on the message, and select **Cable Setup**. You should get the window in step **VI.**



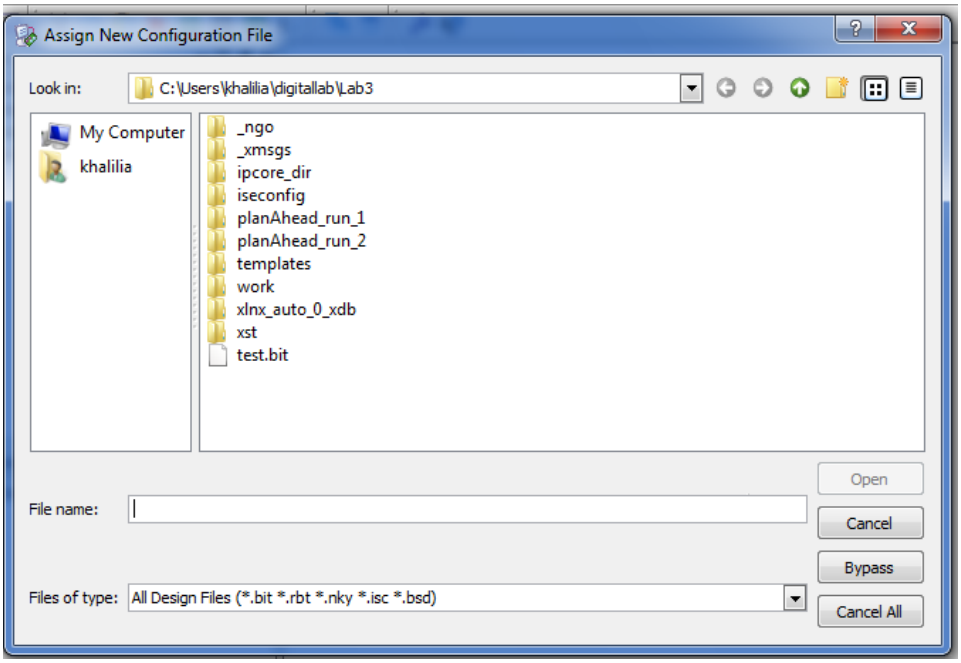
VI) Select **Digilent USB JTAG Cable** and click on **OK**.



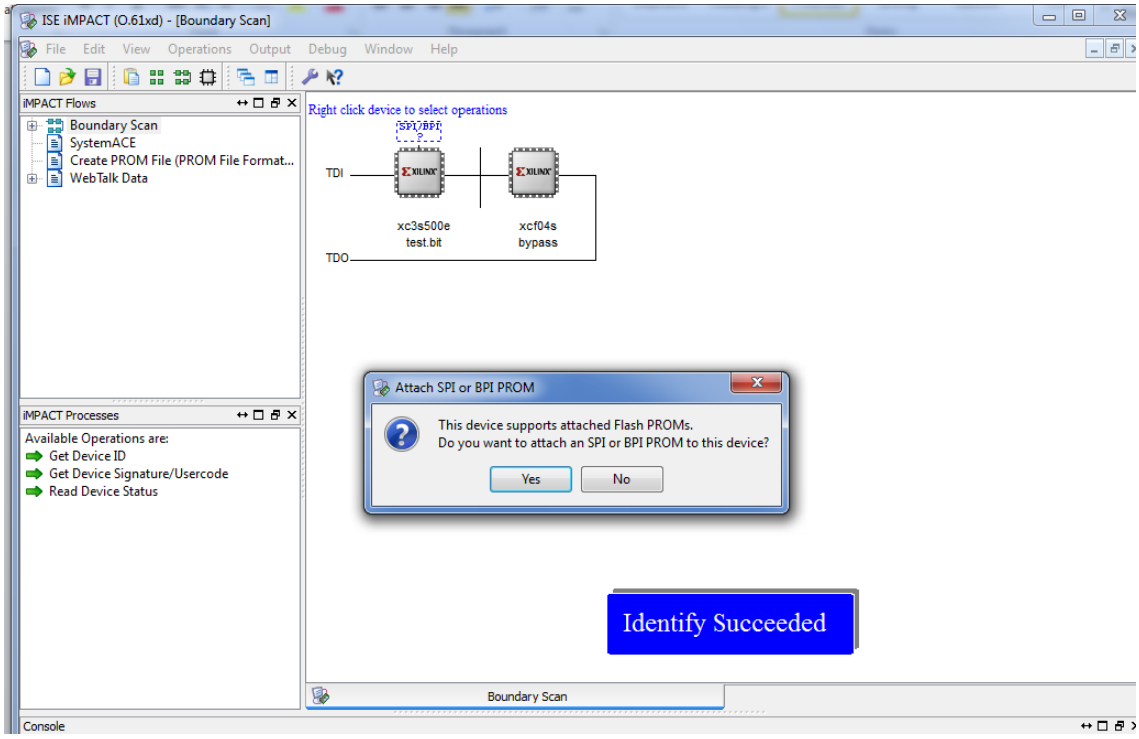
VII) Right click on **"Right click to Add Device or Initialize JTAG chain"**, and select **Initialize chain**. You should get the following window. Click on **Yes** and you should have the window in step **VIII**.



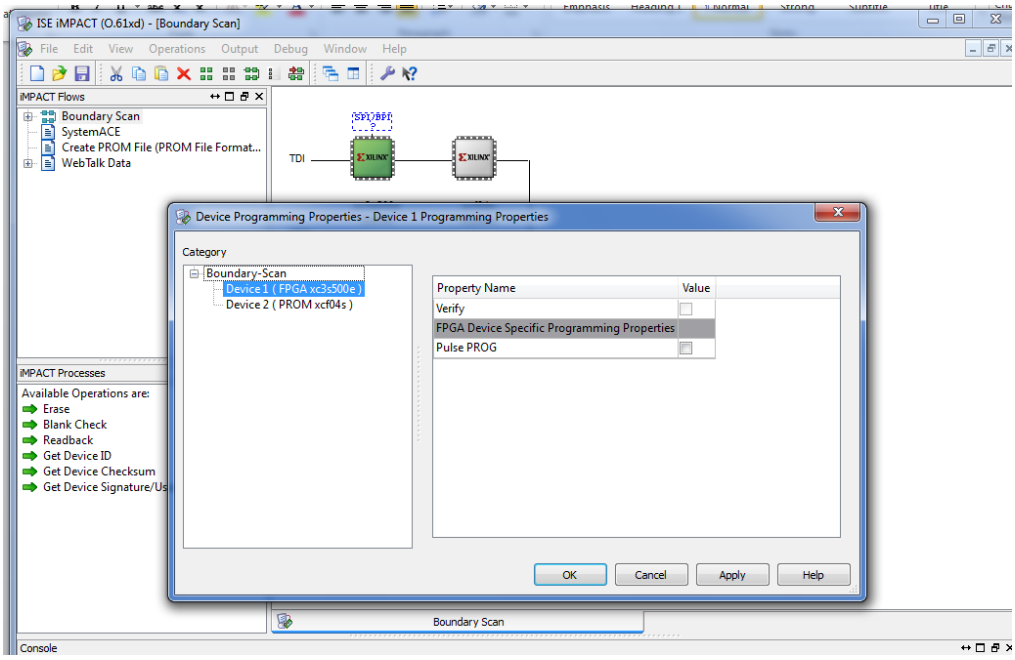
VIII) High light your **filename.bit** file, and click on open. You should have the window in step **IX.**



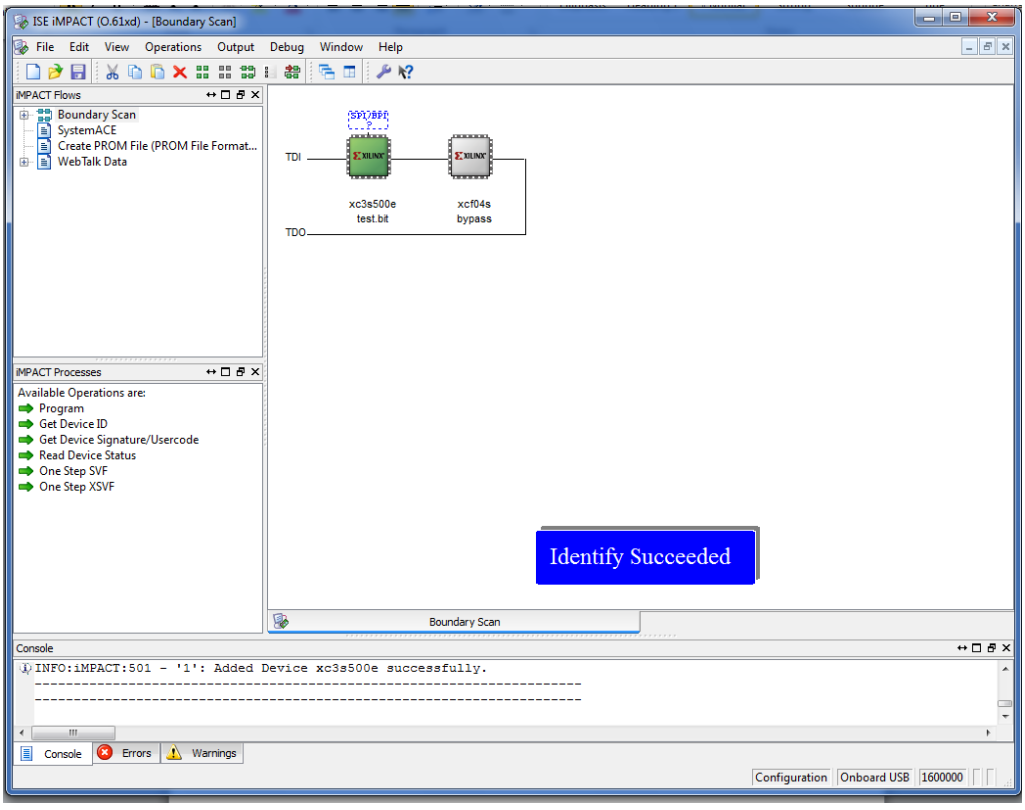
IX) Click on **NO**, then **Bypass** or **Cancel**. You should have the window in step **X**.



X) Click on **OK**, you should have the window in step **XI**.



XI) Right click on the high lighted chip, and select **program**. You have downloaded your circuit on the board. Test your circuit for all possible combinations.



20) To simulate a design with time delays included:

20.1 In the **Processes** window first, expand **Implement Design** next, expand **Place and Route,** and double click on **Generate Post-Place & Route Simulation Model.**

20.2 In the **Design** window, highlight your file and set the option to **Simulation**. Choose the **Post-Route** option from the list (default is the **behavioral** option).
In the **Processes** window expand the **ModelSim Simulator,** and double click on **Simulate Post-Place & Route Model**.

20.3 The ModelSim Simulator will launch. It may be behind the current windows.

20.4 The windows we are interested in are:

e. ModelSim SE 10.0b
f. Objects
g. Wave
h. Transcript

Make sure these are open.

20.5 In the **Transcript** window, type **restart** to erase the red lines in the **Wave** window.

20.6 Place driving patterns on your input lines using the **Modify → Force** option and set the inputs to:

a. A = 1 B = 0 C=0 D=0 and run the simulator for 10ns.
b. A = 1 B = 0 C=1 D=1 and run the simulator for 10ns.

20.7 Observe time delays in the waveforms.

NOTE: The report for this experiment should include:

I) A copy of your schematic diagram
II) A copy of the Behavioral Simulation results
III) A copy of the Post-Place & Route Simulation results
IV) Observations of time delays in the Post-Place & Route Simulation