## Digital Design Prelab #9: Synchronous Counters

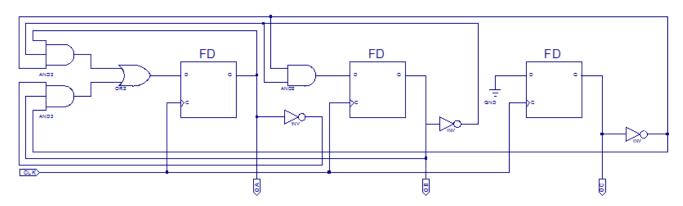
Charlie Coleman 2016 November 02

## 1A)

Present State			Next State (t+1)					
Q2	Q 1	QØ	D2	D 1	DØ	Q2	Q 1	QØ
Ø	Ø	Ø	Ø	1	Ø	Ø	1	Ø
Ø	Ø	1	Ø	1	1	Ø	1	1
Ø	1	Ø	Ø	Ø	1	Ø	Ø	1
Ø	1	1	Ø	Ø	Ø	Ø	Ø	Ø
1	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø
1	Ø	1	Ø	Ø	Ø	Ø	Ø	Ø
1	1	Ø	Ø	Ø	Ø	Ø	Ø	Ø
1	1	1	Ø	Ø	Ø	Ø	Ø	Ø

 $1XX \rightarrow \emptyset\emptyset\emptyset \rightarrow \emptyset1\emptyset \rightarrow \emptyset\emptyset1 \rightarrow \emptyset11 \rightarrow \emptyset\emptyset\emptyset$ 

1B)



```
2A)
entity UpDownCounter is
    Port ( CLK : in STD_LOGIC;
                    UpDown : in STD_LOGIC;
                    Q : inout STD_LOGIC_VECTOR(3 downto Ø));
end UpDownCounter;
architecture Behavioral of UpDownCounter is
signal D : STD_LOGIC_VECTOR(3 downto Ø);
begin
      process(CLK)
      begin
            if(CLK' event and CLK = '1') then
                  case UpDown is
                        when 'Ø' =>
                              case Q is
                                    when "ØØØ1" => D <= "1111";
```

```
when "0011" => D <= "0001";
                                             when "\emptyset1\emptyset1" => D <= "\emptyset\emptyset11";
                                             when "\emptyset111" => D <= "\emptyset1\emptyset1";
                                             when "1001" => D <= "0111";
                                             when "1011" => D <= "1001";
                                             when "1101" => D <= "1011";
                                             when "1111" => D <= "11\emptyset1";
                                             when others => D <= "0001":
                                     end case;
                              when '1' =>
                                     case Q is
                                             when "0001" => D <= "0011";
                                             when "\emptyset\emptyset11" => D <= "\emptyset1\emptyset1";
                                             when "\emptyset1\emptyset1" => D <= "\emptyset111";
                                             when "\emptyset111" => D <= "1\emptyset\emptyset1";
                                             when "1001" => D <= "1011";
                                             when "1011" => D <= "1101";
                                             when "11\emptyset1" => D <= "1111";
                                             when "1111" => D <= "ØØØ1";
                                             when others => D <= "ØØØ1";
                                      end case;
                              when others => D <= "XXXX";
                      end case;
                      Q <= D;
               end if;
       end process;
end Behavioral;
```