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Present State			Next State (t+1)					
Q2	Q1	Q0	D2	D1	D0	Q2	Q1	Q0
0	0	0	0	1	0	0	1	0
0	0	1	0	1	1	0	1	1
0	1	0	0	0	1	0	0	1
0	1	1	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0

```

entity UpDownCounter is
    Port ( CLK : in STD_LOGIC;
           UpDown : in STD_LOGIC;
           Q : inout STD_LOGIC_VECTOR(3 downto 0));
end UpDownCounter;

architecture Behavioral of UpDownCounter is

    signal D : STD_LOGIC_VECTOR(3 downto 0);

begin
    process(CLK)
    begin
        if(CLK' event and CLK = '1') then
            case UpDown is
                when '0' =>
                    case Q is
                        when "0001" => D <= "1111";
                    end case;
                end case;
            end case;
        end if;
    end process;
end Behavioral;

```

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        when "0011" => D <= "0001";
        when "0101" => D <= "0011";
        when "0111" => D <= "0101";
        when "1001" => D <= "0111";
        when "1011" => D <= "1001";
        when "1101" => D <= "1011";
        when "1111" => D <= "1101";
        when others => D <= "0001";
    end case;
when '1' =>
    case Q is
        when "0001" => D <= "0011";
        when "0011" => D <= "0101";
        when "0101" => D <= "0111";
        when "0111" => D <= "1001";
        when "1001" => D <= "1011";
        when "1011" => D <= "1101";
        when "1101" => D <= "1111";
        when "1111" => D <= "0001";
        when others => D <= "0001";
    end case;
    when others => D <= "XXXX";
end case;
Q <= D;
end if;
end process;
end Behavioral;

```