Digital Design Postlab #4: Full Adder

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Objective: The objective of this lab was to practice the design of a circuit based on given criteria. In the lab, we implemented a full adder and used that circuit to build a 3 bit full adder.

Design:

Cin	A	B	Cin	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Cout	00	01	11	10
0	0	0	1	0
0	0	1	1	1

$$C_{out}=C_{in}\left(A+B\right)+A\ B$$

S	00	01	11	10
0	0	1	0	1
0	1	0	1	0

$$S=C_{in}\left(\bar{A}\ \bar{B}+A\ B\right)+\bar{C}_{in}\left(\bar{A}\ B+A\ \bar{B}\right)$$

Procedure: We began the lab in Xilinx by drawing the design in a schematic file. The schematic was saved and compiled to correct any errors made. The circuit was then simulated for all input combinations using the behavioral simulation. These results were double checked for accuracy and printed. The circuit was then simulated for all input combinations with time delays using the Post-Route Simulation feature in the software. These results were also printed. The design was then downloaded onto the board, and the inputs were assigned to switches and the outputs were assigned to LEDs. Next, one of our single bit full adders was extended to a 3 bit adder with a single carry in and a single carry out resulting in a 4 bit result. This was done by creating a schematic symbol for the one bit adder. To create the schematic symbol, in the design window we highlighted the schematic file, and in the process window expanded the design and utilities tab. From here, create schematic symbol is an option. Next, a new schematic was created for the three bit adder. In symbols, in the schematic window, the design directory was selected in the categories window, and the symbol we just created was now available. We placed 3 copies of the one bit adder in the new schematic. We connected Cout0 to Cin1, and Cout1 to Cin2. We named every input and every output and saved the schematic. Finally, we compiled and simulated the 3 bit adder for the following combinations, and a copy of the results were checked and printed.

CIN	$A_2A_1A_0$	$B_2B_1B_0$
0	000	000
0	001	010
0	011	011
0	011	100
0	011	101
0	001	110
0	110	101
0	111	111
1	111	111

The combinations were tested by forcing 5ns for each combination. The 3 bit adder was then tested with time delays using Post-Route. Only the first 4 combinations above were used for the time delay, for 20 ns each. The 3 bit adder was then downloaded to the board and tested.

Data:

Cin	A2	A1	A0	B2	B1	B0	Cout	S2	S1	S0
0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	0	0	1	1
0	0	1	1	0	1	1	0	1	1	0
0	0	1	1	1	0	0	0	1	1	1
0	0	1	1	1	0	1	1	0	0	0
0	0	0	1	1	1	0	0	1	1	1
0	1	1	0	1	0	1	1	0	1	1
0	1	1	1	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1	1	1	1

Data Analysis: Based on the simulations run and the on-board testing, our circuit performed as was expected. The delays observed in the simulation showed that the delay for bit S2 was longer than the delay for S0, because it had to wait for the carry out from the second full adder, which had to wait for the carry out from the first full adder. The benefits of creating a simple full adder and combining multiple instead of creating a 3 bit full adder, because the number of inputs in a 3 bit full adder is 128, much larger than the 8 that were dealt with for this lab.

Conclusion: The goal of this experiment was to create a full adder and practice using that simple circuit to create one much more complex. During the simulation of the design, there was an incorrect file in that the Xilinx software was attempting to use. This caused errors that stopped us from simulating the design for a while, but once the file was removed, we were able to test our circuit and see that it worked properly.