Computer System Design Test #2 Note Sheet

ISA

CPU and ISA versions:

Processor	Address Bus	Data Bus	Control Bus
8086	20 bit	16 bit	
8088	20 bit	8 bit	
80286	24 bit	16 bit	
80386 80486 Pentium I Pentium II Pentium III	32 bit	32 bit	
Pentium IV	32/36 bit	32 bit	
Pentium D	32/36 bit	32/64 bit	

Address Time: Driven by internals of the processor, the PCLK cycle where address is output (Ts)

Data Time: Driven by internals of processor, the PCLK cycle(s) where data is sent/recieved (Tc)

Wait State: Driven by ICs outside the processor when >1 PCLK is needed to complete work

Ready_n: Signal that allows external devices to insert wait states

Address Space, IO Space:

Memory map

64KB Boot ROM
64KB Option ROM
128KB Device ROM
128KB Video Memory
640KB Conventional Memory

I/O Map

I/O Sub Range	
0000h to 001Fh	DMAC1CS#
0020h to 003Fh	PIC1CS#
0040h to 005Fh	PITCS#
0060h to 007Fh	MISC1CS#
0080h to 009Fh	MISC2CS#
00A0h to 00BFh	PIC2CS#
00C0h to 00DFh	DMAC2CS#
00E0h to 00FFh	NCPCS#

Address Decoders: Typically made using a MUX, unique address lines as the select lines and M/IO# going into the enable

Register:

AX: General Purpose Register (GPR), ALU input and the output

BX: GPR, ALU input

CX: GPR or the loop index

DX: GPR, holds values in fast memory

CS: Code Seg Reg, holds start of code seg

DS: Data Seg Reg, points to user variables

SS: Stack Seg Reg, start of stack

ES: Extrasegment Reg, stores an extra segment

IP: Instruction Pointer, inside the current CS

SP: Stack pointer, inside the current SS

Address Generation from Registers: Shift CS left by 4, add IP. Carry bit is saved in >286

Little-Endian Byte Ordering: LSB at the lowest address

Extended Memory: Memory past 1Meg, accessable by a 286 in real mode (carry out of CS+IP is 1)

Cardinal Rules:

1. In any system based on the X86 microprocessors, every memory and I/O storage location contains 1 byte, no more or less.
2. Every memory and I/O address is considered to be either an even or odd address
3. When the 80286 microprocessor reads from or writes to an even address, the data is transferred over the lower data path. Upper path for an address.

Control Signals:

Processor Signals:

BHE#: Byte High Enable, D15-D8 are used in transfer

A0: Odd (1) or even (0) address accessed

M/IO#	S1#	S0#	Cycle Type	ISA Line Assert
0	0	0	Interrupt ack.	none
0	0	1	I/0 read	IOWC#
0	1	0	I/0 write	IORC#
1	0	0	Halt shutdown	none
1	0	1	Mem read	(S)MWTC#
1	1	0	Mem write	(S)MRDC#

Bus Signals:

Upper Enable: Read the name

Lower Enable: Read the name

Copy Enable: copy from upper half to lower

DT/R#: Data transmit/recieve, tell tranceivers what direction to allow flow

Copy Enable: turns on/off steering logic

SA0: Same as A0

Bus Mastering:

HOLD: input to the processor requesting the processor stop driving the bus

HLDA: output from the process indicating the bus is now undriven

LOCK#: output from processor, set by software indicating the current instruction set is being executed atomically

Power on Reset: Holds the processor in reset for a certain amount of time after turn on

First Bus Cycle: CS and IP set to F000h and FFF0h respectively. First instruction from top 16 bytes of memory space.

Address Latch: see SA

LA vs. SA:

LA: Latchable address lines, on the 16 bit half, updated before address phase to allow mem cards to perform bank selection

SA: Latched version of the processor address lines on lower half. Presented during address phase, held until next address phase.

ALE: Add. Latch En., indicates address lines valid

Bus Steering Logic: routes data from up half to low half, needed for 8 bit compatibility

Data Bus Transceivers: half duplex latches that control data flow direction on up/low halves of bus

Stretching the Transfer Time (Wait States): For operations that require more than 1 PCLK cycle

Default Wait States / Ready Timers:

16-bit RAM	1	8-bit RAM	4
16-bit I/0	1	8-bit I/0	4

NOWS#: reduces the number of wait states to 0 for 16-bit, 1 for 8-bit

CHRDY#: card forces extra wait states by deasserting

Protected Mode vs. Real Mode:

Protected Mode: Only have access to 1M of memory, compatible with 8086

Real Mode: Have acces to 1M + the extended memory, compatible with 80286+

ISA Bus Structure:

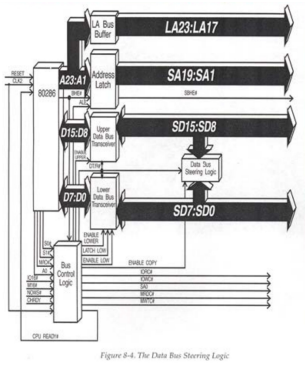

Figure 8-4. The Data Bus Steering Logic

ISA Bus Cycle Timing:

BCLK: Derived from input clock, designed to be 8MHz

Device Size Indication:

M16#: signals whether a device is capable of 16 bit memory transactions. 0 = 8 bit device. 1 = 16 bit

I016#: Sames as M16#, but for I/O devices

ISA Bus Cycles:

Detailed view of 286 Bus Cycle:

Detailed View of ISA Bus Cycle: