Final Project for Digital Design Lab

Design and Implementation of an Alarm System for a Safe

Objective:

1. To design a finite state machine for an alarm system.
2. To use VHDL to define a finite state machine.
3. To implement the finite state machine of the alarm on a FPGA,
4. To experimentally check the operation of the alarm system

Problem statement and specifications:

Design an alarm system for a safe that has five input push-buttons: X_4, X_3, X_2, X_1 and X_0. Assume that the buttons cannot be pressed simultaneously (an electromechanical interlock guarantees this). The alarm system should have the following features:

1. The three states are:
   A. Reset State
   B. Armed State
   C. Alarm state

2. The alarm system cannot be turned on if door of the safe is open.
   The system should also have an asynchronous reset signal to go to the reset state.

3. A. The combination for turning on (arming) the alarm system is **X_3-X_1-X_1-X_4-X_2**.

Arming sequence:	X_4	X_3	X_2	X_1	X_0	Note: One button at a time is pressed.
	0	1	0	0	0	press
	0	0	0	0	0	release
	0	0	0	1	0	press
	0	0	0	0	0	release
	0	0	0	1	0	
	0	0	0	0	0	
	1	0	0	0	0	
	0	0	0	0	0	
	0	0	1	0	0	
	0	0	0	0	0	

B. If any wrong button is pressed during the arming sequence, the system should go back to the Reset state and the sequence should be reentered.

4. For turning off (disarming) the system from the ARMED state, the combination **X_1-X_4-X_2-X_0-X_2** should be pressed.

Disarming sequence: X_4 X_3 X_2 X_1 X_0 Note: One button at a time is pressed.

0	0	0	1	0	press
0	0	0	0	0	release
1	0	0	0	0	press
0	0	0	0	0	release
0	0	1	0	0	
0	0	0	0	0	
0	0	0	0	1	
0	0	0	0	0	
0	0	1	0	0	
0	0	0	0	0	

5. In order to prevent tampering with the alarm system, an ALARM signal will get activated if any wrong button was pressed. However, in order to make it harder to figure out the right sequence:

   A. We don't want the alarm signal to get activated after the first wrong button has been pressed. Instead, the alarm signal should get activated after pressing 5 buttons, as long as one of the 5 buttons pressed is a wrong one. (e.g. the sequences X_1-X_0- X_1-X_2-X_0, X_2-X_1-X_0-X_2-X_1, X_0-X_4-X_2-X_0-X_2, etc. would trigger the alarm.)

   B. While disarming, pressing the sequence **X_3-X_3** from any state, **except** the ARMED and ALARM states should get the system back to the ARMED state. (X_3-X_3 during 2nd through 4th pushes should get the system back to the ARMED state.)

6. The only way to get out of the ALARM state is by pressing the **X_0-X_2-X_4-X_4** sequence. (It goes back to the ARMED state.) If any wrong button is pressed during the sequence, the system should go back to the ALARM state and the sequence should be reentered.

7. Use as few states as possible without compromising the operation or security of the alarm system.

8. The alarm system should have two output signals ARMED_out and ALARM _out.

   A. When the system is armed and there is no tampering then ARMED_out = 1 and ALARM_out = 0.
   B. When armed and there is tampering (after 5 presses) then ARMED_out = 1 and ALARM_out = 1.
   C. When it is disarmed then ARMED_ out= 0 and ALARM_out= 0.

Pre-lab: Please turn in parts 1 through 3 by Monday Nov. 14, 3:30 PM.

1. As with any project specifications not all possibilities may be covered. Feel free to make reasonable assumptions and state them clearly.

2. Draw the state diagram for the Alarm system design. If you make assumptions because not everything was specified, include them in your pre-lab. Indicate what each state represents, the input conditions that cause the state transitions, and the corresponding outputs.

3. Design an experiment to test your prototype. The experiment should include a list of test vectors.

Turn in part 4 by Thursday November 17, at the beginning of Lab hour.

4. Implement your design using VHDL code.

Lab Report:

1. Follow the guidelines provided at the beginning of semester.
2. Include state diagram, final VHDL source file, simulation printouts.

Time Line and grading:

	Due Dates	Grading
Pre-lab: Parts 1 − 3	**Monday November 14 (3:30 PM)**	**85 pts (50% off of late pre-lab)**
Pre-lab Part 4	**Thursday November 17 (Beginning of lab hour)**	**5 pts**
Operational design	**Thursday November 17**	**70 pts**
Lab report	**Monday November 28**	**40 pts**
	Total	**200 pts**