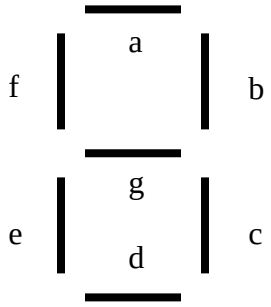
Experiment # 5
7-Segment Decoder Driver

Objective: To design and test a hex seven segment decoder driver.

Prelab:
Design the seven circuits required to drive a 7-segment hex display from a 4 bit binary input. Use K-maps. The seven segment displays on the board are active low, it means the segments on each display will light up, when driven low.
Turn in a copy of your design at the beginning of the lab hour. (Truth Table and K-maps)

The output patterns should match the following table:

The following diagram shows the segments' assignments.



Experiment:

1) Create a new project. In your new project create individual schematics for each segment containing your designs from the preliminary. (The design for all segments will not fit in a single schematic file.) Make schematic symbols for each segment. Open a new schematic file and add schematic symbols of each segment in your new schematic file. Connect the appropriate inputs together and add I/O markers to the inputs and outputs.

NOTE1: When the software makes the schematic symbols, it may rearrange the order of the inputs or outputs on the schematic symbol. Therefore, make sure you are accessing the intended input or output.

NOTE2: There are four 7-segment displays on the **NEXYS2** board and their inputs (a-g) are all connected to the same lines. Each 7-segment display has an enable line, that needs to be driven low for enabling the display. Therefore you need an output line from the design that can control enable input of the 7-segment display. You need to add a buffer to the schematic with I/O markers. When assigning pins in your .ucf file, make sure the output of this buffer is connected to the enable line of one of the 7-segment displays. (AN0 = pin F17, AN1 = pin H17, AN2 = pin C18, AN3 = pin F15). The input of this buffer can be connected to any available switch of the board.

2) Simulate your 7-segment driver design for all possible input combinations.

(For simulation : Use clock and assign 16ns for MSB (bit3)
8ns for (bit2)
4ns for (bit1)
2ns for (bit0)
Simulate for 20 ns.)

Check the simulation results for accuracy of your design.

3) Simulate the circuit for the following input combinations with time delays included (Post-Route Simulation). Print the simulation results. A copy of the simulation results should be submitted with your lab report. (Step 20 from lab #3)
Simulate each combination for 15ns.

A	B	C	D
0	0	0	1
0	0	1	0
0	1	0	0

4) Download and test your design for all possible input combinations.

5) Create a schematic symbol of your seven segment design.

6) Copy the schematic files of the one-bit-adder and three-bit-adder from lab 4 and paste it in your current working directory. Next use **Add Source** to add these two files to your current project. Highlight the-one-bit adder file and click on **Create Schematic Symbol**.

7) Open the three-bit-adder schematic file, and remove the **output markers** from the three-bit adder.

8) Place a copy of your **7-segment symbol** into the three-bit-adder schematic file.

9) Connect the **carry out** from your adder to the MSB input of your 7-sgement and the **sum(2:0)** to the other appropriate inputs. Place output markers on the outputs of your 7-segment decoder. Save the schematic. Synthesize the schematic file.

10) No simulation is required.

11) Download and test your design for the following input combinations.

CIN	A(2:0)	B(2:0)
0	000	000
0	001	010
0	011	011
0	011	100
0	011	101
0	001	110
0	110	101
0	111	111
1	111	111

Question: In your report state your observations of time delays in the seven segment decoder.

Note: A copy of schematic diagram of each segment, a copy of schematic diagram of the seven segment decoder, and the simulation results of the seven segment decoder should be included in the report. For the second part, (three-bit-adder and the seven segment decoder) submit only the schematic diagram.