HW2 Report

姓名：金家逸　學號：B10502076 系級：電機三

```
Statistics for case statements in always block at line 72 in file
        '/home/raid7_2/userb10/b0502010/HW2/01_RTL/HW2.v'
================================================
|           Line           |  full/ parallel  |
================================================
|            73            |    auto/auto     |
================================================

Statistics for case statements in always block at line 113 in file
        '/home/raid7_2/userb10/b0502010/HW2/01_RTL/HW2.v'
================================================
|           Line           |  full/ parallel  |
================================================
|           116            |    auto/auto     |
================================================

Statistics for case statements in always block at line 192 in file
        '/home/raid7_2/userb10/b0502010/HW2/01_RTL/HW2.v'
================================================
|           Line           |  full/ parallel  |
================================================
|           193            |    auto/auto     |
================================================

Statistics for case statements in always block at line 213 in file
        '/home/raid7_2/userb10/b0502010/HW2/01_RTL/HW2.v'
================================================
|           Line           |  full/ parallel  |
================================================
|           215            |    auto/auto     |
================================================
```

```
Inferred memory devices in process
        in routine ALU line 259 in file
                '/home/raid7_2/userb10/b0502010/HW2/01_RTL/HW2.v'.
===============================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|     counter_reg     | Flip-flop |   5   |  Y  | N  | Y  | N  | N  | N  | N  |
| shift_register_reg  | Flip-flop |  64   |  Y  | N  | Y  | N  | N  | N  | N  |
|      state_reg      | Flip-flop |   2   |  Y  | N  | Y  | N  | N  | N  | N  |
|    operand_b_reg    | Flip-flop |  32   |  Y  | N  | Y  | N  | N  | N  | N  |
|      inst_reg       | Flip-flop |   3   |  Y  | N  | Y  | N  | N  | N  | N  |
|      done_reg       | Flip-flop |   1   |  N  | N  | Y  | N  | N  | N  | N  |
===============================================================================
Presto compilation completed successfully.
Current design is now '/home/raid7_2/userb10/b0502010/HW2/01_RTL/ALU.db:ALU'
Loaded 1 design.
Current design is 'ALU'.
ALU
```