NTUEE DCLAB

Introduction to SpyGlass

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DCSL

Introduction to SpyGlass Lint

- The SpyGlass platform provides designers with insight about their design, early in the process at RTL
- SpyGlass Lint is a comprehensive HDL design rule checker
- We can use SpyGlass Lint to check the coding style of our design and if it is synthesizable

Before Using SpyGlass

- Source the environment settings of CAD tools.

```
source /usr/cad/synopsys/CIC/license.csh
```

```
source /usr/cad/synopsys/CIC/spyglass.cshrc
```

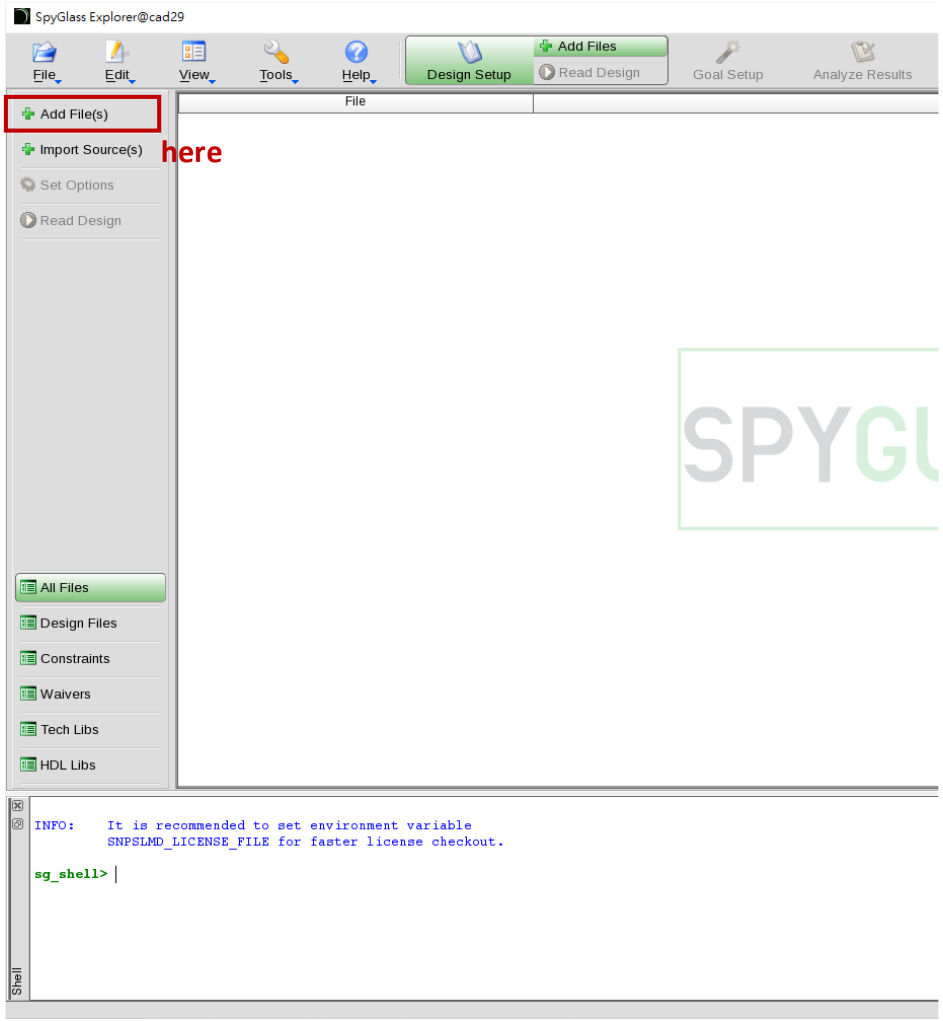
Start SpyGlass

- Type the following command

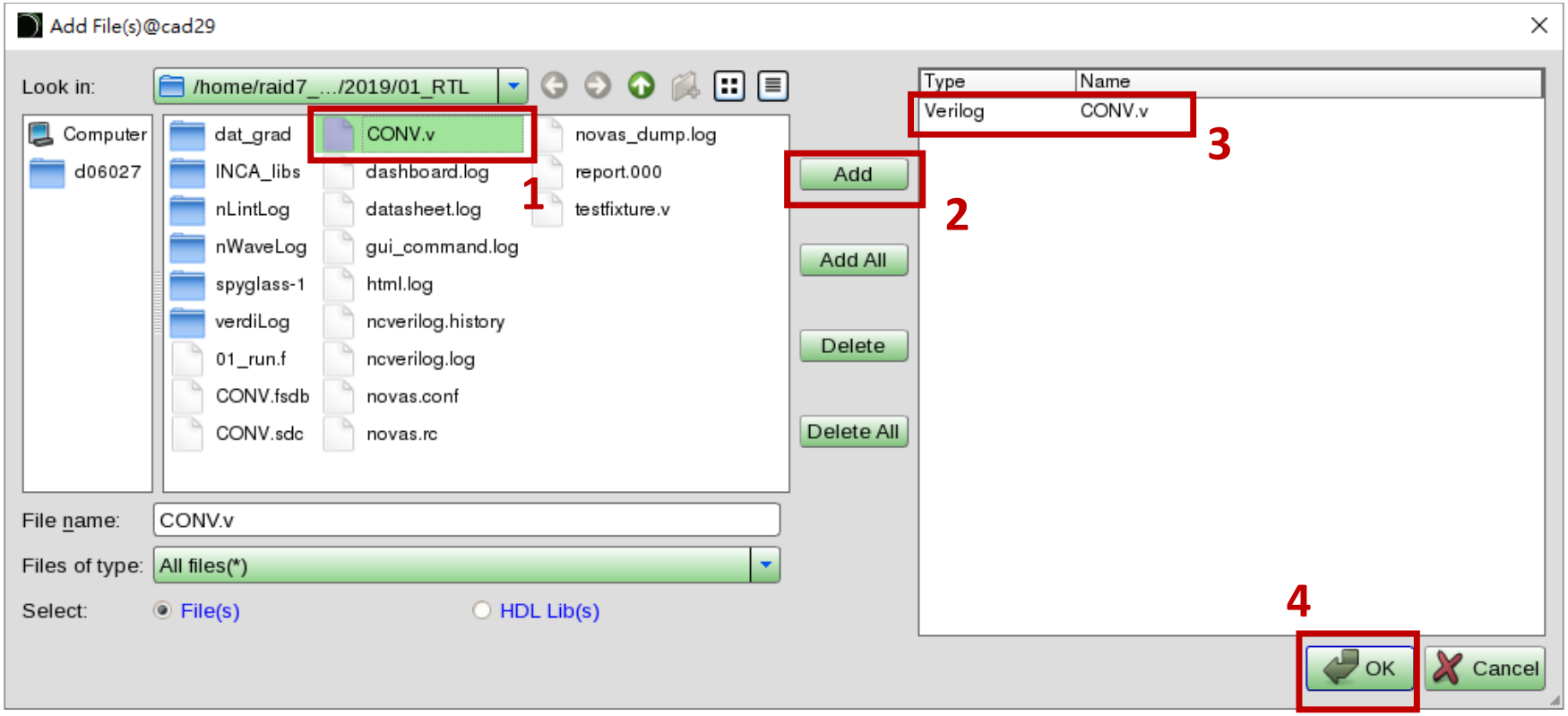
```
spyglass &
```

- The token “&” enable you to use the terminal while Verdi is running in the background.

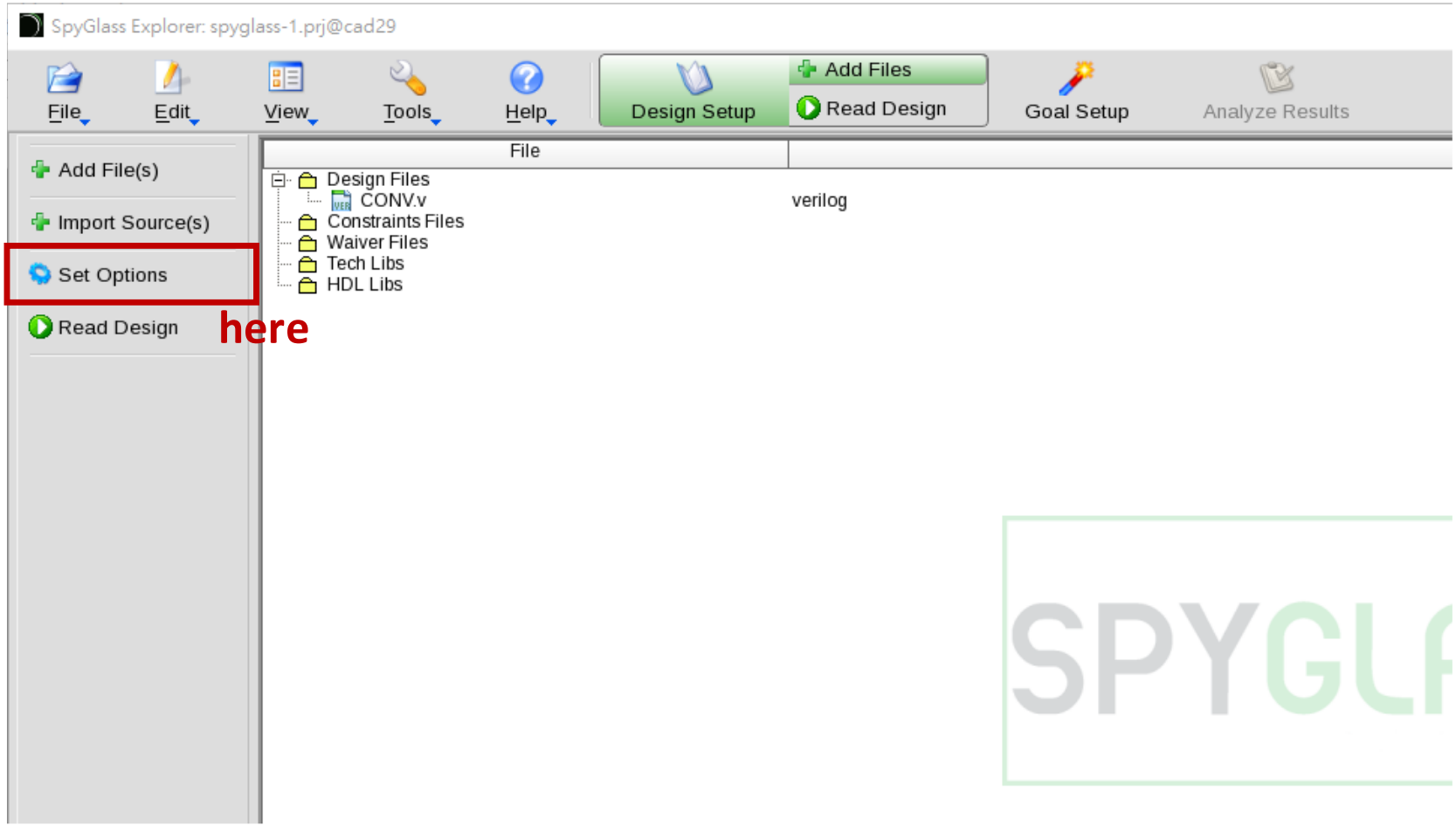
Specify the Design File



Specify the Design File



Specify Top Module Name



Specify Top Module Name

SpyGlass Explorer: spyglass-1.prj@cad29

File Edit View Tools Help | Design Setup | Add Files | Read Design | Goal Setup | Analyze Results

- Add File(s)
- Import Source(s)
- Set Options
- Read Design

☐ Advanced Options

Option	Value
Top Level Design Unit	**CONV**
Stop Design Unit(s)	
Ignore Design Unit(s)	
Diveable Block Abstracted Design Unit(s)	
Interpret Pragma(s)	
Ignore VHDL code within pragma block 'translate'	☐
Ignore VHDL code within pragma block 'synthesis'	☐
Enter Macros for Analysis	
Set HDL Parameter(s) Value	
Searches the specified paths for include files	
Specify the library files in the source design	
Specify the library directories containing libraries	
Specify library file extensions	
Enable System Verilog Processing	☐
Enable auto-compilation of gateslib into sglib	☐
Allow Duplicate Module Names in Verilog Designs	☐
Disable Verilog 2k Processing	☐
Run in VHDL87 Compatibility Mode	☐
Automatically Sort VHDL File(s)	

Read Design

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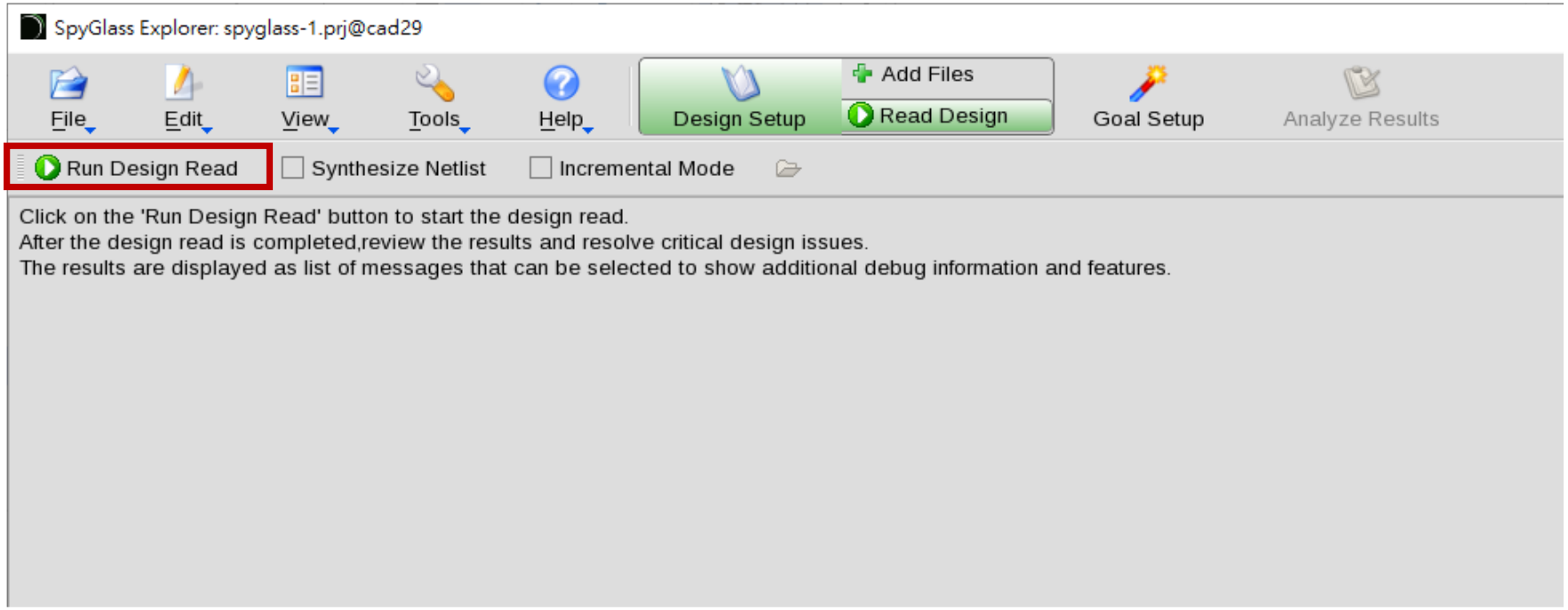
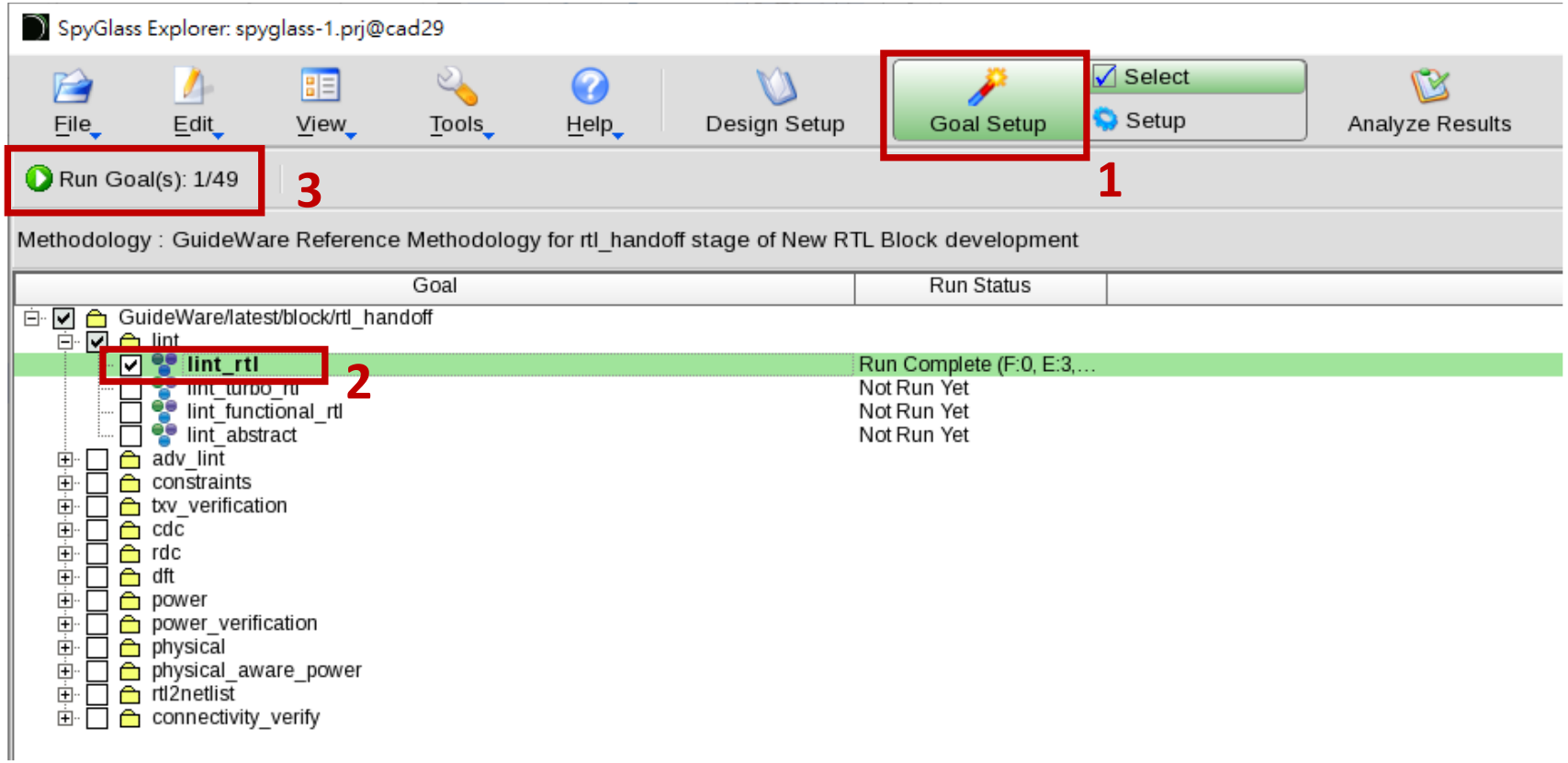
Read Design


SpyGlass Explorer: spyglass-1.prj@cad29
File
Edit
View
Tools
Help
Design Setup
Add Files
Read Design
Goal Setup
Analyze Results
Run Design Read
Synthesize Netlist
Incremental Mode
Click on the 'Run Design Read' button to start the design read.
After the design read is completed,review the results and resolve critical design issues.
The results are displayed as list of messages that can be selected to show additional debug information and features.

Goal Setup


SpyGlass Explorer: spyglass-1.prj@cad29
File
Edit
View
Tools
Help
Design Setup
Goal Setup
Select
Setup
Analyze Results
Run Goal(s): 1/49
3
1
Methodology : GuideWare Reference Methodology for rtl_handoff stage of New RTL Block development
Goal
Run Status
GuideWare/latest/block/rtl_handoff
lint
lint_rtl
2
Run Complete (F:0, E:3,...
lint_turbo_rtl
Not Run Yet
lint_functional_rtl
Not Run Yet
lint_abstract
Not Run Yet
adv_lint
constraints
txv_verification
cdc
rdc
dft
power
power_verification
physical
physical_aware_power
rtl2netlist
connectivity_verify

Message Window