

數位電路實驗

Lab 3

數位錄音機

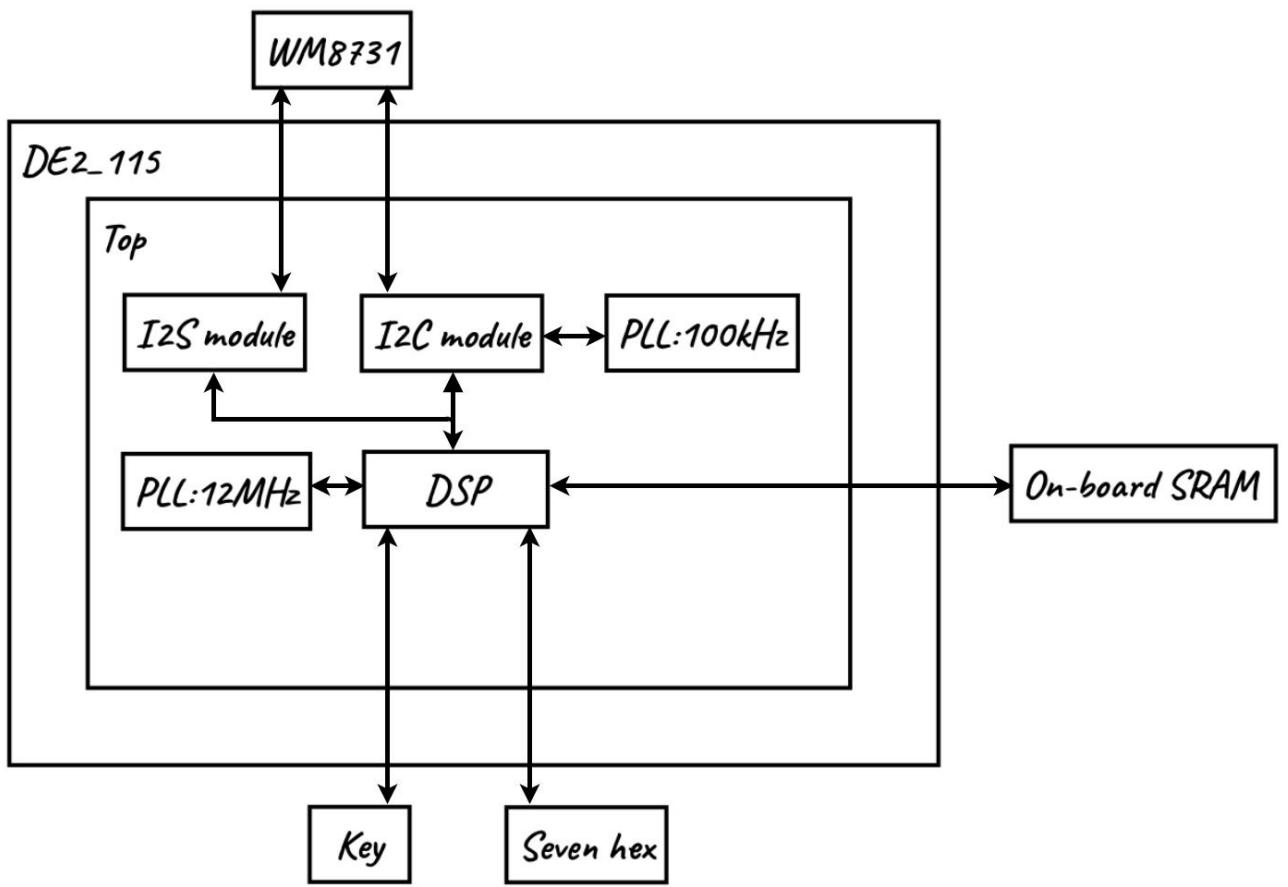
Team 02

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1. Introduction:

We created a recording device capable of capturing 32 seconds of audio with additional features like normal play, fast play, and slow play. The play speed is adjustable, ranging from 2 to 8 times the normal speed. Additionally, we incorporated a feature that displays the current playback time in seconds.

2. System Architecture:



(1) AudDSP.sv:

Processing the audio data read from SRAM in various ways, including normal play, fast play, and slow play, with slow play further divided into constant interpolation and linear interpolation. The processed data is then provided to AudPlayer.

(2) AudPlayer:

Transmitting the audio data processed by AudDSP to the WM8731 chip inside the FPGA, which then plays the audio.

(3) AudRecorder.sv :

Receiving audio data from WM8731 and extracting data from one of the audio channels, then saving it to SRAM.

(4) I2cInitializer.sv

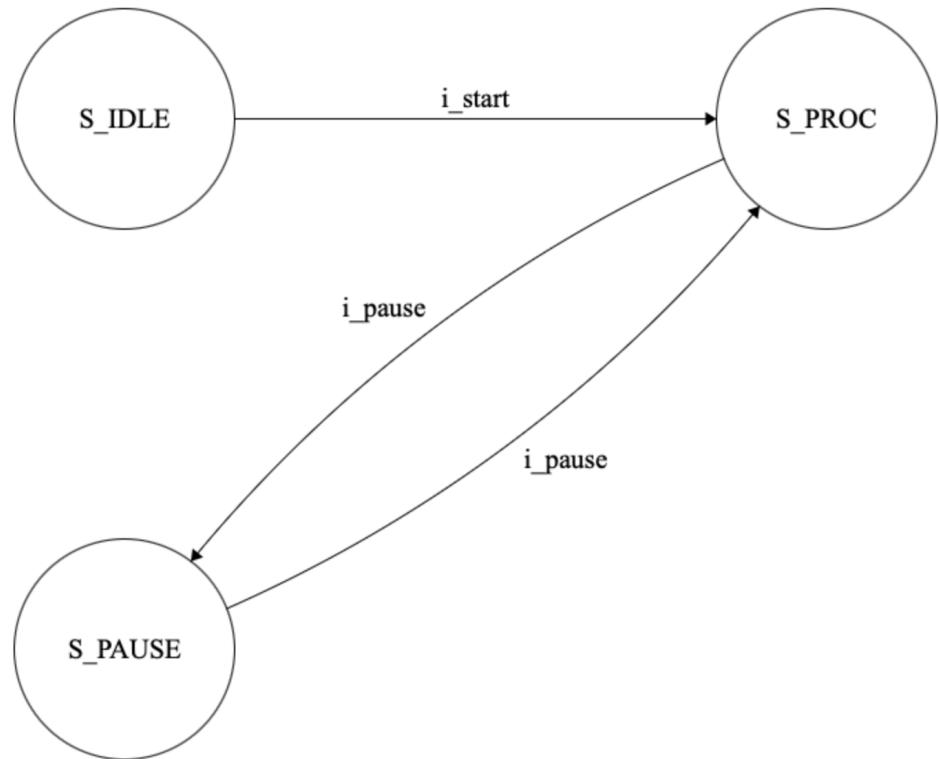
Initializing the WM8731 chip inside the FPGA using the I2C protocol.

(5) Top.sv

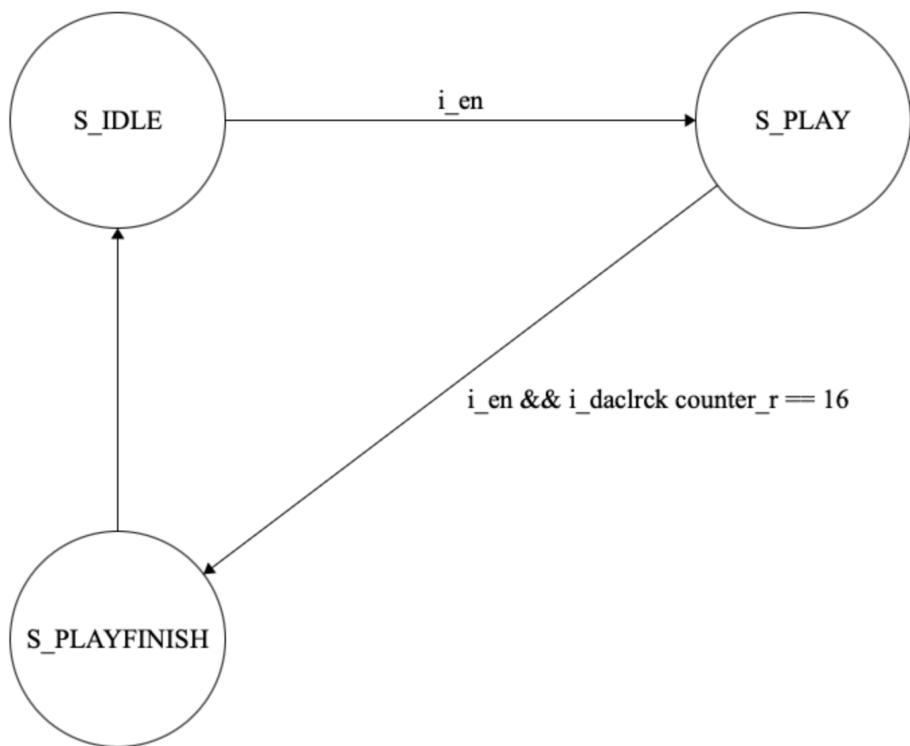
Control the operations between each submodule to achieve various logical operations from recording to playback, including record, pause record, stop record, play, pause play, stop play, and the ability to repeat play after stopping.

3. Finite state machine:

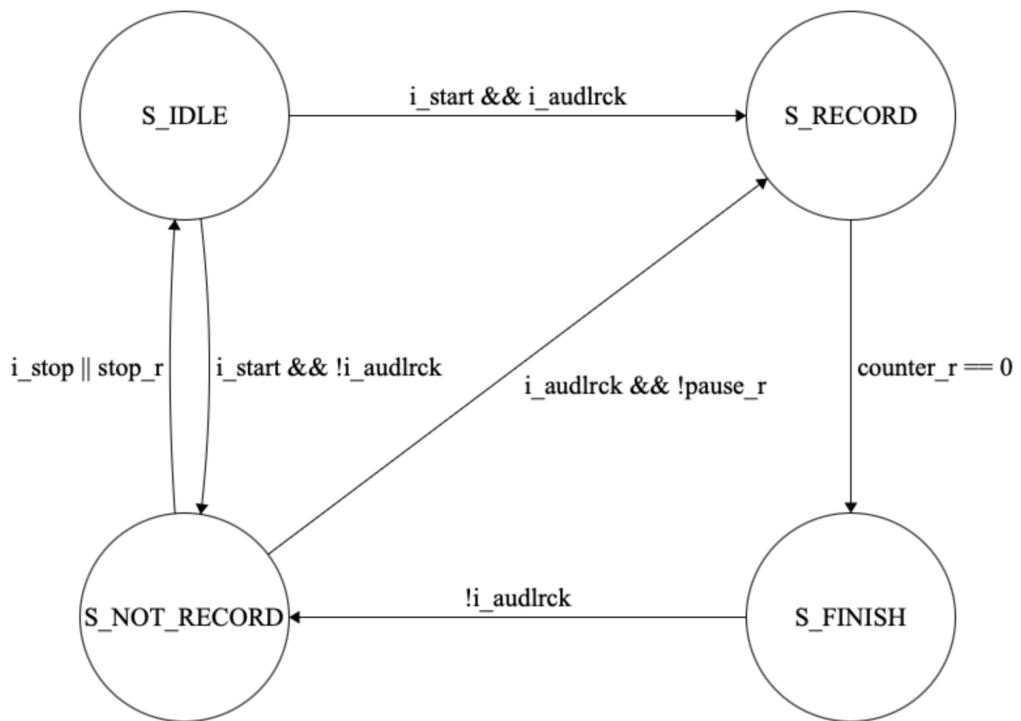
a. AudDSP.sv:



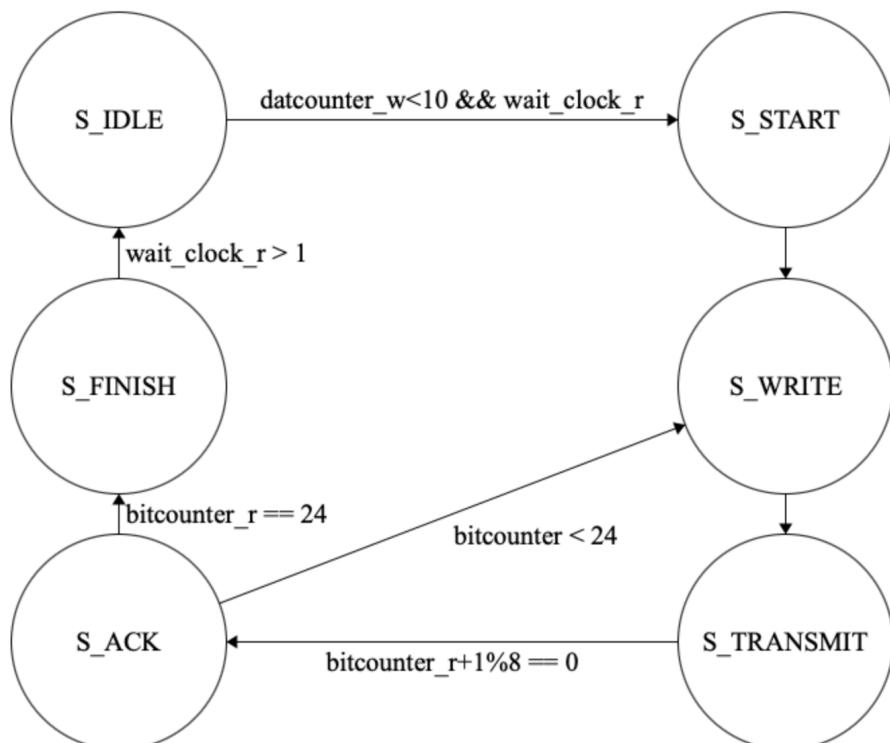
b. AudPlayer:



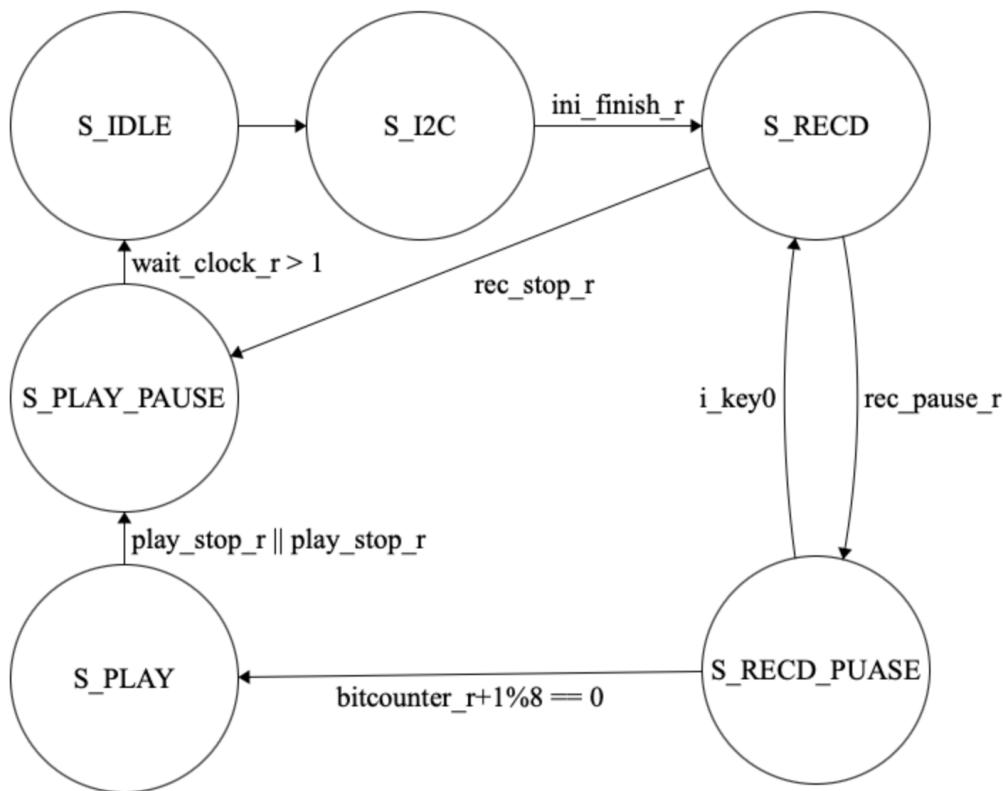
c. AudRecorder.sv :



d. I2cInitializer.sv



e. Top.sv



4. File Structure:

```

team02_lab3/
├── team02_lab3_report
└── src/
    ├── alltpl11_qsys.v
    ├── alltpl11_qsys.qip
    ├── DE2_115.sv
    ├── AudDSP.sv
    ├── AudPlayer.sv
    ├── AudRecorder.sv
    ├── I2cInitializer.sv
    ├── SevenHexDecoder.sv
    ├── Debounce.sv
    └── Top.sv
  
```

5. usage steps:

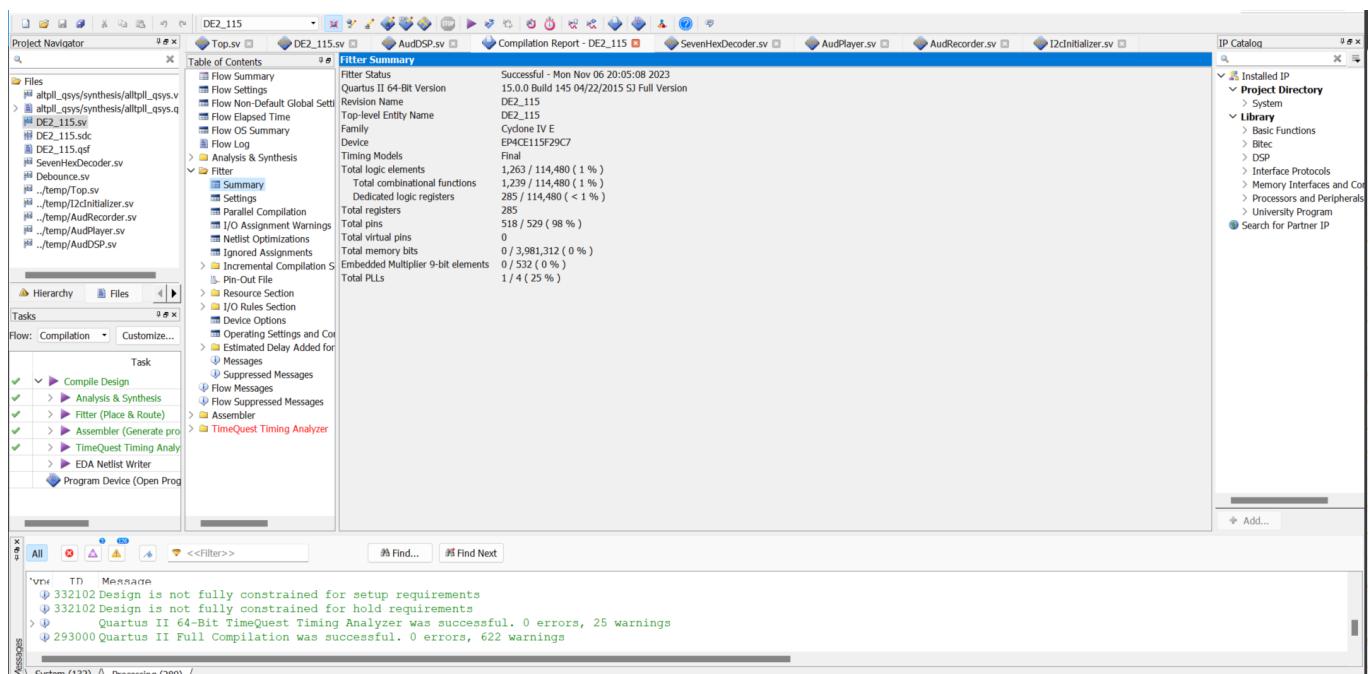
- (1) Press key 3 to reset (move to state 3).
- (2) Press key 0 to start recording (move to state 2). Pressing key 0 will pause the recording (move to state 3), and pressing key 0 again will resume recording (move back to state 2).
- (3) During recording, pressing key 2 will stop the recording (move to state 5).
- (4) Use switches 0 to 3 to adjust the speed (2x to 8x), and switches 4 and 5 to adjust the mode (0: original speed, 1: fast, 2: constant interpolation, 3: linear interpolation).
- (5) Press key 0 to start playing (move to state 4). Pressing key 0 will pause playing (move to state 5), and pressing key 0 again will resume playing (move back to state 4).
- (6) After playing, you can press key 0 to restart playing (move to state 4).

6. bonus:

- (1) During recording, you can pause or stop.
- (2) SevenHexDecoder will display the recording and playing duration, and the playing speed will change dynamically as you switch between fast and slow play, resulting in a changing playing speed.
- (3) After playing, you can choose to play again.

7. screenshot:

(1) Fitter Summary



(2) Timing Analyzer

Table of Contents

- Summary
- Parallel Compilation
- SDC File List
- Clocks
 - Slow 1200mV 85C Model**
 - Fmax Summary
 - Timing Closure Recommendations**
 - Setup Summary**
 - Hold Summary
 - Recovery Summary
 - Removal Summary
 - Minimum Pulse Width Summary
 - Worst-Case Timing Paths**
 - Datasheet Report
 - Metastability Summary
 - Slow 1200mV OC Model**
 - Fmax Summary
 - Setup Summary**
 - Hold Summary
 - Recovery Summary
 - Removal Summary
 - Minimum Pulse Width Summary
 - Worst-Case Timing Paths**
 - Datasheet Report
 - Metastability Summary
 - Fast 1200mV OC Model**
 - Multicorner Timing Analysis Summary**
 - Multicorner Datasheet Report Summary
 - Advanced I/O Timing
 - Clock Transfers**
 - Report TCCS
 - Report RSKM
 - Unconstrained Paths

Slow 1200mV 85C Model Setup Summary

	Clock	Slack	End Point TNS
1	pll0 altpll_0 sd1 pll7 clk[1]	-6.294	-123.872
2	AUD_BCLK	-3.666	-54.509
3	pll0 altpll_0 sd1 pll7 clk[0]	9994.108	0.000

Table of Contents

- Summary
- Parallel Compilation
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 - Fmax Summary
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 - Hold Summary
 - Recovery Summary
 - Removal Summary
 - Minimum Pulse Width Summary
 - Worst-Case Timing Paths**
 - Setup: 'pll0|altpll_0|sd1|pll7|clk[1]'
 - Setup: 'AUD_BCLK'
 - Setup: 'pll0|altpll_0|sd1|pll7|clk[0]' Hold: 'pll0|altpll_0|sd1|pll7|clk[1]'
 - Hold: 'pll0|altpll_0|sd1|pll7|clk[0]' Hold: 'AUD_BCLK'
 - Minimum Pulse Width: 'CLOCK_50'
 - Minimum Pulse Width: 'CLOCK2_50'
 - Minimum Pulse Width: 'CLOCK3_50'
 - Minimum Pulse Width: 'AUD_BCLK'
 - Minimum Pulse Width: 'pll0|altpll_0|sc'
 - Minimum Pulse Width: 'pll0|altpll_0|sc'
 - Datasheet Report
 - Metastability Summary
 - Slow 1200mV OC Model**
 - Fmax Summary
 - Setup Summary**
 - Hold Summary
 - Recovery Summary
 - Removal Summary

Slow 1200mV 85C Model Setup: 'pll0|altpll_0|sd1|pll7|clk[1]'

	Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew
1	-6.294	Top:top0 AudRecorder:recorder0 o_address_r[2]	Top:top0 rec_pause_r	AUD_BCLK	pll0 altpll_0 sd1 pll7 clk[1]	0.001	-2.831
2	-6.282	Top:top0 AudRecorder:recorder0 o_address_r[7]	Top:top0 rec_pause_r	AUD_BCLK	pll0 altpll_0 sd1 pll7 clk[1]	0.001	-2.831
3	-6.271	Top:top0 AudRecorder:recorder0 o_address_r[6]	Top:top0 rec_pause_r	AUD_BCLK	pll0 altpll_0 sd1 pll7 clk[1]	0.001	-2.831
4	-6.256	Top:top0 AudRecorder:recorder0 o_address_r[0]	Top:top0 rec_pause_r	AUD_BCLK	pll0 altpll_0 sd1 pll7 clk[1]	0.001	-2.789
5	-6.237	Top:top0 AudRecorder:recorder0 o_address_r[13]	Top:top0 rec_pause_r	AUD_BCLK	pll0 altpll_0 sd1 pll7 clk[1]	0.001	-2.690
6	-6.236	Top:top0 AudRecorder:recorder0 o_address_r[12]	Top:top0 rec_pause_r	AUD_BCLK	pll0 altpll_0 sd1 pll7 clk[1]	0.001	-2.690
7	-6.210	Top:top0 AudRecorder:recorder0 o_address_r[9]	Top:top0 rec_pause_r	AUD_BCLK	pll0 altpll_0 sd1 pll7 clk[1]	0.001	-2.831
8	-6.193	Top:top0 AudRecorder:recorder0 o_address_r[8]	Top:top0 rec_pause_r	AUD_BCLK	pll0 altpll_0 sd1 pll7 clk[1]	0.001	-2.831
9	-6.178	Top:top0 AudRecorder:recorder0 o_address_r[11]	Top:top0 rec_pause_r	AUD_BCLK	pll0 altpll_0 sd1 pll7 clk[1]	0.001	-2.831
10	-6.166	Top:top0 AudRecorder:recorder0 o_address_r[5]	Top:top0 rec_pause_r	AUD_BCLK	pll0 altpll_0 sd1 pll7 clk[1]	0.001	-2.831
11	-6.122	Top:top0 AudRecorder:recorder0 o_address_r[19]	Top:top0 rec_pause_r	AUD_BCLK	pll0 altpll_0 sd1 pll7 clk[1]	0.001	-2.690
12	-6.121	Top:top0 AudRecorder:recorder0 o_address_r[15]	Top:top0 rec_pause_r	AUD_BCLK	pll0 altpll_0 sd1 pll7 clk[1]	0.001	-2.690
13	-6.105	Top:top0 AudRecorder:recorder0 o_address_r[16]	Top:top0 rec_pause_r	AUD_BCLK	pll0 altpll_0 sd1 pll7 clk[1]	0.001	-2.690
14	-6.093	Top:top0 AudRecorder:recorder0 o_address_r[17]	Top:top0 rec_pause_r	AUD_BCLK	pll0 altpll_0 sd1 pll7 clk[1]	0.001	-2.690
15	-6.088	Top:top0 AudRecorder:recorder0 o_address_r[10]	Top:top0 rec_pause_r	AUD_BCLK	pll0 altpll_0 sd1 pll7 clk[1]	0.001	-2.831
16	-6.017	Top:top0 AudRecorder:recorder0 o_address_r[3]	Top:top0 rec_pause_r	AUD_BCLK	pll0 altpll_0 sd1 pll7 clk[1]	0.001	-2.831
17	-6.015	Top:top0 AudRecorder:recorder0 o_address_r[4]	Top:top0 rec_pause_r	AUD_BCLK	pll0 altpll_0 sd1 pll7 clk[1]	0.001	-2.831
18	-5.988	Top:top0 AudRecorder:recorder0 o_address_r[2]	Top:top0 rec_stop_r	AUD_BCLK	pll0 altpll_0 sd1 pll7 clk[1]	0.001	-2.831
19	-5.976	Top:top0 AudRecorder:recorder0 o_address_r[7]	Top:top0 rec_stop_r	AUD_BCLK	pll0 altpll_0 sd1 pll7 clk[1]	0.001	-2.831
20	-5.965	Top:top0 AudRecorder:recorder0 o_address_r[6]	Top:top0 rec_stop_r	AUD_BCLK	pll0 altpll_0 sd1 pll7 clk[1]	0.001	-2.831
21	-5.959	Top:top0 AudRecorder:recorder0 o_address_r[14]	Top:top0 rec_pause_r	AUD_BCLK	pll0 altpll_0 sd1 pll7 clk[1]	0.001	-2.690
22	-5.950	Top:top0 AudRecorder:recorder0 o_address_r[0]	Top:top0 rec_stop_r	AUD_BCLK	pll0 altpll_0 sd1 pll7 clk[1]	0.001	-2.789
23	-5.938	Top:top0 AudRecorder:recorder0 o_address_r[11]	Top:top0 rec_pause_r	AUD_BCLK	pll0 altpll_0 sd1 pll7 clk[1]	0.001	-2.831
24	-5.931	Top:top0 AudRecorder:recorder0 o_address_r[13]	Top:top0 rec_stop_r	AUD_BCLK	pll0 altpll_0 sd1 pll7 clk[1]	0.001	-2.690
25	-5.930	Top:top0 AudRecorder:recorder0 o_address_r[12]	Top:top0 rec_stop_r	AUD_BCLK	pll0 altpll_0 sd1 pll7 clk[1]	0.001	-2.690
26	-5.904	Top:top0 AudRecorder:recorder0 o_address_r[9]	Top:top0 rec_stop_r	AUD_BCLK	pll0 altpll_0 sd1 pll7 clk[1]	0.001	-2.831
27	-5.887	Top:top0 AudRecorder:recorder0 o_address_r[8]	Top:top0 rec_stop_r	AUD_BCLK	pll0 altpll_0 sd1 pll7 clk[1]	0.001	-2.831
28	-5.872	Top:top0 AudRecorder:recorder0 o_address_r[1]	Top:top0 rec_stop_r	AUD_BCLK	pll0 altpll_0 sd1 pll7 clk[1]	0.001	-2.831
29	-5.860	Top:top0 AudRecorder:recorder0 o_address_r[5]	Top:top0 rec_stop_r	AUD_BCLK	pll0 altpll_0 sd1 pll7 clk[1]	0.001	-2.831
30	-5.825	Top:top0 AudRecorder:recorder0 o_address_r[18]	Top:top0 rec_pause_r	AUD_BCLK	pll0 altpll_0 sd1 pll7 clk[1]	0.001	-2.690
31	-5.815	Top:top0 AudRecorder:recorder0 o_address_r[15]	Top:top0 rec_stop_r	AUD_BCLK	pll0 altpll_0 sd1 pll7 clk[1]	0.001	-2.690
32	-5.800	Ton-ton0 AudRecorder:recorder0 o_address_r[10]	Ton-ton0 rfr_dnn_r	AUD_BCLK	pll0 altpll_0 sd1 pll7 clk[1]	0.001	-2.600

Table of Contents		Slow 1200mV 85C Model Setup: 'AUD_BCLK'				
		Slack	From Node	To Node	Launch Clock	Latch Clock
	Summary	-3.666	Top:top0 play_pause_r	Top:top0 AudPlayer:player0 state_r.S_PLAY	pll0 altpll_0 sd1 pll7 clk[1]	AUD_BCLK
	Parallel Compilation	-3.596	Top:top0 play_pause_r	Top:top0 AudPlayer:player0 state_r.S_IDLE	pll0 altpll_0 sd1 pll7 clk[1]	AUD_BCLK
	SDC File List	-2.531	Top:top0 rec_stop_r	Top:top0 AudRecorder:recorder0 o_data_r[13]	pll0 altpll_0 sd1 pll7 clk[1]	AUD_BCLK
	Clocks	-2.522	Top:top0 rec_start_r	Top:top0 AudRecorder:recorder0 state_r.S_NOT_RECORD	pll0 altpll_0 sd1 pll7 clk[1]	AUD_BCLK
Slow 1200mV 85C Model	Fmax Summary	-2.519	Top:top0 rec_stop_r	Top:top0 AudRecorder:recorder0 stop_r	pll0 altpll_0 sd1 pll7 clk[1]	AUD_BCLK
	Timing Closure Recommendations	-2.473	Top:top0 rec_stop_r	Top:top0 AudRecorder:recorder0 o_data_r[1]	pll0 altpll_0 sd1 pll7 clk[1]	AUD_BCLK
	Setup Summary	-2.468	Top:top0 rec_stop_r	Top:top0 AudRecorder:recorder0 o_data_r[5]	pll0 altpll_0 sd1 pll7 clk[1]	AUD_BCLK
	Hold Summary	-2.450	Top:top0 rec_stop_r	Top:top0 AudRecorder:recorder0 o_data_r[9]	pll0 altpll_0 sd1 pll7 clk[1]	AUD_BCLK
	Recovery Summary	-2.448	Top:top0 rec_stop_r	Top:top0 AudRecorder:recorder0 o_data_r[4]	pll0 altpll_0 sd1 pll7 clk[1]	AUD_BCLK
	Removal Summary	-2.442	Top:top0 rec_start_r	Top:top0 AudRecorder:recorder0 state_r.S_RECORD	pll0 altpll_0 sd1 pll7 clk[1]	AUD_BCLK
	Minimum Pulse Width Summary	-2.438	Top:top0 rec_stop_r	Top:top0 AudRecorder:recorder0 stop_r	pll0 altpll_0 sd1 pll7 clk[1]	AUD_BCLK
Worst-Case Timing Paths	Setup: 'pll0 altpll_0 sd1 pll7 clk[1]'	-2.426	Top:top0 rec_stop_r	Top:top0 AudRecorder:recorder0 state_r.S_RECORD	pll0 altpll_0 sd1 pll7 clk[1]	AUD_BCLK
	Setup: 'AUD_BCLK'	-2.383	Top:top0 rec_stop_r	Top:top0 AudRecorder:recorder0 o_data_r[11]	pll0 altpll_0 sd1 pll7 clk[1]	AUD_BCLK
	Setup: 'pll0 altpll_0 sd1 pll7 clk[0]'	-2.377	Top:top0 rec_stop_r	Top:top0 AudRecorder:recorder0 o_data_r[12]	pll0 altpll_0 sd1 pll7 clk[1]	AUD_BCLK
	Hold: 'pll0 altpll_0 sd1 pll7 clk[1]'	-2.372	Top:top0 rec_stop_r	Top:top0 AudRecorder:recorder0 o_data_r[3]	pll0 altpll_0 sd1 pll7 clk[1]	AUD_BCLK
	Hold: 'pll0 altpll_0 sd1 pll7 clk[0]'	-2.348	Top:top0 rec_stop_r	Top:top0 AudRecorder:recorder0 o_data_r[8]	pll0 altpll_0 sd1 pll7 clk[1]	AUD_BCLK
	Hold: 'AUD_BCLK'	-2.337	Top:top0 rec_stop_r	Top:top0 AudRecorder:recorder0 o_data_r[0]	pll0 altpll_0 sd1 pll7 clk[1]	AUD_BCLK
	Minimum Pulse Width: 'CLOCK_50'	-2.311	Top:top0 rec_stop_r	Top:top0 AudRecorder:recorder0 state_r.S_NOT_RECORD	pll0 altpll_0 sd1 pll7 clk[1]	AUD_BCLK
	Minimum Pulse Width: 'CLOCK2_50'	-2.300	Top:top0 rec_stop_r	Top:top0 AudRecorder:recorder0 o_data_r[14]	pll0 altpll_0 sd1 pll7 clk[1]	AUD_BCLK
	Minimum Pulse Width: 'CLOCK3_50'	-2.258	Top:top0 rec_stop_r	Top:top0 AudRecorder:recorder0 o_data_r[7]	pll0 altpll_0 sd1 pll7 clk[1]	AUD_BCLK
	Minimum Pulse Width: 'AUD_BCLK'	-2.243	Top:top0 rec_start_r	Top:top0 AudRecorder:recorder0 state_r.S_IDLE	pll0 altpll_0 sd1 pll7 clk[1]	AUD_BCLK
	Minimum Pulse Width: 'pll0 altpll_0 sc'	-2.213	Top:top0 rec_stop_r	Top:top0 AudRecorder:recorder0 o_data_r[2]	pll0 altpll_0 sd1 pll7 clk[1]	AUD_BCLK
	Minimum Pulse Width: 'pll0 altpll_0 sc'	-2.135	Top:top0 rec_stop_r	Top:top0 AudRecorder:recorder0 o_data_r[10]	pll0 altpll_0 sd1 pll7 clk[1]	AUD_BCLK
	Worst-Case Timing I	-2.132	Top:top0 rec_stop_r	Top:top0 AudRecorder:recorder0 o_data_r[6]	pll0 altpll_0 sd1 pll7 clk[1]	AUD_BCLK
	Datasheet Report	-2.101	Top:top0 rec_stop_r	Top:top0 AudRecorder:recorder0 o_data_r[15]	pll0 altpll_0 sd1 pll7 clk[1]	AUD_BCLK
	Metastability Summary	74.579	Top:top0 AudPlayer:player0 counter_r[0]	Top:top0 AudPlayer:player0 o_aud_dacdat_r	AUD_BCLK	AUD_BCLK
Slow 1200mV 85C Model	Fmax Summary	75.286	Top:top0 AudPlayer:player0 counter_r[1]	Top:top0 AudPlayer:player0 o_aud_dacdat_r	AUD_BCLK	AUD_BCLK
	Timing Closure Rec	77.007	Top:top0 AudPlayer:player0 counter_r[3]	Top:top0 AudPlayer:player0 state_r.S_PLAY	AUD_BCLK	AUD_BCLK
	Setup Summary	77.027	Top:top0 AudPlayer:player0 counter_r[2]	Top:top0 AudPlayer:player0 state_r.S_PLAY	AUD_BCLK	AUD_BCLK
	Hold Summary	77.148	Top:top0 AudPlayer:player0 counter_r[4]	Top:top0 AudPlayer:player0 state_r.S_PLAY	AUD_BCLK	AUD_BCLK
	Recovery Summary	77.205	Top:top0 AudPlayer:player0 counter_r[0]	Top:top0 AudPlayer:player0 state_r.S_PLAY	AUD_BCLK	AUD_BCLK
	Removal Summary	77.276	Top:top0 AudPlayer:player0 counter_r[11]	Top:top0 AudPlayer:player0 state_r.S_PLAY	AUD_BCLK	AUD_BCLK

Table of Contents		Slow 1200mV 85C Model Setup Summary		
		Clock	Slack	End Point TNS
	SDC File List	pll0 altpll_0 sd1 pll7 clk[1]	-6.294	-123.872
	Clocks	AUD_BCLK	-3.666	-54.509
Slow 1200mV 85C Model	Fmax Summary	pll0 altpll_0 sd1 pll7 clk[0]	9994.108	0.000
	Timing Closure Rec			
	Setup Summary			
	Hold Summary			
	Recovery Summary			
	Removal Summary			
	Minimum Pulse Wdt			
Worst-Case Timing I				
Datasheet Report				
Metastability Summary				
Slow 1200mV 85C Model	Fmax Summary			
	Setup Summary			
	Hold Summary			
	Recovery Summary			
	Removal Summary			
	Minimum Pulse Wdt			
Worst-Case Timing I				
Datasheet Report				
Metastability Summary				
Fast 1200mV 85C Model	Multicorner Timing Analysis			
	Multicorner Datasheet F			
	Advanced I/O Timing			
	Clock Transfers			
	Report TCCS			
	Report RSKM			
	Unconstrained Paths			
	Messages			

Table of Contents							Fast 1200mV OC Model Setup Summary							
			Clock	Slack	End Point TNS									
Worst-Case Timing Paths	<ul style="list-style-type: none">Setup: 'pll0 altpll_0 sd1 pll7 clk[1]'Hold: 'AUD_BCLK'Setup: 'pll0 altpll_0 sd1 pll7 clk[0]'Hold: 'pll0 altpll_0 sd1 pll7 clk[1]'Hold: 'pll0 altpll_0 sd1 pll7 clk[0]'Hold: 'AUD_BCLK'Minimum Pulse Width: 'CLOCK_50'Minimum Pulse Width: 'CLOCK2_50'Minimum Pulse Width: 'CLOCK3_50'Minimum Pulse Width: 'AUD_BCLK'Minimum Pulse Width: 'pll0 altpll_0 sd1 pll7 clk[1]'Minimum Pulse Width: 'pll0 altpll_0 sd1 pll7 clk[0]'		1	pll0 altpll_0 sd1 pll7 clk[1]	-3.176	-62.498	2	AUD_BCLK	-1.557	-27.539	3	pll0 altpll_0 sd1 pll7 clk[0]	9997.085	0.000
Datasheet Report														
Metastability Summary														
Fast 1200mV OC Model	<ul style="list-style-type: none">Setup SummaryHold SummaryRecovery SummaryRemoval SummaryMinimum Pulse Width Summary													
Worst-Case Timing Paths														
Datasheet Report														
Metastability Summary														
Multicorner Timing Analysis Summary														
Multicorner Datasheet Report Summary														
Advanced I/O Timing														
Clock Transfers														
Report TCSC														
Report RSKM														
Unconstraint Paths														
Messages														

Table of Contents							Fast 1200mV OC Model Setup: 'pll0 altpll_0 sd1 pll7 clk[1]'				
			From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew			
Setup: 'pll0 altpll_0 sd1 pll7 clk[1]'	Slack										
Hold: 'pll0 altpll_0 sd1 pll7 clk[1]'	-3.176	Top:top0 AudRecorder:recorder0 o_address_r[2]	Top:top0 rec_pause_r	AUD_BCLK	pll0 altpll_0 sd1 pll7 clk[1]	0.001	-1.436				
Hold: 'pll0 altpll_0 sd1 pll7 clk[0]'	-3.175	Top:top0 AudRecorder:recorder0 o_address_r[7]	Top:top0 rec_pause_r	AUD_BCLK	pll0 altpll_0 sd1 pll7 clk[1]	0.001	-1.436				
Hold: 'AUD_BCLK'	-3.172	Top:top0 AudRecorder:recorder0 o_address_r[12]	Top:top0 rec_pause_r	AUD_BCLK	pll0 altpll_0 sd1 pll7 clk[1]	0.001	-1.366				
Minimum Pulse Width: 'CLOCK_50'	-3.172	Top:top0 AudRecorder:recorder0 o_address_r[6]	Top:top0 rec_pause_r	AUD_BCLK	pll0 altpll_0 sd1 pll7 clk[1]	0.001	-1.436				
Minimum Pulse Width: 'CLOCK2_50'	-3.170	Top:top0 AudRecorder:recorder0 o_address_r[13]	Top:top0 rec_pause_r	AUD_BCLK	pll0 altpll_0 sd1 pll7 clk[1]	0.001	-1.366				
Minimum Pulse Width: 'CLOCK3_50'	-3.166	Top:top0 AudRecorder:recorder0 o_address_r[0]	Top:top0 rec_pause_r	AUD_BCLK	pll0 altpll_0 sd1 pll7 clk[1]	0.001	-1.417				
Minimum Pulse Width: 'AUD_BCLK'	-3.132	Top:top0 AudRecorder:recorder0 o_address_r[9]	Top:top0 rec_pause_r	AUD_BCLK	pll0 altpll_0 sd1 pll7 clk[1]	0.001	-1.436				
Minimum Pulse Width: 'pll0 altpll_0 sd1 pll7 clk[1]'	-3.124	Top:top0 AudRecorder:recorder0 o_address_r[8]	Top:top0 rec_pause_r	AUD_BCLK	pll0 altpll_0 sd1 pll7 clk[1]	0.001	-1.436				
Minimum Pulse Width: 'pll0 altpll_0 sd1 pll7 clk[0]'	-3.117	Top:top0 AudRecorder:recorder0 o_address_r[19]	Top:top0 rec_pause_r	AUD_BCLK	pll0 altpll_0 sd1 pll7 clk[1]	0.001	-1.366				
Datasheet Report											
Metastability Summary											
Fast 1200mV OC Model	<ul style="list-style-type: none">Setup SummaryHold SummaryRecovery SummaryRemoval SummaryMinimum Pulse Width Summary										
Worst-Case Timing Paths	<ul style="list-style-type: none">Setup: 'pll0 altpll_0 sd1 pll7 clk[1]'Setup: 'AUD_BCLK'Setup: 'pll0 altpll_0 sd1 pll7 clk[0]'Hold: 'pll0 altpll_0 sd1 pll7 clk[0]'Hold: 'pll0 altpll_0 sd1 pll7 clk[1]'Hold: 'AUD_BCLK'Minimum Pulse Width: 'CLOCK_50'Minimum Pulse Width: 'CLOCK2_50'Minimum Pulse Width: 'CLOCK3_50'Minimum Pulse Width: 'AUD_BCLK'Minimum Pulse Width: 'pll0 altpll_0 sd1 pll7 clk[1]'Minimum Pulse Width: 'pll0 altpll_0 sd1 pll7 clk[0]'										
Datasheet Report											
Metastability Summary											

Table of Contents		Multicorner OC Model Setup: Top_BCLK					
		Slack	From Node	To Node	Launch Clock	Latch Clock	
	Setup: 'pll0 altpll_0 sd1 pli7 clk[0]' Hold: 'pll0 altpll_0 sd1 pli7 clk[1]' Hold: 'AUD_BCLK' Minimum Pulse Width: 'CLOCK_50' Minimum Pulse Width: 'CLOCK2_50' Minimum Pulse Width: 'AUD_BCLK' Minimum Pulse Width: 'pll0 altpll_0 sc' Minimum Pulse Width: 'pll0 altpll_0 sc'	-1.557	Top:top0 play_pause_r	Top:top0 AudPlayer:player0 rstate_r.S_PLAY	pll0 altpll_0 sd1 pli7 clk[1]	AUD_BCLK	
		-1.508	Top:top0 play_pause_r	Top:top0 AudPlayer:player0 rstate_r.S_IDLE	pll0 altpll_0 sd1 pli7 clk[1]	AUD_BCLK	
		-1.449	Top:top0 rec_stop_r	Top:top0 AudRecorder:recorder0 rstate_r.S_RECORD	pll0 altpll_0 sd1 pli7 clk[1]	AUD_BCLK	
		-1.438	Top:top0 rec_stop_r	Top:top0 AudRecorder:recorder0 rstate_r.S_IDLE	pll0 altpll_0 sd1 pli7 clk[1]	AUD_BCLK	
		-1.438	Top:top0 rec_start_r	Top:top0 AudRecorder:recorder0 rstate_r.S_NOT_RECORD	pll0 altpll_0 sd1 pli7 clk[1]	AUD_BCLK	
		-1.362	Top:top0 rec_stop_r	Top:top0 AudRecorder:recorder0 stop_r	pll0 altpll_0 sd1 pli7 clk[1]	AUD_BCLK	
		-1.325	Top:top0 rec_start_r	Top:top0 AudRecorder:recorder0 rstate_r.S_RECORD	pll0 altpll_0 sd1 pli7 clk[1]	AUD_BCLK	
		-1.257	Top:top0 rec_stop_r	Top:top0 AudRecorder:recorder0 o_data_r[13]	pll0 altpll_0 sd1 pli7 clk[1]	AUD_BCLK	
		-1.255	Top:top0 rec_stop_r	Top:top0 AudRecorder:recorder0 o_data_r[1]	pll0 altpll_0 sd1 pli7 clk[1]	AUD_BCLK	
		-1.233	Top:top0 rec_stop_r	Top:top0 AudRecorder:recorder0 o_data_r[9]	pll0 altpll_0 sd1 pli7 clk[1]	AUD_BCLK	
		-1.232	Top:top0 rec_stop_r	Top:top0 AudRecorder:recorder0 o_data_r[5]	pll0 altpll_0 sd1 pli7 clk[1]	AUD_BCLK	
		-1.231	Top:top0 rec_stop_r	Top:top0 AudRecorder:recorder0 rstate_r.S_NOT_RECORD	pll0 altpll_0 sd1 pli7 clk[1]	AUD_BCLK	
		-1.221	Top:top0 rec_stop_r	Top:top0 AudRecorder:recorder0 o_data_r[4]	pll0 altpll_0 sd1 pli7 clk[1]	AUD_BCLK	
		-1.193	Top:top0 rec_stop_r	Top:top0 AudRecorder:recorder0 o_data_r[11]	pll0 altpll_0 sd1 pli7 clk[1]	AUD_BCLK	
		-1.184	Top:top0 rec_stop_r	Top:top0 AudRecorder:recorder0 o_data_r[12]	pll0 altpll_0 sd1 pli7 clk[1]	AUD_BCLK	
		-1.180	Top:top0 rec_stop_r	Top:top0 AudRecorder:recorder0 o_data_r[3]	pll0 altpll_0 sd1 pli7 clk[1]	AUD_BCLK	
		-1.178	Top:top0 rec_stop_r	Top:top0 AudRecorder:recorder0 o_data_r[8]	pll0 altpll_0 sd1 pli7 clk[1]	AUD_BCLK	
		-1.175	Top:top0 rec_stop_r	Top:top0 AudRecorder:recorder0 o_data_r[0]	pll0 altpll_0 sd1 pli7 clk[1]	AUD_BCLK	
		-1.154	Top:top0 rec_stop_r	Top:top0 AudRecorder:recorder0 o_data_r[14]	pll0 altpll_0 sd1 pli7 clk[1]	AUD_BCLK	
		-1.148	Top:top0 rec_start_r	Top:top0 AudRecorder:recorder0 rstate_r.S_IDLE	pll0 altpll_0 sd1 pli7 clk[1]	AUD_BCLK	
		-1.131	Top:top0 rec_stop_r	Top:top0 AudRecorder:recorder0 o_data_r[7]	pll0 altpll_0 sd1 pli7 clk[1]	AUD_BCLK	
		-1.130	Top:top0 rec_stop_r	Top:top0 AudRecorder:recorder0 o_data_r[2]	pll0 altpll_0 sd1 pli7 clk[1]	AUD_BCLK	
		-1.096	Top:top0 rec_stop_r	Top:top0 AudRecorder:recorder0 o_data_r[10]	pll0 altpll_0 sd1 pli7 clk[1]	AUD_BCLK	
		-1.084	Top:top0 rec_stop_r	Top:top0 AudRecorder:recorder0 o_data_r[6]	pll0 altpll_0 sd1 pli7 clk[1]	AUD_BCLK	
		-1.084	Top:top0 rec_stop_r	Top:top0 AudRecorder:recorder0 o_data_r[15]	pll0 altpll_0 sd1 pli7 clk[1]	AUD_BCLK	
		78.579	Top:top0 AudPlayer:player0 counter_r[0]	Top:top0 AudPlayer:player0 o_aud_dacdat_r	AUD_BCLK	AUD_BCLK	
		78.995	Top:top0 AudPlayer:player0 counter_r[1]	Top:top0 AudPlayer:player0 o_aud_dacdat_r	AUD_BCLK	AUD_BCLK	
		79.957	Top:top0 AudPlayer:player0 counter_r[3]	Top:top0 AudPlayer:player0 rstate_r.S_PLAY	AUD_BCLK	AUD_BCLK	
		79.968	Top:top0 AudPlayer:player0 counter_r[2]	Top:top0 AudPlayer:player0 rstate_r.S_PLAY	AUD_BCLK	AUD_BCLK	
		79.989	Top:top0 AudPlayer:player0 counter_r[0]	Top:top0 AudPlayer:player0 rstate_r.S_PLAY	AUD_BCLK	AUD_BCLK	
		80.093	Top:top0 AudPlayer:player0 counter_r[1]	Top:top0 AudPlayer:player0 rstate_r.S_PLAY	AUD_BCLK	AUD_BCLK	
		80.101	Top:top0 AudPlayer:player0 counter_r[4]	Top:top0 AudPlayer:player0 rstate_r.S_PLAY	AUD_BCLK	AUD_BCLK	

Table of Contents		Multicorner Timing Analysis Summary					
		Clock	Setup	Hold	Recovery	Removal	Minimum Pulse Width
	Minimum Pulse Width: 'pll0 altpll_0 sc'	Worst-case Slack	-6.294	0.181	N/A	N/A	9.400
		AUD_BCLK	-3.666	0.199	N/A	N/A	40.668
		CLOCK2_50	N/A	N/A	N/A	N/A	16.000
		CLOCK_50	N/A	N/A	N/A	N/A	16.000
		pll0 altpll_0 sd1 pli7 clk[0]	9994.108	0.181	N/A	N/A	4999.754
		pll0 altpll_0 sd1 pli7 clk[1]	-6.294	0.183	N/A	N/A	41.359
		Design-wide TNS		-178.381	0.0	0.0	0.0
		AUD_BCLK	-54.509	0.000	N/A	N/A	0.000
		CLOCK2_50	N/A	N/A	N/A	N/A	0.000
		CLOCK_50	N/A	N/A	N/A	N/A	0.000
		pll0 altpll_0 sd1 pli7 clk[0]	0.000	0.000	N/A	N/A	0.000
		pll0 altpll_0 sd1 pli7 clk[1]	-123.872	0.000	N/A	N/A	0.000

Table of Contents			
Unconstrained Paths			
	Property	Setup	Hold
1	Illegal Clocks	0	0
2	Unconstrained Clocks	2	2
3	Unconstrained Input Ports	29	29
4	Unconstrained Input Port Paths	1111	1111
5	Unconstrained Output Ports	74	74
6	Unconstrained Output Port Paths	275	275

Table of Contents:

- Minimum Pulse Width: 'pll0|altpll_0|sc'
 - Datasheet Report
 - Metastability Summary
- Fast 1200mV OC Model
 - Setup Summary
 - Hold Summary
 - Recovery Summary
 - Removal Summary
 - Minimum Pulse Width Summary
- Worst-Case Timing Paths
 - Setup: 'pll0|altpll_0|sd1|pll7|dk[1]'
 - Setup: 'AUD_BCLK'
 - Setup: 'pll0|altpll_0|sd1|pll7|clk[0]'
 - Hold: 'pll0|altpll_0|sd1|pll7|clk[0]'
 - Hold: 'pll0|altpll_0|sd1|pll7|dk[1]'
 - Hold: 'AUD_BCLK'
 - Minimum Pulse Width: 'CLOCK_50'
 - Minimum Pulse Width: 'CLOCK2_50'
 - Minimum Pulse Width: 'CLOCK3_50'
 - Minimum Pulse Width: 'AUD_BCLK'
 - Minimum Pulse Width: 'pll0|altpll_0|sc'
 - Minimum Pulse Width: 'pll0|altpll_0|sc'
- Datasheet Report
- Metastability Summary
- Multicorner Timing Analysis Summary
 - Multicorner Datasheet Report Summary
- Advanced I/O Timing
- Clock Transfers
 - Report TCCS
 - Report RSKM
 - Unconstrained Paths
- Messages

8. Problems Encountered and Solutions:

- This experiment was different from previous ones because there was no provided testbench, and we had to create the testbench files ourselves. After completing our respective modules, we individually ran the testbenches to ensure our code was correct before integrating all the modules.
- Due to the midterm exams, we had to pause our work for a week to prepare. This limited our preparation time, and this experiment was more challenging and complex than previous ones. With less time to prepare and increased difficulty, we struggled to resolve all issues and implement all the functionalities. We managed to solve all problems and implement the features only the day before the demo. This experience taught us the importance of planning and scheduling in advance to complete the experiment more smoothly.
- After programming the code into the FPGA, we encountered issues with linear interpolation, which resulted in severe noise during audio playback. We later discovered the problem was related to signed operations, and after fixing it, the audio playback worked correctly.