NTUEE DCLab

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Example: An 8-bit ALU

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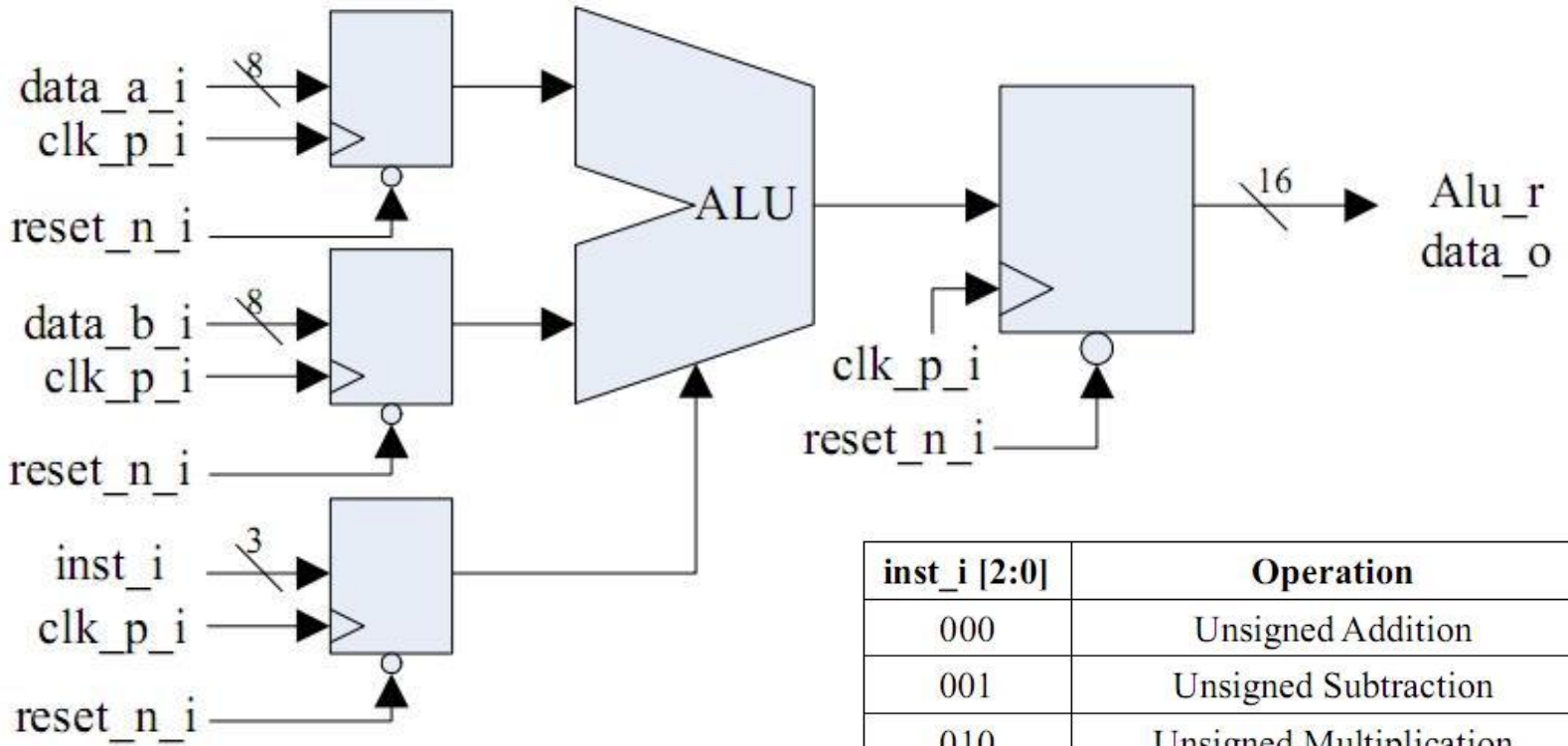
Objectives

- In this lab, you will learn
  - How to verify your Verilog HDL
  - How to run the NC-Verilog simulator with test-bench

- Check if you have these files
  - Lab0_alu.v
  - Lab0_alu_tb.v

An 8-bit ALU



inst_i [2:0]	Operation	Notes
000	Unsigned Addition	data_o=data_a_i+data_b_i
001	Unsigned Subtraction	data_o=data_b_i-data_a_i
010	Unsigned Multiplication	data_o= data_a_i*data_b_i
011	NOT	data_o=~data_a_i
100	XOR	data_o= data_a_i⊕data_b_i
101	Absolute Value	Data_o=|data_a_i|
110	Subtraction & Divide by 2	data_o=(data_b_i-data_a_i)>>1
111	Unused	Unused

Check Verilog Code and Simulation

- Check Verilog Code via NC-Verilog
  - ncverilog Lab0_alu.v
  - NC-Verilog will report your RTL code
  - Ensure there are no errors
- Run simulation with a test bench via NC-Verilog
  - ncverilog Lab0_alu_tb.v +access+r
  - Check if there are any warnings/errors
- Open the waveform
  - nWave &

References

- NTU VLSI Lab course material, Lab 1, 2014