IC Design HW4 report

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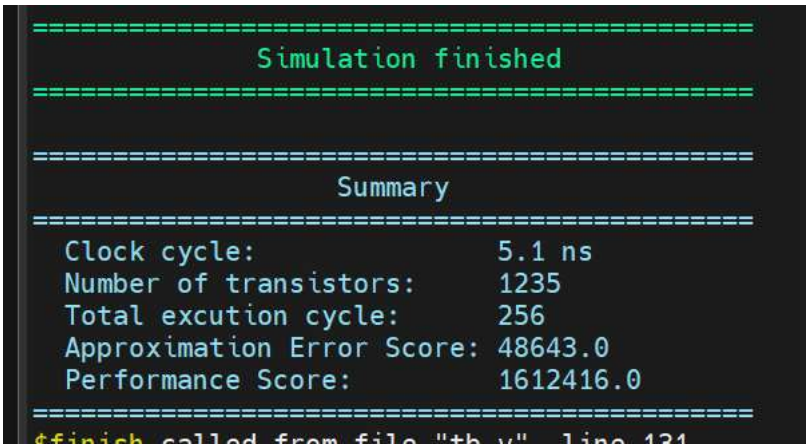
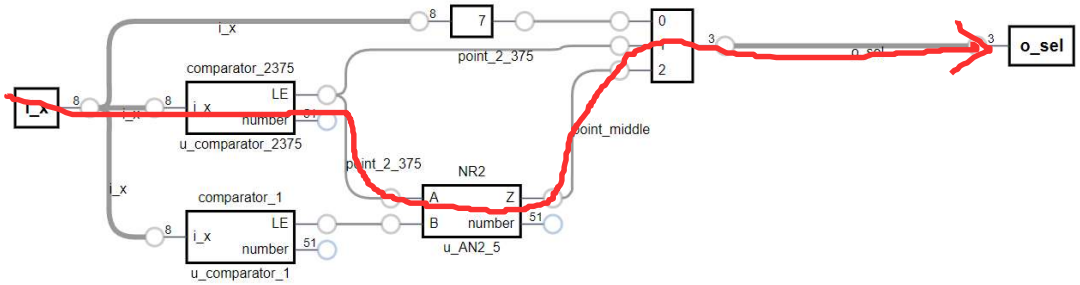
(a) Simulation

minimum cycle time: 5.1ns

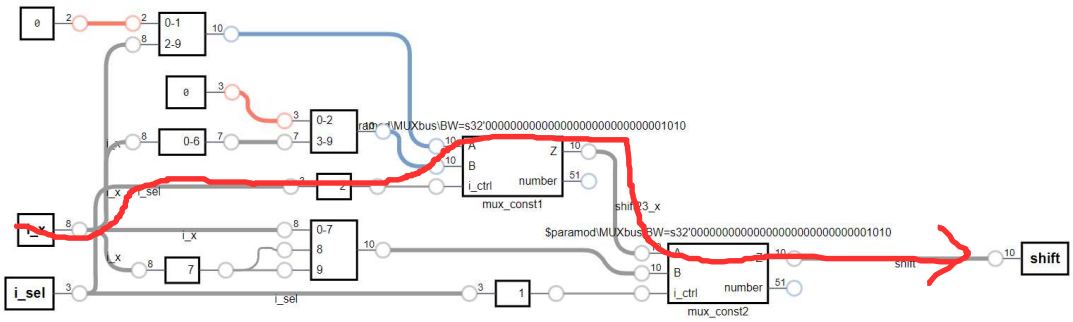


(b) Circuit diagram:

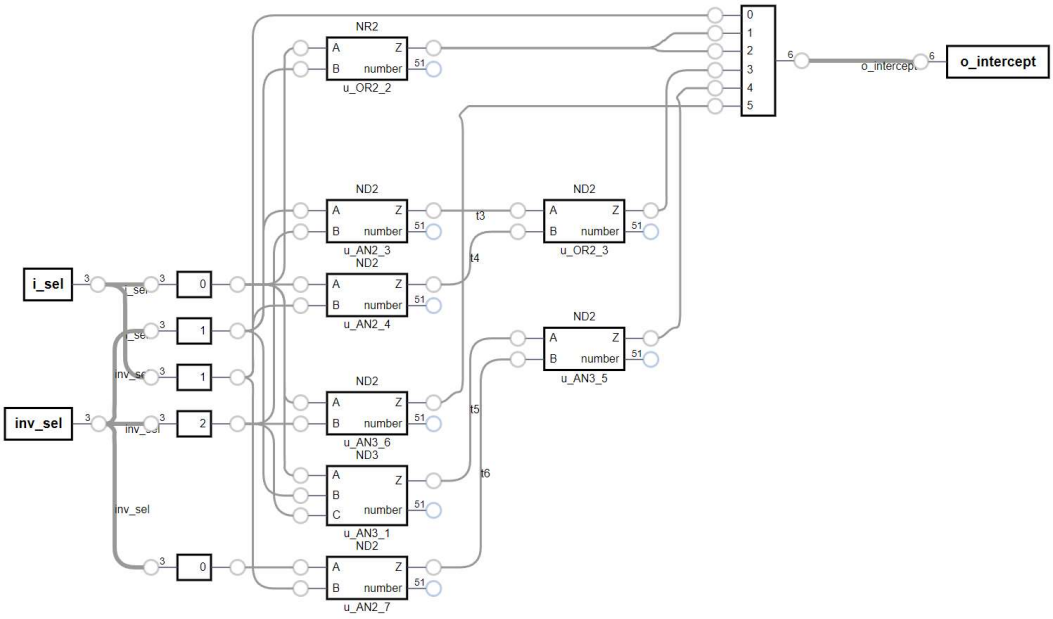
Range Selector:



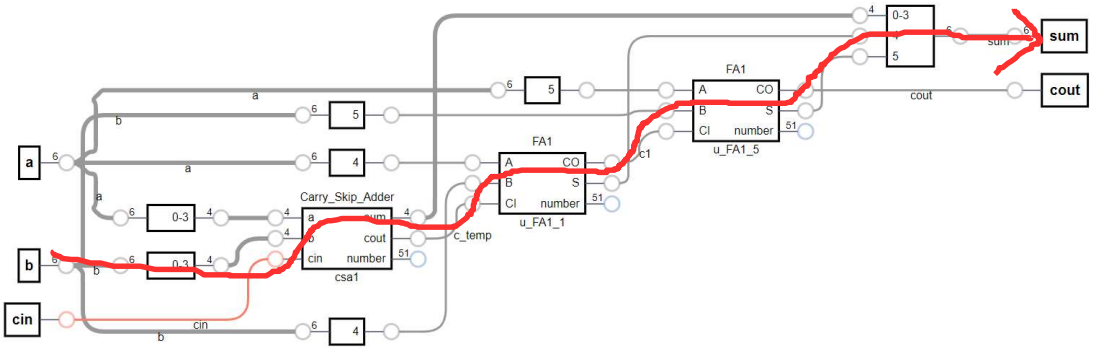
Getshift:



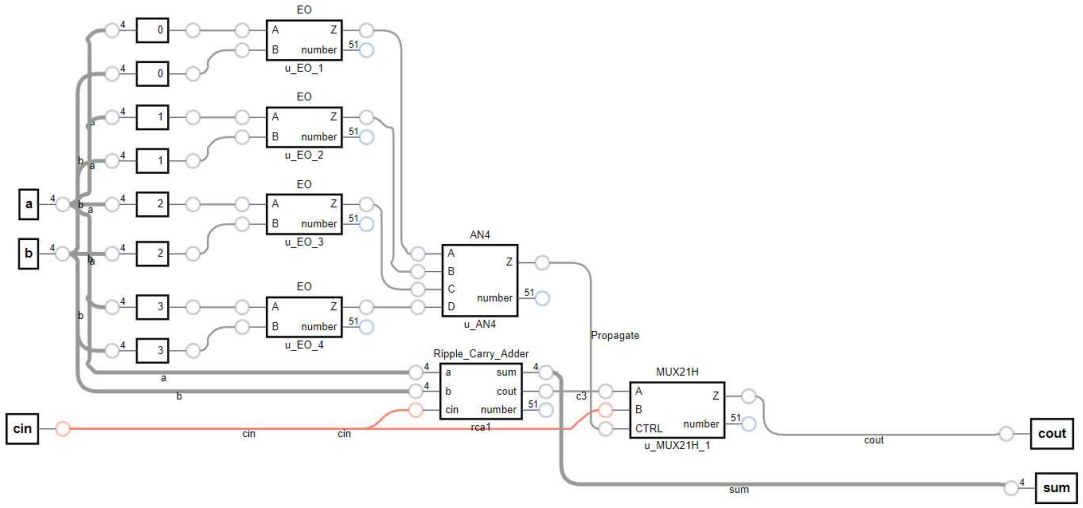
Intercept:



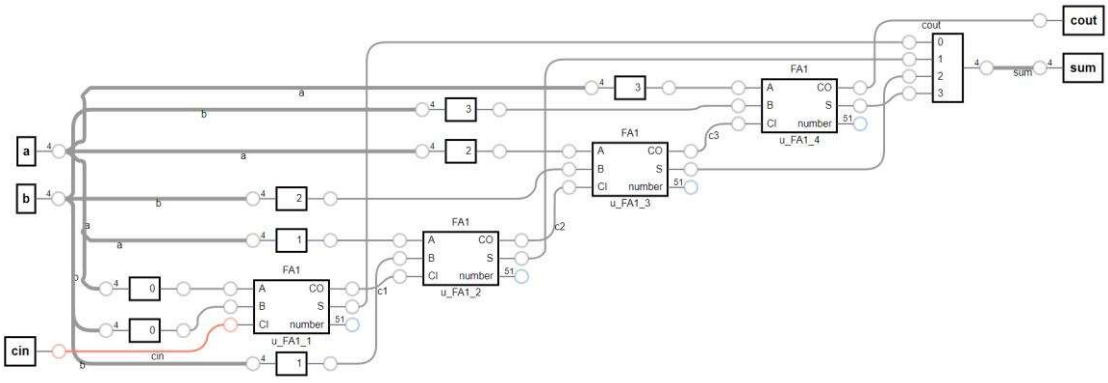
Carry Skip Adder (6-bit):



Carry Skip Adder (4-bit):



Ripple Carry Adder:



The critical path is highlighted in read line above circuit diagram.

(c) Discussion:

(1) Introduce your design:

I using 5 piecewise-linear approximate the sigmoid function,

the 5 linear function is following:

For -4 <= i_x < -2.375, y(x) = 0.140625 + 0.03125 x

For -2.375 <= i_x < -1, y(x) = 0.375 + 0.125 x

For -1 <= i_x < 1, y(x) = 0.5 + 0.25 x

For 1 <= i_x < 2.375, y(x) = 0.625 + 0.125 x

For 2.375 <= i_x <= 4, y(x) = 0.859375 + 0.03125 x

I use shift operation to get the slope, and I use K-map to get the intercept.

(2) How do you improve your critical path and the number of transistors?

1. I use NAND、NOR gate as much as possible, instead of using AND、OR gate.
2. Because the result of y only need the fraction bit, so the adder only add the fraction bit of two input, which make transistors of adder decreased.
3. I think I use more transistor to achieve low clock time, but will cost more area. In addition, I use five piecewise linear which also increase the number of transistor.
4. First time , when I shift the input i_x, I discard the bit 1, which make the approximation error so big. That is, I only use the result from adder to output o_y, and let the remaining bit all 0.

Second time, when I shift input i_x, I reserve the bit 1, and final assign to output o_y. This makes my approximation error decreases so much.