IC Design

Homework #1

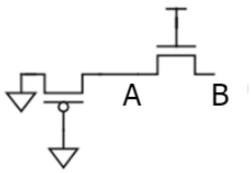
Due on 10/05/2023, 9:20 AM in class,
10% penalty for each day of delay

1. (20%) Please answer the following questions. Your answer should contain pictures and texts for a better explanation. A single page of A4 is recommended.
   (a) By using TSMC's CoWoS technology, Nvidia puts computing chip and high-bandwidth memory together and makes H100, its most powerful GPU. Explain what CoWoS is, how it works, what it is different from other packaging technology, and where it can be used. (學號尾數為單號者回答此題)
   (b) Intel 20A, Intel's most advanced technology node, uses backside power delivery technology (PowerVia) to supply power to the chip. Explain briefly what backside power delivery is, how it works, what advantages it has, and what difficulties it has to overcome. (學號尾數為雙號者回答此題)

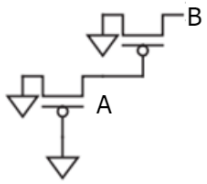
2. (15%) Please draw the compound gate using only NAND, NOR, and INV gates for the following function
   (a) $Y = \overline{(\bar{A} \cdot B)} + \overline{(B \cdot C)}$
   (b) $Y = \overline{(A \oplus B)} \cdot \overline{(C + \bar{D})}$
   (c) $Y = \overline{(A \oplus (B \cdot C)) + (D \oplus E)}$

3. (20%) Please express **all the node voltages** in the pass transistor networks shown below (neglect the body effect).
   (You can use **V_{DD}, GND, $|V_{tp}|$, or V_{tn}** to express your answer.)
   (Assume that every NMOS has the same threshold voltage, and so does the PMOS.)

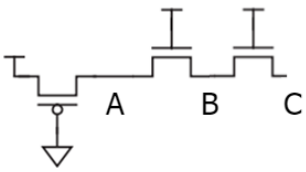
(a)



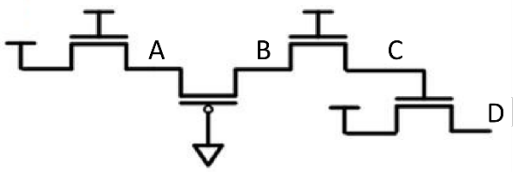
(b)



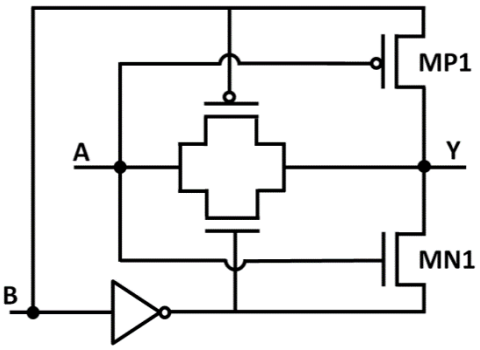
(c)



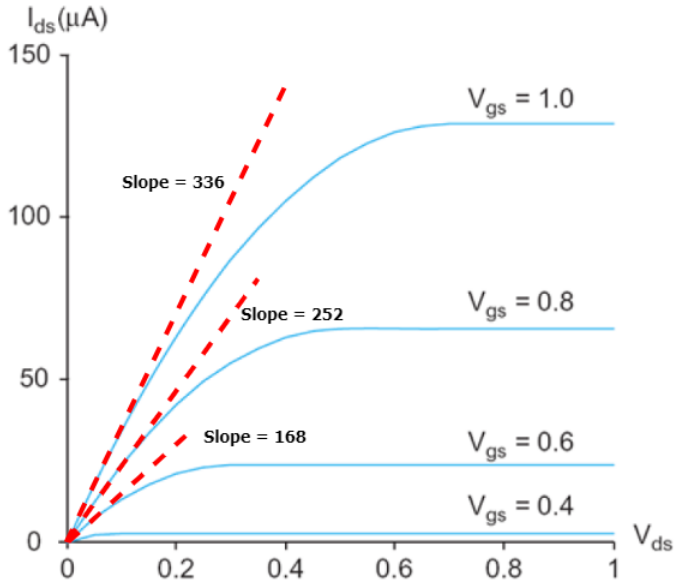
(d)



4. (20%) For the following transmission-gate circuit,
   (a) (10%) Please show the function of this circuit.
   Hint: You can use the truth table method to find the function of Y.
   (b) (10%) Is there any bad-zero or bad-one problem in this circuit? **Explain why.** (Bad-one means the voltage of logic-1 is only VDD-V_{tn}; bad-zero means the voltage of logic-0 is $|V_{tp}|$)



5. (10%) For the following I-V curves of an NMOS transistor, given the slope at 0 for the top three curves, estimate a precise value of V_t (小數點以下兩位). Explain how you find this value from the three slopes.



6. (15%) A 3-input minority gate returns output "**1**" if no more than two of the inputs are "**1**".
   (a) (5%) Sketch a **transistor-level** circuit diagram for a 3-input minority gate using a single stage of CMOS static logic. Please use the least number of

transistors. Note that all three inputs and their complements are available for this circuit.

(b) (10%) Design a 3-input minority gate using CMOS **NANDs**, **NORs,** and **inverters**. Compare the numbers of transistors required in (a) and (b).

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HW1 Office hours: 10/3 14:00-16:00 @電二 329 室
10/4 14:00-16:00 @電二 329 室

If you have no time during office hours, you can email TA to discuss another time for an appointment.