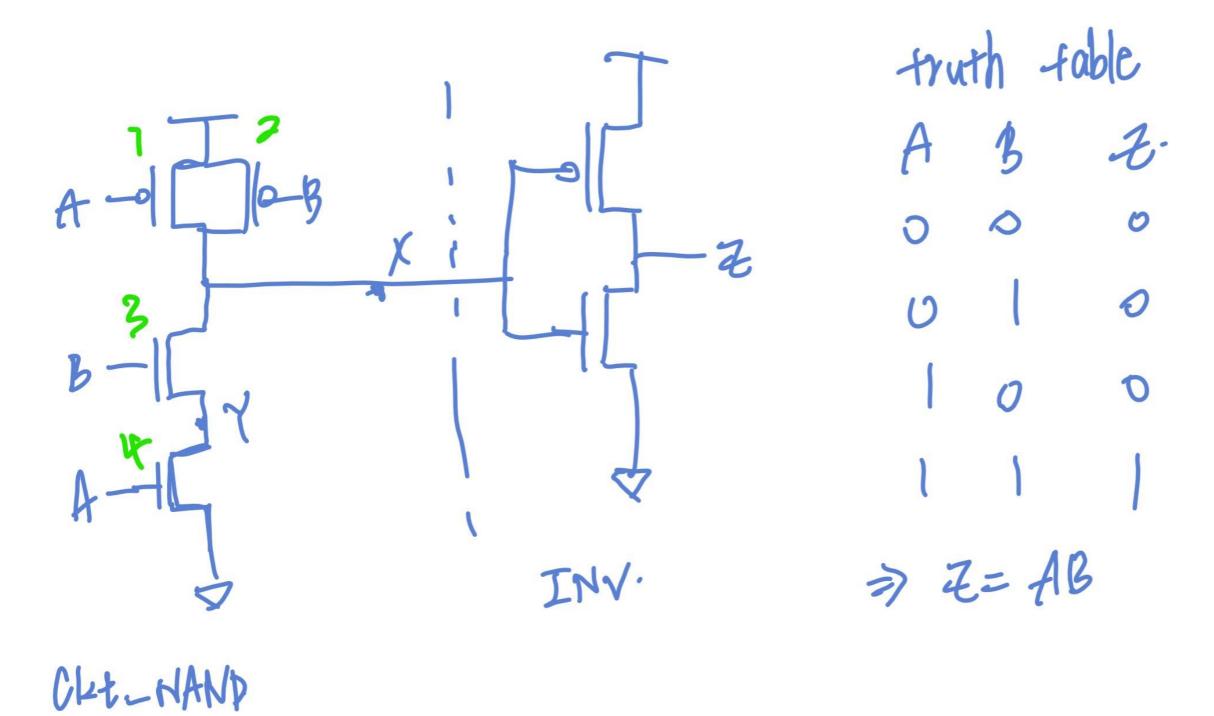
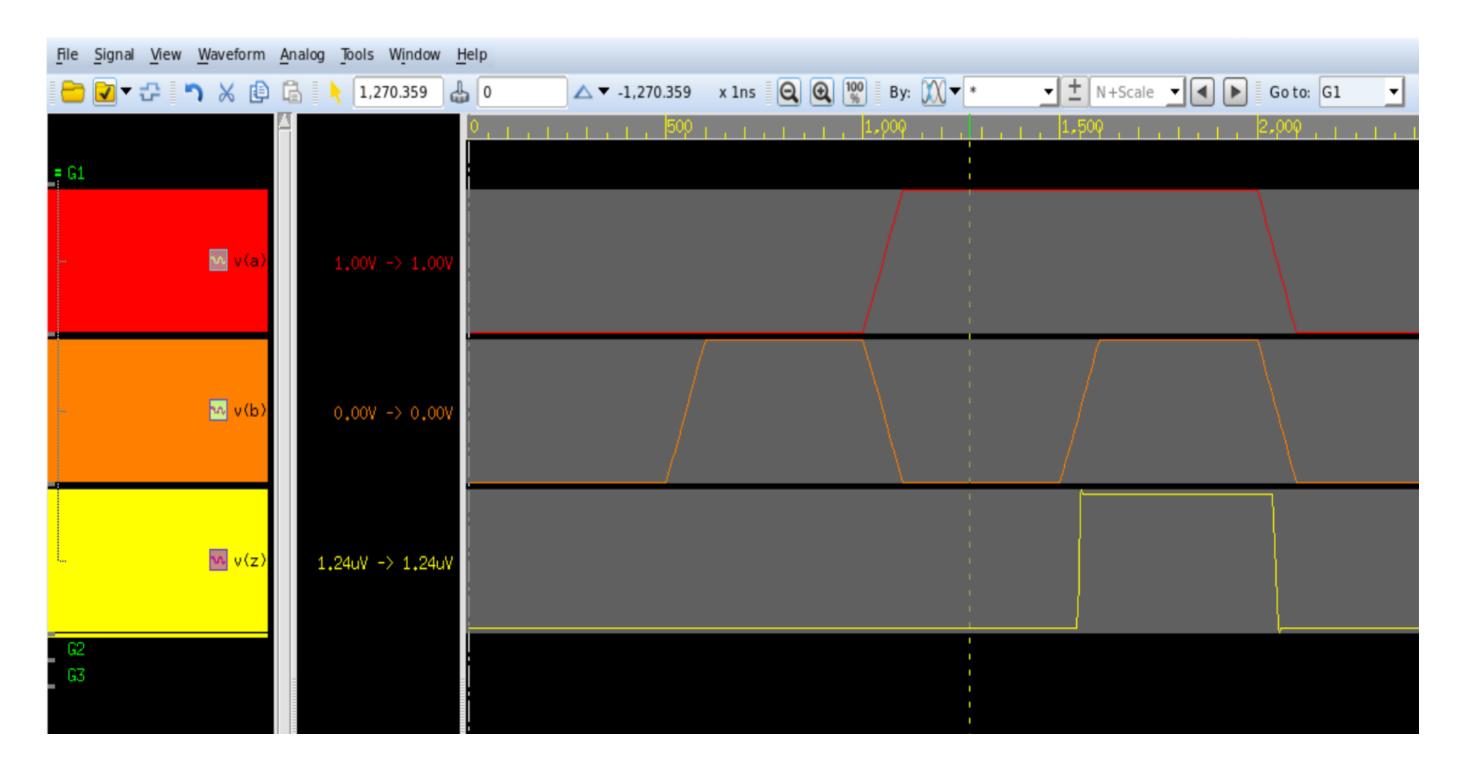
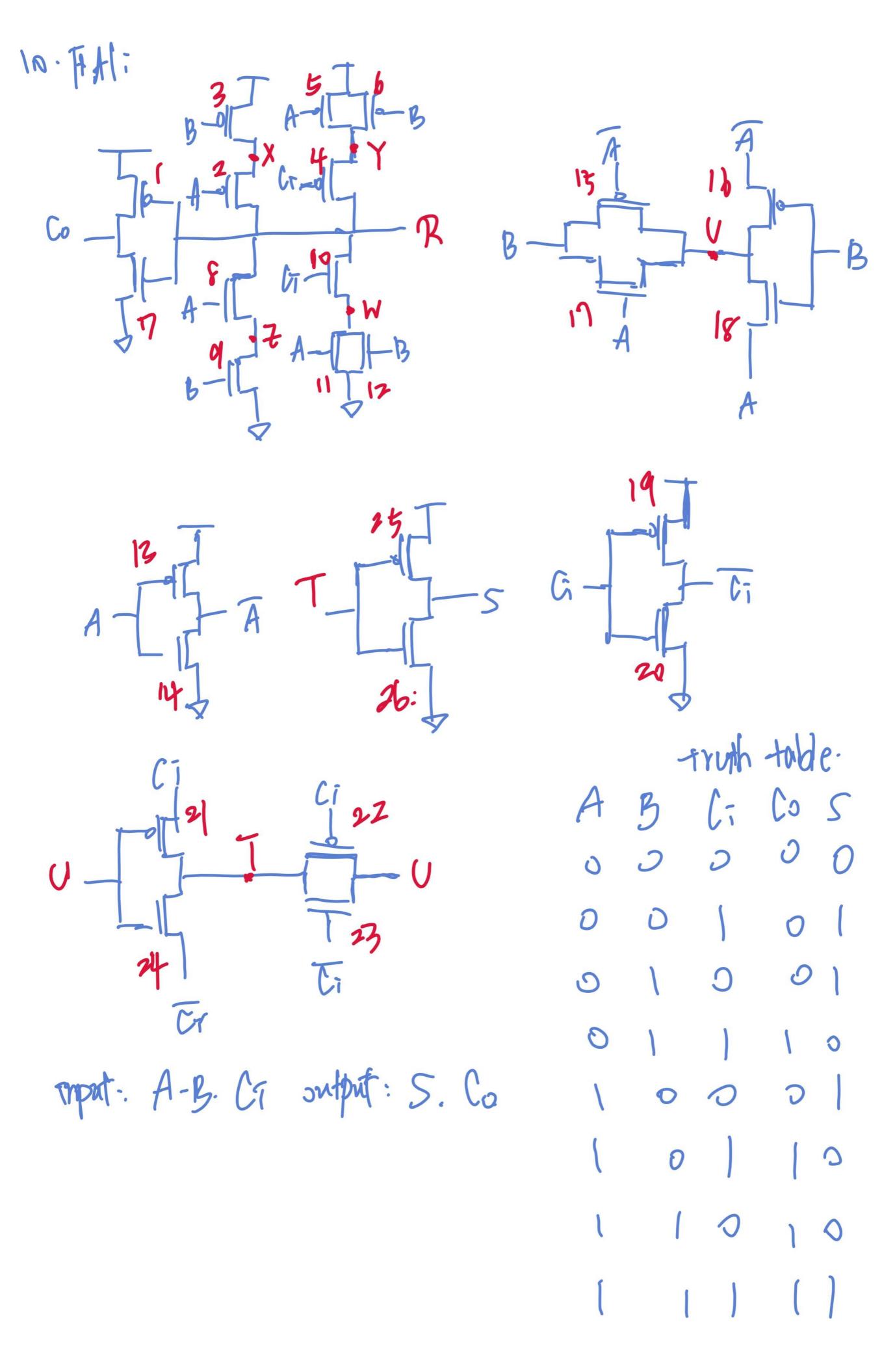
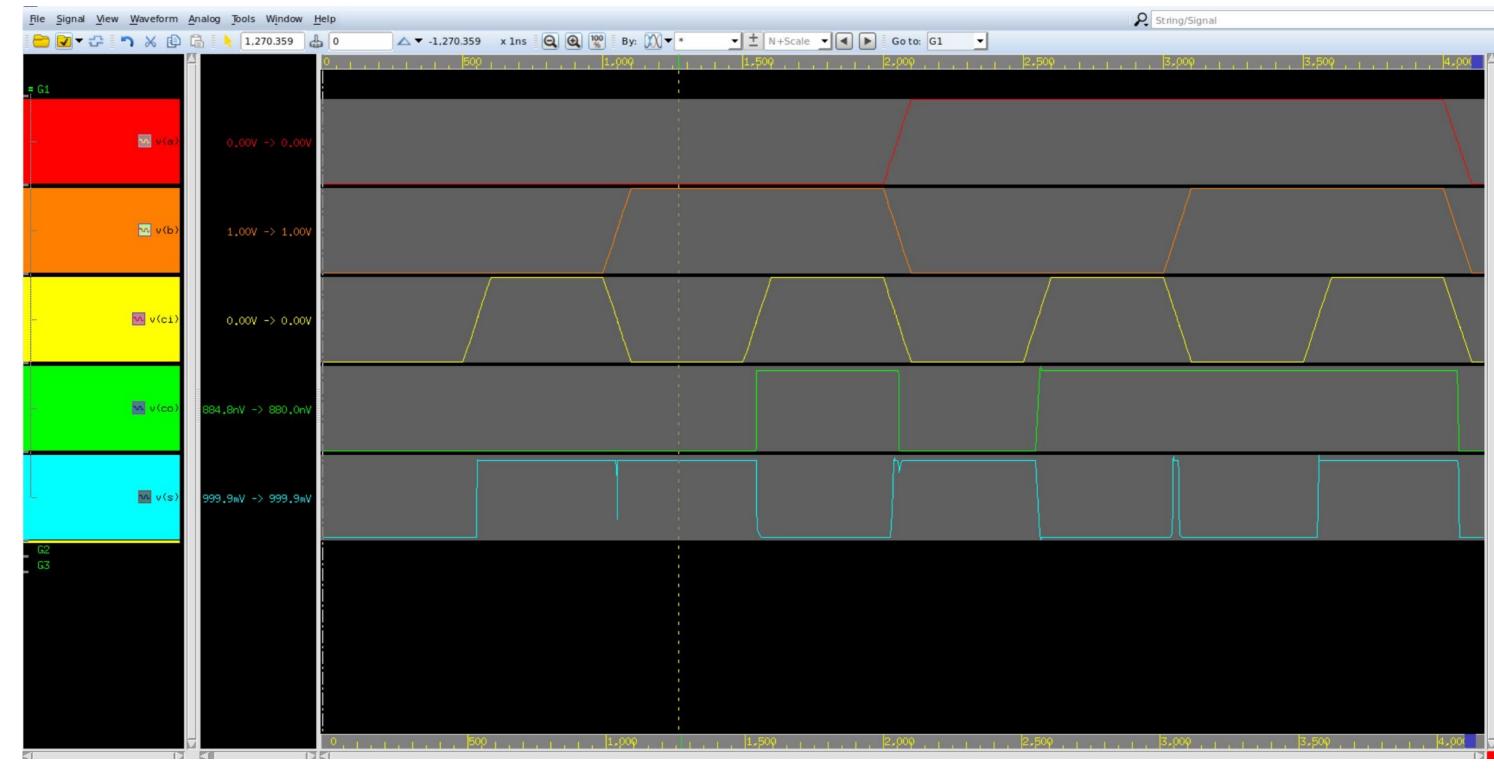
6. AN2. Triput: A.B. output=2.





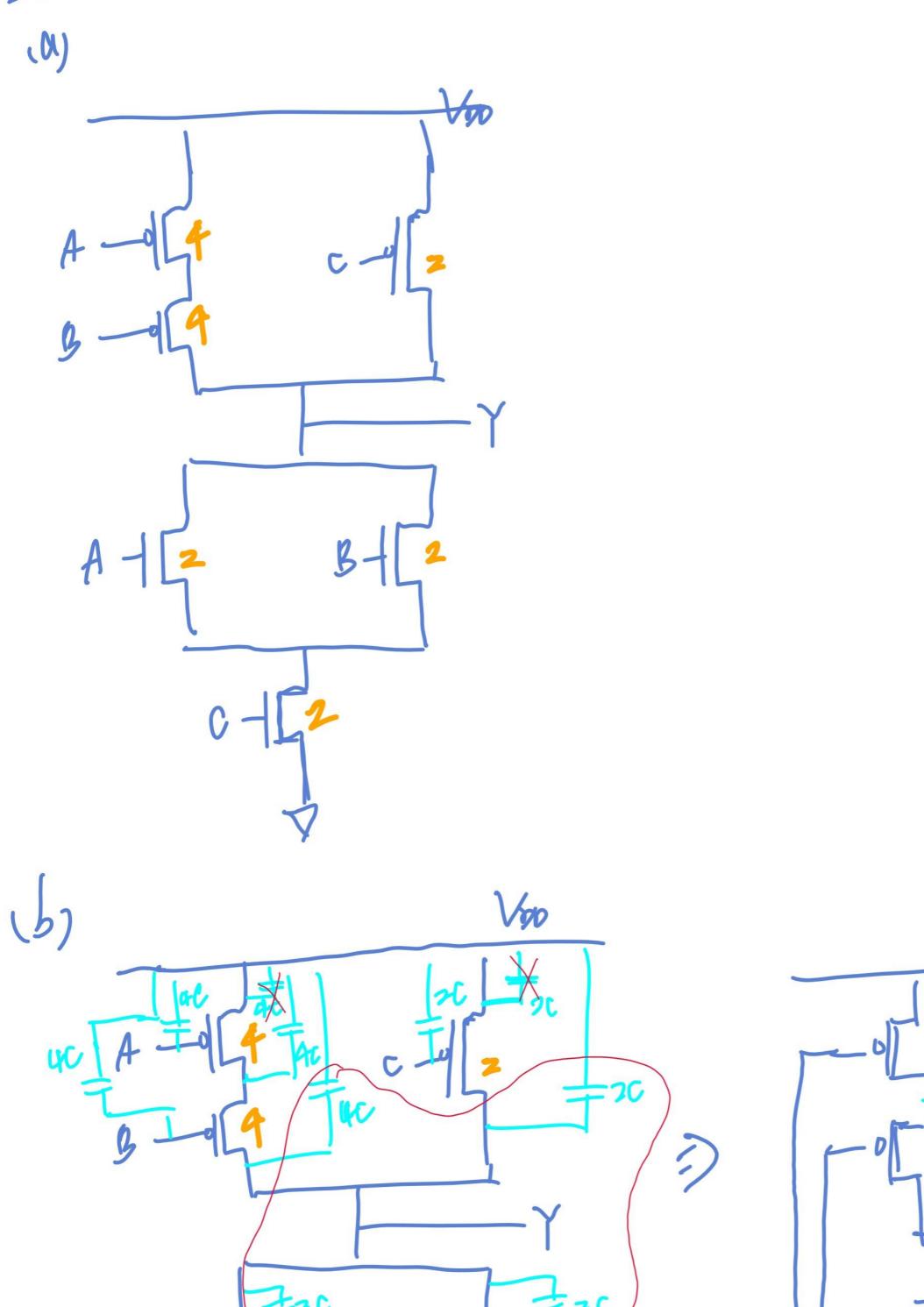
觀察: rising time and falling time is very small, and the function is correct.





觀察: some interval time have some ripple, but the function result is correct.

這是我第一次觀察一個基本電路的layout,讓我花了很多時間理解與熟悉,其中最難的部分是判斷哪些等電位以及哪些部分沒有連接等,之後把整個cell分成很多區塊個別擊破,並且在Hspice裡接在一起就能模擬出基本電路了。

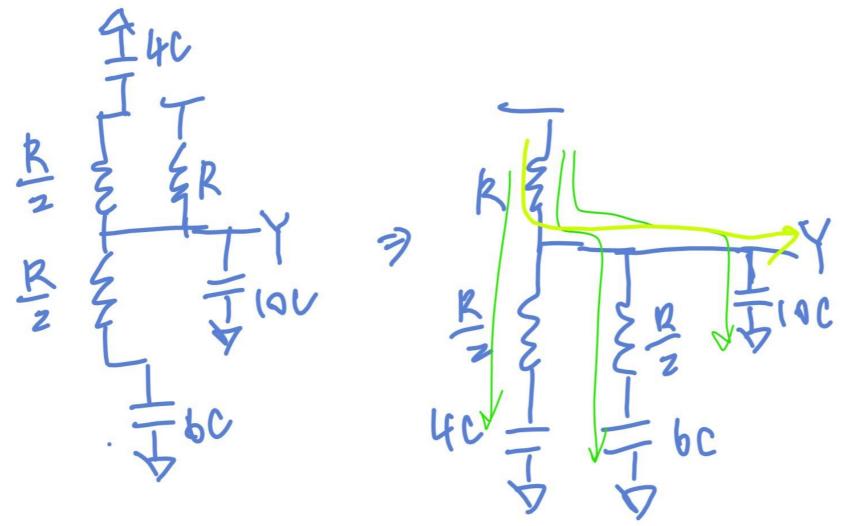


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falling: for worst case. A=|...B=0-L=| (covor the nost capacitor)  $\frac{1}{2} CC \qquad delay = \frac{1}{2} \times 6C + (\frac{1}{2} + \frac{12}{2}) \times 6C + (\frac{1}{2} + \frac{12}{2}) \times 6C$  = 3RC + (0RC + 4RC = 17RC)

rising: for worst case. - A= |. B=0. C=0

( cover the most capacitor)



7 doly= Rx4C+Rx6C+Rx10C= 20RC

