金家逸　　B10502076　　電機三

1.

what backside power delivery is:

Aims to separate power and I/O wiring, shifting power lines to the back of the wafer.

how it works:

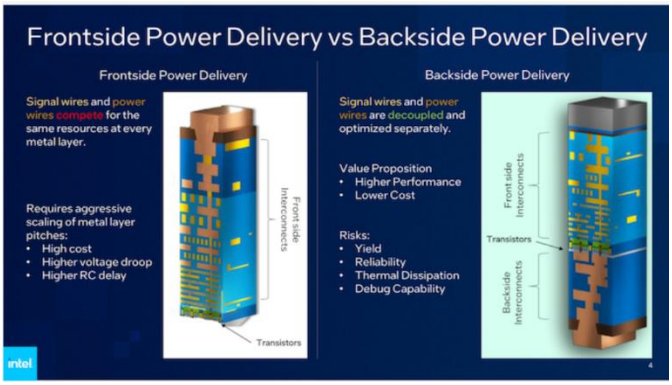
In the chip manufacturing process using PowerVia backside power delivery technology, all complex logic layers and signal lines are first constructed. Then, the wafer is flipped, and the power supply network is built above the logic layers.

what advantages it has:

Address the connectivity bottlenecks in area scaling, improve transistor performance, and reduce its power consumption. It can also eliminate potential interference between data and power lines while increasing the logic transistor density.

what difficulties it has to overcome:

Creating a backside power delivery is very different from traditional front-side power supply methods. Each wafer's fabrication begins with the most complex M0 transistor layer, using cutting-edge manufacturing tools like EUV scanners. Then, chip manufacturers build less complex transistor layers on top of the first layer and gradually increase in size while connecting all layers and powering all transistors as needed, such that the physical I/O and power lines appear massive, and each generation of new products becomes more expensive.



參考資料: Intel Details PowerVia Backside Power Delivery Technology | Tom's Hardware (tomshardware.com)

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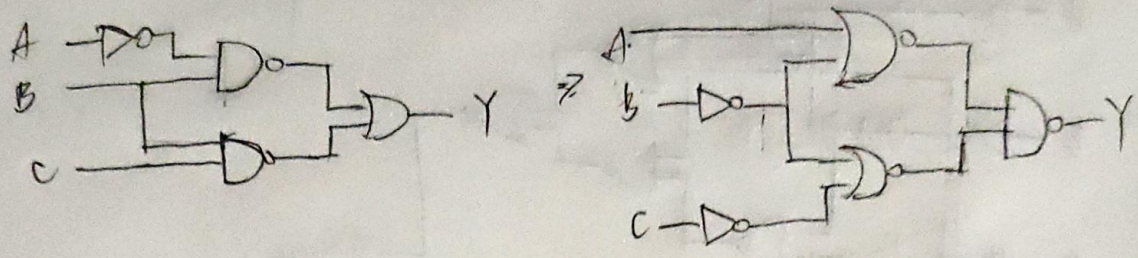
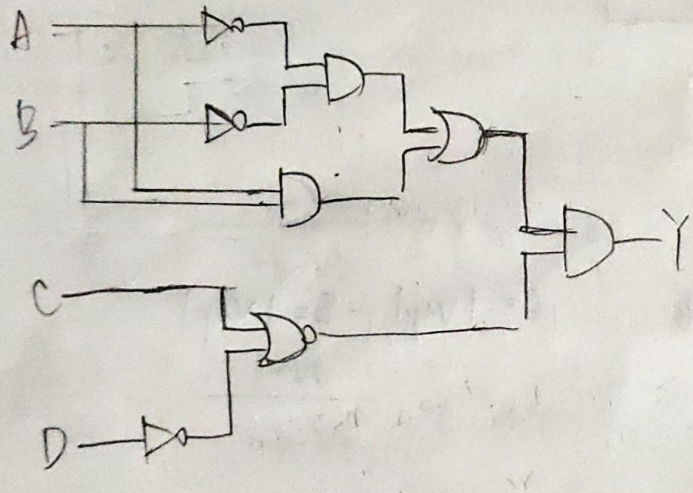
(a)



(b) $Y = \overline{A \oplus B} \cdot \overline{C + D} = (A' \oplus B) \cdot \overline{(C + D)} = (A'B + AB') \cdot \overline{(C + D)}$



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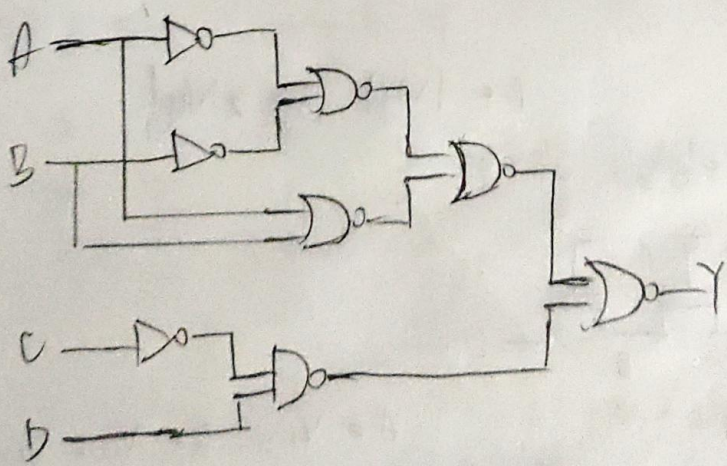
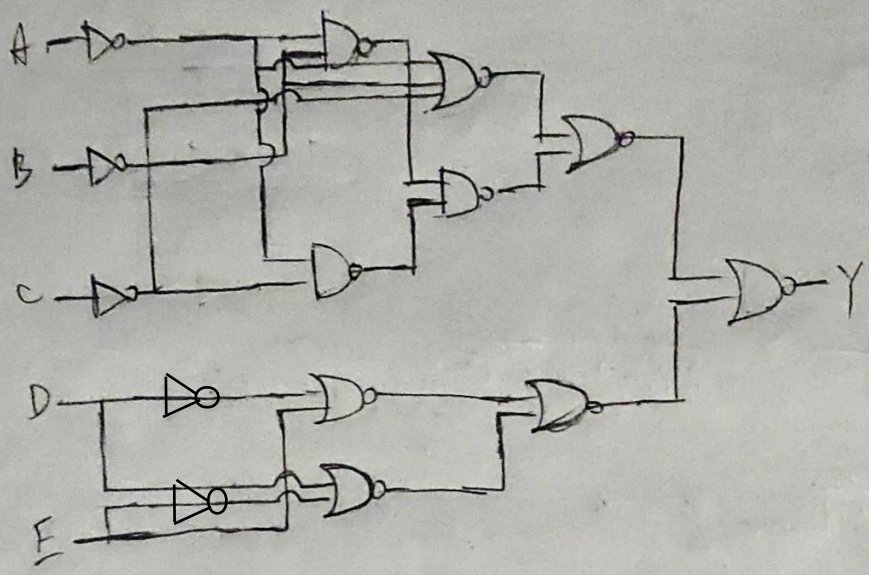


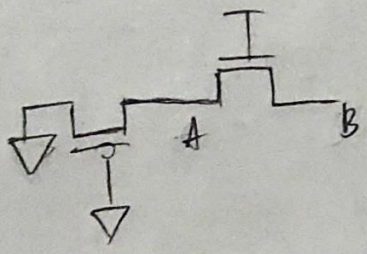
(4) $Y = \overline{A \oplus (B \cdot C)}\,(\overline{D \oplus E}) = [A' \oplus (B \cdot C)](D' \oplus E)$

$= [A'(B'+C') + ABC](D'E + DE')$



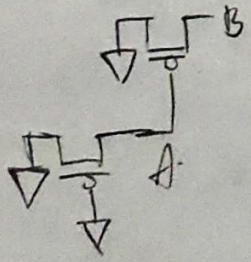
3.

(a)



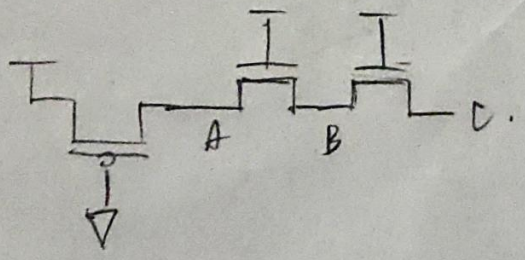
$A = |V_{tp}|$ $B = |V_{tp}|$

(b)



$A = |V_{tp}|$ $B = 2|V_{tp}|$

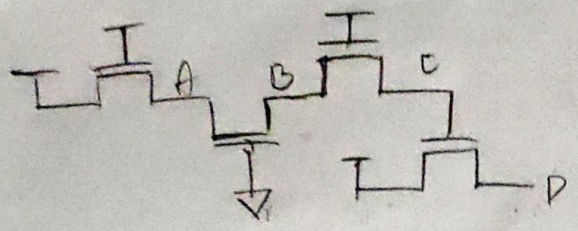
(c)



$A = V_{DD}$ $B = V_{DD} - V_{tn}$

$C = V_{DD} - V_{tn}$

(4)



$A = V_{DD} - V_{tn}$

$B = V_{DD} - V_{tn}$

$C = V_{DD} - V_{tn}$

$D = V_{DD} - 2V_{tn}$

5.

$$\text{slope at zero} = \frac{1}{k_n V_{ov}} = \frac{1}{k_n (V_{gs} - V_{tn})}$$

$$\frac{336}{252} = \frac{1 - V_t}{0.8 - V_t} \Rightarrow V_t = 0.2$$

$$\frac{252}{168} = \frac{0.8 - V_t}{0.6 - V_t} \Rightarrow V_t = 0.2 \qquad \Rightarrow V_t = 0.20$$

$$\frac{336}{168} = \frac{1 - V_t}{0.6 - V_t} \Rightarrow V_t = 0.2$$

6. inputs: A, B, C output: Y

A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

$\Rightarrow Y = B'C' + A'B' + A'C'$

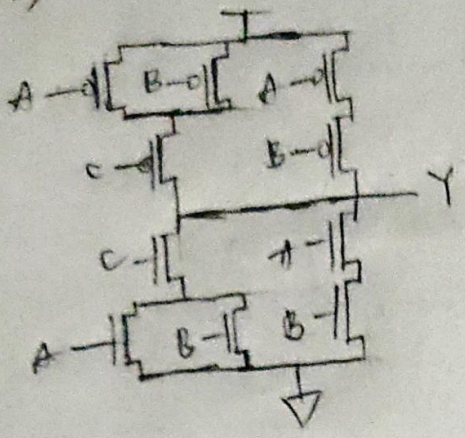
$= A'B' + (A' + B')C'$

$\overline{Y} = (A+B)(C+AB)$

$= AC + BC + AB$

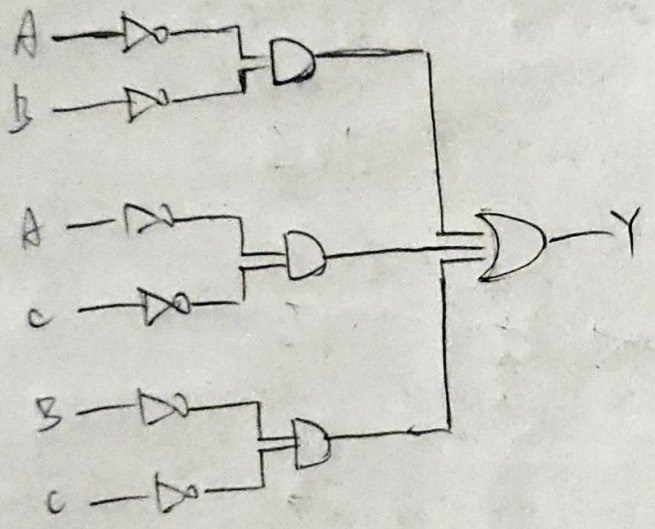
$= AB + (A+B)C$

(a)

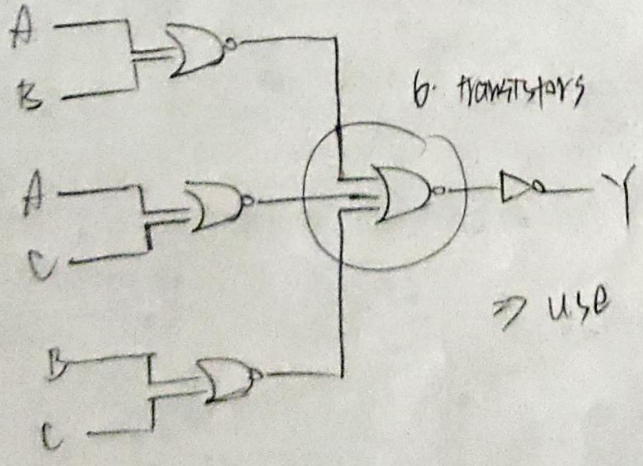


⇒ use 10 transistors

(b)



⇒



6 transistors

⇒ use 20 transistors

4.

(a)

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

$\Rightarrow Y = A \oplus B$

(b)

當 A=0 B=0 ⇒ transmission-gate NMOS is on.

⇒ Y=0 no bad zero

當 A=0 B=1 ⇒ MP1 is on ⇒ Y=1 no bad one.

當 A=1. B=0. ⇒ transmission-gate PMOS is on

⇒ Y=1. no bad one

當 A=1 B=1 ⇒ MN1 on ⇒ Y=0 no bad zero

⇒ no any bad zero or bad one in this circuit