IC Design
Homework # 2

Due on 10/19/2023, 9:20 online

Plagiarism is not allowed. 10% penalty for each day of delay.

In this homework, you will learn the following:

- Hspice
- nWave

1. (70%)

Two of the following cells are assigned to each of you. **Everyone must do cell (10). Those whose student ID ends with '*k*' must also do cell *k*.** (Ex. If your ID is Bxx901123, you need to do (3) EO3, (10) FA1.)

(0) EN
(1) NR2
(2) OR2
(3) EO3
(4) AN3
(5) ND2
(6) AN2
(7) EO
(8) DRIVER
(9) IV
(10) FA1

For each cell,

a. Base on the layout view, draw **transistor-level** diagrams (using PowerPoint, paint or 手畫)

b. Identify all **inputs** and **outputs**

c. List **truth table**

d. Revise the given netlist file to construct your cells. All PMOS transistors have width 0.5um and length 0.1um. All NMOS transistors have width 0.25um and length 0.1um. Parameters of the 90nm model file (90nm_bulk.l) must be included during the simulation. The substrate of PMOS is connected to VDD and the substrate of NMOS is connected to VSS.

e. Run *Hspice* simulation on **all possible input** combinations. Assume

VDD=1.0V and VSS=0V. Use *nWave* to verify the truth table. Copy the **I/O waveform** to your report. State what you have observed.

f. Please discuss the problems you have encountered.

Files that you will need (available on the class website)

HW2_2023.zip includes the following files

- HW2_2023.pdf (this document)
- HW2_tutorial_2023.pdf
- example.sp (CMOS inverter的範例程式)
- 90nm_bulk.l
- Pictures of layouts (in "pic" folder)

Files that you need to submit

- Your report named StudentID_hw2_report.pdf (ex: b05901058_hw2_report.pdf)

- List the names of the cells you did in homework.
- The inputs, outputs, transistor-level diagrams, and truth tables of the cells you did in homework
- The waveform results of your HSpice simulation
- The answers to the following problems 2. and 3.

- The HSpice codes named after the cell names

References

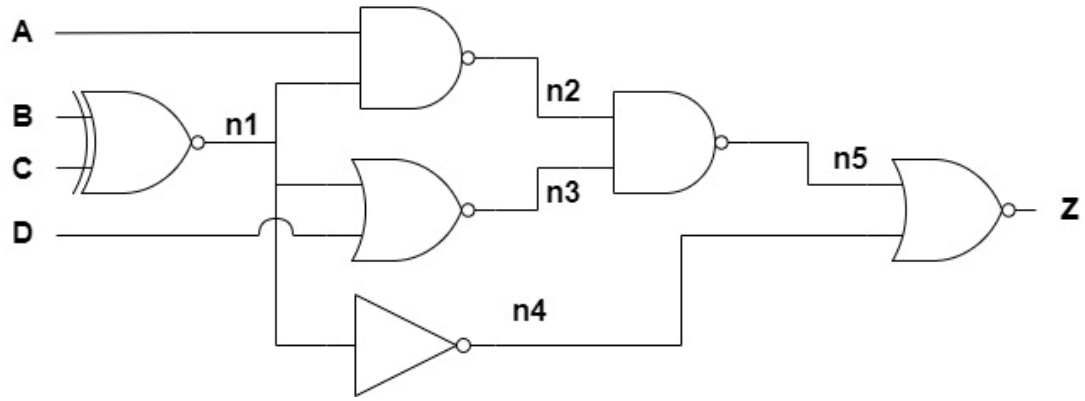
[1] "SPICE," CIC handout, 2001

[2] "鳥哥的 Linux 私房菜," http://linux.vbird.org/

If there's any workstation account/password problem, please directly contact the workstation administrator，林明廣，f09943114@ntu.edu.tw

2. **(20%)** In Chapter 3, we analyzed the rising and falling delays of a NAND3 gate with fanout *h* (slide 10 of Chapter 3).
   (a). Following a similar approach, for the single-stage CMOS static gate with logic Y=[(A+B)C]', where L=1 for all transistors, **draw the circuit** and **specify the inputs and the W** for all transistors that balance the rising and falling delays.
   (b). Derive the falling and rising delays of the gate assuming $h = 0$. (consider the worst case)

3. **(10%)** Determine the activity factors at each node in the following circuit assuming the input probabilities $P_A = P_B = P_C = P_D = 0.5$. (be careful with the dependency)



TA：陳帝宇，EE2-329

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HW2 Office hours: 10/16 14:00-16:00 @ EE2-329

10/18 14:30-16:30 @ EE2-329

If you have no time during office hours, you can email TA to discuss another time for an appointment.