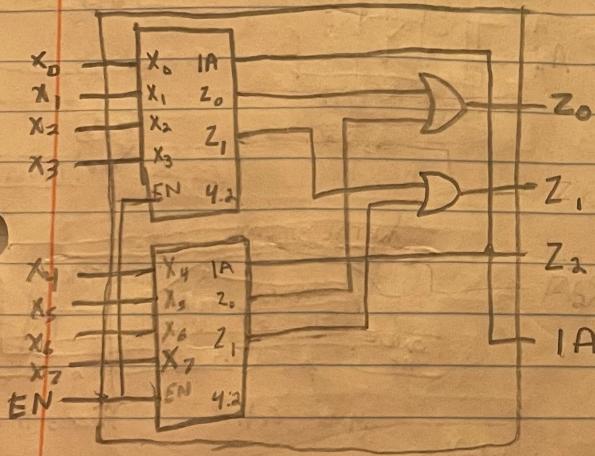
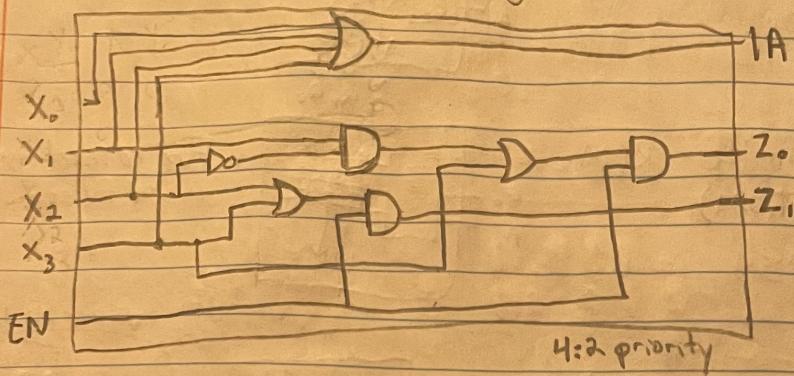


# Homework III

## Problem I

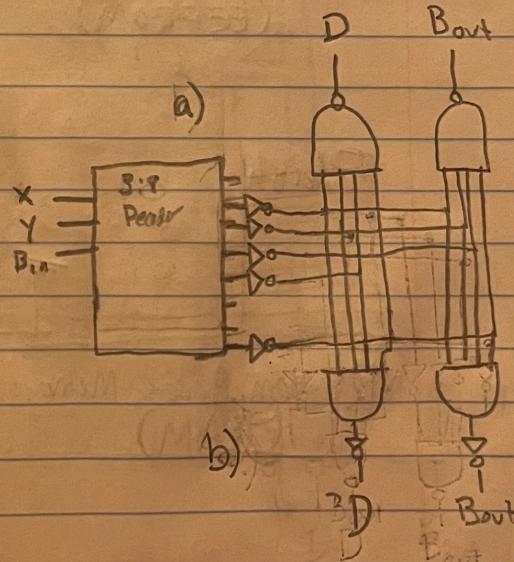
II midday

1. 8 to 3 priority encoder using two 4-to-2 priority encoders

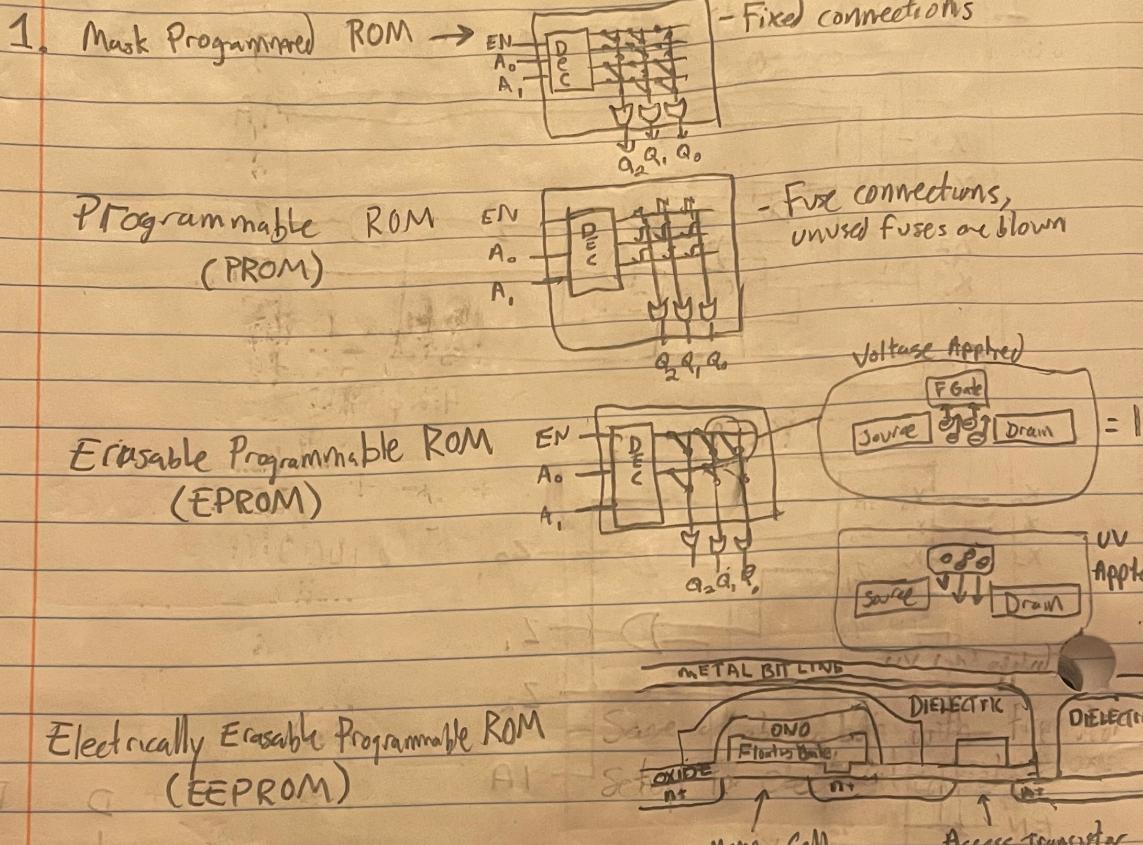


2.

$X$	$Y$	$B_{in}$	$D$	$B_{out}$
0	0	0	0	0
0	0	1	1	1
0	1	0	2	1
0	1	1	3	1
1	0	0	4	0
1	0	1	5	0
1	1	0	6	0
1	1	1	7	1

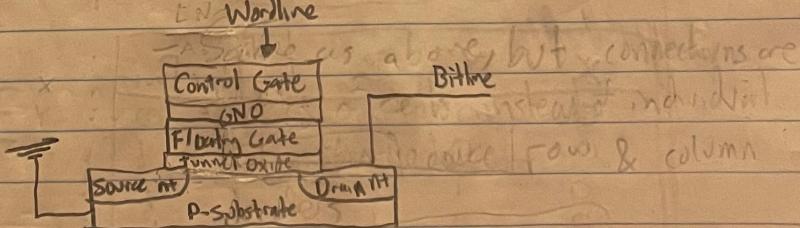


## Problem II

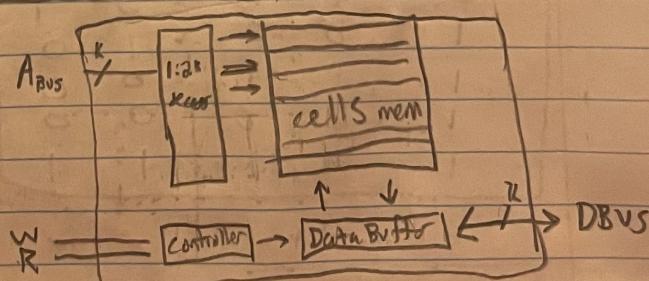


Electrically Erasable Programmable ROM (EEPROM)

Flash



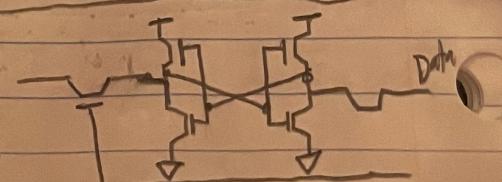
Random Access Memory (RAM)



Static RAM (SRAM)

Each memory cell

Holds data as long as power is supplied



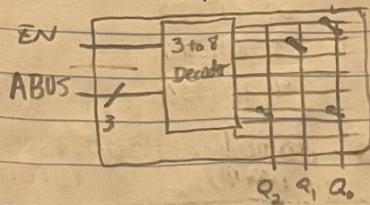
## Problem II

1  
continued

Dynamic RAM  
DRAM



2.

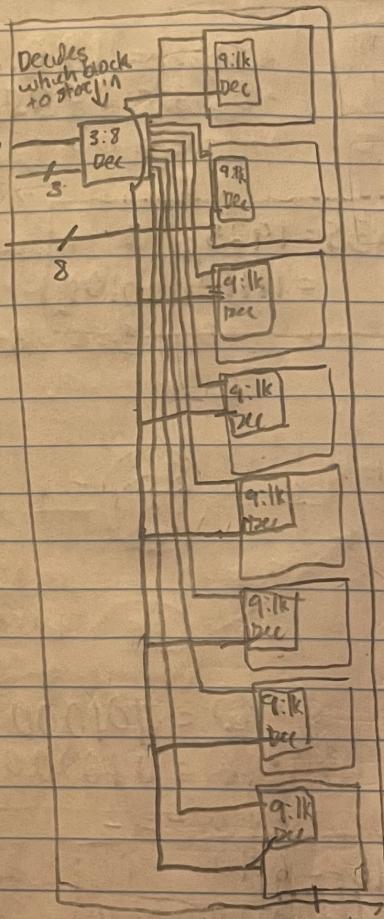


$$3. \quad 1K \times 8 \rightarrow 8K \times 8 \rightarrow$$

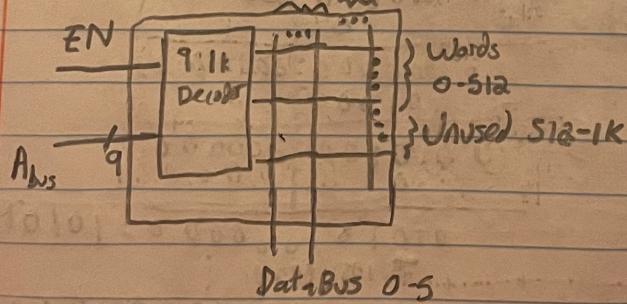
Enable

sel.

ABUS



4.



### Problem III

#### 1. Shift / Add Algorithm

$$\cdot 15_{10} = 00101111_2 = X$$

$$\cdot 66_{10} = 1000010_2 = Y$$

$$0: 00000000 \quad 5: 111100000$$

$$1: 11110 \quad 6: 11101110$$

$$2: 111100$$

$$3: 111000$$

$$4: 1110000$$

$$15 \times 66 = 1111011110 = 990$$

$$\cdot 55_{10} = 110111$$

$$\cdot 35_{10} = 100011$$

$$0--- = +$$

$$0\ 000000\ 100011$$

$$+ 11101111$$

$$\hline 0\ 11011111\ 000011$$

$$0\ 011011110001$$

$$+ 110111010$$

$$\hline 1\ 010010110001$$

$$0\ 101001011000$$

$$+ 000000$$

$$\hline 0\ 101001011000$$

$$0\ 010100101100$$

$$+ \hline 0$$

$$\hline 0001010010110$$

$$+ \hline 0$$

$$\hline 0\ 000101001011$$

$$+ 110111$$

$$\hline 111100001011$$

$$111100001011$$

$$\cdot 40 = 101000$$

$$\cdot 16 = 010000$$

$$0 + 0 - = -$$

$$40 \bar{x} 16 = -640$$

$$= 101100000000$$

$$0\ 000000\ 010000$$

$$+ 0\ 000000\ 001000$$

$$+ 0\ 000000\ 000100$$

$$+ 0\ 000000\ 000010$$

$$+ 0\ 000000\ 000001$$

$$+ 101000$$

$$+ 0\ 010100\ 000000$$

$$+ 0\ 000000\ 000000$$

$$+ 01010\ 000000 = 1010111111 + 1$$

Two's Comp

$$10110000000$$

### Problem III (continued)

#### 2. Restory Algorithm

$$\cdot S_8 = 111010$$

$$\cdot I_3 = 001101$$

$$Q = 100_2 = 4_{10} \checkmark$$

$$AC = 110_2 = 6_{10} \checkmark$$

AC	Q
000000	111010
- 000001	110100 L shift - (1)
001101	Sub Y
0000011101000	Not possible
- 000011101000	L shift - (2)
001101	Sub Y, not possible
000111010000	L shift - (3)
- 001101	Sub Y, not possible
0011100100000	L shift - (4)
- 001101	Sub Y, add 1
000001100001	L shift - (5)
- 001101	Sub Y, not possible
000011000010	Sub Y, not possible
- 001101	Sub Y, not possible
00001100001000	L shift (b)

$$\cdot -85 = 1010101$$

$$\cdot 27 = 0011011$$

$$\cdot n = 7$$

$$Q = 11_2 = 3_{10} \checkmark$$

$$AC = 100_2 = 4_{10} \checkmark$$

AC	Q
0000000	1010101
- 0000001	0101010 L shift - (1)
0011011	Sub Y, not pos
000001010101000	L shift - (2)
- 0011011	Sub Y, not pos
000010101010000	L shift - (3)
- 0011011	Sub Y, not pos
000101010100000	L shift - (4)
- 0011011	Sub Y, not pos
001010101000000	L shift - (5)
- 0011011	Sub Y, not pos
000000000000000	L shift - (6)
- 0011011	Sub Y, add 1
00011110000001	L shift - (7)
- 0011011	Sub Y, add 1
00001000000011	

## Problem IV

1. C is the counter value. Since the total # of 1's can be 8, C must have 3 bits and they should all be initialized to 0. therefore, input should be 000.

## 2. Controller as a microprogrammed Unit

Algorithms:

1. Wait until  $S = 1$

2.  $R \leftarrow A, LR = 1$

3.  $C \leftarrow 000, LC = 1$

4. For  $i = 0 \dots 7$

5. If  $A_{A_0} = '1'$

$C \leftarrow C + 1, IncC = 1$

6. Set  $SR = 1, LR = 1$

7. Set  $S = 0$ , Done to 1

Control / Status Signals

$S$

$LR = 1$

$LC$

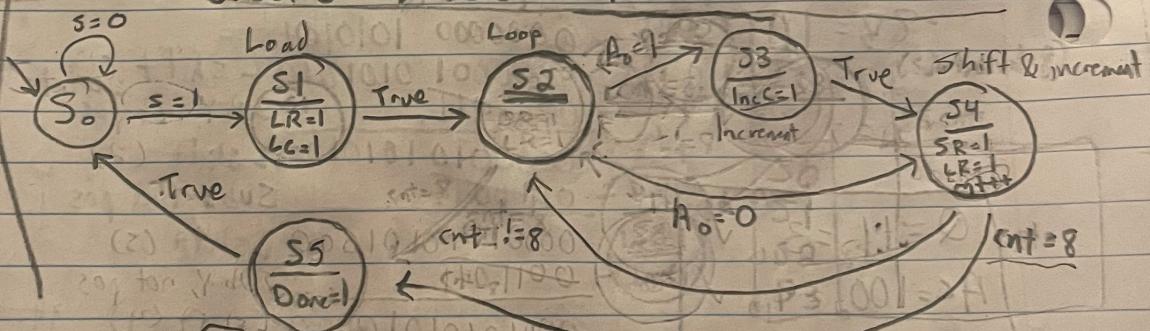
$IncC$

$SR$

Done

int

Notes



$(S, A_0, cnt = 8)$

1  
2

$S, A_0, cnt = 8$

$(0, 0, 0), (0, 0, 1), (0, 1, 0), (0, 1, 1), (1, 0, 0), (1, 0, 1), (1, 1, 0), (1, 1, 1)$

$(LR, LC, IncC, SR, LR, Done)$

	$S_0$	$S_0$	$S_0$	$S_0$	$S_1$	$S_1$	$S_1$	$S_1$	$(0, 0, 0, 0, 0, 0)$
$S_1$	$S_1$	$S_2$	$(1, 1, 0, 0, 0, 0)$						
$S_2$	$S_2$	$S_4$	$S_4$	$S_3$	$S_4$	$S_4$	$S_3$	$S_3$	$(0, 0, 0, 0, 0, 0)$
$S_3$	$S_3$	$S_4$	$(0, 0, 1, 0, 0, 0)$						
$S_4$	$S_4$	$S_2$	$S_5$	$S_2$	$S_5$	$S_5$	$S_2$	$S_5$	$(0, 0, 0, 1, 1, 0)$
$S_5$	$S_0$	$S_0$	$S_6$	$S_0$	$S_0$	$S_0$	$S_0$	$S_0$	$(0, 0, 0, 0, 0, 1)$

↓ Output