EEL 3701C - Digital Logic & Computer Systems

Lab 1 Report

Due one week after regular lab completion.
Delay penalty: 10% per week, maximum 40%

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Prelab Report

Prelab Design and Implementation

This prelab was designed much more effectively than Lab0. I had a far better idea of what I was working with, so it was easier to keep all of the components organized. I made use of many of the DIP gates and components, so I began to label them for future use, for further efficiency.

In terms of implementation, I tried to follow one step at a time to manage the lab. This lab took a while to complete, and it was completed over many days, in two different cities, so managing all the pieces that I needed was much simpler when I kept it organized.

Reflection

I learned that completing the prelab takes the least amount of time when I read ALL of the resources related to the lab before reading the lab. There were numerous tutorials that I overlooked to try to speed through this lab, which ended up making the lab take longer. In the end, I was happy to be able to reuse the circuitry on the breadboard for many of the prelab questions, and Copy/Paste the diagrams on Quartus by using complementary logic.

Prelab Homework

i) Truth Tables and Optimized Equations for Y1 and Y2

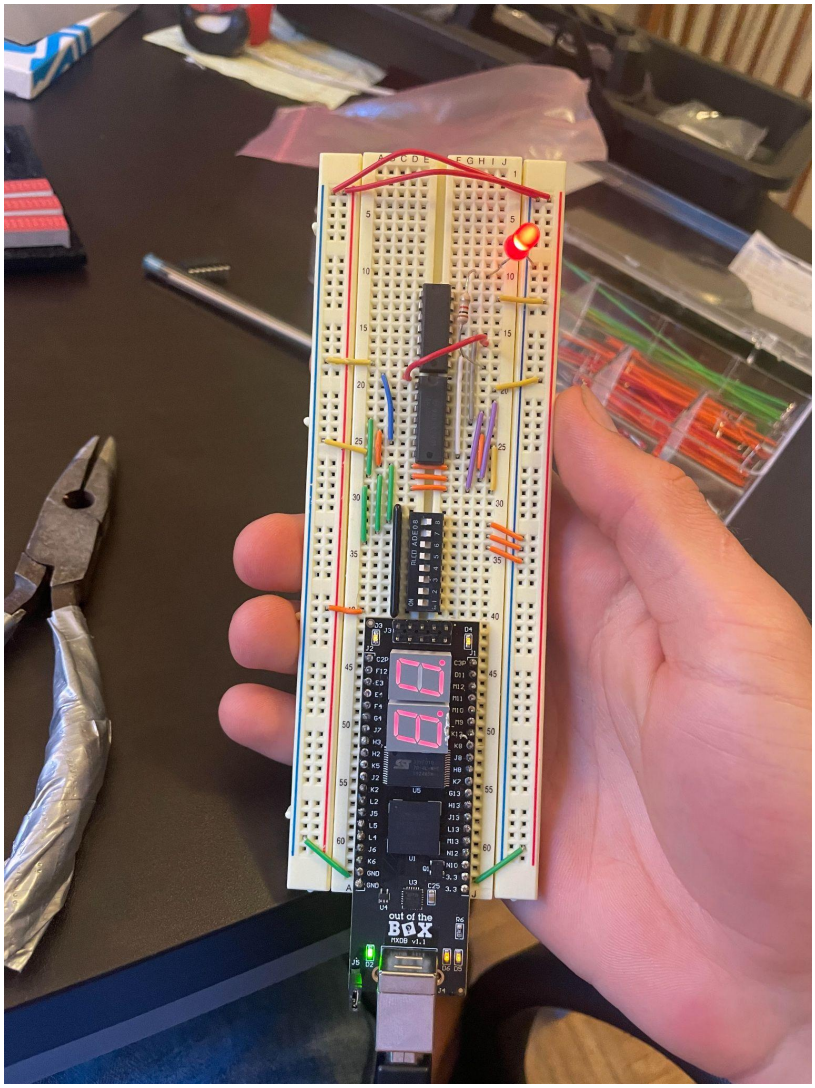
1. Optimize logic equations and find truth table
   1. Y1 = AC + AB + BC

A	B	C	Y1
0	0	0	0
0	0	1	0
0	1	0	0
1	0	0	0
1	1	0	1
1	0	1	1
0	1	1	1
1	1	1	1

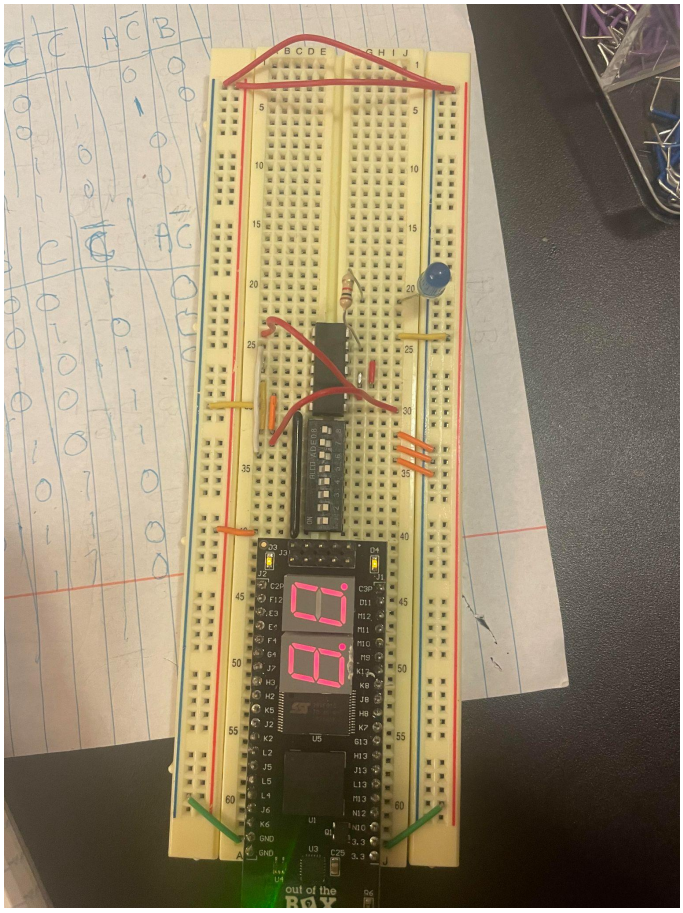
2. Y2 = AC'+B

A	B	C	Y1
0	0	0	0
0	0	1	0
0	1	0	1
1	0	0	0
1	1	0	1
1	0	1	0
0	1	1	1
1	1	1	1

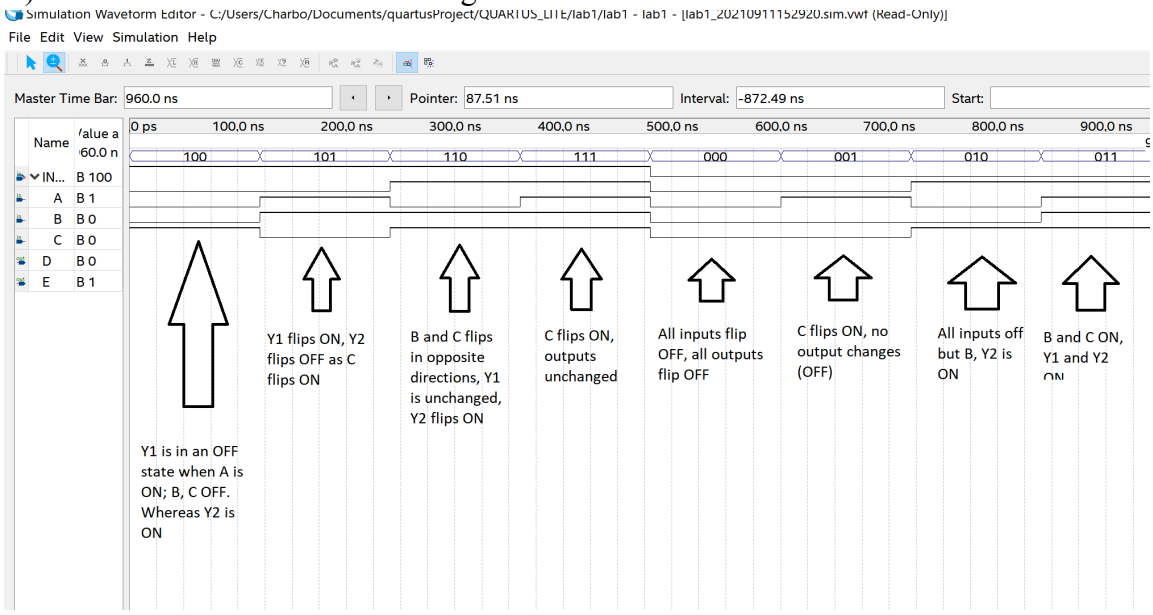
ii)Circuitry for Y1

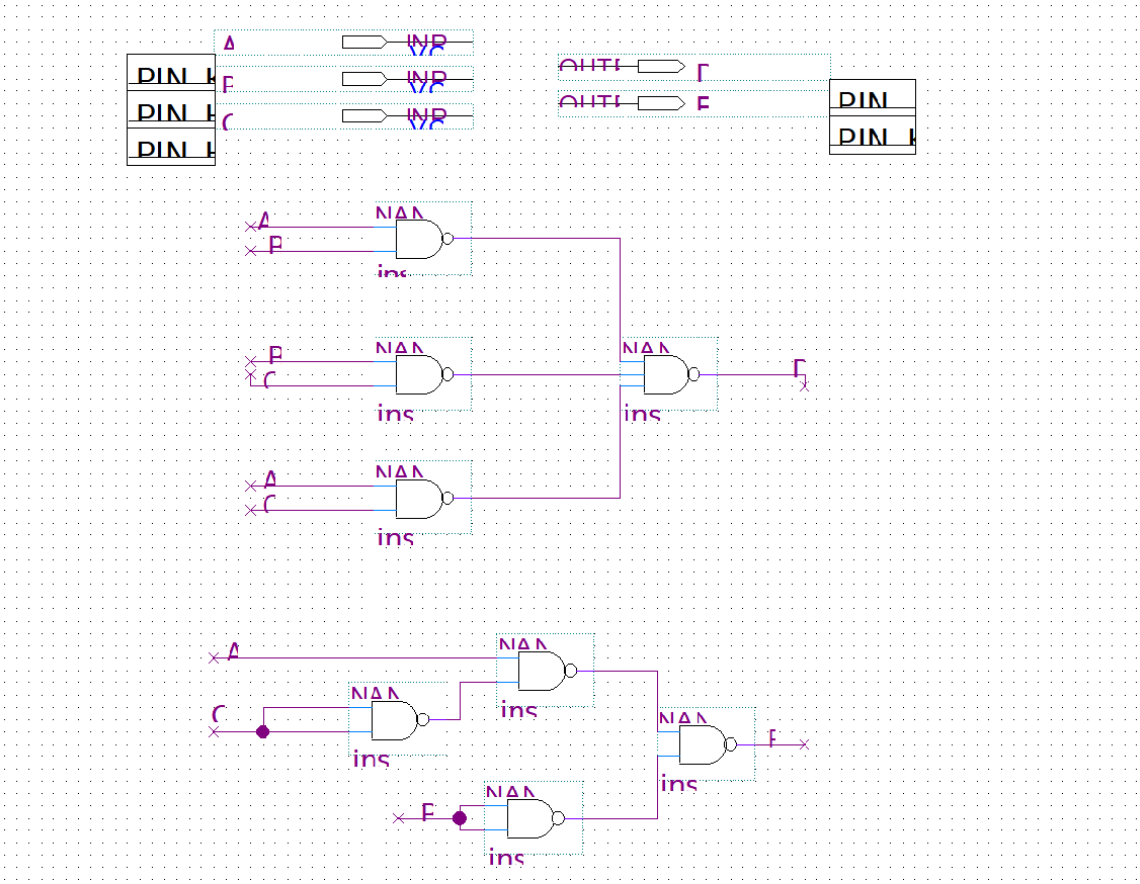


iii) Circuitry for Y2

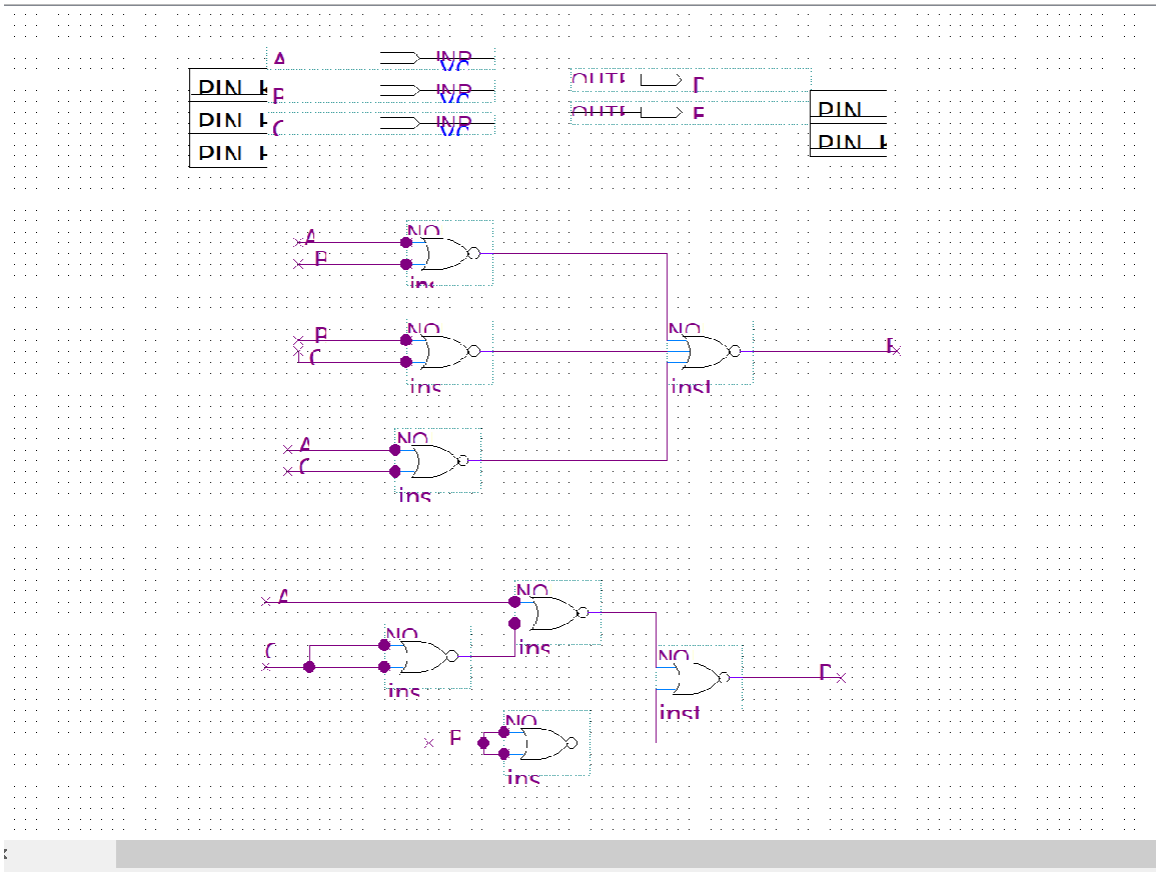


iv) NAND Gate Simulation and Diagram





v) NOR Simulation and Diagram


A
B
C
INP
INP
INP
OUTP
OUTP
F
DIN
DIN
NO
ins
NO
ins
NO
inst
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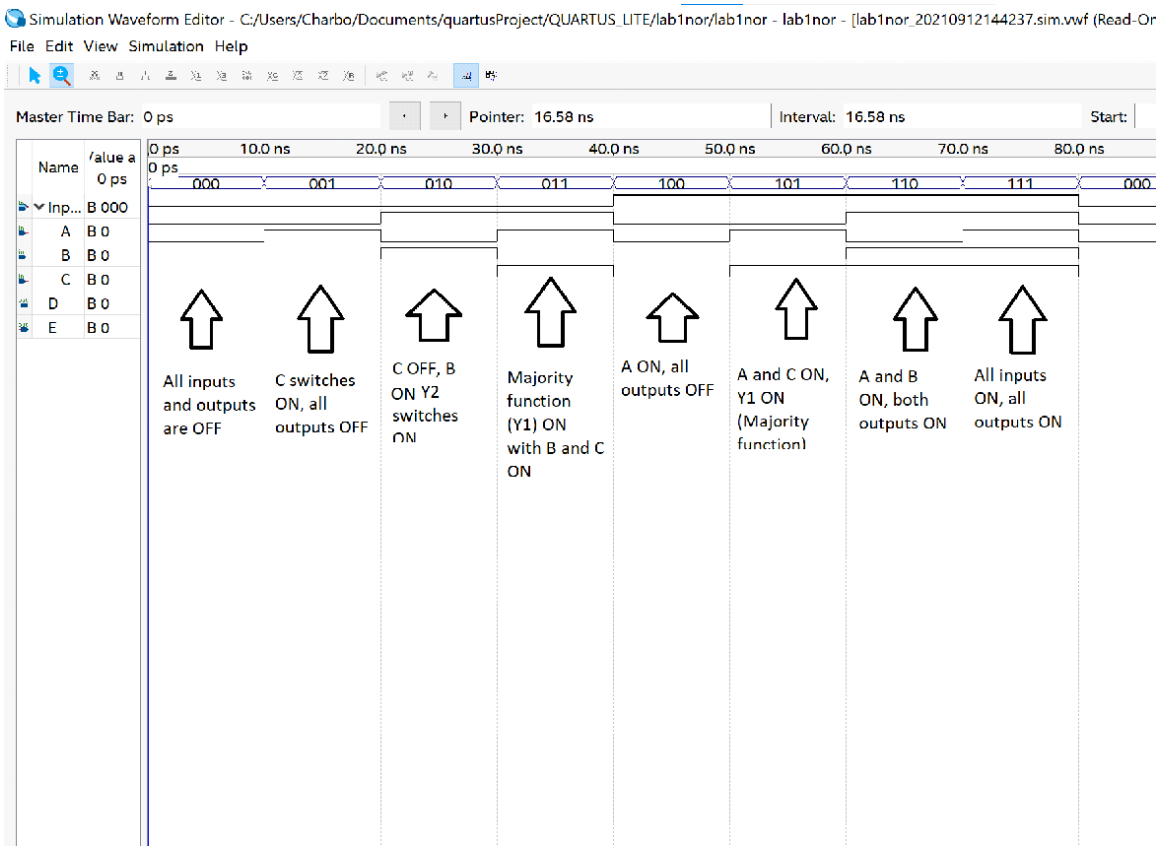


Part H attached to the submission

Post lab Report

Problem Statement:

The goal of this lab is to familiarize students with optimizing binary algebraic statements, using circuitry modeling software, and programming to a processor. The requirements for this lab required plenty of patience and problem-solving. Particularly on the software configuration side. The inputs to the lab were optimized binary equations and circuits. The output was insights into patterns in circuit design and increased fluency in-circuit CAD. The ultimate function of the lab was to teach students to develop a familiarity with the tools of the class.

Design:

With plenty of margin for error, the effective design was essential for this lab. Having all of the tools ready-handed and error-free was a top priority. Given that most of the components given to me were used during this lab (Ex. Quartus, breadboard, resistors, gates, switches, wires MXDB, USB Blaster) having a clean workspace also made a massive difference. While executing these circuit builds, I followed the steps presented by the tutorials, since they seemed to be the path of least resistance. One noticeable con of working with the tutorial and the modeling software together was my lack of expertise on the Windows OS. Had I prepared a bit more on windows, I imagine the lab would be completed much faster.

Implementation:

This is my weakest link. Implementing my plan is the weakest area of the lab for me since I struggle the most with managing the time I spend on my priorities. Work for the lab began about half a week before it was due and then was dragged with me out of town, which was a bit of a hassle. The lab was done in at least a dozen segments, which lengthened the time it took to get familiar with what was necessary. For the next lab, I plan to be prepared days ahead of time to avoid issues like this.

Testing:

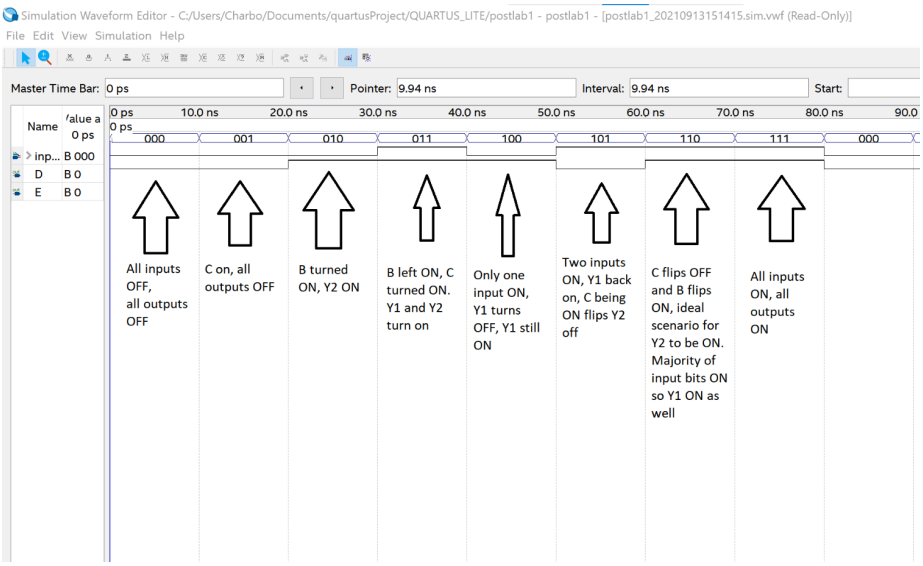
My design was tested by simply following the instructions. If I was able to make it to the next part, it means I was successful. With this lab, the result was very binary, it was either pass or fail, there was no in-between. Everything worked as expected after many clear failures, but once it worked, it was working for good. Everything was executed as expected.

Conclusions:

Unfortunately, I was not in town for the most important moments of the lab, which set my productivity way back. I learned that in order to be successful with these labs, many hours at a time must be dedicated, as well as great focus. Following a routine will be the best way to excel in this class, with this lab.

TODO: **Appendix**

Part 2:



VHDL simulation of Y1 and Y2