

Final Exam Page 1.

Name: Charles Richardson
UFID: 73112398

Problem I: General Understanding

1. Registers - To store constant N

To store j variable

To store a, b variables

ALU - To subtract variables from each other

To compare variables with each other

To compare variables with constants

MUX - To determine next address of PC

To determine which operation to complete in ALU

2. Multiplexers -

1. Multiplexer - Determine which input to pass through given n control signals and 2^n inputs, outputs

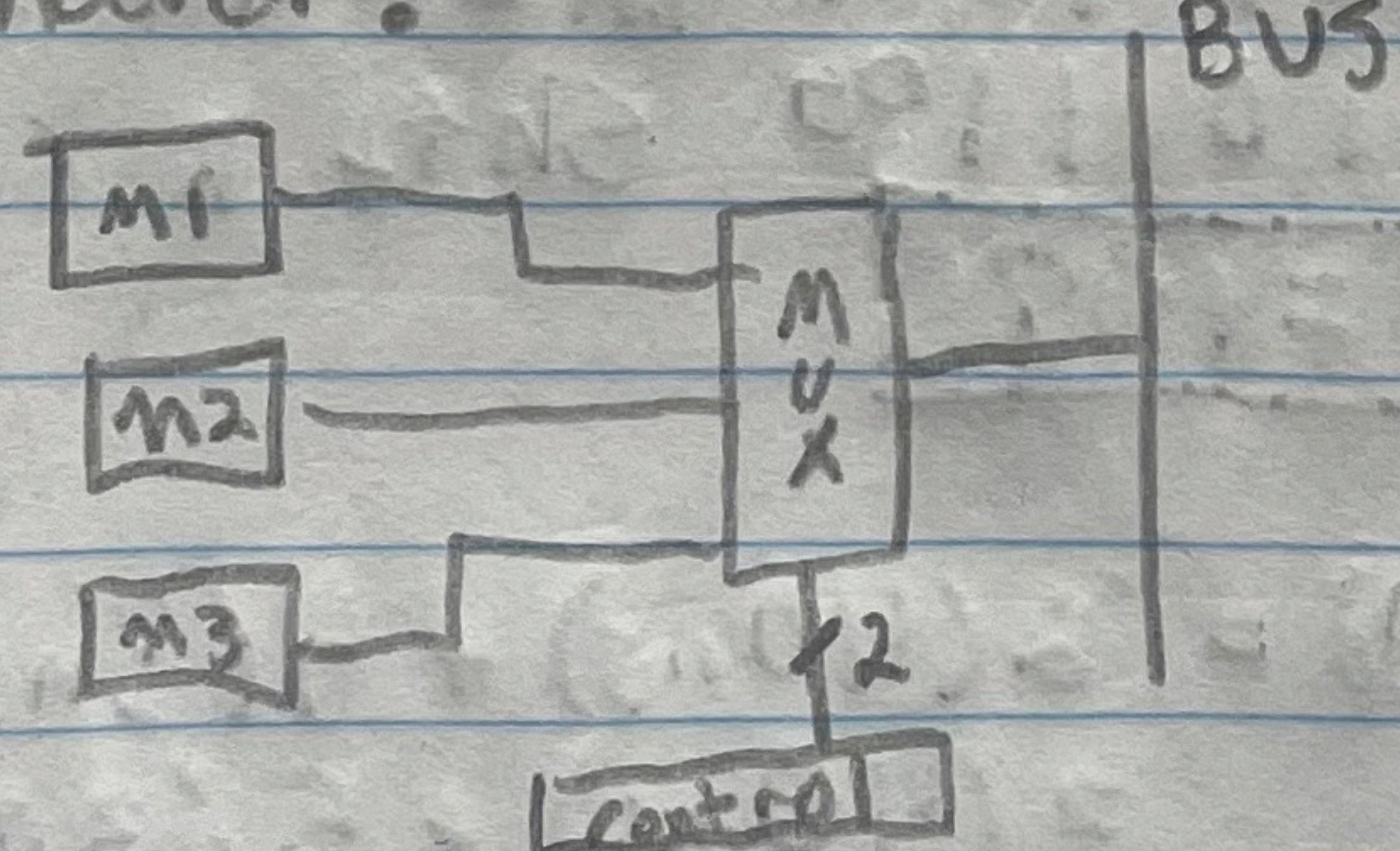
2. Decoder - Given a set of inputs representing a binary #, return an output corresponding to that binary number. n inputs, 2^n outputs

3. Binary Encoder - Opposite of a decoder, takes a set of bits that corresponds to a given number & returns an output which is the binary value of the #.

3.

1. This would not work because the modules may be writing different values which would have undefined behavior.

2.



Final Exam Pg 2

Charles Richardson

Problem I: General Understanding

4. Use a full adder (5 gates per 2 bits + carry)
- $$= 5 \times 64 = 320 \times 0.001 = \$0.32 \text{ Cost}$$
- $$\text{Delay} = 320 \times 5 \text{ ns} = 1600 \text{ ns} = 1.6 \mu\text{s Delay}$$

Adam \rightarrow Gates = 1312 $\Rightarrow \$1.312 \text{ cost}$

Brian \rightarrow Gates = 800 $\Rightarrow \$0.8 \text{ cost}$

Ryan \rightarrow Gates = 544 $\Rightarrow \$0.54 \text{ cost}$

Ryan made the best choice

Problem II: (Binary Multiplication)

1. $(-12) * (-9)$ $\bullet (- \times -) = +$

$\bullet 12 = 1100 \leq M$

$\bullet 9 = 1001 = Q$

M	C	A	Q	OP
1100	0	0000	1001	Init
1100	0	1100	1001	1. A = A + M
0	0110	0100	0	Shift R CAQ
0	0011	0010	0	2. Shift R CAQ
0	0001	1000	0	3. Shift R CAQ
0	1101	1001	0	4. A \leq A + M
0110	1100			Shift R CAQ

$-12 \times 9 = 9101100 = 108$

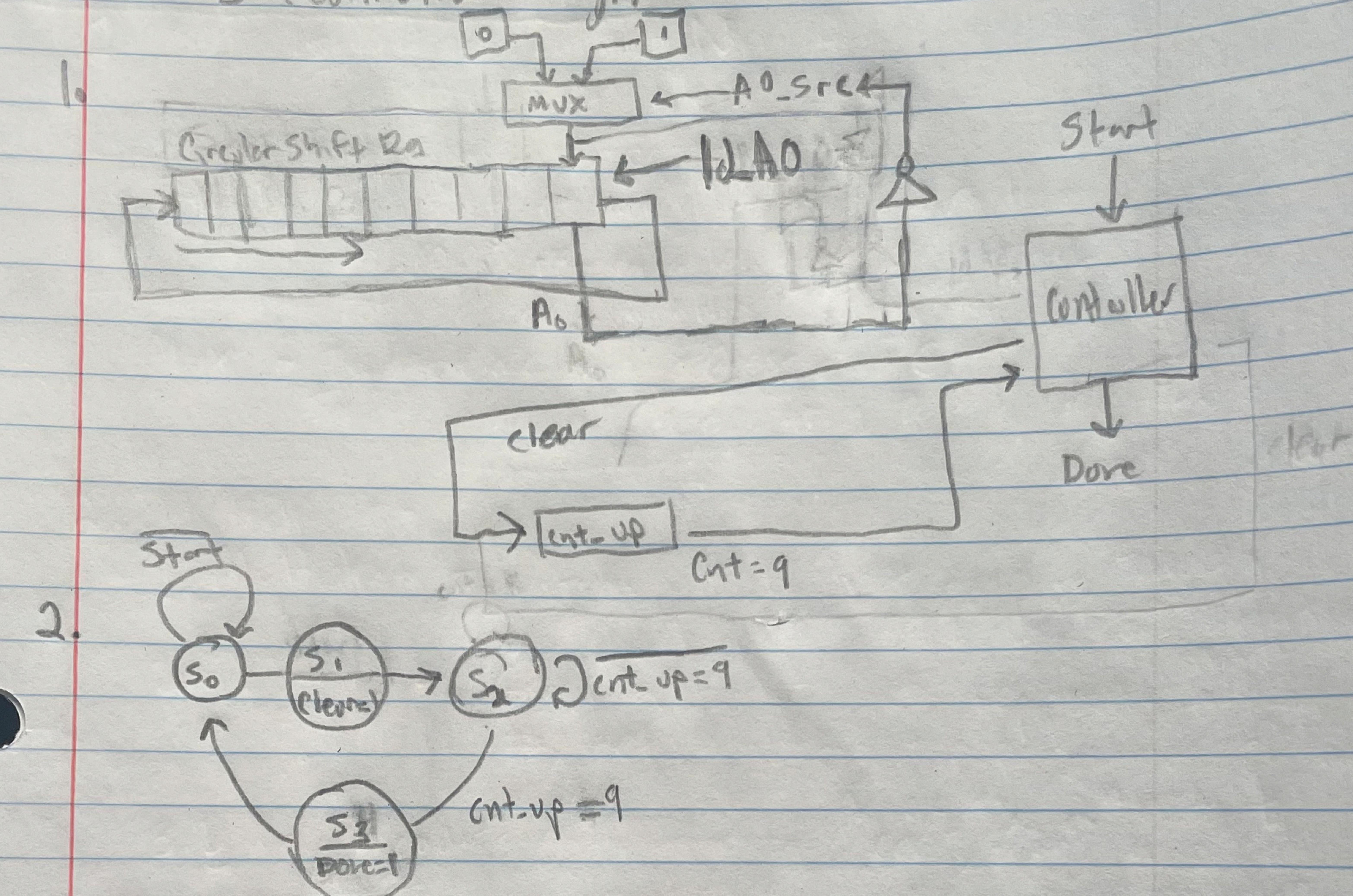
2. a) Shift & Add = $2(40 \text{ ns}) + 4(3 \text{ ns}) = 80 \text{ ns} + 12 \text{ ns} = 96 \text{ ns}$

b) Booth's = $3(40 \text{ ns}) + 5(3 \text{ ns}) = 120 \text{ ns} + 15 \text{ ns} = 135 \text{ ns}$

Final Exam Pg 3

Charles Richardson

Problem 3 (controller Design)



3.

	Outputs	(start, cnt-up=9)
		(0,0) (0,1) (1,0) (1,1)
S ₀		S ₀ S ₀ S ₁ S ₁
S ₁	clear=1	S ₂ S ₂ S ₂ S ₂
S ₂		S ₂ S ₃ S ₂ S ₃
S ₃	Done=1	S ₀ S ₀ S ₀ S ₀

