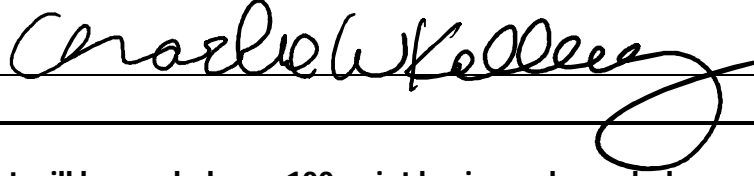


ECE 3544: Digital Design I

Project 1 (Part B): Simulation in the ModelSim Environment; Continuous Assignment Models

Student Name: Charles Kelley

Honor Code Pledge: I have neither given nor received unauthorized assistance on this assignment.



Grading: The design project will be graded on a 100 point basis, as shown below:

Manner of Presentation (30 points)

_____ Completed cover sheet included with report (5 points)

_____ Organization: Clear, concise presentation of content; Use of appropriate, well-organized sections (15 points)

_____ Mechanics: Spelling and grammar (10 points)

Technical Merit (70 points)

_____ General discussion: *Did you describe the objectives in your own words? Did you address the questions posed in the project specification? Did you discuss your conclusions and the lessons you learned from the assignment?* (10 points)

_____ Design discussion: *What was your approach to deriving the circuit you had to design? How does the design process that resulted in your continuous assignment model compare to the one you used to obtain a structural model that used primitive gates? How applicable is the design process you followed in this assignment to larger and more general designs?* (10 points)

_____ Testing discussion: *What was your approach to formulating your test benches, and how did you verify the correctness of your design and implementation?* (10 points)

_____ Supporting figures (20 points total)

- Correct waveforms showing simulation of both decoder modules. (5 points)
- Correct waveforms showing correct operation of your design. (15 points)

_____ Supporting files: *Do the submitted files produce the correct response?* (20 points)

_____ **Project Grade**

Project 1B

Objectives

The purpose of Project 1B is an introduction to the processes relevant for Digital Design, ECE 3544, including an understanding of the basic design and simulation tools of ModelSim. Furthering from Project 1A, Project 1B explores the implications of continuous assignment in Verilog. This project specifies two parts: an exploration of continuous assignment versus their structural counterparts and an introduction to designing and testing a circuit from specifications. Specifically, three modules will be simulated, and one will be designed to meet the project specifications.

Project Specification Questions

Two test benches were used to verify continuous assignment designs of two decoder modules in Verilog. Included below in Figure 1 and 2 are the two waveforms that verify the behavior of the two decoders. The simulation modules showcase the same behavior as their structural designs; The enable signal as well as the decoding of the input signal yield the same results under the simulated values.

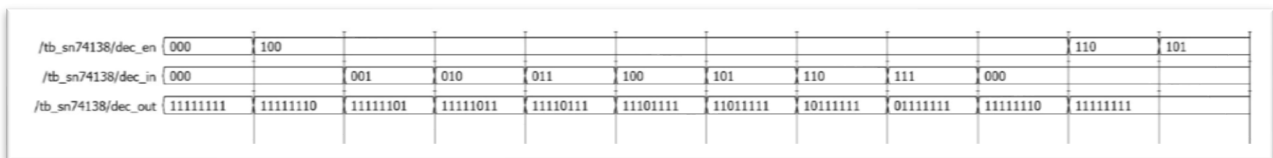


Figure 1. Simulation waveform of sn74138 module

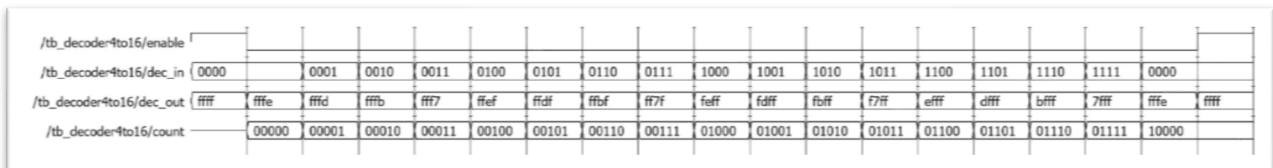


Figure 2. Simulation waveform of 4 to 16 decoder module

Design Process

The Rock, Paper, and Scissors Judge, RPS Judge, was implemented using a continuous assignment structure. This design specification changed both the actual implementation and the approach to solving this problem. Continuous assignment provides a level of abstraction that allowed for a more algorithmic approach to the RPS Judge. Before, the hand input values were chosen in order to reduce terms in a sum of products design, but a pattern in the game allowed for the inputs to be ordered sequentially. The inputs included below in Table 1 represent a ordered list where each input beats the two inputs behind it and loses to the two inputs in front of itself. When you take the difference of the smaller input to the larger input the outcome of the game is partitioned by the result.

Player's Hand	Rock	Spock	Paper	Lizard	Scissors	Unused
Input Value(s)	000	001	010	011	100	101, 110, 111

Table 1. Player hands and input values

The continuous assignment implementation of the RPS Judge took place over four lines. The first line used a conditional statement to find the absolute value of the difference of the inputs. The next three lines were used to determine the values of the RPS Judge output based on the magnitude of the difference. The level of abstraction provided in a continuous assignment module allowed for this simplification of both logic and program size. The simplified process of design would make this project easily scalable to account for larger input domains without exhausting the resources of both program size and our own logical capability. Versus the structural design of Project 1A, Project 1B relies more on the synthesis of the Verilog compiler and could potentially increase the complexity of the hardware implementation.

Simulation Results

Testing the continuous assignment module of the RPS Judge yielded the same results as from Project 1A. The waveform displaying all twenty-five possible games and their results is included below in Figure 3. The testbench used to test the RPS Judge was simplified because the possible hand inputs changed from carefully chosen digits to be sequential. The new test bench looped through the possible values using two nested for loops for player one and player two. The order in which the games were tested changed, but all results held per the specifications of a win or a tie.

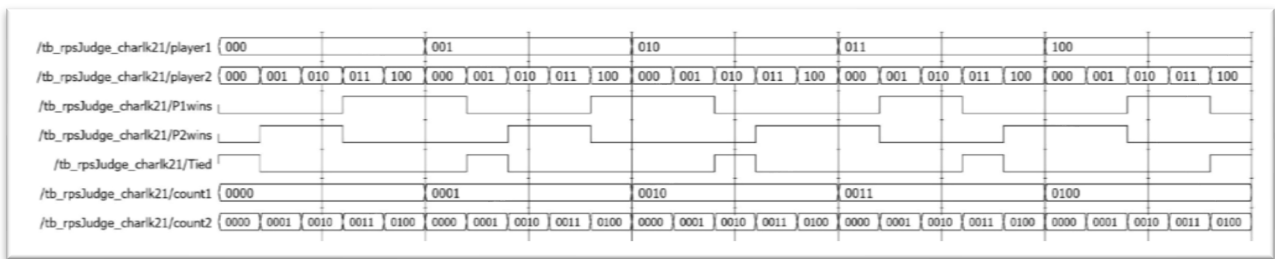


Figure 3. Simulation waveform of the continuous assignment RPS Judge module

Conclusion

The results of this project revealed that structural and continuous assignment models yield the same results when properly implemented. The continuous assignment implementation simplified the logic used in the design process and the Verilog module while compromising on the complexity of the hardware. This process showed the use abstraction provided by continuous assignment that allows far greater possibilities in problems that may be solved. This contrasts the previously used structural model that simplified the hardware the compiler synthesized, but it lost scalability for larger problems.