COMPUTER SYSTEMS AND ORGANIZATION
Part 1

Daniel G. Graham Ph.D

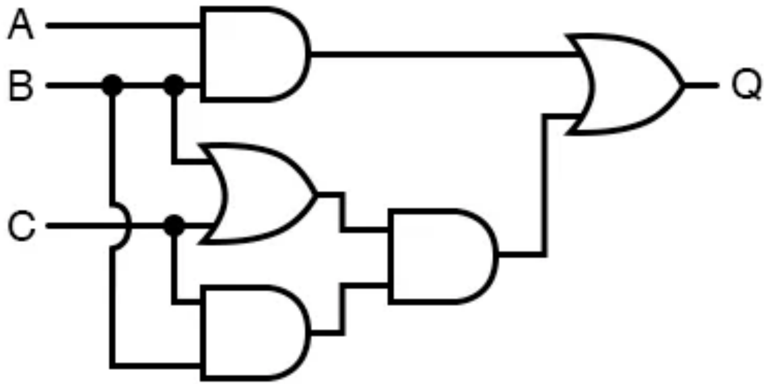
University of Virginia | Engineering

Contents

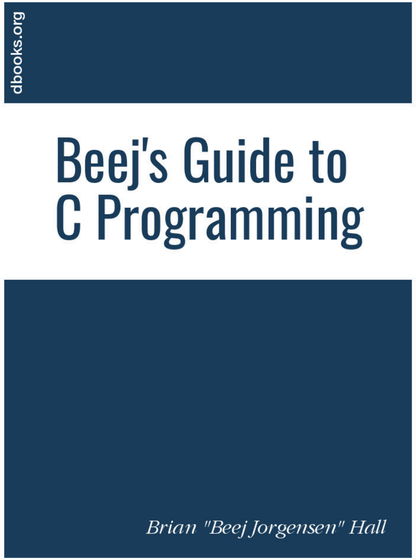
1. Transistor Fundamentals
2. Build Gates from transistors
3. Using a breadboard to build a gate
4. Combine Gates to build logic circuits
5. Express logic circuits as equations

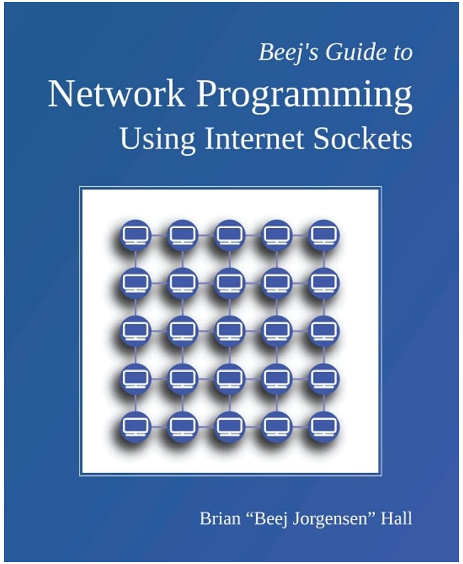
SKILLS

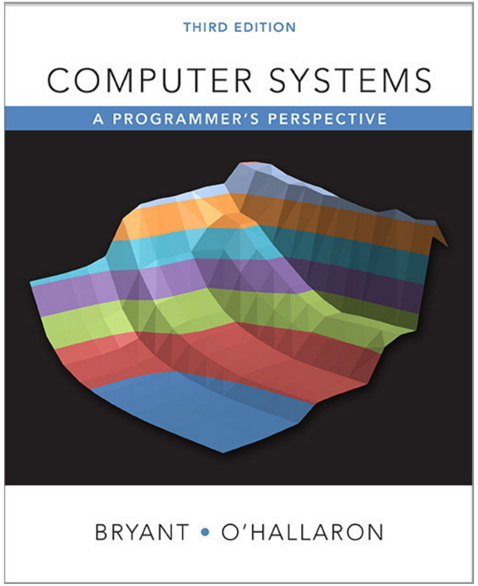
1. By the end lecture, you should be able to look at the circuit on the right and tell what it will output given different inputs
2. You should be able to express the circuit as a Boolean logic equation
3. Understand how to combine gates to implement a Boolean logic equation.
4. Combine transistors to implement a gate or logic circuit.

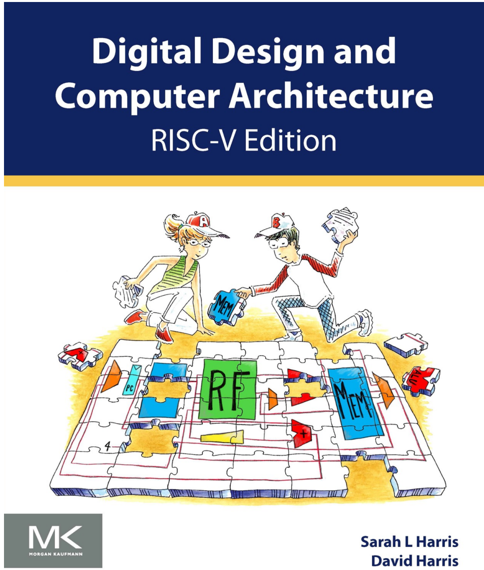


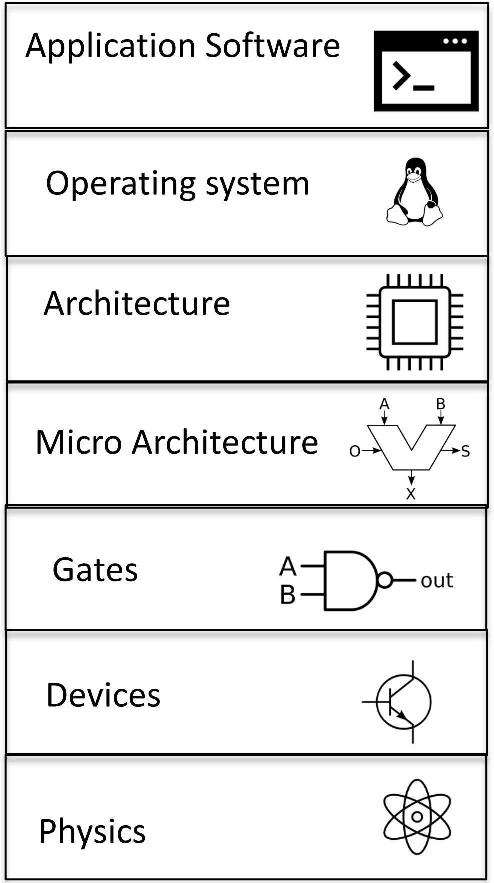
RESOURCES


dbooks.org
Beej's Guide to
C Programming
Brian "Beej Jorgensen" Hall


Beej's Guide to
Network Programming
Using Internet Sockets
Brian “Beej Jorgensen” Hall


THIRD EDITION
COMPUTER SYSTEMS
A PROGRAMMER'S PERSPECTIVE
BRYANT • O'HALLARON


Digital Design and
Computer Architecture
RISC-V Edition
RF
MEM
MK
Sarah L Harris
David Harris



C

Linux

Risc-V

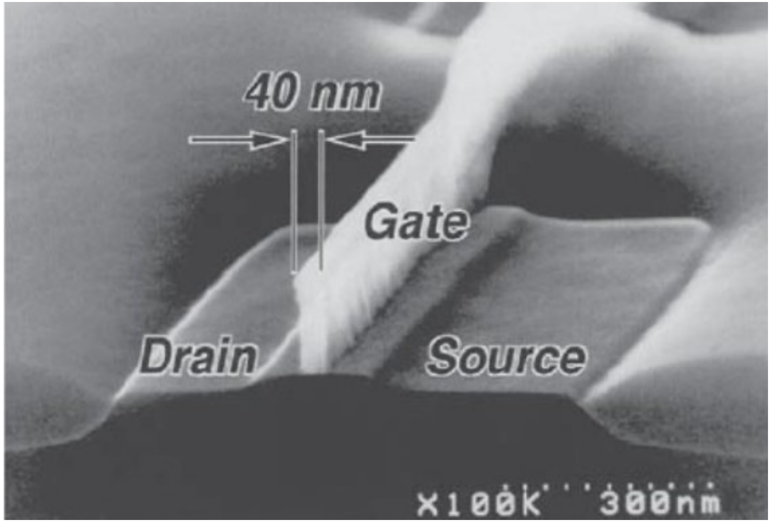
Data path, Stages

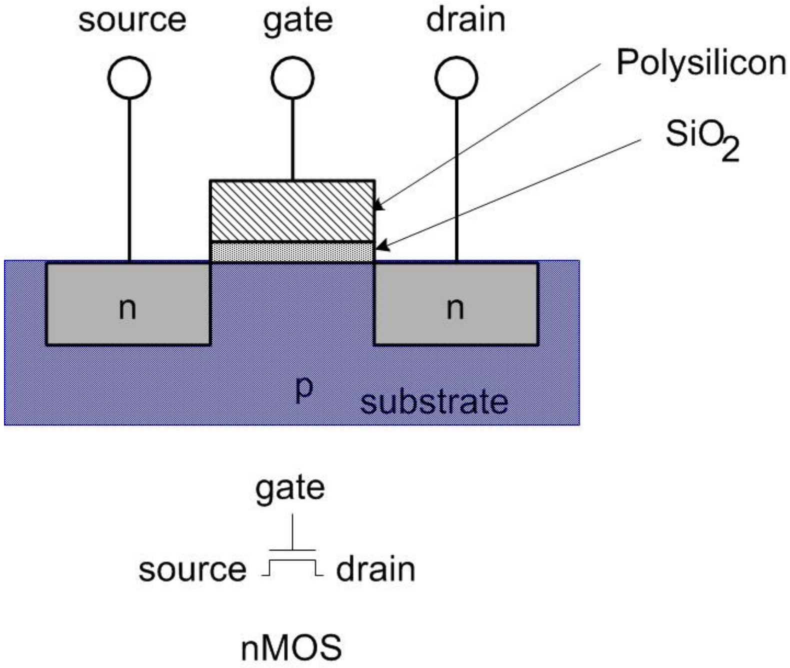
Nand, NOR, NOT ..

PNP NPN Transistors

Electrons

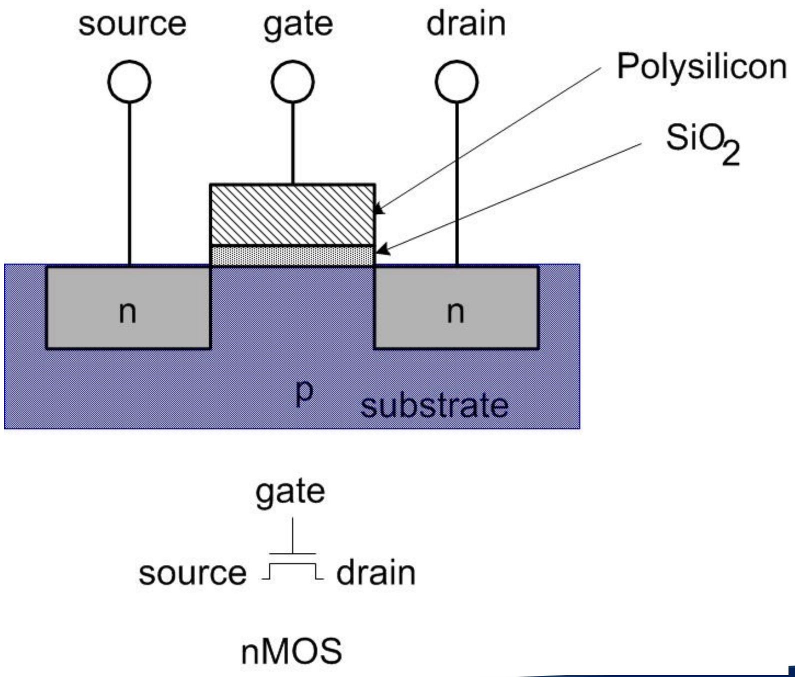
TRANSISTOR


40 nm
Gate
Drain
Source
x100K 300nm


source
gate
drain
Polysilicon
SiO_2
n
n
p
substrate
gate
source
drain
nMOS

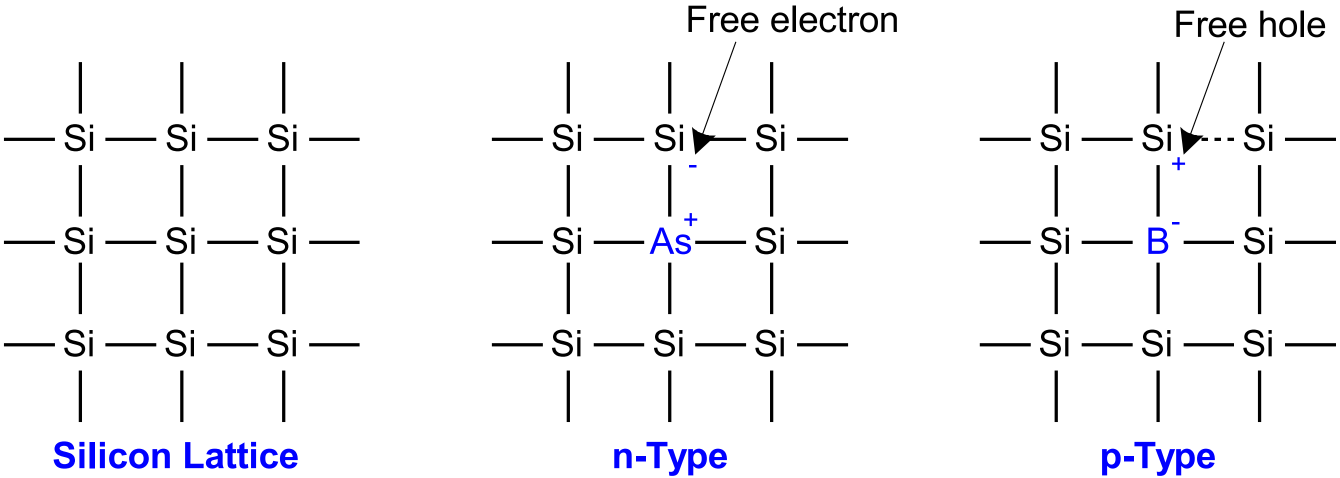
THIS WERE WE'LL START OUR JOURNEY

- **Metal oxide silicon (MOS) transistors:**
  - Polysilicon (used to be **metal**) gate
  - **Oxide** (silicon dioxide) insulator
  - Doped **silicon**



DOPED SILICON

- Pure silicon is a poor conductor (no free charges)
- Doped silicon is a good conductor (free charges)
  - n-type (free ***n***egative charges, electrons)
  - p-type (free ***p***ositive charges, holes)



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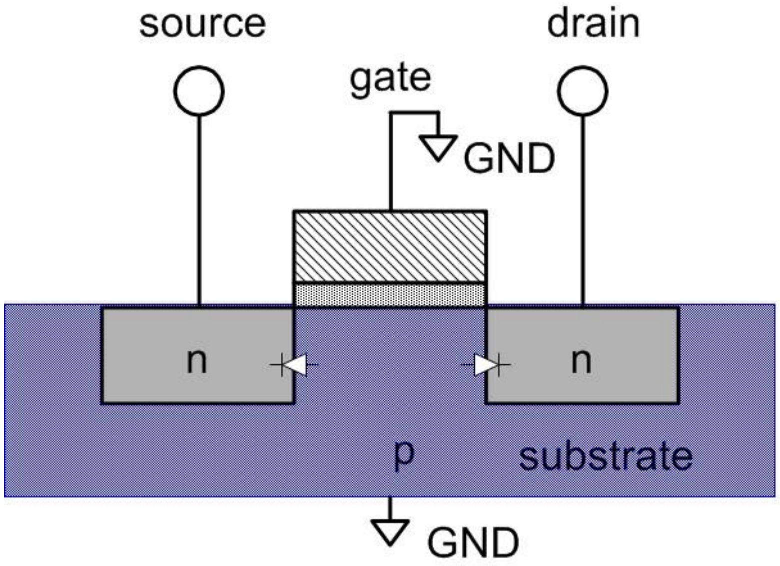
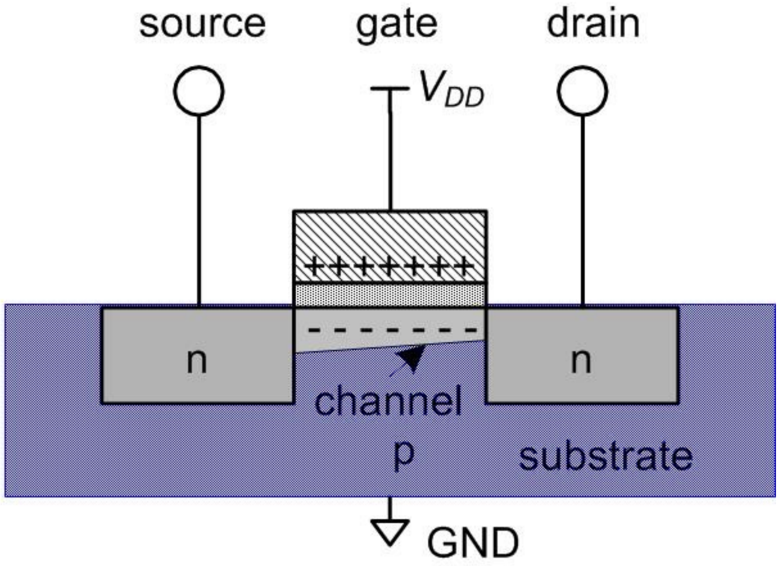
Gate = 0

OFF (no connection between source and drain)



Gate = 1

ON (channel between source and drain)



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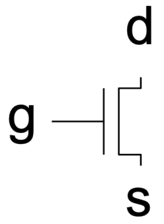
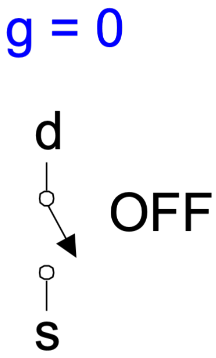
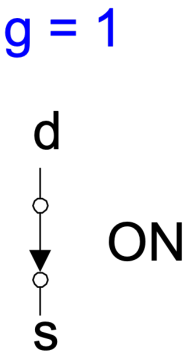
THINKING OF TRANSISTORS AS SWITCHES

nMOS







CAN WE USER TRANSISTORS TO BUILD GATES

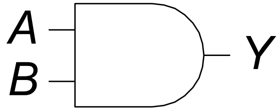
Questions we need to answer

- What are logic gates?
- How do logic gates work?
- Are there different types of gates?

WHAT ARE LOGIC GATES

- Logic gates are circuits that perform logic functions
  - such as AND, OR, (NOT) , etc
- Logic gates have different symbols and their behavior is normally described using a truth table.
-

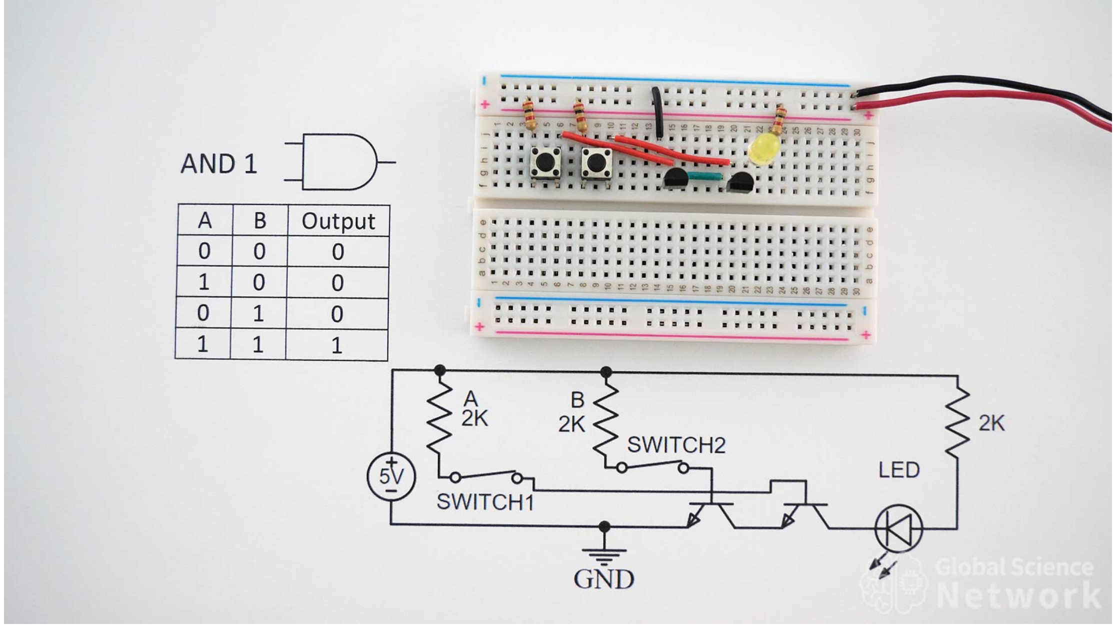
AND



$$Y = AB$$

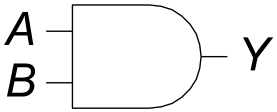
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

BUILD AN AND GATE FROM TRANSISTORS



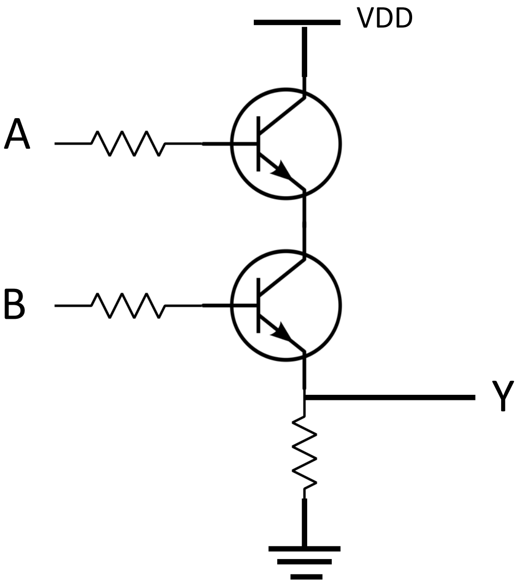
AND GATE CIRCUIT DIAGRAM

AND



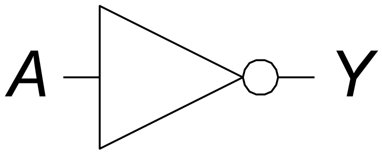
$Y = AB$

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1



SINGLE INPUT VS TWO INPUT GATES

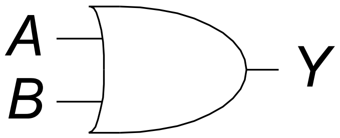
NOT



$$Y = \overline{A}$$

A	Y
0	
1	

OR

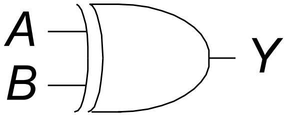


$$Y = A + B$$

A	B	Y
0	0	
0	1	
1	0	
1	1	

MORE LOGIC GATES

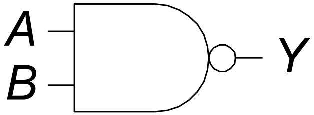
XOR



$$Y = A \oplus B$$

A	B	Y
0	0	
0	1	
1	0	
1	1	

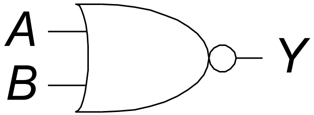
NAND



$$Y = \overline{AB}$$

A	B	Y
0	0	
0	1	
1	0	
1	1	

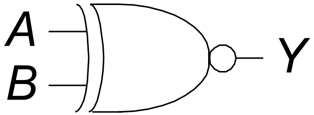
NOR



$$Y = \overline{A + B}$$

A	B	Y
0	0	
0	1	
1	0	
1	1	

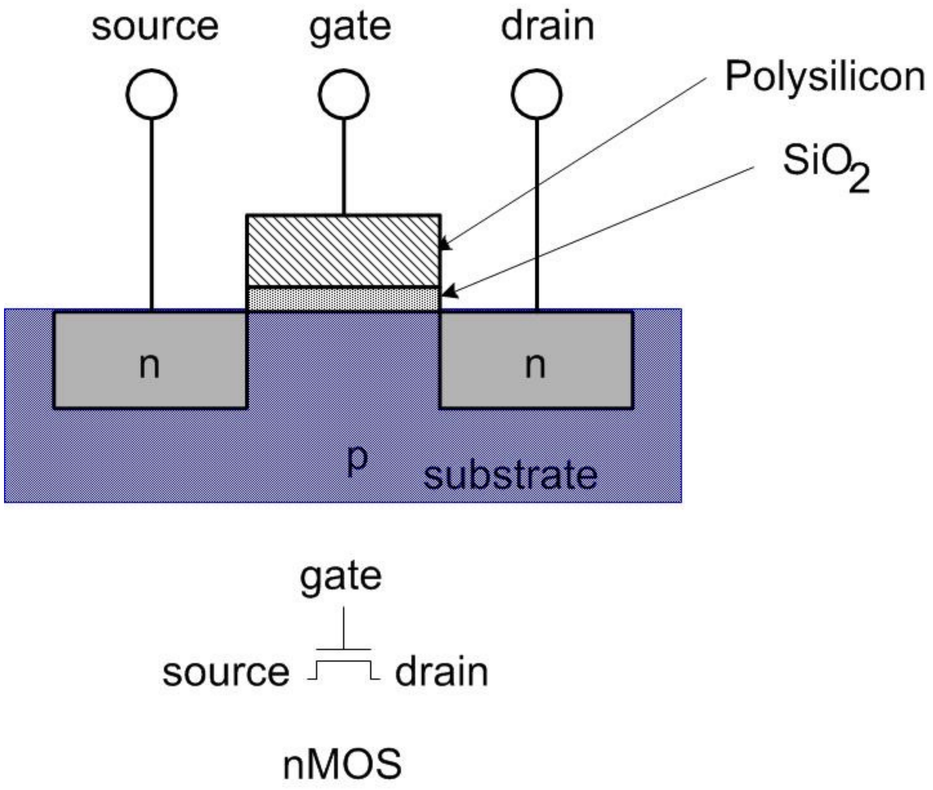
XNOR

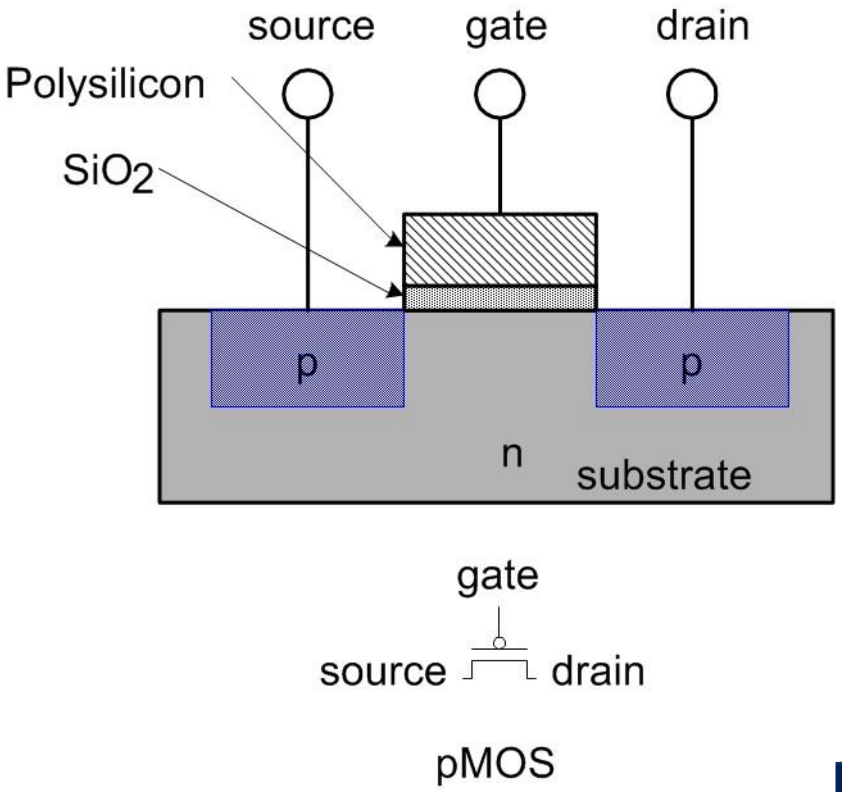


$$Y = \overline{A \oplus B}$$

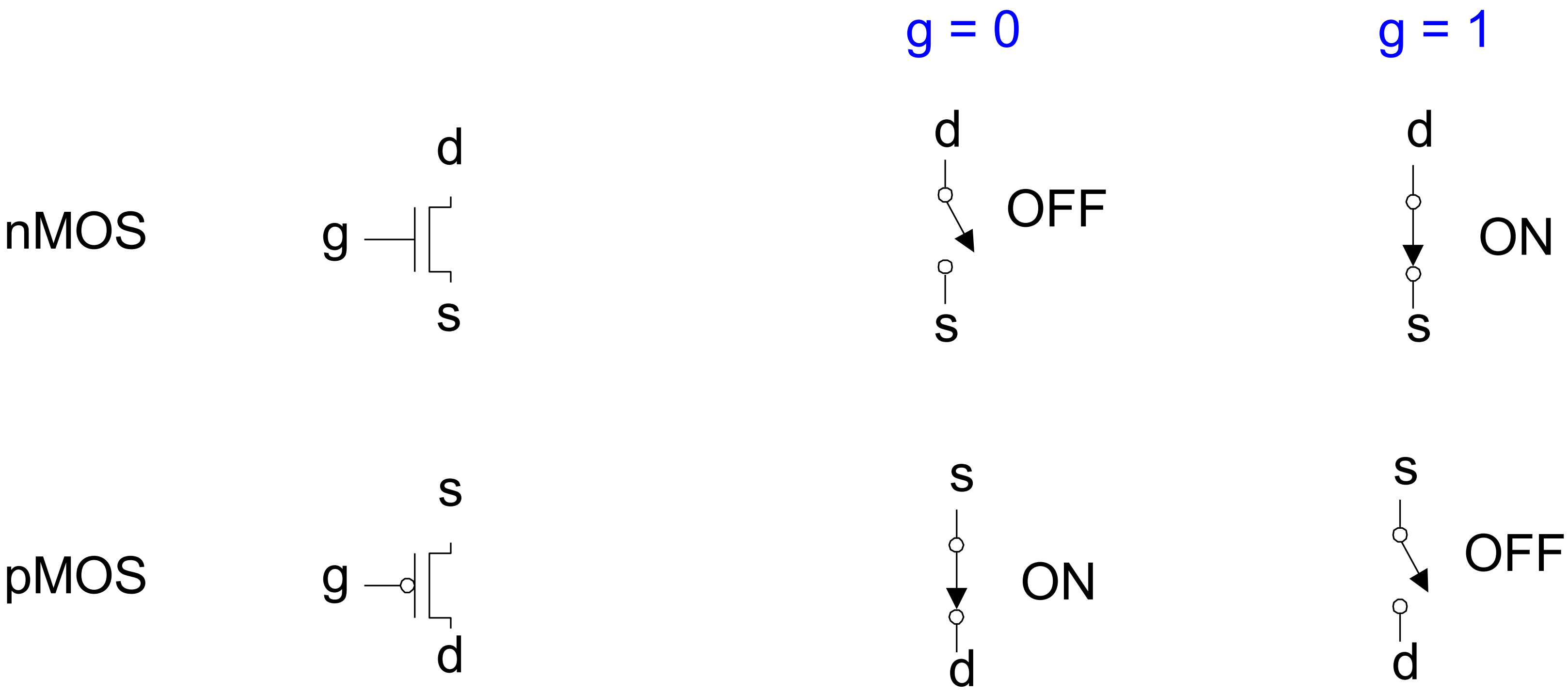
A	B	Y
0	0	
0	1	
1	0	
1	1	

NPN (NMOS) VS PNP (PMOS) TRANSISTORS



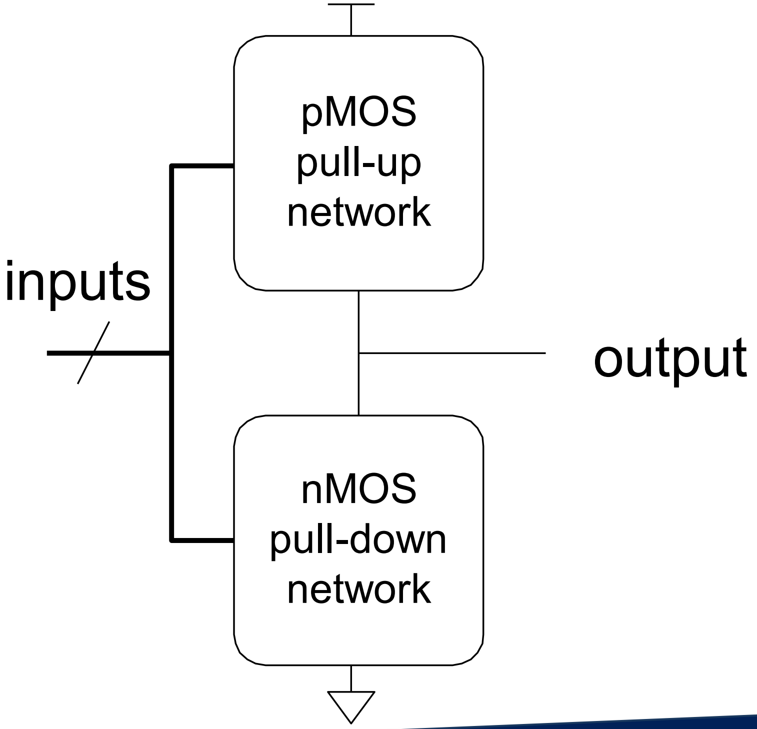


NMOS VS PMOS



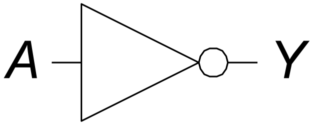
PULL UP PULL DOWN NETWORKS

- **nMOS**: pass good **0**'s, so connect source to GND
- **pMOS**: pass good **1**'s, so connect source to V_{DD}



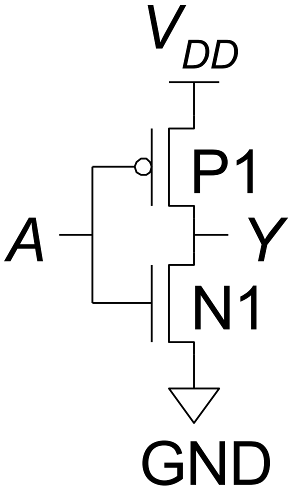
NOT GATE

NOT



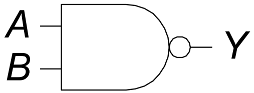
$Y = \overline{A}$

A	Y
0	1
1	0



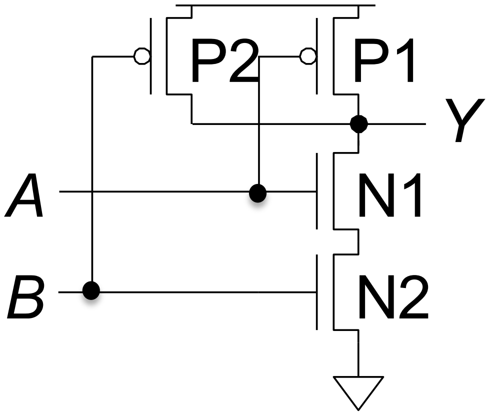
A	P1	N1	*Y*
0			
1			

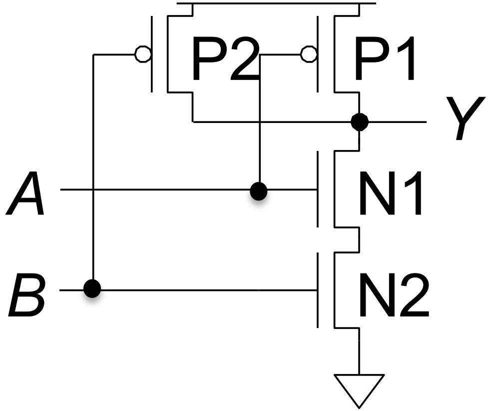
NAND



$$Y = \overline{AB}$$

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

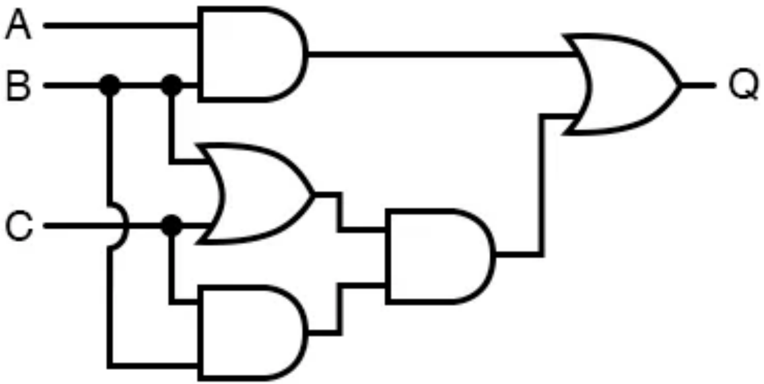




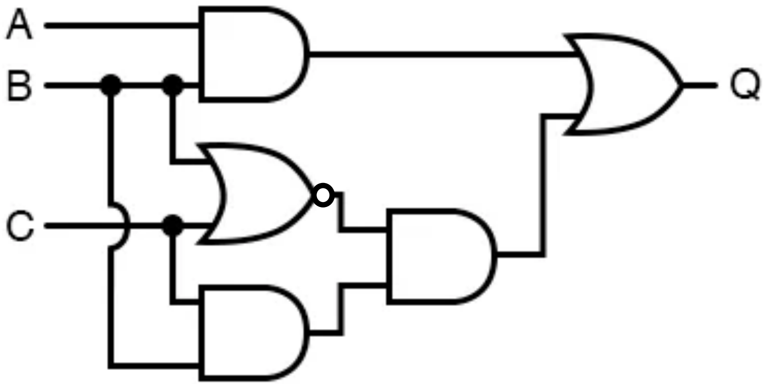
A	*B*	P1	P2	N1	N2	*Y*
0	0					
0	1					
1	0					
1	1					

A	*B*	C	Q
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

WHAT IS THE OUTPUT OF THIS CIRCUIT?



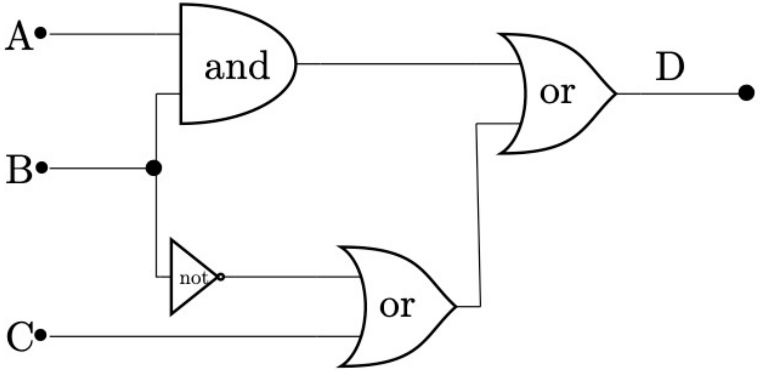
EXPRESS CIRCUIT AS AN EQUATION



Write the equation representing the circuit. Note I replaced the OR with a NOR.

EXAM QUESTION

SPRING 2022
Midterm 1



Fill in the following truth table for this circuit:

A	B	C	D
0	0	0	
0	0	1	
0	1	0	
0	1	1	

CREATIVE QUESTIONS

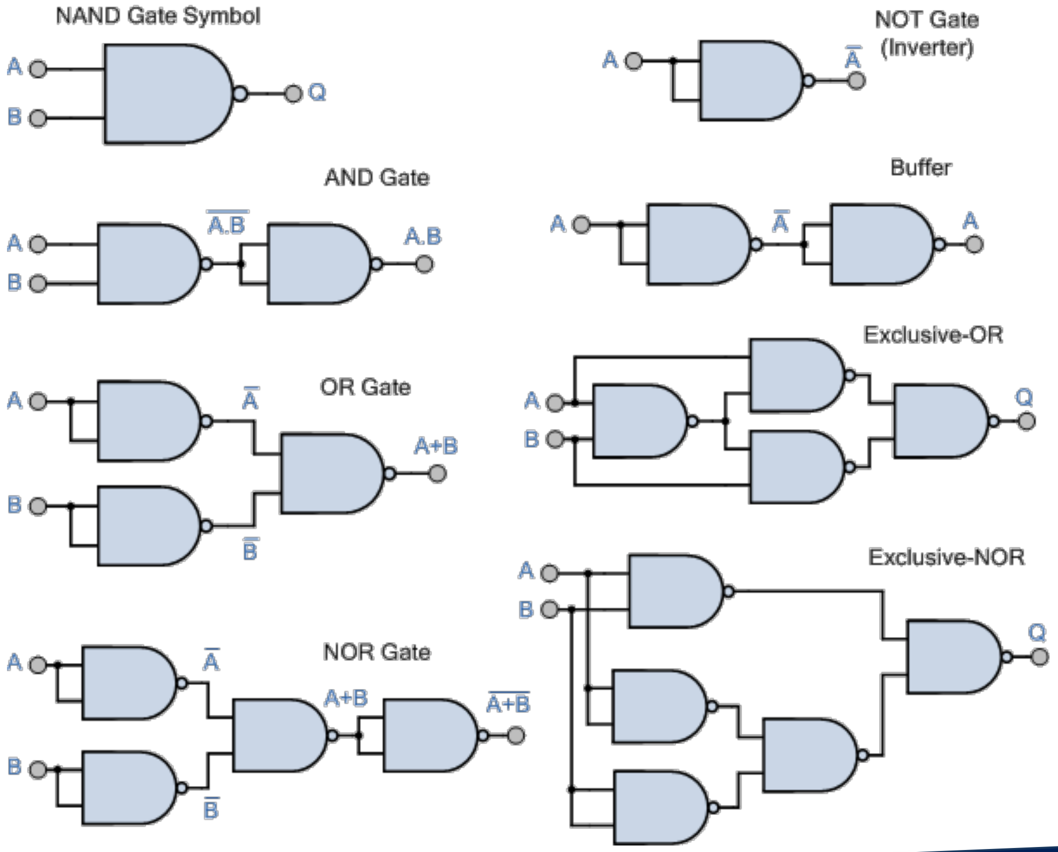
NAND GATES ARE TURNING COMPLETE

It is possible to implement every other gate by using a NAND. You can implement the complete RISC-V architecture using only NAND gates. What a beautiful building block right ☺

Hint: Start by asking NOT what a NAND gate can do for you but what you can do with a NAND gate.

Use a NAND gate to implement the following gates:

1. NOT
2. AND
3. OR
4. NOR
5. XOR


NAND Gate Symbol
A
B
Q
NOT Gate (Inverter)
A
$\overline{A}$
AND Gate
A
B
$\overline{A.B}$
A.B
Buffer
A
$\overline{A}$
A
OR Gate
A
B
$\overline{A}$
$\overline{B}$
A+B
Exclusive-OR
A
B
Q
NOR Gate
A
B
$\overline{A}$
$\overline{B}$
A+B
$\overline{A+B}$
Exclusive-NOR
A
B
Q