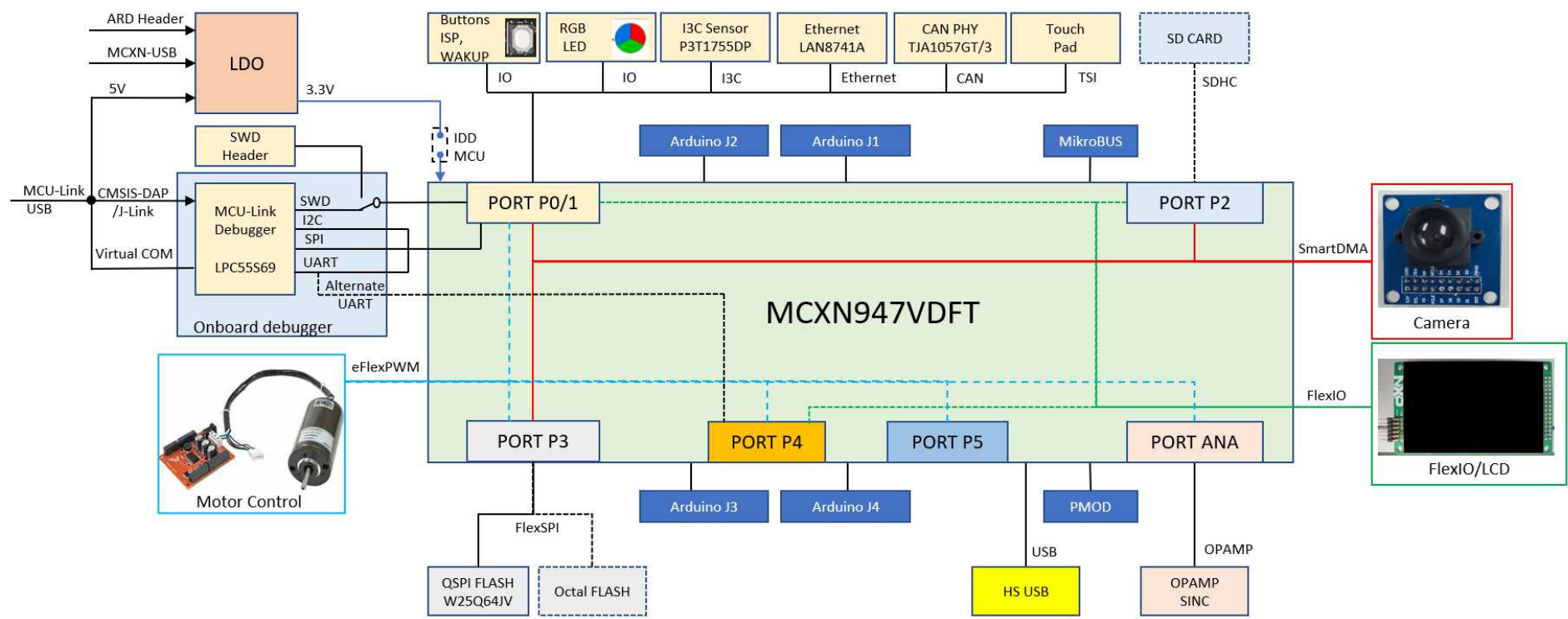


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07	SD & QSPI & SENSOR
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09	MCU_LINK_USB
10	MCU_LINK_DEBUG
11	SWITCH & LED
12	HEADERS
13	APPENDIX JUMPER/DNP

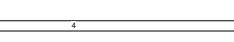
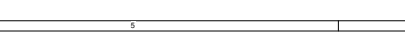
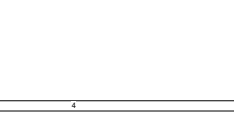
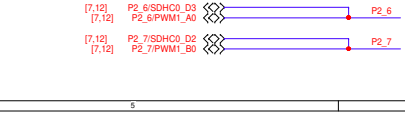
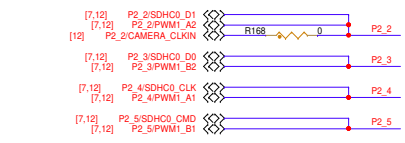
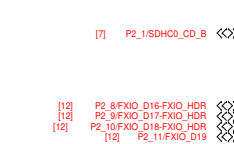
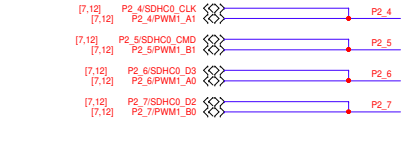
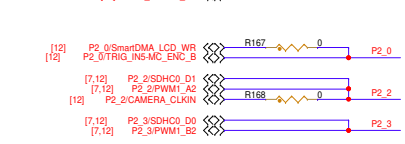
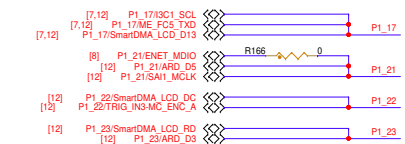
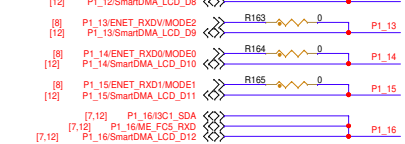
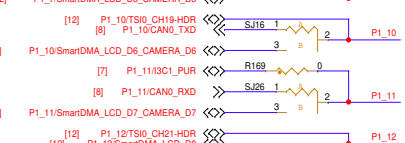
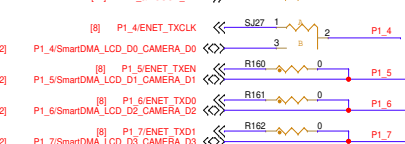
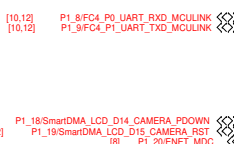
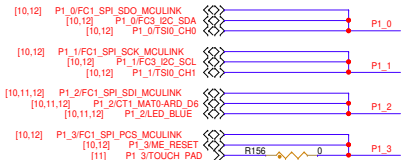
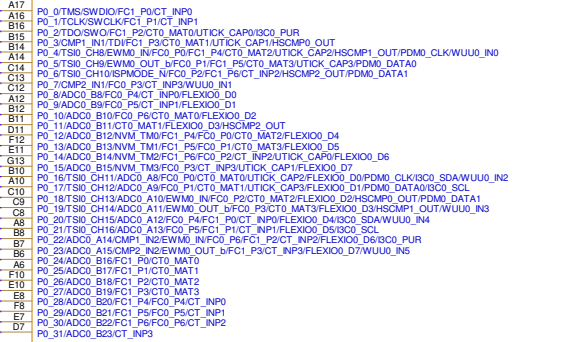
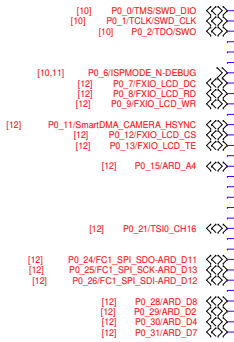
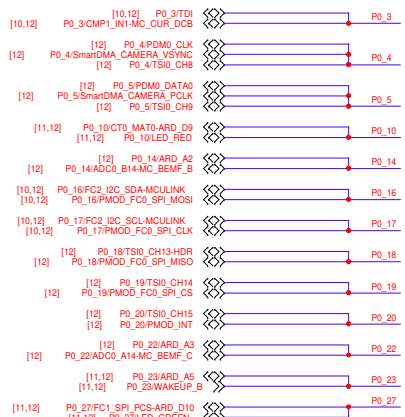
Revision History		
REV	REVISION NOTES	Date
X1	Initial	Jun 10, 2023
A	Final Release	Jul 10, 2023
B	1.Change 3pin solder pads. 2.Update schematic per Ver.A test result.	Sep 15, 2023
B1	1.DNP J12&J7. 2.Change J10 MPN.	Nov 13, 2023
B2	1.Change C21 from 1uf to 4.7uf. 2.Change C24 from 0.1uf to 2.2uf. 3.Change R82&R192&R193 MPN due to material shortage.	Jan 25, 2024
C	1.Add TP32~TP34, TP36~TP38, TP43~TP47 for automatic testing. 2.Add C107 (DNP). 3.Change R192&R193 from 1M to 0ohm. DNP C102&C103. 4.Change R27 from 10K to 0ohm. DNP R29. 5.Update some net names. 6.Update MCU symbol per the latest pinout file.	Mar 28, 2024

FRDM-MCXN947

# BLOCK DIAGRAM



# SOC PORT0~2



# SOC PORT3~5

UID

B17 P3\_0TRIG\_IN0FC7\_P3CT\_INP16/PWM0\_A0/FLEXIO0\_D8/SmartDMA\_PIO0/FLEXSP0\_A\_SS0\_bPF\_QSPI\_CS0\_DS/WU00\_IN22  
C15 P3\_1TRIG\_IN1FC6\_P3CT\_P3CT\_INP17/PWM0\_B0/FLEXIO0\_D9/SmartDMA\_PIO1/FLEXSP0\_A\_SS1\_bPF\_QSPI\_CS1\_DS  
D15 P3\_2FC7\_P3CT\_P3CT\_INP18/PWM0\_X0/FLEXIO0\_D10/SmartDMA\_PIO2/SIM1\_PD  
D16 P3\_3FC7\_P1CT4\_MAT1/PWM0\_X1/FLEXIO0\_D11/SmartDMA\_PIO3/SIM1\_RST  
F14 P3\_4FC7\_P3CT\_INP18/PWM0\_X2/FLEXIO0\_D12/SmartDMA\_PIO4/SIM1\_CLK  
G14 P3\_5FC7\_P3CT\_INP19/PWM0\_X3/FLEXIO0\_D13/SmartDMA\_PIO5/SIM1\_IO  
D17 P3\_6CLKOUT\_F08\_P1CT4\_MAT2/PWM0\_A1/FLEXIO0\_D14/SmartDMA\_PIO6/FLEXSP0\_A\_DS/SIM1\_VCCENSAI\_MCLK/PF\_QSPI\_CS\_n  
D14 P3\_7FC6\_P3CT\_P1CT4\_MAT0/PWM0\_B1/FLEXIO0\_D15/SmartDMA\_PIO7/FLEXSP0\_A\_SCLK/SIM0\_VCCENSAI\_MCLK/PF\_QSPI\_SCKIN  
F15 P3\_8FC6\_P4FC7\_P3CT\_INP4/PWM0\_A2/FLEXIO0\_D16/SmartDMA\_PIO8/FLEXSP0\_A\_DATA0/SIM0\_P0/SAI0\_TX\_BCLK/PF\_QSPI\_DATA0/WU00\_IN23  
F17 P3\_9FC6\_P3CT\_P3CT\_INP5/PWM0\_B2/FLEXIO0\_D17/SmartDMA\_PIO9/FLEXSP0\_A\_DATA1/SIM0\_RST/SAI0\_TX\_FSPF\_QSPI\_DATA1  
F16 P3\_10FC6\_P2FC7\_P4CT1\_MAT0/PWM0\_A3/FLEXIO0\_D18/SmartDMA\_PIO10/FLEXSP0\_A\_DATA2/SIM0\_CLK/SAI0\_TXD0/PF\_QSPI\_DATA2  
G16 P3\_11FC6\_P3FC7\_P5CT1\_MAT1/PWM0\_B3/FLEXIO0\_D19/SmartDMA\_PIO11/FLEXSP0\_A\_DATA3/SIM0\_IO/SAI0\_RXD0/PF\_QSPI\_DATA3/WU00\_IN24  
H17 P3\_12FC7\_P4FC6\_P4CT1\_MAT2/PWM1\_A0/FLEXIO0\_D20/SmartDMA\_PIO12/FLEXSP0\_A\_DATA4/SAI0\_RXD1  
H16 P3\_13FC7\_P5FC6\_P5CT1\_MAT3/PWM1\_B0/FLEXIO0\_D21/SmartDMA\_PIO13/FLEXSP0\_A\_DATA5/SAI0\_TXD1/PF\_SPI\_CS0\_n  
H15 P3\_14FC6\_P3CT\_INP6/PWM1\_A1/FLEXIO0\_D22/SmartDMA\_PIO14/FLEXSP0\_A\_DATA6/SAI0\_RX\_BCLK/PF\_SPI\_DATA/WU00\_IN25  
J15 P3\_15FC6\_P1CT\_INP7/PWM1\_B1/FLEXIO0\_D23/SmartDMA\_PIO15/FLEXSP0\_A\_DATA7/SAI0\_RX\_FSPF\_SPI\_SCKIN  
K15 P3\_16FC6\_P2CT\_INP8/PWM1\_A2/FLEXIO0\_D24/SmartDMA\_PIO16/SIM0\_CLK/SAI1\_TX\_BCLK  
K16 P3\_17FC6\_P3CT\_INP9/PWM1\_B2/FLEXIO0\_D25/SmartDMA\_PIO17/SIM0\_IO/SAI1\_TX\_FSWU00\_IN26  
K17 P3\_18FC6\_P5CT2\_MAT0/PWM1\_X0/FLEXIO0\_D26/SmartDMA\_PIO18/SAI1\_RX\_BCLK  
M17 P3\_19FC7\_P6CT2\_MAT1/PWM1\_X1/FLEXIO0\_D27/SmartDMA\_PIO19/SAI1\_RX\_FS  
M16 P3\_20TRIG\_OUT0FC8\_P4FC6\_P3CT2\_MAT2/PWM1\_A3/FLEXIO0\_D28/SmartDMA\_PIO20/SIM0\_P0/SAI1\_TXD0/PF\_SPI\_CS0\_DS\_n/WU00\_IN27  
M15 P3\_21TRIG\_OUT1FC8\_P4FC6\_P1CT2\_MAT3/PWM1\_B3/FLEXIO0\_D29/SmartDMA\_PIO21/SIM0\_RST/SAI1\_RXD0/PF\_SPI\_CS1\_DS\_n  
P3\_22FC6\_P6FC6\_P2CT\_INP10/PWM1\_X2/FLEXIO0\_D30/SmartDMA\_PIO22/SIM0\_VCCENSAI\_RXD1  
P3\_23FC6\_P3CT\_INP11/PWM1\_X3/FLEXIO0\_D31/SmartDMA\_PIO23/SAI1\_TXD1

MCXN947VDF

UIE

P1 P4\_0TRIG\_IN6FC2\_P0CT\_INP16/SmartDMA\_PIO24/PLU\_IN0/SINC0\_MCLK3/WU00\_IN18  
P2 P4\_1TRIG\_IN7FC2\_P1CT\_INP17/SmartDMA\_PIO25/PLU\_IN1  
T1 P4\_2ADAC0\_OUT/ADC0\_A4/ADC1\_A4/CMP0\_IN4N/CMP1\_IN4N/CMP2\_IN4N/TRIG\_IN6FC2\_P2CT\_INP12/SmartDMA\_PIO26/PLU\_IN2/SINC0\_MBIT3  
U1 P4\_3ADAC1\_OUT/ADC0\_B4/ADC1\_B4/CMP0\_IN5N/CMP1\_IN5N/CMP2\_IN5N/TRIG\_IN7FC2\_P3CT\_INP13/SmartDMA\_PIO27/PLU\_IN3/WU00\_IN19  
M6 P4\_4FC2\_P4CT\_INP14/SmartDMA\_PIO28/PLU\_IN4/SINC0\_MCLK4  
N7 P4\_5FC2\_P5CT\_INP15/SmartDMA\_PIO29/PLU\_IN5/SINC0\_MBIT4  
Y4 P4\_6TRIG\_OUT4FC2\_P3CT\_INP18/SmartDMA\_PIO30/PLU\_CLK  
Y6 P4\_7CT\_INP19/SmartDMA\_PIO31  
Y7 P4\_12OPAMP0\_INP0/ADC0\_A5/ADC1\_A5/USB0\_VBUS\_DET/FC2\_P0CT4\_MAT0/FLEXIO0\_D20/PLU\_OUT0/SINC0\_MCLK0/CAN0\_RXD0/WU00\_IN20  
P8 P4\_13OPAMP0\_INP1/ADC0\_B5/ADC1\_B5/TRIG\_IN6FC2\_P1/USB1\_OTG\_IDCT4\_MAT1/FLEXIO0\_D21/PLU\_OUT1/SINC0\_MBIT0/CAN0\_TXD  
P16 P4\_14CT4\_MAT2/FLEXIO0\_D22/PLU\_OUT2  
P18 P4\_15OPAMP0\_OUT/ADC0\_A1/CMP0\_IN4P/TRIG\_OUT4USB1\_VBUSVALID\_EXT/CT4\_MAT3/FLEXIO0\_D23/PLU\_OUT3/SINC0\_MCLK\_OUT0/CAN1\_RXD0/WU00\_IN21  
P9 P4\_16OPAMP1\_INP0/ADC0\_A6/FC2\_P5/USB1\_OTG\_PWR/CT3\_MAT0/FLEXIO0\_D4/PLU\_OUT4/SINC0\_MCLK1/CAN1\_TXD  
N10 P4\_17OPAMP1\_INP1/ADC0\_B6/TRIG\_IN6FC2\_P3/USB1\_OTG\_OC/CT3\_MAT1/FLEXIO0\_D25/PLU\_OUT5/SINC0\_MBIT1  
R10 P4\_18CT3\_MAT2/FLEXIO0\_D26/PLU\_OUT6  
T10 P4\_19OPAMP1\_OUT/ADC0\_B1/CMP1\_IN4P/TRIG\_OUT5CT3\_MAT3/FLEXIO0\_D27/PLU\_OUT7/SINC0\_MCLK\_OUT1  
T11 P4\_20OPAMP2\_INP0/ADC1\_A6/TRIG\_IN6FC2\_P4/CT2\_MAT0/FLEXIO0\_D28/SINC0\_MCLK2  
T12 P4\_21OPAMP2\_INP1/ADC1\_B6/TRIG\_IN6FC2\_P5/CT2\_MAT1/FLEXIO0\_D29/SINC0\_MBIT2  
U12 P4\_22CT2\_MAT2/FLEXIO0\_D30  
P4\_23OPAMP2\_OUT/ADC0\_A2/ADC0\_B2/ADC1\_B3/CMP2\_IN4P/TRIG\_OUT5FC2\_P6/CT2\_MAT3/FLEXIO0\_D31/SINC0\_MCLK\_OUT2

MCXN947VDF

UIF

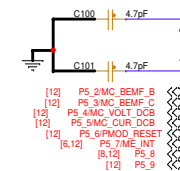
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N11 P5\_2ADC1\_B10/VBAT\_WAKEUP\_bSPC\_LPREQ/TAMPER0  
M12 P5\_3ADC1\_B11/TRIG\_OUT11/RTC\_CLKOUT/TAMPER1  
K12 P5\_4ADC1\_B12/TRIG\_OUT7/SPC\_LPREQ/TAMPER2  
K13 P5\_5ADC1\_B13/TRIG\_OUT0/LPTMR0\_ALT2/TAMPER3  
L13 P5\_6ADC1\_B14/TRIG\_OUT6/LPTMR1\_ALT2/TAMPER4  
L14 P5\_7ADC1\_B15/TRIG\_OUT11/TAMPER5  
M14 P5\_8ADC1\_B16/TRIG\_OUT7/TAMPER6  
P5\_9ADC1\_B17/TAMPER7

MCXN947VDF

[7] P3\_0/FLEXSP0\_A\_SS0\_b  
[7] P3\_1/FLEXSP0\_A\_SS1\_b  
[12] P3\_2/FC7\_IC2\_SCL  
[12] P3\_3/FC7\_IC2\_SCL  
[12] P3\_4/SmartDMA\_LCD\_D4\_CAMERA\_D4  
[12] P3\_5/SmartDMA\_LCD\_D5\_CAMERA\_D5  
[7] P3\_6/FLEXSP0\_A\_DS  
[7] P3\_7/FLEXSP0\_A\_SCLK  
[7] P3\_8/FLEXSP0\_A\_DATA0  
[7] P3\_9/FLEXSP0\_A\_DATA1  
[7] P3\_10/FLEXSP0\_A\_DATA2  
[7] P3\_11/FLEXSP0\_A\_DATA3  
[7] P3\_12/FLEXSP0\_A\_DATA4  
[7] P3\_13/FLEXSP0\_A\_DATA5  
[7] P3\_14/FLEXSP0\_A\_DATA6  
[7] P3\_15/FLEXSP0\_A\_DATA7  
[12] P3\_16/SAI1\_TX\_BCLK  
[12] P3\_17/SAI1\_TX\_FS  
[12] P3\_18/SAI1\_RX\_BCLK  
[12] P3\_19/ME\_PWM  
[12] P3\_19/SAI1\_RX\_FS  
[12] P3\_20/ME\_FC6\_SPI\_MOSI  
[12] P3\_20/SAI1\_TXD0  
[12] P3\_21/ME\_FC6\_SPI\_CLK  
[12] P3\_21/SAI1\_RXD0  
[12] P3\_22/ME\_FC6\_SPI\_MISO  
[12] P3\_23/ME\_FC6\_SPI\_CS

[6,12] P4\_0/FC2\_IC2\_SDA-FXIO\_HDR  
[6,12] P4\_0/FC2\_IC2\_SDA-ARD\_D18  
[6,12] P4\_1/FC2\_IC2\_SCL-FXIO\_HDR  
[6,12] P4\_1/FC2\_IC2\_SCL-ARD\_D18  
[10,12] P4\_2/FC2\_UART\_TXD-ARD\_D1  
[10,12] P4\_3/FC2\_P2\_UART\_TXD\_MCU\_LINW  
[10,12] P4\_3/FC2\_UART\_RXD-ARD\_D0  
[10,12] P4\_3/FC2\_P3\_UART\_TXD\_MCU\_LINW  
[12] P4\_4/SINC0\_MBIT4-HDR  
[12] P4\_4/SFIO0\_LCD\_GPIO  
[12] P4\_12/RSHUNT\_CURA\_P  
[12] P4\_12/FXIO\_D20  
[12] P4\_13/MC\_ENC\_I  
[12] P4\_13/FXIO\_D21  
[6,12] P4\_16/USB1\_OTG\_PWR  
[6,12] P4\_16/RSHUNT\_CURB\_P  
[6,12] P4\_16/FXIO\_D24  
[6,12] P4\_17/FXIO\_D25  
[6,12] P4\_17/USB1\_OTG\_OC  
[12] P4\_20/RSHUNT\_CURC\_P  
[12] P4\_20/FXIO\_D28

[12] P5\_2/MC\_BEMF\_B  
[12] P5\_3/MC\_BEMF\_C  
[12] P5\_4/MC\_VOLT\_DCB  
[12] P5\_5/MC\_CLR\_DCB  
[12] P5\_6/MCQ\_RESET  
[6,12] P5\_7/ME\_INT  
[6,12] P5\_9  
[12] P5\_9



Classification: Company Internal/Proprietary

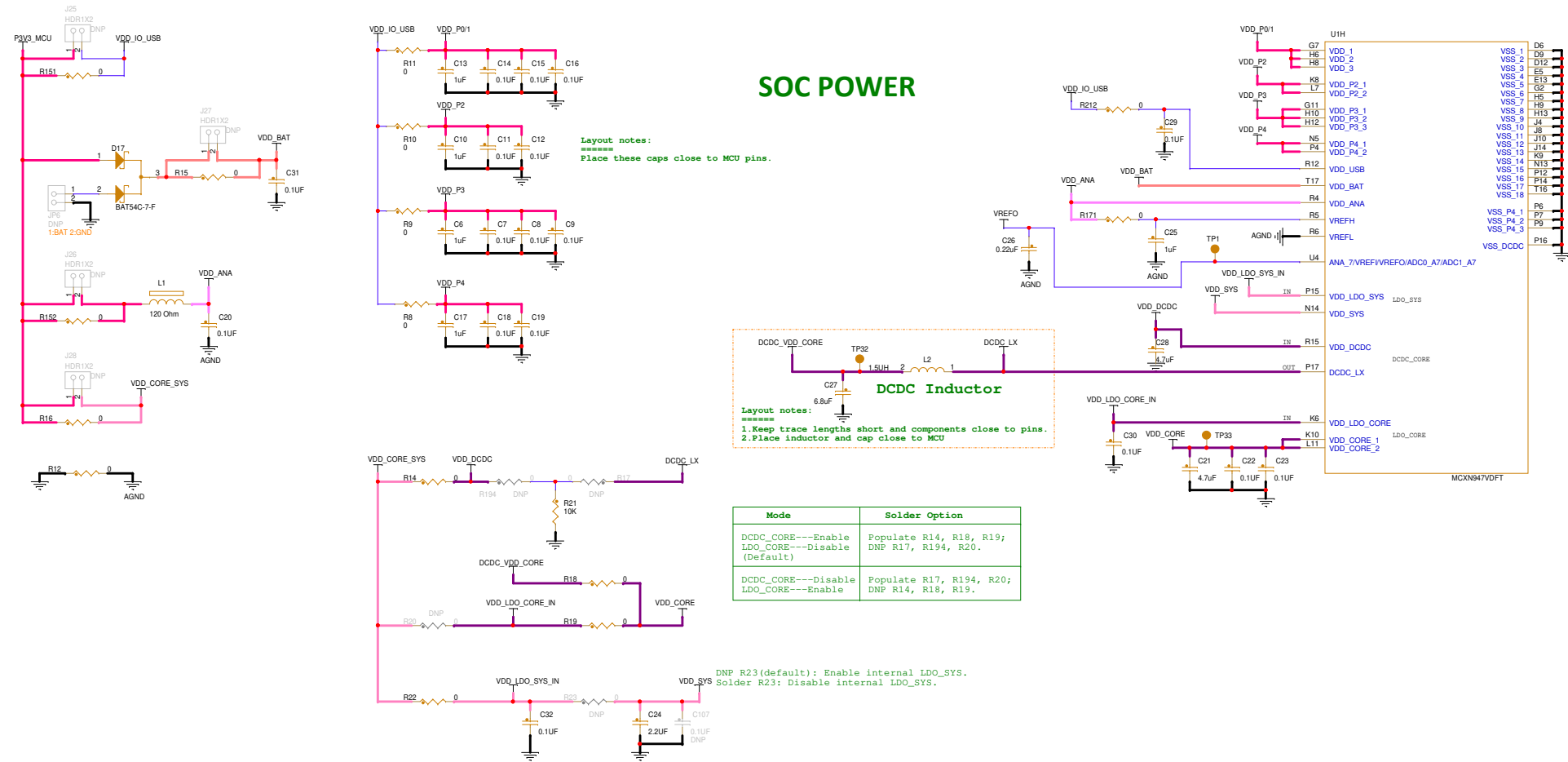
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Page Title: SOC\_PORT3-5

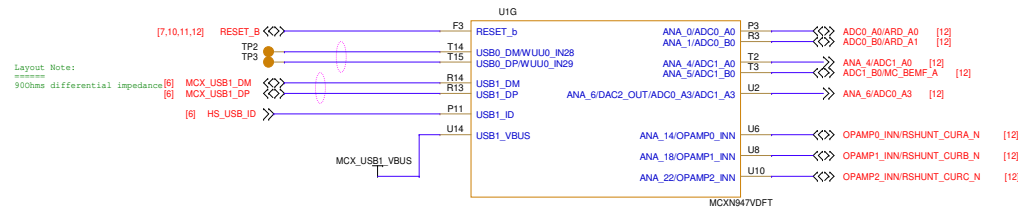
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## SOC POWER



## SOC USB & Analog Signals



<Core Design>



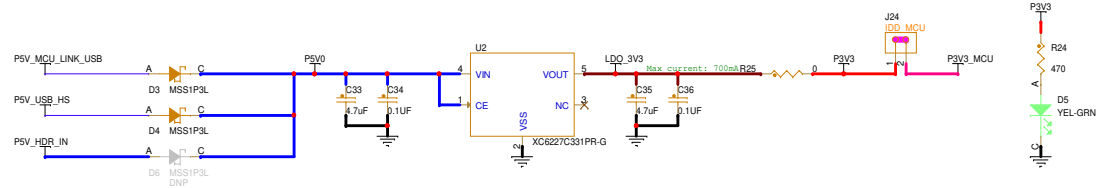
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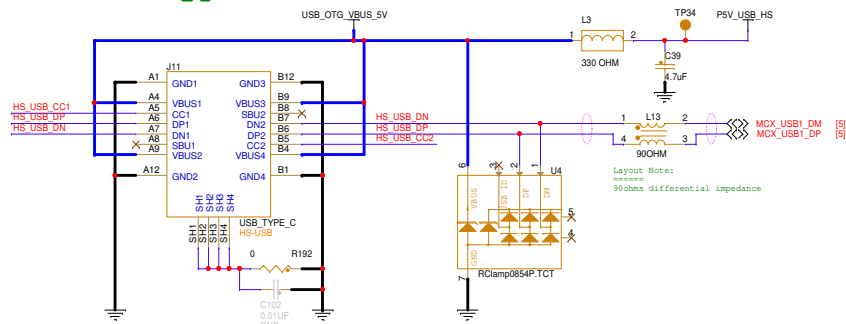
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Size C	Document Number SCH-90818 PDF: SPF-90818	Rev C
Date: Thursday, March 28, 2024	Sheet 5	of 13

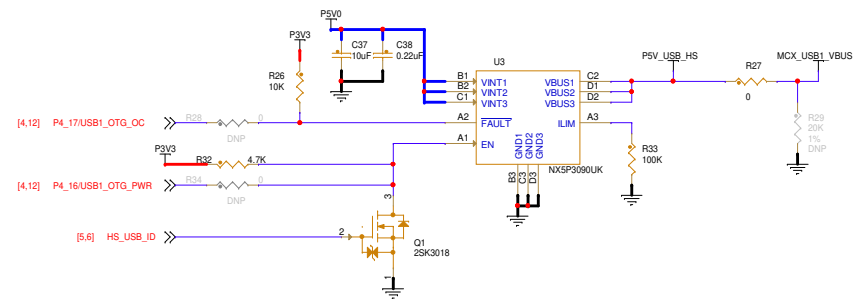
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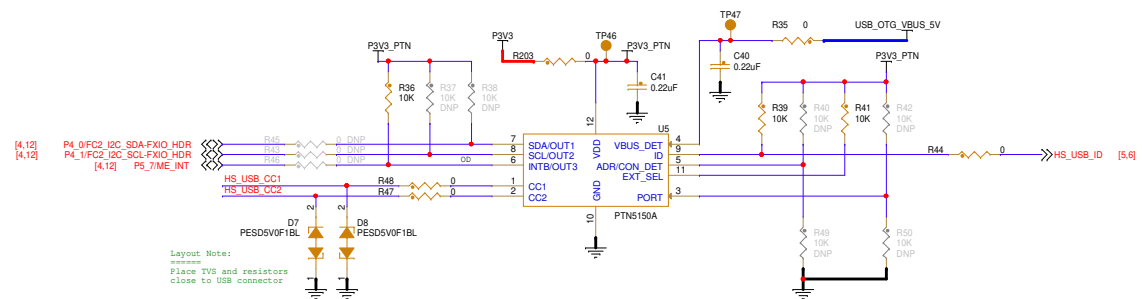
USB1\_HIGH SPEED  
USB2.0 Type C



## VBUS Power Control



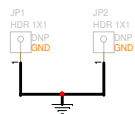
## CC Logic



## MOUNTING HOLE



## Test Points



ADR/CON\_DET:  
When Power-up, ADR(input) function:  
ADR=1: I2C Address: 0x7A(ADR)  
ADR=0: I2C Address: 0x3A(ADR)  
ADR=MID/FLOATING  
After TINPUTLATCH, CON\_DET(output) function:  
CON\_DET=1: Connection Detected  
CON\_DET=0: No Connection

EXT\_SEL: External selection  
High = CC1 orientation or no valid CC1/CC2 detection  
Low = CC2 orientation

PORT=:

- 1: DFP mode
- 0: UFP mode
- Floating: DRP mode



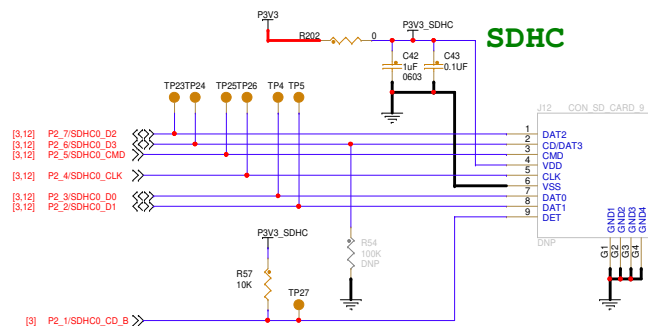
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Page Title: **USB & PWR**

Size C	Document Number SCH-90818 PDF: SPF-90818
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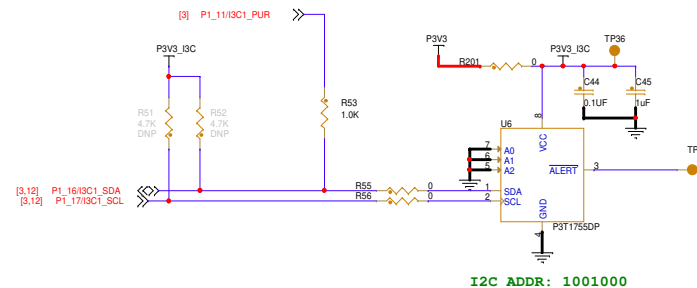
Date:	Thursday, March 28, 2024	Sheet	6	of	13
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#### Layout Notes:

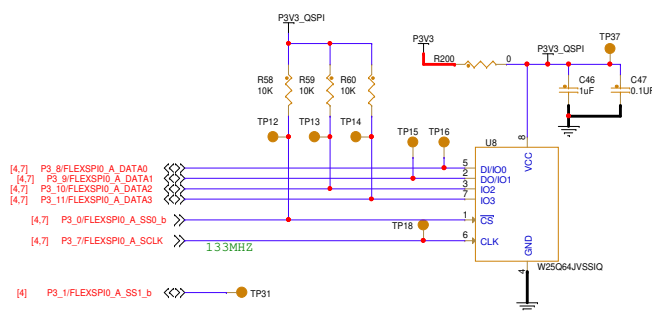
- 1) SDHC signals: equal length routing with 50ohm resistance. And as short as possible.
- 2) Place R54 to easily rework.

## I3C SENSOR



I2C ADDR: 1001000

## QSPI

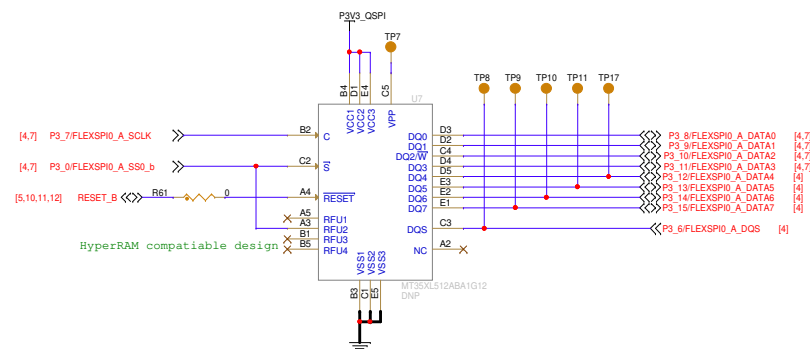


Other QSPI Flash Option: MT25QL128ABA1ESE-0SIT (MICRON)

#### Layout Notes:

- 1.U7 & U8 footprint overlapped.
- 2.Equal length routing with 50ohm resistance.
- 3.Place TP31 close to TP12.

## Octal Flash



HyperRAM compatible design

<Core Design>



Classification: Company Internal/Proprietary

Drawing Title: **FRDM-MCXXN947**

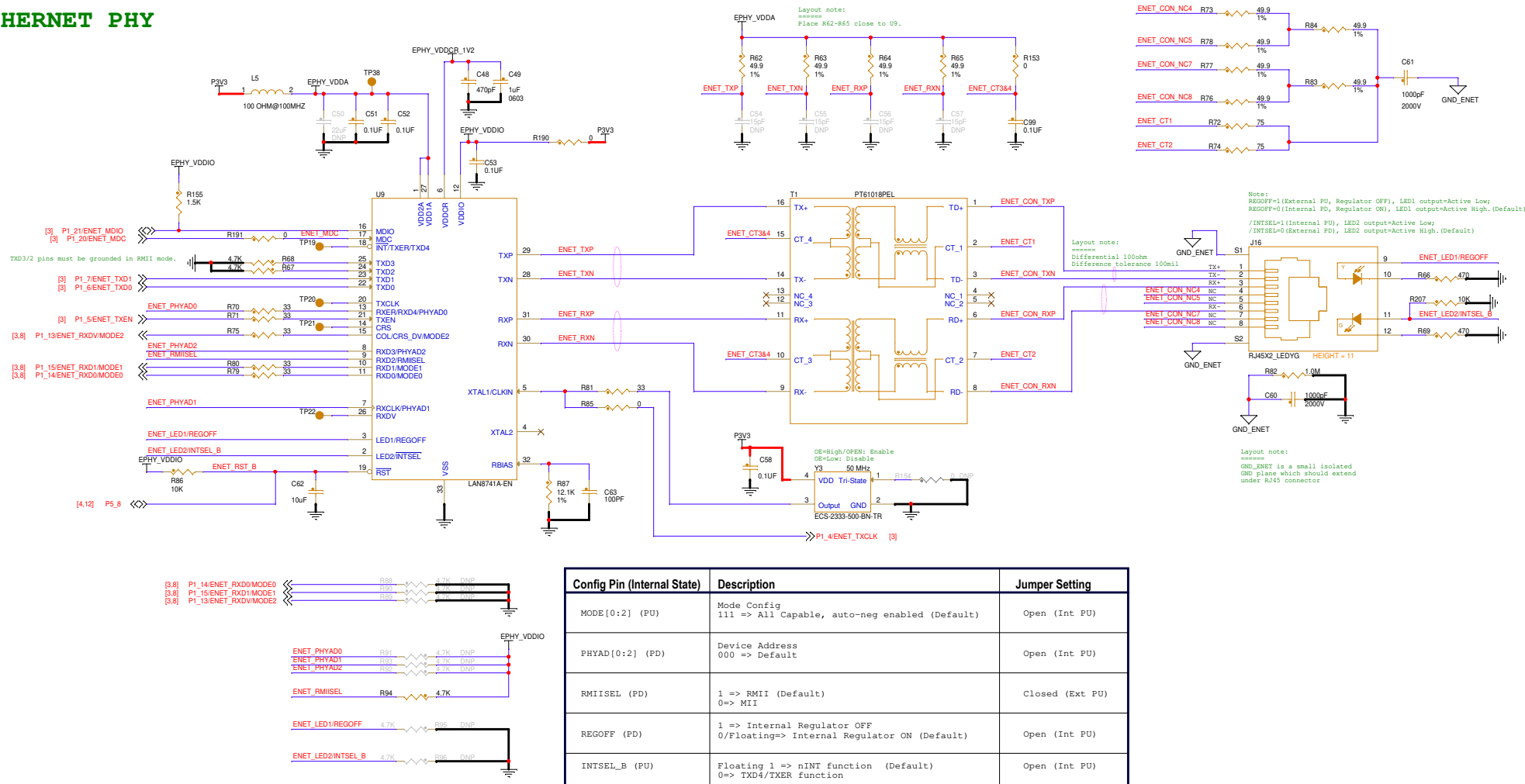
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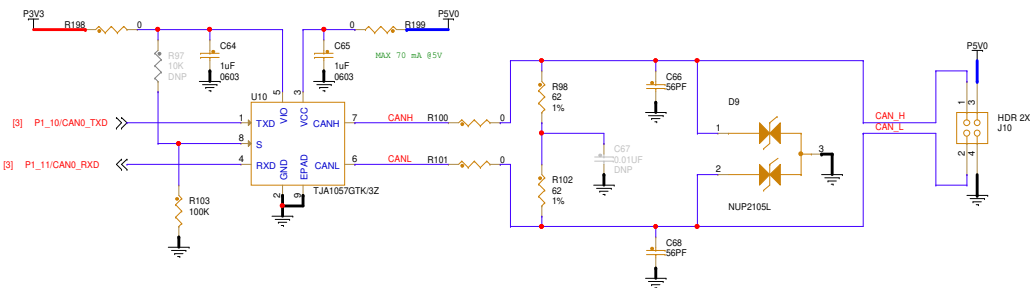
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Rev C

## ETHERNET PHY



**CAN PHY**



**Classification:** Company Internal/Proprietary

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Page Title: CAN PHY &amp; ETHERNET PHY

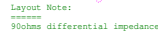
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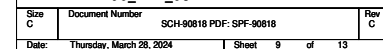
	R
--	---



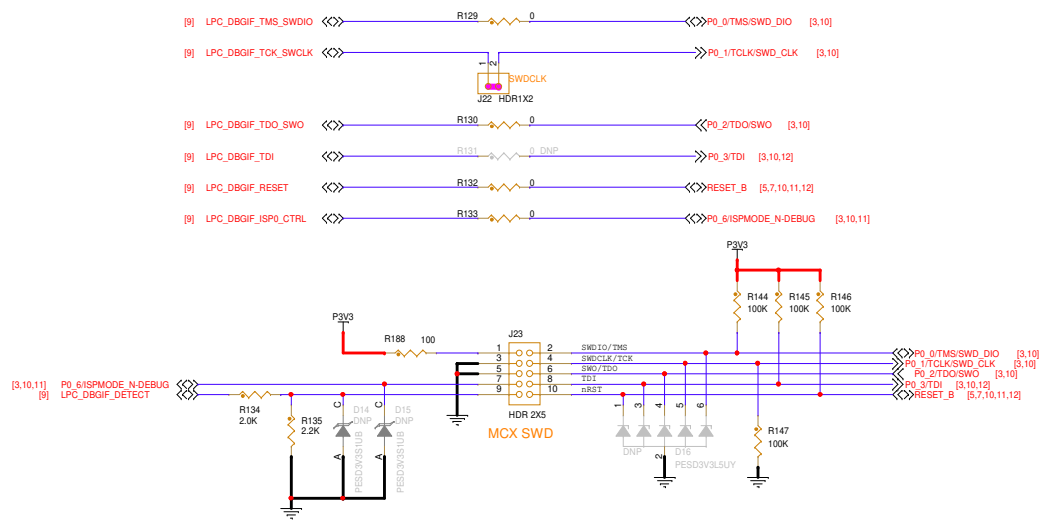
Layout Note:  
 =====  
 Add a outline for MCU LINK related components.



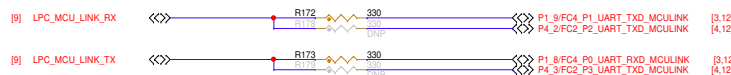
```
HW_VER_0: USB power negotiation enable when low
HW_VER_2: USB-SIO bridge disable when low
HW_VER_3: OS selection when low
HW_VER_4: Board identity code used when low
HW_VER_5: Power measurement disable if leave open
HW_VER_6: VCOM disable when low
HW_VER_7: SWD disable when low
HW_VER_8: Secondary VCOM disable when low
```



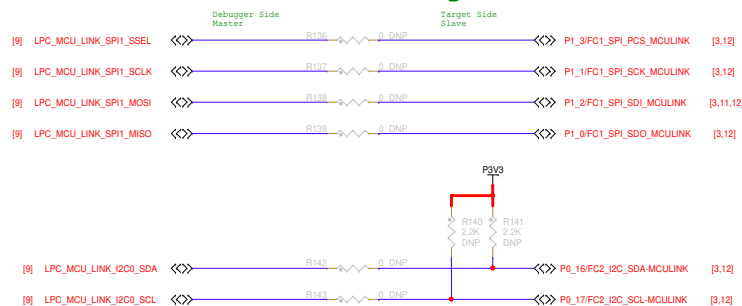
MCU-Link Debug Interface



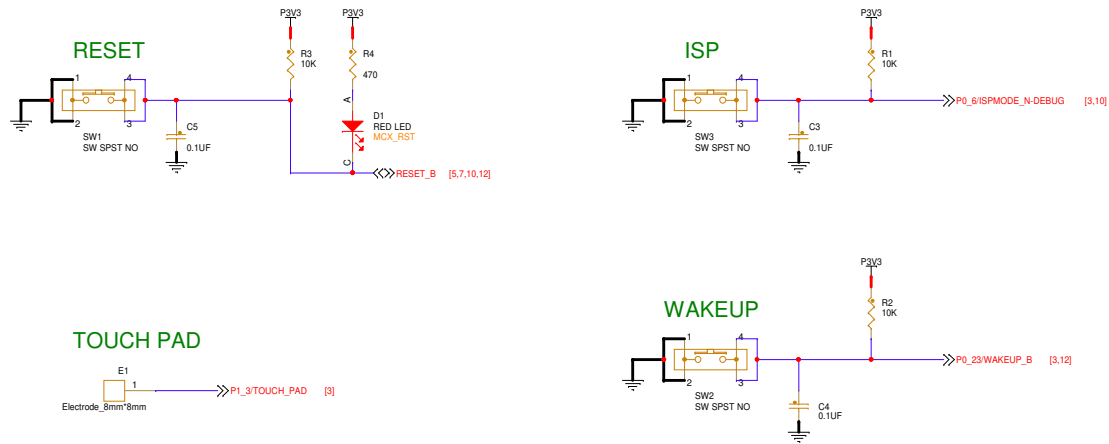
MCU-Link UART



USB Bridge



## HMI



## RGB



Classification: Company Internal/Proprietary

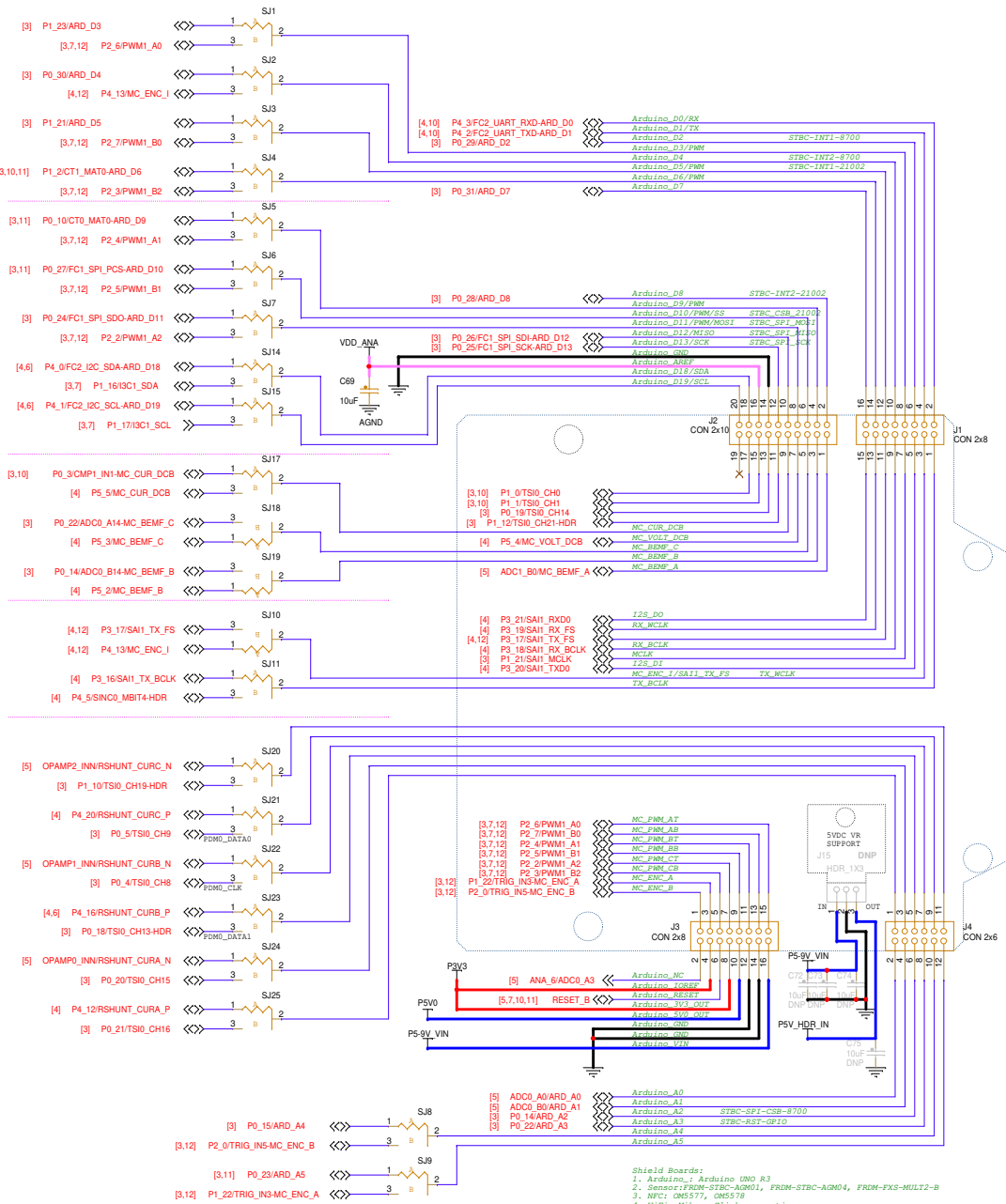
Drawing Title:  
**FRDM-MCXN947**

Page Title:  
**SWITCH & LED**

Size C	Document Number SCH-90818 PDF: SPF-90818	Rev C
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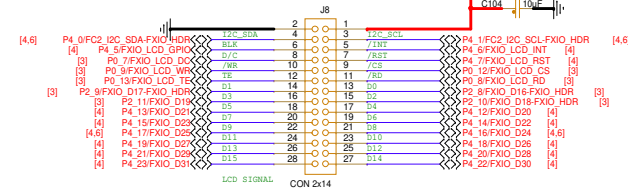
# ARDUINO SHIELD COMPATIBLE HEADERS



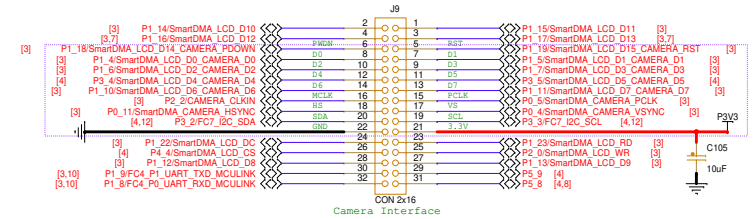
## FlexIO LCD

Layout notes:

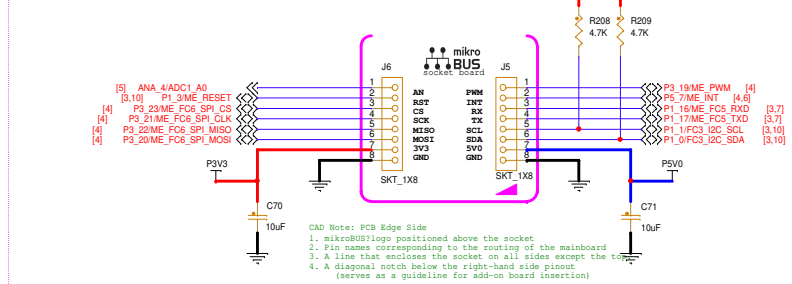
Add clear silkscreens for each pins of these connectors in this page.



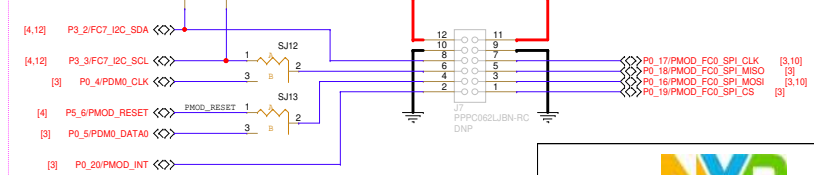
## Camera



## Mikro Bus



## PMOD



Classification: Company Internal/Proprietary

Drawing Title: **FRDM-MCXN947**

Page Title: **HEADERS**

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REF DES	JUMPER(DEFAULT)	PAGE NAME
J24	1-2	06 USB & PWR
J18,J19	OPEN	09 MCU_LINK_USB
J22	1-2	10 MCU_LINK_DEBUG

# APPENDIX JUMPER/DNP

REF DES	ASSY_OPT	PAGE NAME
C107,J25,J26,J27,J28,JP6,R17,R20,R23,R194	DNP	05 SOC_PWR
C102,D6,JP1,JP2,R28,R29,R34,R37,R38,R40,R42,R43,R45,R46,R49,R50	DNP	06 USB & PWR
J12,R51,R52,R54,U7	DNP	07 SD & QSPI & SENSOR
C50,C54,C55,C56,C57,C67,R88,R89,R90,R91,R92,R93,R95,R96,R97,R154	DNP	08 CAN PHY & ETHERNET PHY
C96,C97,C103,R118,R119,R121,R123,U12	DNP	09 MCU_LINK_USB
D14,D15,D16,R131,R136,R137,R138,R139,R140,R141,R142,R143,R178,R179	DNP	10 MCU_LINK_DEBUG
C72,C73,C74,C75,J7,J15	DNP	12 HEADERS

REF DES	SHORT(DEFAULT)	PAGE NAME
SJ16,SJ26,SJ27	1-2	03 SOC_PORT0-2
SJ1,SJ2,SJ3,SJ4,SJ5,SJ6,SJ7,SJ8,SJ9,SJ10,SJ11,SJ12,SJ13,SJ14,SJ15,SJ17,SJ18,SJ19,SJ20,SJ21,SJ22,SJ23,SJ24,SJ25	1-2	12 HEADERS

