

8

7

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1

NOTES (UNLESS OTHERWISE SPECIFIED):

1. THIS DRAWING SPECIFIES THE REQUIREMENTS FOR A PRINTED WIRING BOARD IN ACCORDANCE WITH SPECIFICATION IPC-6012 CLASS 2 (LATEST REVISION).

2. THE PWB MUST BE LEAD FREE ASSEMBLY PROCESS COMPATIBLE AND MUST BE ABLE TO HANDLE A MINIMUM OF 5 CYCLES AT 260 DEGREES CELSIUS FOR 10 SECONDS.

3. BASE MATERIAL - LAMINATE AND PREPREG SHALL MEET IPC-4101D-26, 83 or 98
Tg - MUST BE GREATER THAN OR EQUAL TO 150 DEGREES CELSIUS.
Td - MUST BE GREATER THAN OR EQUAL TO 330 DEGREES CELSIUS.

4. COPPER FOIL WEIGHT - SEE STACKUP DETAIL 'A'

5. CHARACTERISTIC IMPEDANCE - SEE DETAIL 'B'

6. MINIMUM CONDUCTIVE WIDTH/SPACING TO BE .00315"/.004"

7. PLATING FINISH: A, BOTH SIDES ENIG; TO MEET THE REQUIREMENTS OF IPC-4552 (LATEST REVISION).

8. FAB VENDOR IS NOT ALLOWED TO USE ODB FOR FABRICATION. CAN BE USED ONLY FOR REFERENCE.

9. SOLDERMASK - TO MEET THE REQUIREMENTS OF IPC-SM-840E (OR LATEST REVISION).
BLACK COLOR, BOTH SIDES. MODIFICATION OF SOLDERMASK IS NOT ALLOWED WITHOUT WRITTEN PERMISSION FROM NXP.
TYPE: LP1 OR EQUIVALENT.
A. LOCATION +/- .002" OF PLATED PADS.
B. DIAMETER OR SIZE +/- .002 OF ORIGINAL DATA

10. SILKSCREEN - WHITE EPOXY OR ACRYLIC INK, BOTH SIDES. NO SILKSCREEN ON ANY EXPOSED COPPER FEATURE.

11. ELECTRICAL TEST - 100% IPCD356. PCB FABRICATOR TO PERFORM A NET COMPARE AGAINST THE IPCD356 NETLIST PROVIDED BY NXP.

12. PRINTED WIRING BOARD IS TO BE INDIVIDUALLY BAGGED.

13. DFM CHECK MUST BE RUN ON BOARD DATA BEFORE BUILDING BOARDS, UNLESS PRIOR APPROVAL IS GIVEN IN WRITING BY NXP.

14. TEARDROPS MAY BE ADDED AT THE FAB HOUSE TO ALL SIGNAL LAYERS.

15. TWO SOLDER SAMPLES TO BE PROVIDED.

16. SUPPLIER MARKINGS - ON SECONDARY SIDE ONLY, WHERE SHOWN.
- MUST BE UL RECOGNIZED AND MUST HAVE AN ID THAT CONFORMS TO UL94V-0

17. THE PWB WILL BE MARKED AS LEAD FREE BY USE OF AN INK STAMP (Pb)

18. THE PWB WILL BE MARKED AS LEAD FREE PROCESS COMPATIBLE BY USE OF AN INK STAMP (260P)

19. ALL PLATED AND NON-PLATED THROUGH HOLES ARE TO BE DRILLED AT PRIMARY DRILL STEP. ALL HOLE LOCATION TOLERANCES ARE TO BE +/- .002 IN REFERENCE TO THE PRIMARY DATUM UNLESS OTHERWISE SPECIFIED.

20. FINISHED PCB MUST BE PANELIZED FOR ASSEMBLY ACCORDING TO CONTRACT MANUFACTURERS REQUIREMENTS. THE ADDITION OF RAILS AND .125" NON-PLATED TOOLING HOLES ARE AT THE DISCRETION OF CONTRACT MANUFACTURER. PANELIZATION MUST BE APPROVED BY CONTRACT MANUFACTURER.

21. THIEVING REQUIREMENT:
C. COPPER THIEVING ADDITION IS NOT ALLOWED.

22. THIS BOARD USES VIA-IN-PAD; SEE FAB_VIAFILL.ART
A. ALL VIAS USING 10.1 DRILL SIZES ARE TO BE FILLED WITH NON-CONDUCTIVE VIA FILL. LACKWITZ-PETERS P92795 OR EQUIVALENT AND MADE PLANAR TO THE PADS.
B. OVERPLATE THE FILLED VIA AND APPLY FINISH METAL TREATMENT.
C. DIMPLE ON VIA-IN-PADS MUST BE NO GREATER THAN .003" AND PROTRUSION NO GREATER THAN .002"

4645.67 [118.00]

2165.35 [55.00]

0 [0]

0 [0]

PRIMARY DATUM GRID ORIGIN

BOARD CUTOUT

0 [0]

DRILL CHART: TOP to BOTTOM

ALL UNITS ARE IN MILS

FIGURE	FINISHED SIZE	TOLERANCE	DRILL	PLATED	QTY
⌀	8.0	+0.0/-8.0		PLATED	275
⌀	10.0	+0.0/-10.0		PLATED	451
⌀	10.1	+0.0/-10.1		PLATED	18
⌀	16.0	+2.0/-2.0		PLATED	32
⌀	28.0	+2.0/-2.0		PLATED	10
⌀	35.0	+3.0/-3.0		PLATED	12
⌀	40.0	+3.0/-3.0		PLATED	89
⌀	41.0	+3.0/-3.0		PLATED	72
⌀	44.0	+2.0/-2.0		PLATED	20
⌀	37.0	+2.0/-2.0		NON-PLATED	2
⌀	125.0	+2.0/-2.0		NON-PLATED	4
⌀	55.0x24.0	+2.0/-2.0		PLATED	4
⌀	83.0x24.0	+2.0/-2.0		PLATED	4
⌀	87.0x28.0	+2.0/-2.0		PLATED	2

TOTAL HOLES: 995

* SURFACE - AIR 0 MIL(+0/-0)
* SOLDERMASK TOP MASK - POLYIMIDE 1.18 MIL(+0/-0)
L1 TOP CONDUCTOR - COPPER PLATED 1.8 MIL(+0/-0)
* DIELECTRIC - FR-4 3.01 MIL(+0/-0)
L2 GND PLANE - COPPER 1.2 MIL(+0/-0)

* DIELECTRIC - FR-4 48.43 MIL(+0/-0)

L3 POWER PLANE - COPPER 1.2 MIL(+0/-0)
* DIELECTRIC - FR-4 3.01 MIL(+0/-0)
L4 BOTTOM CONDUCTOR - COPPER PLATED 1.8 MIL(+0/-0)
* SOLDERMASK BOTTOM MASK - POLYIMIDE 1.18 MIL(+0/-0)
* SURFACE - AIR 0 MIL(+0/-0)

DESIGN CROSS SECTION CHART

TOTAL THICKNESS 62.81 MIL

BOARD THICKNESS TOLERANCE +/-10%

ALL VALUES ARE FINISHED VALUES

DETAIL A

LAYER STACKUP

SCALE: NONE

DETAIL B

IMPEDANCE REQUIREMENTS

IMPEDANCE TOLERANCE IS 10%

SE				DIFF			
LAYERS	TRACE WIDTH	IMPEDANCE	REFERENCE LAYER	TRACE WIDTH	IMPEDANCE	REFERENCE LAYER	
L1 PS	4.40	50.00	3.50	4.30	90.00	3.15	5.95
L4 SS	4.40	50.00	3.50	4.30	90.00	3.15	5.95

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COMPANY INTERNAL

COMPANY CONFIDENTIAL

UNLESS OTHERWISE SPECIFIED

DIMENSIONS ARE IN INCHES

TOLERANCES ARE

DECIMALS

ANGLES

D-10°

XXX .005

✓ FIN ALL MACHINED SURFACES

BREAK ALL SHARP EDGES AND CORNERS

REMOVE BURRS

UNLESS INDICATED, NOT TO SCALE

THIRD ANGLE ORTHOGRAPHIC PROJECTION

IN USAS

PART NO.

170-90818

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PROPRIETARY TO NXP AND SHALL NOT

BE USED FOR ENGINEERING DESIGN

PROCUREMENT OR MANUFACTURING IN WHOLE

OR IN PART WITHOUT THE CONSENT OF

NXP

APPROVALS

DATE

DRAWN

Aiison Zhou

03-28-24

CHECKED

Steven Ding

03-28-24

DESIGN ENGINEER

Kate Fan

03-28-24

6501 WILLIAM CANNON DRIVE WEST AUSTIN, TEXAS 78735 USA

TITLE

PRINTED WIRING BOARD

FRDM-MCXN947

SIZE

D

LAY-90818

DWG. NO.

FAB-90818

REV

C

SCALE

1/1

DO NOT SCALE DRAWING

SHEET

1

OF

2

8 7 6 5 4 3 2 1

D

C

B

A

NOTES UNLESS OTHERWISE SPECIFIED:

ZONE	REV	DESCRIPTION	DATE	DE	PE	CAD
	A	ORIGINAL RELEASE	07-07-23	K.F.	S.D.	A.Z.
	B	UPDATE	09-18-23	K.F.	S.D.	A.Z.
	C	UPDATE	03-28-24	K.F.	S.D.	A.Z.

THIS FAB_VIAFILL.ART SHOWS LOCATIONS OF VIA-IN-PAD TO BE FILLED.

PART NO.
170-90818

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X COMPANY INTERNAL
COMPANY CONFIDENTIAL

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UNLESS OTHERWISE SPECIFIED:
DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
XXX .XX
XXX .005
ANGLES 2°-30°
✓ TWO ALL MACHINED SURFACES
BREAK ALL SHARP EDGES AND CORNERS.
REMOVE BURRS.
UNDERLINED DIM. NOT TO SCALE.
THIRD ANGLE ORTHOGRAPHIC PROJECTION IS USED.

APPROVALS DATE
DRAWN Alison Zhou 03-28-24
CHECKED Steven Ding 03-28-24
DESIGN ENGINEER Kate Fan 03-28-24

TITLE
6501 WILLIAM CANNON DRIVE WEST AUSTIN, TEXAS 78735 USA
PRINTED WIRING BOARD
FRDM-MCXN947

SIZE CAD FILE NAME Dwg. No. REV
LAY-90818 FAB-90818 C

SCALE 1/1 DO NOT SCALE DRAWING SHEET 2 OF 2

8 7 6 5 4 3 2 1

A