MBI5051 Application Note

(This article applies to IC Version Code B and specifications Edition VA.0X of MBI5051)

Forward

MBI5051 features an embedded 4K-bit SRAM, which can support up to 1:8 time-multiplexing application. Users only need to send the whole frame data once and store in the embedded SRAM of LED driver, instead of sending every time when the scan line is changed; therefore it can easily achieve high grayscale with slow DCLK frequency. This article provides the application information of MBI5051, such as the input method of image data and the setting of gray scale data. The detail operations are described in the following sections.

Time-multiplexing Application Design

Figure 1 shows the 3pcs cascaded MBI5051 in 1:8 time multiplexing application.

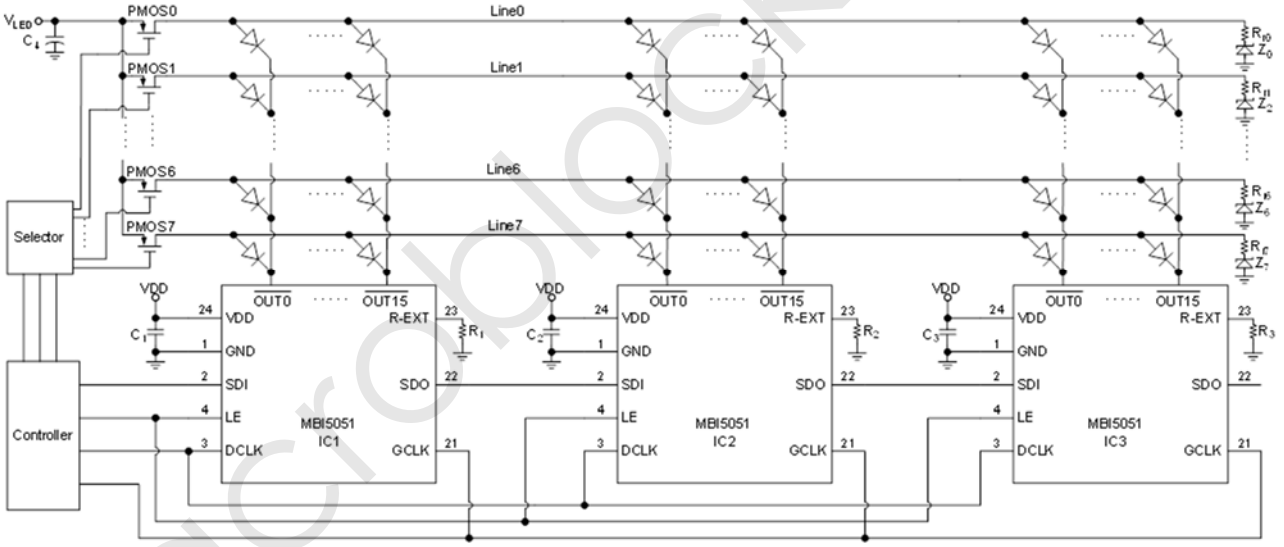

Figure 1. 3pcs cascaded MBI5051 in 1:8 time multiplexing application

Section 1: The Setting of Configuration Register

The setting of configuration data is described as below.

1. The “Pre-Active” command, LE arrested 14-DCLK rising edges, must be announced before “write configuration” command.
2. The data sequence of cascaded IC is ICn→ICn-1→…→IC2→IC1。
3. The sequence of gray scale data is bit15→bit14→…→bit1→bit0。
4. If there are N pcs of MBI5051 in cascaded, then the data length of each “data latch” will be 16 x N bits.
5. When LE is asserted 4-DCLK rising edges, serial data are written to the configuration register 1. When LE is asserted 8-DCLK rising edge, serial data are written to the configuration register 2.
6. The control signals shouldn’t come out until the power of driver board is stable.
7. To ensure the command is valid, the LE false trigger should be avoided in the interval between pre-active and write configuration.

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For lower ghost elimination, the configure registers, which are shown in table 1 and 2, are recommended.

Table 1. The recommended configuration register 1 for lower ghost elimination

The configuration register 1 for R-LED

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
1	0	1	0	0	0	1	1	0	0	1	0	1	0	1	1

The configuration register 1 for G/B-LED

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
1	1	1	0	0	0	1	1	0	0	1	0	1	0	1	1

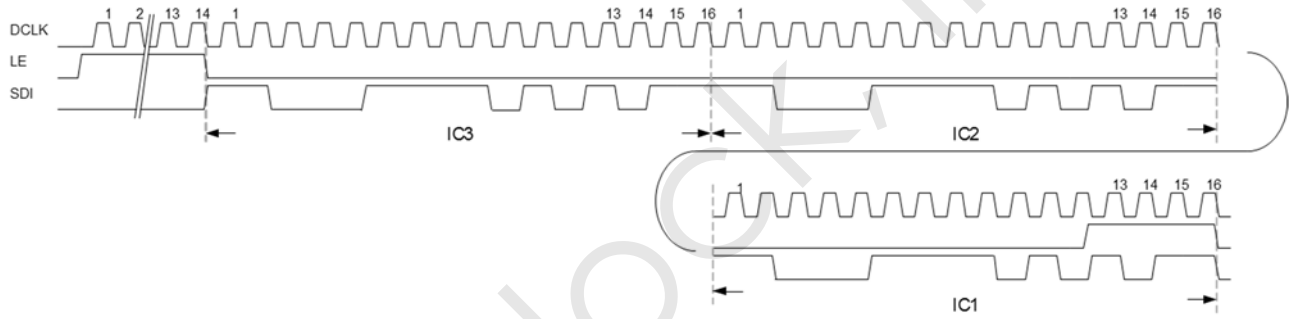

Figure 2. Example of Configuration register 1 for R-LED, which is for 3pcs cascaded MBI5051 (*Here, the input of SDI is not the recommended value.)

Table 2. The recommended configuration register 2 for lower ghost elimination

The configuration register 2 for R-LED

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

The configuration register for G/B-LED

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

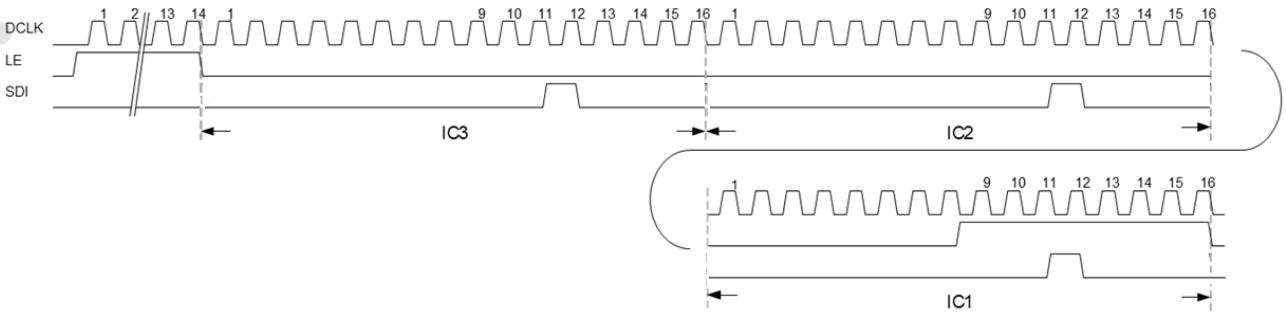

Figure 3. Example of Configuration register 2 for R-LED, which is for 3pcs cascaded MBI5051

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Section 2: The Setting of Gray Scale

The setting of gray scale data describes as below

1. The sequence of input data starts from scan line 0→ scan line 1→…. → scan line M-1.
2. The data sequence of cascaded IC is ICn→ICn-1→…. →IC2→IC1.
3. The data sequence of each channel is ch15→ch14→…. →ch0.
4. The data length of each channel is 16-bits, and the default PWM mode is 16-bits. The sequence of gray scale is bit15→bit14→…→bit1→ bit0 as figure 5 shows. The 14-bits gray scale can be set through Bit[7]=1 in configuration register 1, and the sequence of gray scale data is bit15→bit14→…→bit2→ 0→ 0, the last 2-bits (LSB) are set to “0”, as figure 6 shows.
5. The frequency of GCLK must be higher than 20% of DCLK to get the correct gray scale data.
6. LE executes the data latch to send gray scale data into SRAM. Each 16xN bits data needs a “data latch command”, where N means the number of cascaded driver.
7. After the last data latch, it needs at least 50 GCLKs to read the gray scale data into internal display buffer before the Vsync command comes.
8. GCLK must keep at low level more than 300ns before MBI5051 receives the Vsync signal.
9. Display is updated immediately when MBI5051 receives the Vsync signal.
10. The period of dead time (ie. The 1025th GCLK in 16-bit S-PWM) must be larger than 1500ns.

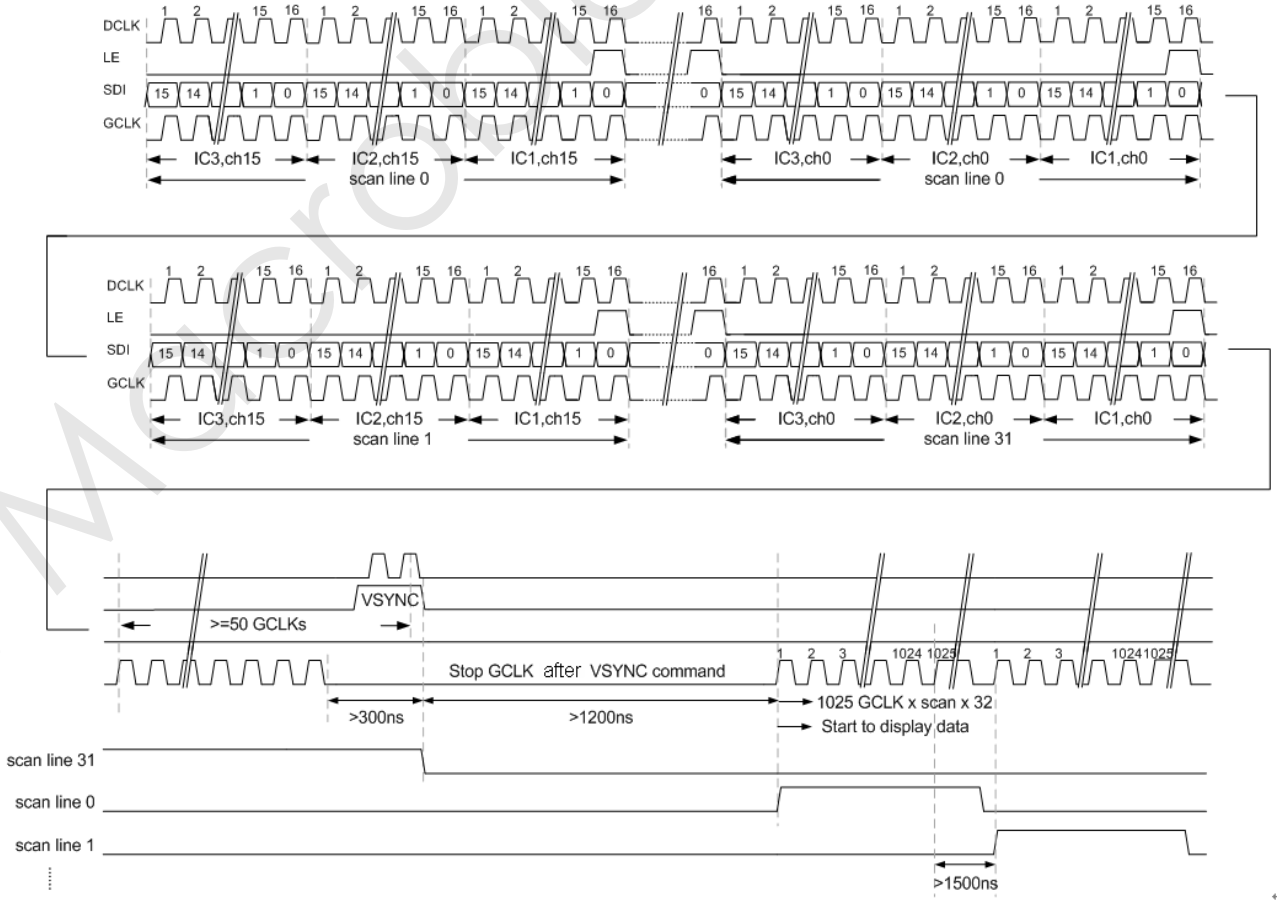

Figure 4. The timing diagram of 16-bit gray scale data

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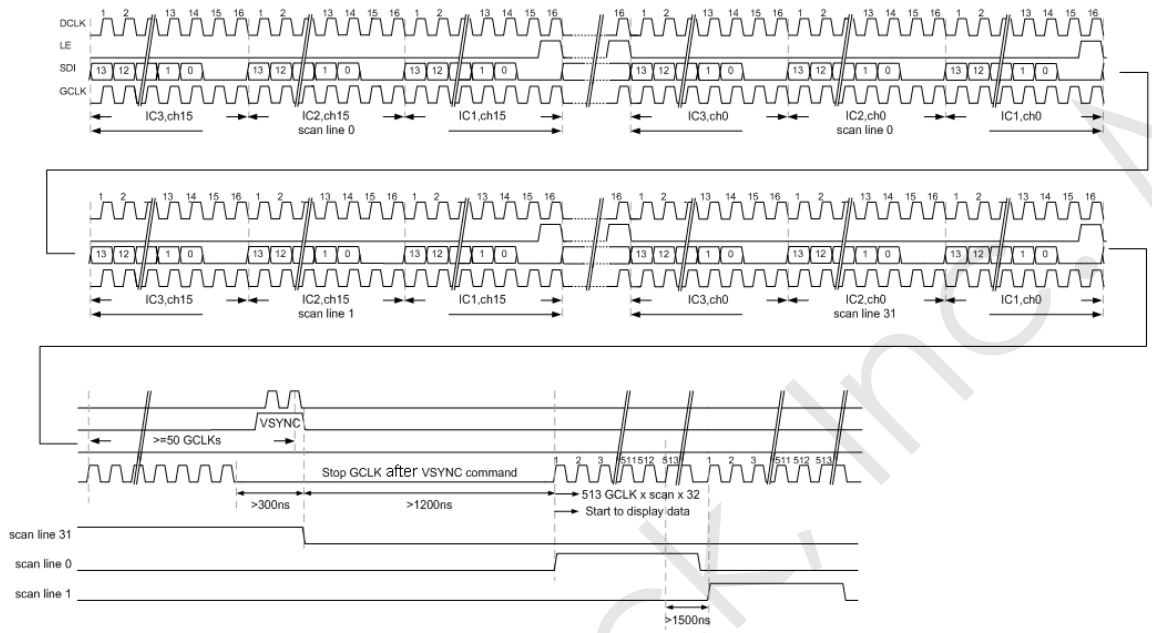

Figure 5. The timing diagram of 14-bit gray scale data

Section 3: Read configuration Register

The setting of read configuration register describes as below.

1. The command to read the configuration register 1 is LE arrested 5-DCLK rising edges, and LE arrested 9-DCLK rising edges is to read the configuration register 2.
2. Configuration register data will be outputted from SDO, and each bit comes out with DCLK.
3. It needs16 x N of DCLK to send configuration register data, where N means the number of cascaded driver.
4. The read out sequence of cascaded IC is ICn→ ICn-1→…. →IC2→IC1.
5. The bit read out sequence is bit15→bit14→…. →bit1→bit0.
6. In the duration of read configuration, the SDI signal can be ignored.
7. Read out the configuration register data in non-display state is recommended.

Figure 6 shows the example of reading configuration register 1 in 3pcs cascaded MBI5051.

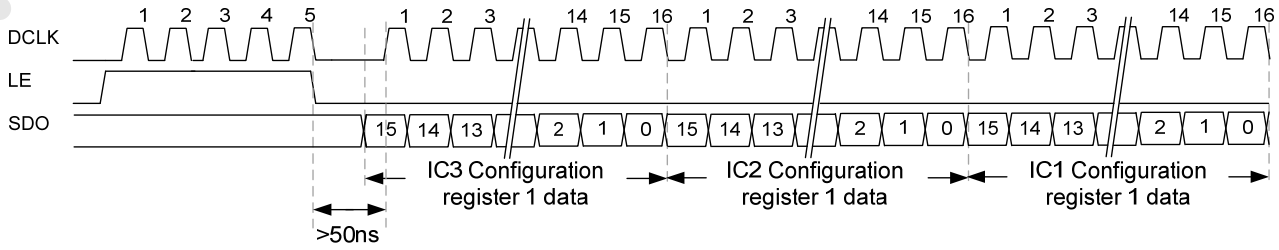

Figure 6. Example of reading configuration register 1 in 3pcs cascaded MBI5051

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Figure 7 shows the example of reading configuration register 2 in 3pcs cascaded MBI5051.

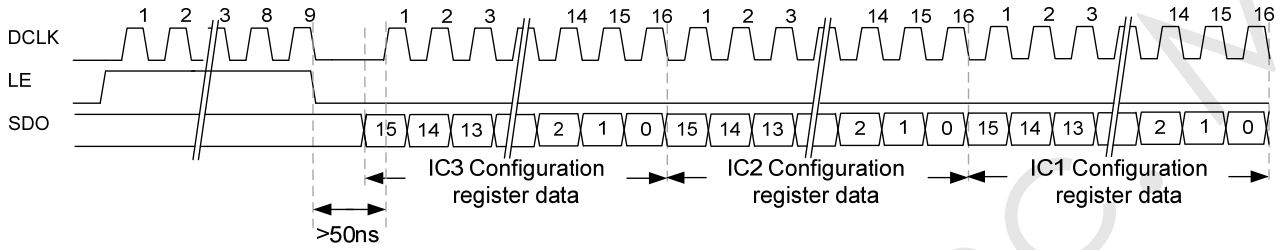

Figure 7. Example of reading configuration register 2 in 3pcs cascaded MBI5051

Section 4: Send Data and Display Image

MBI5051 embeds 4K-bit SRAM and divides it into two banks, SRAM A and SRAM B to reading and writing data frame. SRAM B is used to play the current frame data, and SRAM A receives the gray scale data of next frame. After receive the Vsync command, the assignments of these two SRAM will be exchanged, as figure 9 shows.

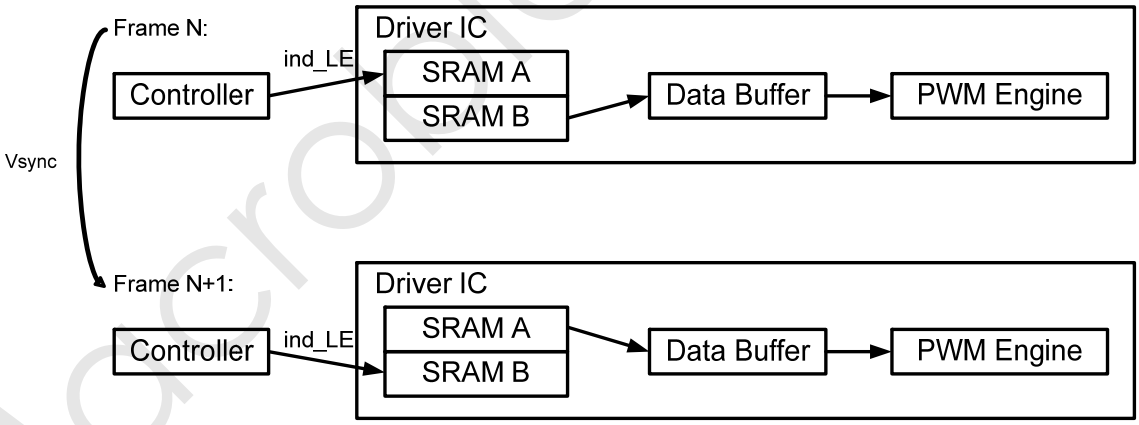

Figure 8. The data transmission structure of MBI5051

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Section 5: Visual Refresh Rate and GCLK Multiplier Technology

Visual Refresh Rate

With S-PWM technology, the 16-bits PWM cycle of MBI5051 is divided into 64 sections, and each section has 1024 GCLKs. The 14-bits PWM cycle of MBI5051 is divided into 32 sections, and each section has 512 GCLKs. The formulas of visual refresh rate are

$$F_{visual}=\frac{1}{[1024 \times (T_{GCLK})+ t_{Dead}] \times N} \quad \text{for 16-bits} \quad (1)$$

$$F_{visual}=\frac{1}{[512 \times (T_{GCLK})+ t_{Dead}] \times N} \quad \text{for 14-bits} \quad (2)$$

where

F_{visual}: Visual Refresh Rate.

T_{GCLK}: Gray Scale Clock Period (ie. $1/F_{GCLK}$)

t_{Dead}: Dead Time.

N: Number of Scan Lines.

For example, for 16-bits S-PWM mode, the 1:8 time-multiplexing application with 20MHz GCLK frequency and the dead time is 40-GCLKs, the visual refresh rate could be calculated as below

$$F_{visual}=\frac{1}{[1024 \times (1/20MHz) + 40 \times (1/20MHz] \times 8}=2350\ (Hz)$$

Since the frame data can be stored in the embedded SRAM of MBI5051, the updated data only need to complete transmission before next frame. The GCLK frequency needn't to follow the frame rate. If MBI5051's GCLK is 20MHz, the dead time is 40-GCLKs, table 3 shows the limitation in each case.

Table 3. The limitation in different cases when GCLK=20MHz

Case	Bit numbers of gray scale control (bit)	Scan line	Frame rate (Hz)	Cycle number of GCLK counter in a period T_{DATA}
1	16	8	60	39
2	16	4	60	78
3	14	8	60	75
4	14	4	60	150

If the driver with 16-bits gray scale data, it needs 64 cycles to complete a frame data. That means case 1 doesn't have enough time to complete a frame data transmission. However in case 2, the number of scan line decreases to 4, then the transmission can be completed in time. 14-bits gray scale data needs 32 cycles to complete a frame data, case 3 and 4 can achieve this mission.

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Double Refresh Rate

The 16-bits S-PWM cycle of MBI5051 is divided into 128 sections, and each section has 512 GCLKs. The 14-bits PWM cycle of MBI5051 is divided into 64 sections, and each section has 256 GCLKs.

If double refresh function is enabled, the number of GCLK counter and S-PWM cycle time will be reduced by half. The display will be dimmed due to the double dead time.

GCLK Multiplier Technology

If GCLK multiplier is enabled, GCLK will be dual edge triggered, that means the cycle time can be reduced by half. If GCLK multiplier is enabled, the 16-bits S-PWM cycle of MBI5051 is divided into 64 sections, and each section has 512 GCLKs. The 14-bits PWM cycle of MBI5051is divided into 32 sections, and each section has 256 GCLKs. Table 4 shows the results of GCLK multiplier enabled.

Table 4. The limitation in different cases when GCLK=20MHz (GCLK multiplier enabled)

Case	Bit numbers of gray scale control (bit)	Scan line	Frame rate (Hz)	Cycle number of GCLK counter in a period T_{DATA}
1	16	8	60	75
2	16	4	60	150
3	14	8	60	140
4	14	4	60	281

As MBI5051 GCLK multiplier is enabled, all the cases can complete a frame transmission.

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In figure 9, take the 16-bit gray scale data for example, the bits 15~6 are used to define the refresh rate (the SDI must larger than 64). The minimum output pulse width (=1/F_{GCLK}) is the reciprocal of GCLK frequency.

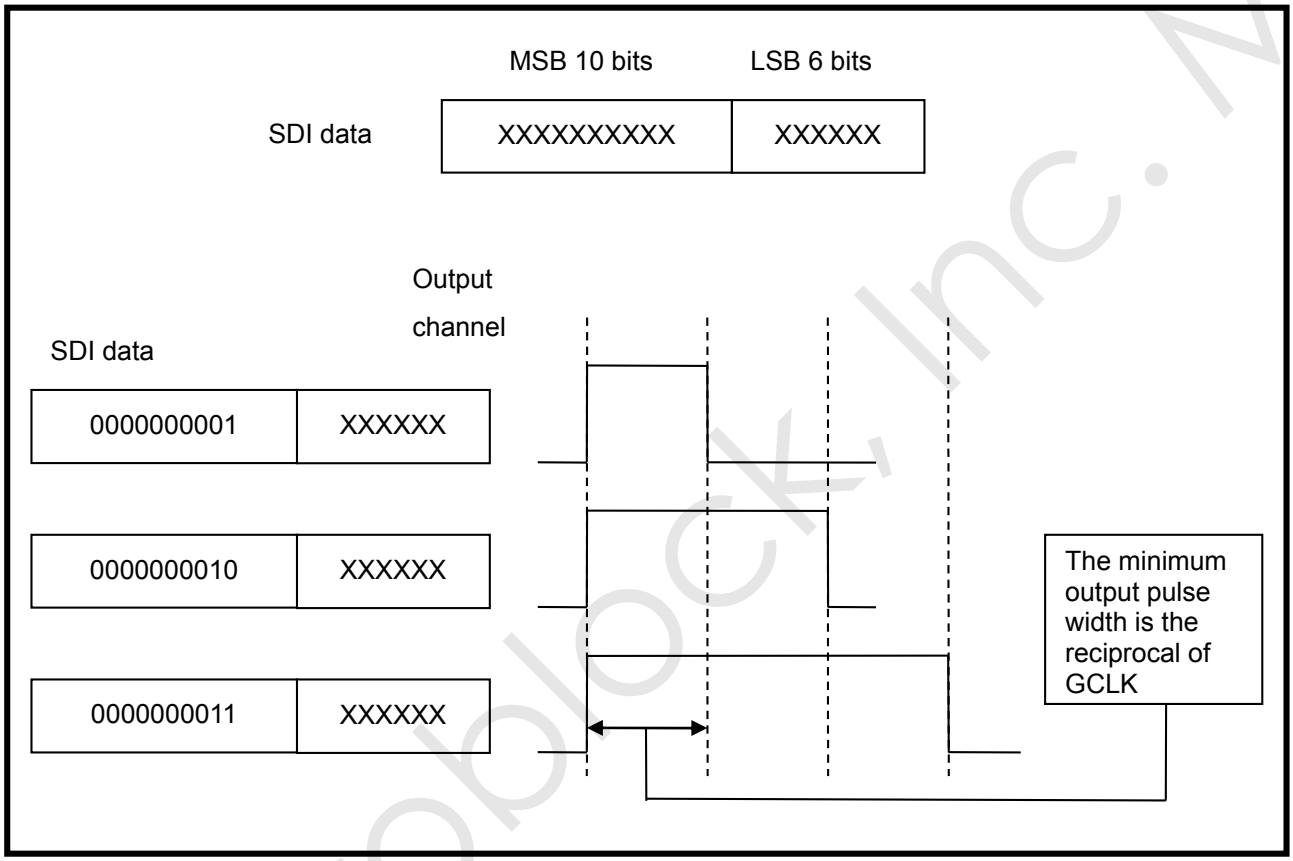

Figure 9. The diagram of SDI data and pulse width

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Section 6: The Maximum Cascaded Number of MBI5051

The frame data must be updated in a picture period. Therefore, the maximum cascaded number of MBI5051 is decided by DCLK frequency and scan lines, and it can be calculated from the following equation

$$N = F_{DCLK} / (\text{the amount of data bit x scan line x frame rate}) \quad (3)$$

Take the case 1 in table 5 for example, if the frame rate is 60 times/s, DCLK frequency is 15MHz, 1:8 time-multiplexing application, then from (3), the maximum cascaded number of MBI5051 is

$$N = (15x10^6) / [(16 \times 16) \times 8 \times 60] = 122$$

Table 5. The maximum cascaded number of MBI5051 at DCLK=15MHz

Case	Bit numbers of gray scale control (bit)	Frame rate (Hz)	Scan line	The maximum cascaded number
1	16	60	8	122
2	16	60	4	244
3	14	60	8	139
4	14	60	4	279

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Section 7: Current Gain Adjustment

MBI5051 current gain can be adjusted from 12.5% (default) to 200%. No matter the output current is set by Rext or current gain, the adjusted current must keep in the constant current range of MBI5051. For example, after current gain adjustment, the output current must in the range of 2mA~45mA when V_{DD}=5V or 2mA~30mA when V_{DD}=3.3V. Otherwise, the over designed output current can't be guaranteed.

The Bit 5 to Bit 0 in configuration register 1 is used to set the current gain, and the defaulted gain code is 6'b101011. The Bit 5 is HC bit, HC=0 means in low current region, and HC=1 is high current region.

Table 6. The setting of current gain

	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
Define	-	-	-	-	-	-	-	-	-	-	HC	DA4	DA3	DA2	DA1	DA0
Default	0	0	0	0	0	0	1	1	0	0	1	0	1	0	1	1
											← 6 bits current gain setting →					

If I_{OUT} =5mA and G=1, user can get the gain code by following steps.

Step 1: The R_{ext} , HC and D can be calculated by following equation (4), (5), and (6)

$$R_{ext} = (V_{R\text{-}EXT} / I_{OUT}) \times 24 \quad (4)$$

where $V_{R\text{-}EXT}$ = 0.61Volt ×G, and G means the current gain.

The relationship of current gain (G) and gain data (D) is

$$HC=1,\ D=(65xG-33)/3 \quad (5)$$

$$HC=0,\ D=(256xG-32)/3 \quad (6)$$

In the high gain region (G≧0.5 or D≧32), that means the HC is 1. In the low gain region (G<0.5 or D<32), the HC is 0. From (4), the R_{ext} = [(0.61 × 1) / 0.005] × 24 = 2928Ω. Current Gain G=1, HC=1. Thus, substitute above information into (5), the D=(65xG-33)/3=10.67≒11.

Step 2: Convert D into binary by following equation (7)

$$D = DA4\times2^4 + DA3\times2^3 + DA2\times2^2 + DA1\times2^1 + DA0\times2^0 \quad (7)$$

Therefore, DA[4:0] is 01011. And the 6 bits (Bit 5~Bit 0) of the configuration register are 6'b101011.

If R_{ext} keeps the same, the adjusted output current is from 5mA to 8mA, then

Step 1: G= 8mA /5mA =1.6 (Current Gain G>0.5, HC=1).

Step 2: From (5), D= (65x1.6-33)/3=23.66 ≒23

Step 3: Convert D=23 into binary by equation (7), therefore DA[4:0] is 10111.

Step 4: The adjusted gain code (Bit 5~Bit 0) is 6'b110111.

If R_{ext} keeps the same, the adjusted output current is from 5mA to 2mA, then

Step 1: G= 2mA /5mA =0.4 (Current Gain G<0.5, HC=0).

Step 2: From (6), D= (256x0.4-32)/3=23.46≒23.

Step 3: Convert D=23 into binary by equation (7), therefore DA[4:0] is 10111.

Step 4: The adjusted gain code is 6'b010111.

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Figure 10 shows the relationship of current gain and gain code. The defaulted gain code of MBI5051 is 6'b101011, is corresponding to 1.015 current gain.

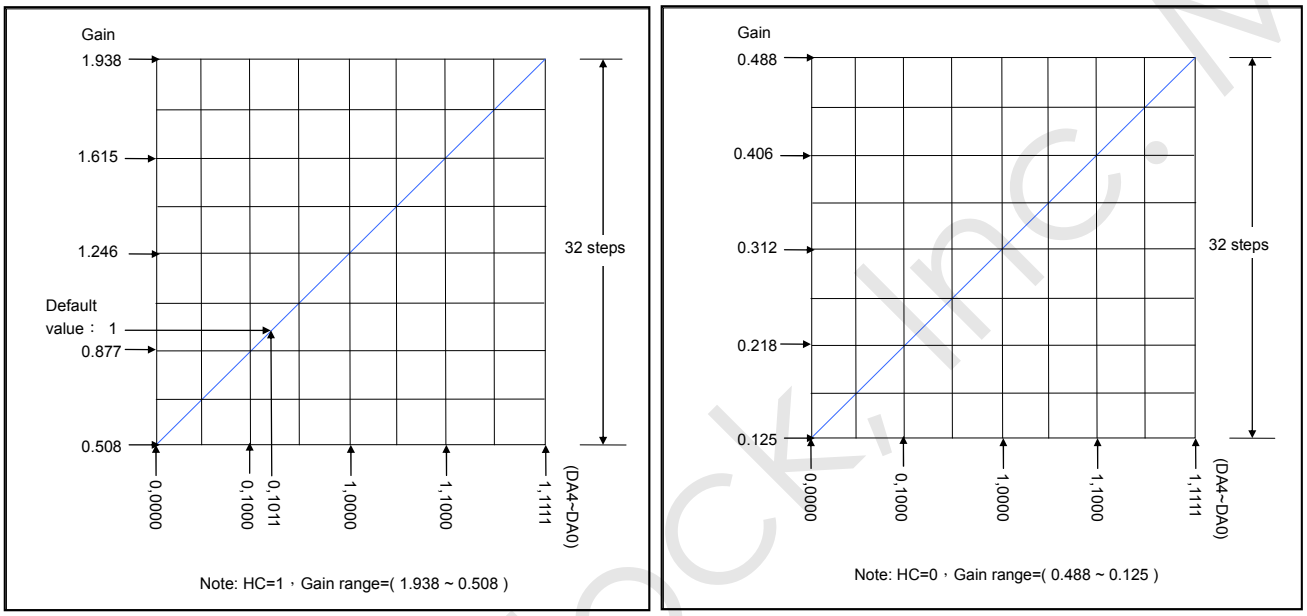

Figure 10. The relationship of current gain and gain code

Figure 11 is the relationship of output current and gain data under V_{DD}=5V and R_{ext}=3000Ω. The defaulted current gain, G =1, is corresponding to 5mA.

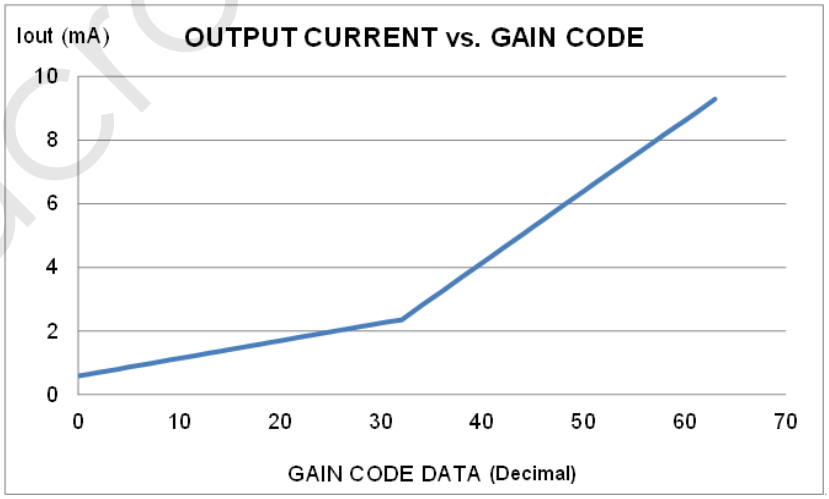

Figure 11. The relationship of output current and gain code at 5V, Rext=3000Ω.

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Section 8: The Notice of LED Open-Circuit Error Detection

As figure 12 shows, MBI5051 executes the compulsory open-circuit detection while the LE high pulse is sampled by 7-DCLK rising edges. In the duration of compulsory open circuit detection, all the output channels will be turned off. When LE high pulse pin is sampled by 1-DCLK rising edge, the result of open circuit detection will be shifted out from the SDO pin and the sequence is from /OUT15 →/OUT14 →… to /OUT0.

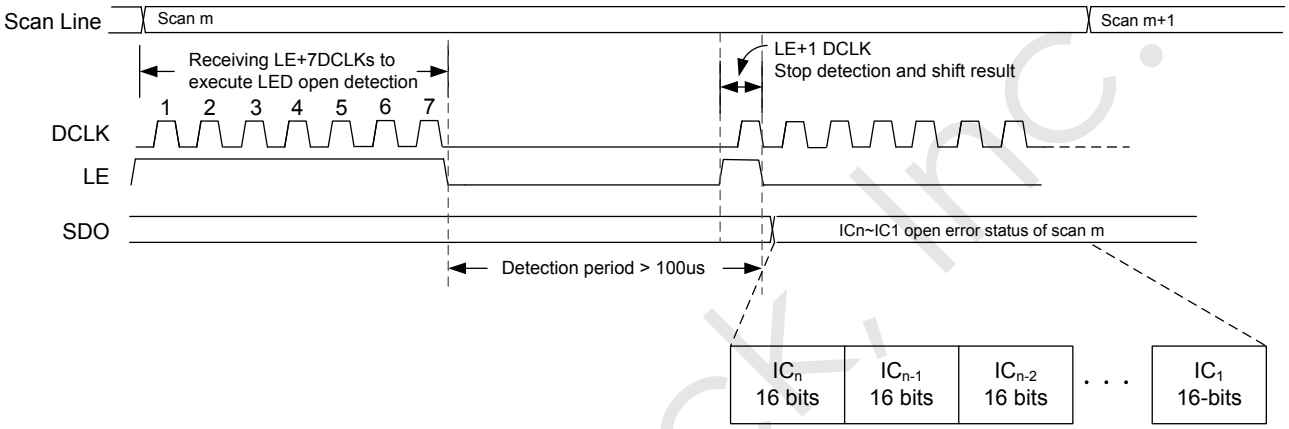

Figure 12. The timing diagram of compulsory open-circuit detection

In the duration of compulsory open-circuit detection, the SDI data can be ignored. In addition, the following notices must be taken

1. During the detection, the frame cannot display normal until LE arrested 1-DCLK rising edge. The duration should be keep longer than 100us, as figure 12 shows. All the LEDs will instantly light up and produce flicker during the time.
2. When output turns on, please make sure the output voltage (V_{DS}) is higher than 0.5V.
3. In the duration of compulsory open circuit detection, the scan line can't switch.
4. MBI5051 doesn't support LED short circuit detection.

Table 7. Error code

Status	Detected Result
Open	0
Normal	1

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Section 9: Ghost Elimination in the Time-Multiplexing LED Displays

There are two types of ghosting problems in time-multiplexing application

1. The phenomenon of unexpected LED in last scan line slightly turns on called “upper ghost problem”. Please refer the follow method to prevent it.

   Figure 13 is an example of time-multiplexing application with n-scan lines. To avoid the upper ghost problem, the discharged circuit between the V_{LED} and GND of each scan line is recommended. Typically, the discharged circuit is a resistor cascaded with a zener diode. The resistance is about 390Ω~1kΩ, and the zener diode is about 3.0~3.3V, it can be adjusted based on the actual condition.

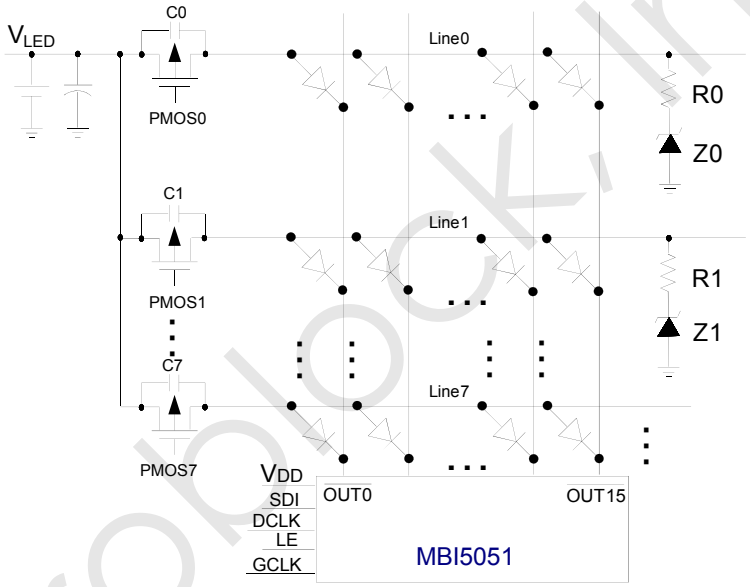

Figure 13. Circuit diagram of upper ghost elimination

2. The phenomenon of unexpected LED in next scan line slightly turns on called “lower ghost problem”.

   The bit[F] of configuration register1 is used to enable the lower ghost elimination, and figure 14 shows the timing diagram. In the dead time, the duration between the falling edge of 1025th GCLK and scan line switched determines the running time of lower ghost elimination.

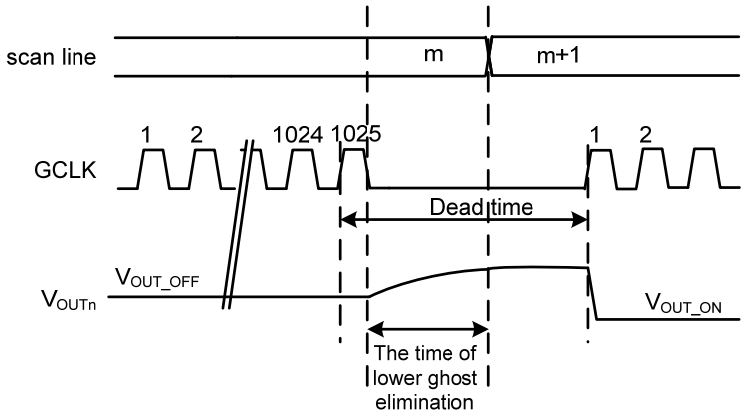

Figure 14. Timing diagram of lower ghost elimination

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Figure 15 shows the display example with diagonal line pattern, the ghost problem is apparent, and figure 16 shows the improvement which has enabled the lower ghost elimination.

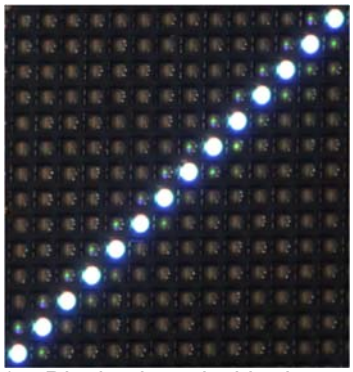

Figure 15. Display board with ghost problem

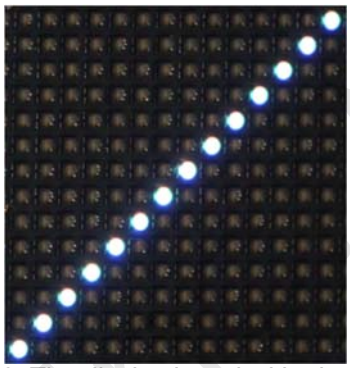

Figure 16. The display board with ghost elimination function

Section 10: High contrast interference

Due to the loading effect, the image with low gray scale will be affected by the high gray scale image. Figure 17 shows the example of high contrast interference by the high gray scale image.

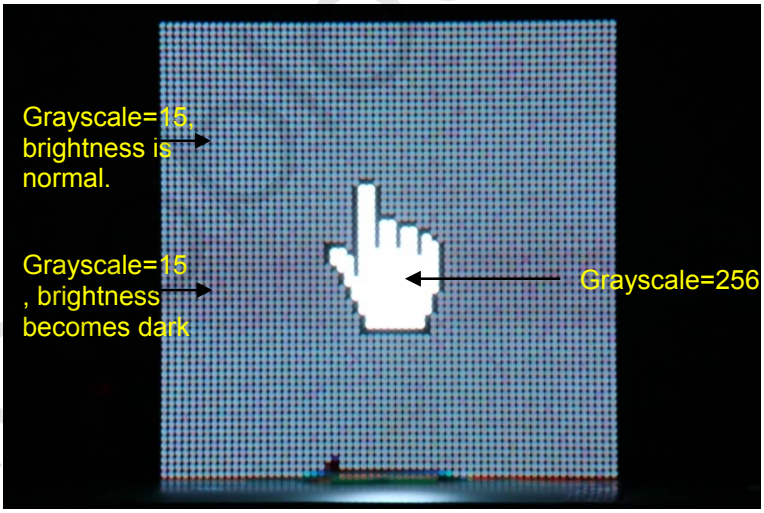

Figure 17. The example of high contrast interference

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To improve the problem of high contrast interference, reduce the resistance of discharge circuit in figure 13 is helpful, but the problem can't be fully solved. The discharge circuit shown in figure 18 can fully solve this problem. A zener diode cascaded with the N-MOSFET, and then parallels a ceramic capacitor between the zener diode. The recommended ceramic capacitor is 0.1uF/6.3V/X7R, however user can adjust the capacitance according to the actual application condition.

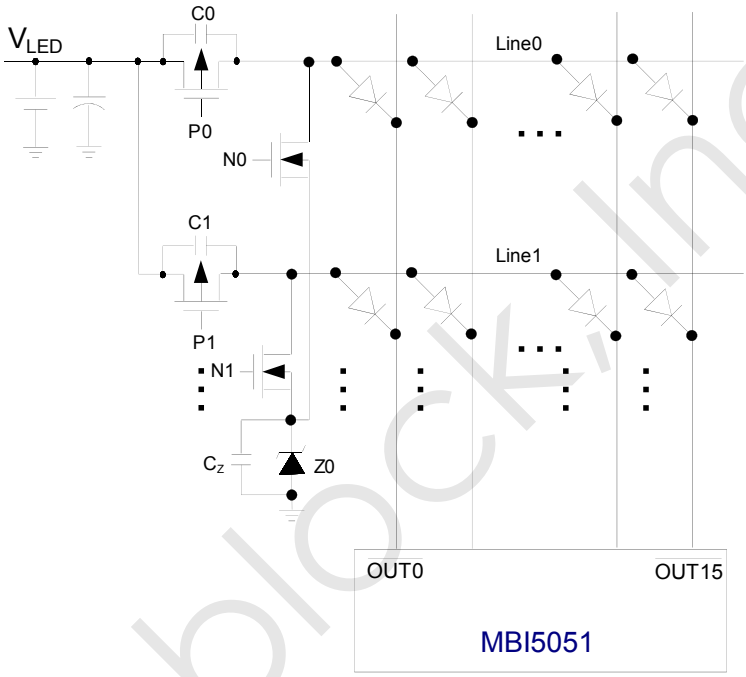

Figure 18. Circuit diagram of image couple problem eliminating

Section 11: Software Reset

When the software reset command is enabled, the internal counters of GCLK and data latch will be reset, and turned off all the output channels. However, the gray scale data stored in the SRAM, configuration register and current gain won't be reset.

Summary

MBI5051 uses the embedded S-PWM to control LED current and provides a storage solution of 4K-bit SRAM. Users don't need to send new data every time. This article provides the design guideline for uses.

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