Multifunction Vehicle Bus Controller

MITRAC CC MVBC02C

Overview

The Multifunction Vehicle Bus (MVB) is a standard communication medium to transport and exchange data among attached devices. These devices, which are physically connected to the bus, may vary in function, size, performance and at the physical layer level.

The *Bombardier* MITRAC** CC MVBC02C (Multifunction Vehicle Bus Controller) is the common communication interface component between the MVB independent circuits and the actual physical layer of the MVB (excluding physical layer drivers). The MVBC02C, when configured accordingly, can be used in Class 1, 2, 3, 4 devices as defined in the IEC TCN Standard [1]. The MVBC02C is available in form of a 100-pin Application Specific Integrated Circuit (ASIC).

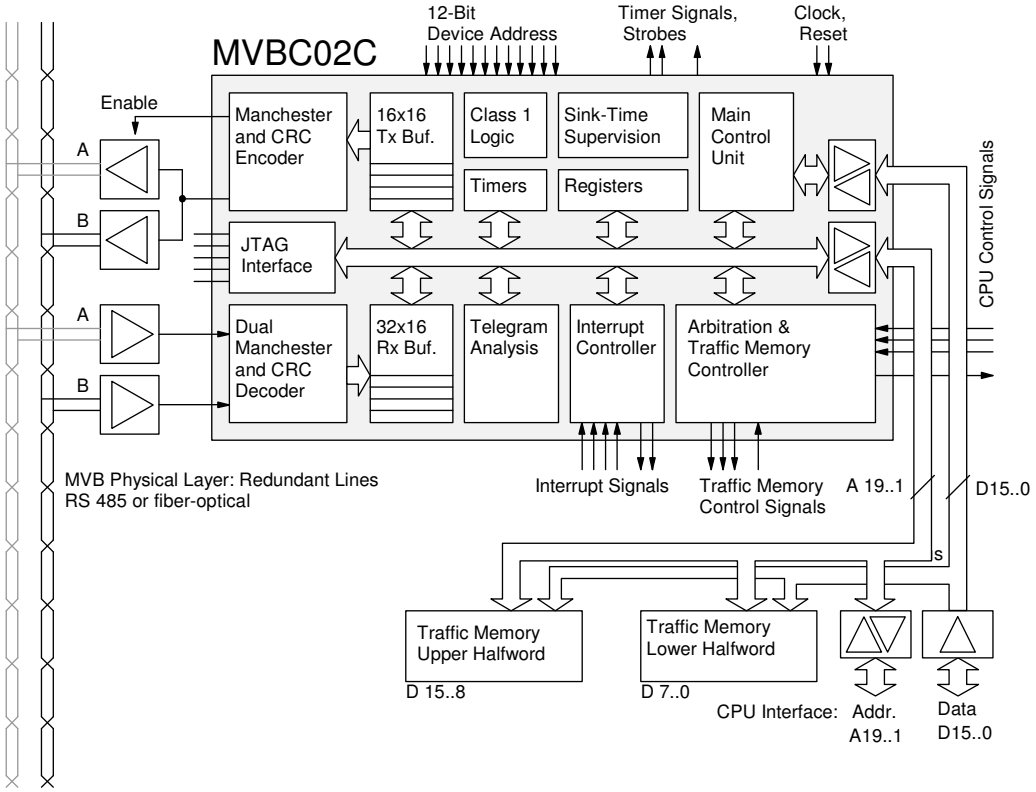

Figure 0.1: Block diagram with periphery

FEATURES

- Full Compliance with the IEC TCN Standard, Part 3: MVB [1]

  - Process Data (PD)
  - Message Data (MD)
  - Supervisory Data (Event Polling, Device Status Polls, Mastership Offer Polls)
  - Bus Administrator and monitoring functions

- Fully backward compatible to MVBC01, same footprint and pin assignment

- 0.5 µm CMOS ASIC
- Easy-to-use universal hardware interface
- 100 pin plastic quad flat pack (QFP)
- Supports computers without real-time capabilities

Communication:

- 1.5 Mbit/s data rate
- Signal Quality Checking
- Adjustable interframe spacing
- Fully Redundant Decoder (frame receiver)
- Powerful error and collision detection
- Full 16-bit support
- Max. 4095 ports for logical addressed telegrams
- Class 1 Mode: Support of 16 ports @ 1-16 word
- Automatic telegram analysis and evaluation
- Event Polling over two priorities
- Supports clocked transmitter outputs with resync. behind line opto couplers (avoiding line bit code distortion)
- Manchester Biphase-L coding
- Hamming Distance: 8
- Frame length supervision
- Extended Line Diagnosis / Error Counters per line
- Detection of permanent transmitters (jabber hold)
- 16 K - 1 M Byte Traffic Memory
- Max. 4095 ports for device addressed telegrams
- Automatic Message Queue handling
- Timeout mechanisms
- Device Address modifiable by software

Advanced Communication Functions:

- Bit-wise data forcing capabilities
- Automatic data Comparison mechanism
- Synchro port for synchronization and data strobing
- User-supplied Check Sequences

Master Functions:

- Transmission of individual Master Frames (MF)
- Timed MF transmission at precise intervals
- Autom. Transmission of max. 32 MFs from a table
- MF-tables are cascadable with *advance requests*

Testability:

- JTAG Boundary and Internal Scan
- On-Line test on Traffic Memory possible
- High degree of ad-hoc testability and observability
- Internal RAM cells isolatable for direct RAM tests

Miscellaneous:

- Two Universal Timers generating interrupts
- Sink-Time Supervision
- Intelligent Interrupt Logic, supports vectors
- 4 external interrupt inputs supported

- External High-Precision synchronization of one Universal Timer
- Synchronized MF Transmission over multiple MVBCs controlling multiple MVBs

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DEFINITIONS AND ABBREVIATIONS

All MVB-related terms are defined in [1]. Other terms can be referenced in the Index at the end of the document).

Not included:

Common computer science and electrical engineering terms;
names of external I/O pins; see section 1.3.2 instead;
timing parameters; see section 9 instead.

Abbreviations:

ACHG	Line A Level Changed (bit in DR)
ALO	Active Level Overbalance (bit in PCS)
ALVL	Current Signal Level Line A (bit in DR)
ATO	Allow Timeout (bit in DR)
AMFX	All Master Frames Transmitted (interrupt)
ARB*i*	Arbitration Strategy Selection bits (1..0; part of SCR)
BA	Bus Administrator
BAS	Bus Administrator Software
BCHG	Line B Level Changed (bit in DR)
BLVL	Current Signal Level Line B (bit in DR)
BNI	Bus Not Idle (bit in PCS)
BUSY	Busy Indicator (MCU busy handling telegrams, bit in MR)
BT	Bit Time for signals transfer (1 BT = 666 ns = 16 clock cycles)
BTI	Bus Timeout Interrupt
CM	Communication Mode (part of 1st word of Message Data)
CPE*i*	Clear Pending Event (0 or 1; part of PCS)
CRC	Cyclic Redundancy Error indicator (bit in PCS)
CS	Check Sequence (8-bit Cyclic Redundancy Check)
CSMF	Cancel Sending Master Frames (bit in MR)
DA	Device Address (12-bit value)
DAOK	Device Address Override Key (Register)
DAOR	Device Address Override Register
DEC	Disable / Enable Counter (part of PCS)
DGA	Device Group Address (12-bit value)
DMAD	DMA Direct (bit in MCR)
DMF	Duplicate Master Frame (interrupt)

DNR	Device Not Ready (bit in DSR)
DP	Data Pointer (queue data structure)
DPR	Dispatch Pointer Register
DPR2	Secondary Dispatch Pointer Register
DR	Decoder Register
DSF	Duplicate Slave Frame (interrupt)
DSR	Device Status Report (Slave Frame body for Device Status Poll)
DTI*i*	Data Transfer Interrupts (7..1)
EA*i*	Event Announced (0 or 1; bit in MR)
EC	Error Counter (Register)
ECA	Line Error Counter A (Register)
ECB	Line Error Counter B (Register)
EC*i*	Event Cancellation (0 or 1, bit in MR)
EF0	Event Frame Source Port for Event Type 0 (Physical Port)
EF1	Event Frame Source Port for Event Type 1 (Physical Port)
EFS	Event Frame Sink Port (Physical Port)
EM	Event Mode
EMF	Erroneous Master Frame (interrupt)
ESF	Erroneous Slave Frame (interrupt)
ERD	Extended Reply Time (bit in DSR)
ET	Event Type
F-Code	Function Code
FC	Frame Counter (Register)
FC8	Mastership Offer Source Port (Physical Port)
FC15	Device Status Port (Physical Port)
FD	Force Data Pattern (part of Force Table)
FE	Forcing Enabled (bit in PCS)
FEV	Frames Evaluated Interrupt
FM	Force Mask Pattern (part of Force Table)
FRC	Some data is forced (bit in DSR); related to data forcing
IAV	Interrupt Available (bit in IVR*i*)
ICD	Intercycle Delay (bit in MCR)
IE*i*	Input Enable (0..2, part of PCS)
IEC	International Electrotechnical Commission
IFS	Interframe Spacing (bit in TCR)
IL*i*	Initialization Level bits (1..0; part of SCR)
IM	Intel/Motorola Mode (bit in SCR)
IMR*i*	Interrupt Mask Register (0 or 1)
IPR*i*	Interrupt Pending Register (0 or 1)
IR	JTAG Instruction Register
ISR*i*	Interrupt Status Register (0 or 1)
IVR*i*	Interrupt Vector Register (0 or 1)
JTAG	IEEE 1149.1: Joint Test Action Group
LA	Logical Address (12-bit value)
LAA	Line A Active (bit in DR and DSR)
LD	Line Diagnosis (bit in SCR) enables extended reporting in PCS1
LLR	Linked List Record (queue data structure)
LS	Line Switchover (bit in DR)
LTE	Late Transmit Enable (bit in DR)
MBC	Message Broadcall (bit in SCR)
MCM	Memory Configuration Mode (part of MCR)
MCR	Memory Configuration Register
MCU	Main Control Unit (MVBC function block)
MD	Message Data
MF	Master Frame (communication packet)
MFC	Master Frame Checked (interrupt)
MFR	Master Frame Register
MFRE	Master Frame Register duplicated for Exceptions
MFS	Master Frame Slot (External Register)
MO*i*	Master Frame Table Offset (1..0, part of MCR)
MOS	Mastership Offer Sink Port (Physical Port)
MR	Master Register
MR2	Secondary Master Register
MSNK	Message Sink Port (Physical Port)
MSRC	Message Source Port (Physical Port)
MVB	Multifunction Vehicle Bus

NDH	No Delimiter Hunting (bit in DR)
NP	Next Pointer (queue data structure)
NUM	Numeric Data transferred (bit in PCS)
PAR*i*	Pending for Arbitration (0 or 1, bit in MR)
PCS	Port Control and Status Register (Set of 4 words per port)
PD	Process Data
PI	Port Index (retrieved value from PIT)
PIT	Port Index Table
PP	Physical Ports (inside Service Area)
PTD	Port temporarily disabled (bit in PCS)
QA	Queues attached (bit in PCS)
QDT	Queue Descriptor Table (External Registers)
QFPP	Quad Flat Package (chip package)
QO*i*	Queue Offset (1..0, part of MCR)
QUIET	Disable Encoder activity (bit in SCR)
RCEV	Receive Events (bit in SCR)
RLD	Redundant Line Disturbed (bit in DR and DSR)
RQ	Receive Queue
RQC	Receive Queue Complete (interrupt)
RQE	Receive Queue Exception (interrupt)
RS*i*	Reset Timer (1 or 2, part of TCR)
RTI	Reply Timeout Interrupt (typically 42.7 µs)
RXB	Receive Buffer (MVBC function block)
SCR	Status Control Register
SDD	Some Device Disturbance (bit in DSR)
SER	Service Reservation (bit in DSR)
SF	Slave Frame (communication packet)
SFC	Slave Frame Checked (interrupt)
SFR	Special Function Register
SI*i*	Sink-Time Supervision Interval (3..0, part of STSR)
SINK	Active Sink (bit in PCS)
SLM	Single Line Mode (bit in DR)
SMF*i*	Send Master Frame Command (bit in MR, MR2)
SMFA	Send Master Frames Automatically (code for SMF*i*)
SMFE	Send Empty Master Frame Table (code for SMF*i*)
SMFM	Send Master Frames Manually (bit in MR, MR2)
SMFT	Send Master Frames Timed (code for SMF*i*)
SQE	Signal Quality Error (bit in PCS)
SDD	Some Device Disturbance (bit in DSR)
SRC	Active Source (bit in PCS)
SSD	Some System Disturbance (bit in DSR)
STO	Slave Timeout (bit in PCS)
STSR	Sink-Time Supervision Register
TA*i*	Timer Active (1 or 2, part of TCR)
TACK	Transfer Acknowledge
TC*i*	Timer Counter Register (0 or 1)
TCN	Train Communication Network (IEC Standard)
TCR	Timer Control Register
TERR	Telegram Error (bit in PCS)
TI*i*	Timer Interrupt (1 or 2)
TM	Traffic Memory (in some documents also known as Traffic Store)
TMC	Traffic Memory Controller (MVBC function block)
TMO*i*	Timeout Selection bits (1..0; part of SCR)
TQC*i*	Transmit Queue Complete (0 or 1, interrupt)
TQE	Transmit Queue Exception (interrupt)
TR*i*	Timer Reload Register (0 or 1)
TRAFO	Physical line Mode Select (bit in DR)
TRP	Clocked Transmitter Output Mode (Control Bit in SFR)
TSNK	Test Sink Port (Physical Port)
TSRC	Test Source Port (Physical Port)
TURBO	Communication Speed Select (bit in DR)
TWCS	Transmit with Check Sequence (bit in PCS)
TXB	Transmission Buffer (MVBC function block)
UTQ	Use Test Source Ports (bit in SCR)
UTS	Use Test Sink Ports (bit in SCR)
VEC*i*	Interrupt Vector (3..0, bit in IVR*i*)

VP Valid Page (Page Pointer; bit in PCS)
WA Write Always (bit in PCS)
WS*i* Waitstate Selection bits (1..0; part of SCR)
WTR Wait Till Reply Timeout (bit in DR)
XI*i* External Interrupt (3..0)
XQ*i* Transmit Queue; *i* = 0 or 1
XSYN External Synchronization (bit in TCR)

Combinations of Abbreviations:

DA-PCS See DA, PCS
DA-PIT See DA, PIT
LA-FRC See LA, FRC
LA-PCS See LA, PCS
LA-PIT See LA, PIT
PP-PCS See PP, PCS

Definition of Terms:

Please refer to Appendix INDEX.

Conventions

Bit and Byte Order

Word:	Understood as a 16-bit word unless specified otherwise (i.e. "32-bit word")
Bit Order:	Bit 15 = Most significant bit (MSB)
	Bit 0 = Least significant bit (LSB)
Byte Order:	Two orders: Big Endian and Little Endian Format
Halfword:	Half part of a 16-bit word. Size: 1 byte.
Upper Halfword:	Bits 15..8 of a word (Numeric data: 215..28)
Lower Halfword:	Bits 7..0 of a word (Numeric data: 27..20)
Low Address Byte:	Byte inside word addressed with A0=0 (even addresses)
High Address Byte:	Byte inside word addressed with A0=1 (odd addresses)

Attention: Low (or High) Address Byte does not automatically imply Upper (or Lower) Halfword. This merely depends on the byte ordering scheme (Endian format) dictated by the supported host CPU or MCU.

Big Endian (i.e. Motorola 680x0s series):
Upper Halfword = Low Address Byte
Lower Halfword = High Address Byte

Little Endian (i.e. Intel 80x86 series):
Upper Halfword = High Address Byte
Lower Halfword = Low Address Byte

This document describes the behavior of the MVBC02C, however mostly the more general term “MVBC” is used as a synonym.

Register Stylistics

An example of a register description is shown below:

Generic Register (GR):

Brief Description: The Generic Register is not part of the MVBC. This name is used for this example only.

Generic Register (GR): Address 0yFFFFH

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	-												AB	CD	EF	GH
Init. Value:	All 0												1	0	0	0
CPU Acc.:	-												R	RW0	RW1	RW
MVBC Acc.:	-												rw	rw	rw	r

1st Row: Bit assignment. In the normal case, a separate table provides a detailed description for each bit. A lower-case "x" indicates an unused bit. This bit cannot be used for general-purpose data storage.

2nd Row: Indicates the initial values after power-up and/or asynchronous MVBC reset. If an 'x' is found on the 1st row, then the specified value will always be read out (permanently wired to '1' or '0'). Reading different values reflect a chip malfunction.

A notice "Initial Value: ..." may substitute this row.

3rd Row: Indicates access modes provided to the CPU (Upper-case symbols):

- Bit not existing or supported
R Read Access
R0 Read zero all time
R1 Read one all time
W Write Access
W0 Write access, only 0 affects register and/or system state (i.e. Reset)
W1 Write access, only 1 affects register and/or system state (i.e. Preset)

Combinations of the above are allowed.

A notice "CPU Access: ..." may substitute this row.

4th Row: Indicates access modes provided to the MVBC:
Possible symbols: -, r, r0, r1, w, w0, w1 and combinations of them
These lower-case symbols carry equivalent functions as the upper-case symbols found in the 3rd row.

A notice "MVBC Access: ..." may substitute this row.

1 MVBC OVERVIEW

1.1 Device Interface Symbol

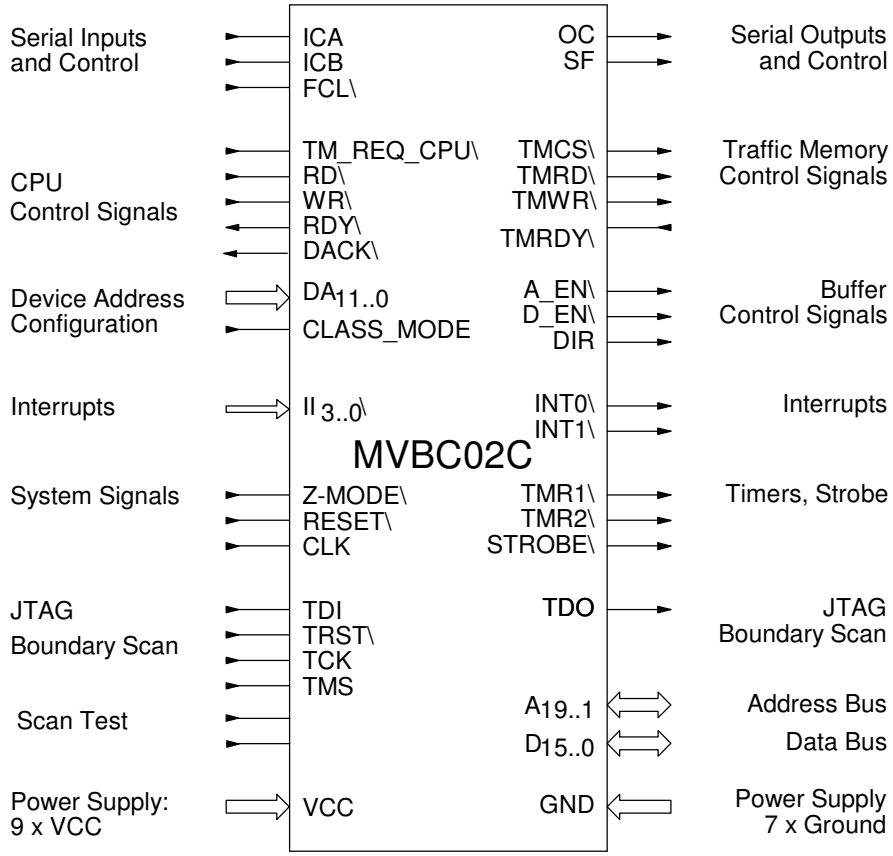

Figure 1.1: Device Interface Symbol

1.2 Systems Supported

The MVBC can either operate with a single host CPU or with assistance of a dedicated communication microprocessor to handle bus administration and upper level communication protocols. Class 1 mode allows autonomous operation without requiring a CPU or a microcontroller.

The functional characteristics of the MVBC can be modified via hardware configuration pins and via configuration registers that are set by software. The MVBC supports all device classes listed below:

- Class 1 Devices:
  - Simple slave boards without µP or µC (Actuators, Sensors)
  - No Traffic Memory
  - Slave boards with 8-bit or bigger µPs or µCs, with or without built-in I/O ports

- Class 2, Class 3 Devices:
  - Slave boards with 16-bit or bigger µPs or µCs
  - Minimum 16 K Bytes Traffic Memory
  - 8-bit µPs or µCs can be attached using external logic

- Class 4 Devices:
  - Boards with 16-bit µPs
  - Minimum 32 K Bytes Traffic Memory (Recommended: 256 K Bytes)
  - Capable to operate as a Bus Administrator

- Bus couplers, Gateways, etc.

1.3 Input / Output Pins

1.3.1 Pinout Diagram

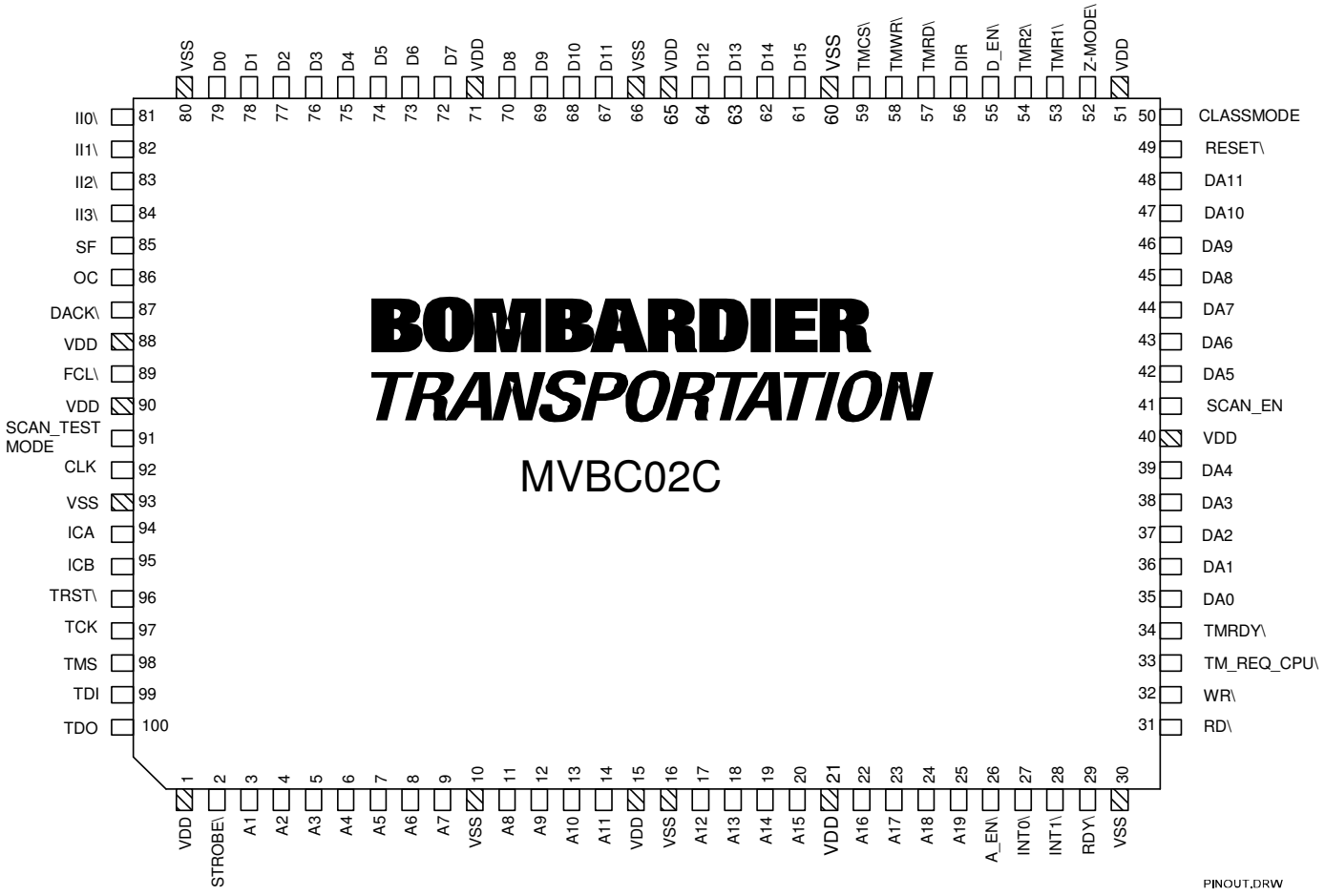

Figure 1.2: Pinout (Top View)

1.3.2 Pin Description

Pin number	Pin name / *Initial Level*	Dir. *Sense*	Description *Short summary*
61 - 79 [1]	$D_{15..0}$ *High Impedance*	I/O *Level*	Data Bus *The bidirectional lines are connected directly to the 16 data lines of the Traffic Memory and to the data transceivers which provide a link to the data bus of the host CPU.*
25 – 3 [1]	$A_{19..1}$ (see [2]) *High Impedance / High Level* [3]	I/O *Level*	Address Bus These lines address the Traffic Memory when the MVBC makes accesses. Also used as address inputs when CPU accesses MVBC or Traffic Memory.
35 - 48 [1]	$DA_{11..0}$ (see [2]) -	Input *Level*	Device Address Inputs *The Device Address input lines are directly connected the component that generates the Device Address bits (i.e. DIP switches). The DA must be valid during entire operation.*
31	RD\ -	Input *Level*	Read Signal from Host CPU *The CPU intends to perform a read-access from the TM or MVBC Internal Registers if both RD\ and TM_REQ_CPU\ are active.*
32	WR\ -	Input *Level*	Write Signal from Host CPU *The CPU intends to perform a write-access to the TM or MVBC Internal Registers if both WR\ and TM_REQ_CPU\ are active.*
33	TM_REQ_CPU\ -	Input *Level*	Traffic Memory or MVBC Request from Host CPU (Chip Select) *By activating this signal the CPU requests that it wishes to access the TM or registers*
29	RDY\ *Low*	Output -	MVBC Ready Signal to Host CPU *indicates that the data bus $D_{15..0}$ contains valid data.*
57	TMRD\ *High*	Output -	MVBC Read Signal to Traffic Memory *TMRD\ is used together with TMCS\ to perform read-accesses from the TM.*
58	TMWR\ *High*	Output -	MVBC Write Signal to Traffic Memory *TMRD\ is used together with TMCS\ to perform write-accesses to the TM.*
59	TMCS\ *High*	Output -	MVBC Chip-Select Signal to Traffic Memory *TMCS\ is used in combination with TMRD\ or TMWR\ to access the TM.*
34	TMRDY\ -	Input *Level*	Traffic Memory Ready Signal to MVBC *It is used to delay accesses made by/via MVBC to TM.*
87	DACK\ *High*	Output -	Data acknowledged. *It is used to acknowledge accesses made by CPU to MVBC / TM ("Motorola – like")*
26	A_EN\ *High*	Output -	Traffic Memory Address Buffer Enable *Enables the address buffer that is used to isolate the CPU from the Traffic Memory. Attention: A_EN may be at '0' if the MVBC is started up with TM_REQ_CPU_N='0'.*
55	D_EN\ *High*	Output -	Traffic Memory Data Transceiver Enable *Enables the data transceiver that is used to isolate the CPU from the TM.*
56	DIR *High*	Output -	CPU <-> MVBC/TM Data Flow Direction 0 = From CPU to MVBC/Traffic Memory 1 = From MVBC/Traffic Memory to CPU
2	STROBE\ *High*	Output -	Strobe Signal *Active for 3 clock cycles (125 ns) if a write access is made to the Synchro Port.*
92	CLK -	Input ↑ *Edge*	24 MHz Master Clock Input *Do not use any different frequencies since they change data rate and timeouts on the MVB.*
49	RESET\ -	Input *Level*	Asynchronous Reset *Initializes the MVBC to a known reset condition.*
50	CLASS_MODE	Input *Level*	Specifies Class Mode the MVBC must operate in *0 = Class 1 Device 1 = Class 2/3/4 Device*
53, 54	TMR1\,2\ *High* internal pullup 50k	Output / Input-	Universal Timer 1 and 2 Outputs (when CLASS_MODE = 1) *Active for 3 clock cycle (125 ns) when respective counter reaches zero.* Selector input for interframe spacing (when CLASS_MODE = 0)
81 - 84	$II_{0..3}$\ (see [2]) -	Input *See* [4]	External Interrupt Inputs (when CLASS_MODE = 1) *These inputs can be used to collect external interrupt sources and process them in the MVBC along with the internal interrupts.* Selector input for Waitstates and Reply Timeout Coefficient (when CLASS_MODE = 0)
27	INT0\ *High*	Output -	Interrupt Output *Each Interrupt output covers up to 16 different interrupt sources.*
28	INT1\ *High* internal pullup 50k	Output -Input	Interrupt Output (when CLASS_MODE = 1) *Each Interrupt output covers up to 16 different interrupt sources.* Self clocked transmitter output selection (when CLASS_MODE = 0)

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Pin number	**Pin name** / ***Initial Level***	**Dir.** ***Sense***	**Description** ***Short summary***
94	ICA -	Input *Level*	MVB Input Data Channel A *MVB format input data from physical layer MVB receiver*
95	ICB -	Input *Level*	MVB Input Data Channel B *MVB format input data from physical layer MVB receiver*
86	OC *Low*	Output -	MVB Output Data Channel *MVB format output data to physical layer transmitter*
85	SF *Low*	Output -	Send Frame *Indicates that a telegram is being sent via OC. This signal is available to enable physical layer drivers.*
89	FCL\ -	Input *Level*	Force Constant Light *Active FCL\ forces OC high. Used for fiber optical line strength calibration.*
52	Z-MODE\ internal pullup	Input *Level*	High-Impedance Mode *Allows all outputs to be switched to high Impedance to allow for easy in-circuit testing.*
96	TRST\ internal pullup	Input *Level*	Test Reset (JTAG Pin) *Must be active at power up to initialize JTAG Boundary Scan Hardware, similar as RESET\.*
97	TCK internal pullup	Input ↑ *Edge*	Test Clock (JTAG Pin)
98	TMS internal pullup	Input *Level*	Test Mode Select (JTAG Pin)
99	TDI internal pullup	Input *Level*	Test Data In (JTAG Pin)
100	TDO *High*	Output -	Test Data Out (JTAG Pin)
41	SCAN_EN	Input *Level*	Scan enable, only for test *Must be connected to VSS in normal operation!*
91	SCAN_TEST_MODE -	Input *Level*	Scan Test Mode, only for test *Must be connected to VSS in normal operation!*
1, 15, 21, 40, 51, 65, 71, 88, 90	VDD -	Power -	+ 3.3 … 5 V Supply Pins
10, 16, 30, 60, 66, 80, 93	VSS	Power -	Ground Pins

[1] These pin number range specifies where these signals can be found. Other pins (i.e. control signals, VDD, VSS) may lie inbetween. Check the pinout diagram for detailed pin assignment information.

[2] Different signal assignments apply when the MVBC operates in Class 1 Mode (CLASS_MODE input is at '0'). See section 5.4.4 for details.

[3] Wherever two initial values are given and separated with the slash character '/', the left value denotes to Class 2/3/4 Mode, the right value to Class 1 Mode.

[4] The interrupt is triggered after the transition from '1' to '0'. Before the transition, the signal must have been at '1' for at least 1 clock cycle (41.7 ns). After the transition, the signal must remain stable for at least one clock cycle again.

Table 1.1: Pin Description

1.4 Physical Layer Interface to the MVB

The physical layer interface suits to both copper twisted pair medium and fiber optical medium. The MVBC provides one common output (OC) and two redundant inputs (ICA, ICB). The transmitted and received signals are active high:

High	=	VDD
Low	=	0 V

The SF-signal must be used to enable the drivers. This signal is activated 125 ns before the beginning and 125 ns after the end of every frame. This time overhead assures correct data transmissions by preventing undesired transients at the frame boundaries.

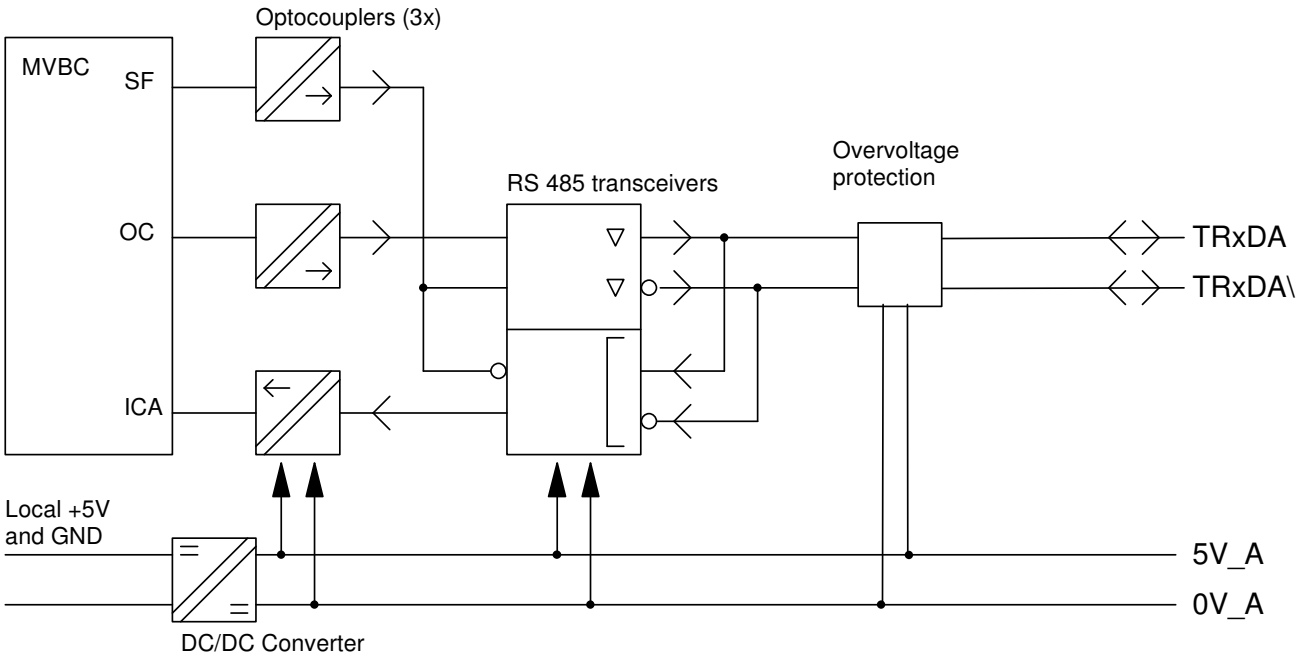


Figure 1.3: Physical layer interface to copper medium (ESDB, line A shown for example)

For timing behaviour of OC, SF signals please refer to encoder description, section 3.2, page 45.

1.5 Physical Interface to the Traffic Memory and CPU

1.5.1 Physical Interconnection to Traffic Memory

The TM access control signals are organized in order to connect static RAM chips directly. Support logic is necessary when more complex memory structures (i.e. DRAMs) are chosen.

The TMRDY\-Signal must be tied to '0' if the Traffic Memory can return data within a definite time period. In this case, the number of wait states must be configured inside the MVBC.

Buffers and bi-directional transceivers must be used to isolate the MVBC address and data buses from the main CPU address and data buses. The following figure illustrate the basic interconnection between the MVBC, TM and host CPU.

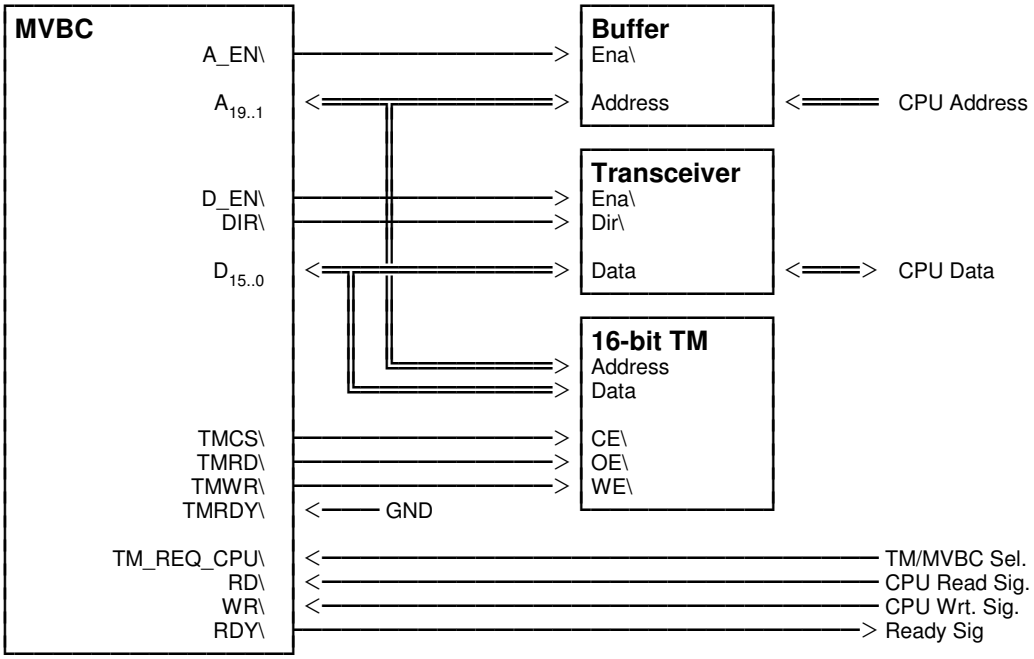


Figure 1.4: Simple CPU / MVBC / TM Interconnection Diagram

1.5.2 Physical Interface to host CPU

The MVBC handles all host CPU accesses made to the Traffic Memory or Internal Registers in the MVBC. The CPU control signals (TM_REQ_CPU\, RD\, WR\) are connected directly to the MVBC. The MVBC takes care of arbitration if both CPU and MVBC intend to access the Traffic Memory simultaneously.

In addition, the two interrupt request signals (INT0\, INT1\) must be connected directly or via an interrupt controller to the CPU.

1.5.3 Word and Byte Access Restrictions

The MVBC supports 16-bit Traffic Memory architectures. No explicitly 8-bit accesses will be performed. However, custom glue logic can be introduced to support 8-bit read and write accesses.

1.5.4 Byte Order

The Byte Order issue must be considered carefully. Consider following cases: Motorola (Big Endian format) and Intel (Little Endian format). The left column in the following figure describes non-numeric data (character strings, stored in memory with incrementing address order). The right column describes numeric data (upper halfword contains obviously the more significant digits) words. The processors write the data (and as well the Force Mask and Force Data) into the Traffic Memory using their native Endian formats:

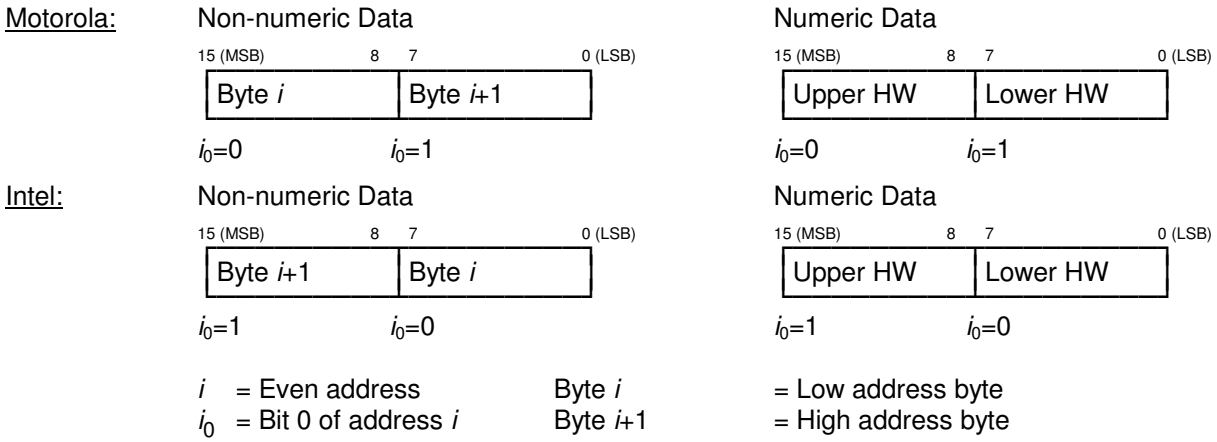


Figure 1.5: Data Format inside Traffic Memory

The MVBC will load these words from Traffic Memory (or internal Receive Buffer) to the internal Transmit Buffer (or Traffic Memory) without performing any byte swaps. However, the following order is required when transferring numeric and non-numeric data over the MVB:

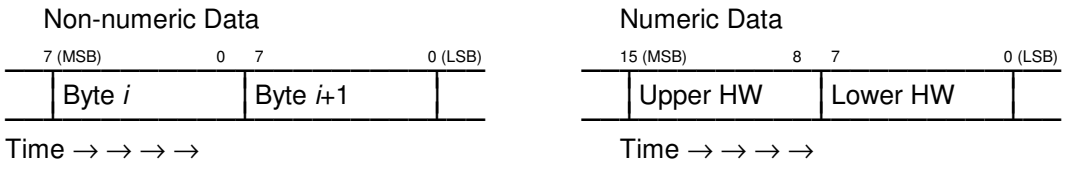


Figure 1.6: Data Format on the MVB

Since the MVBC transmits 16-bit words starting with the most significant bit first, no problems arise when transmitting numeric data. In addition, no problem should occur when transmitting non-numeric data if the host processor uses Big Endian format (like the Motorola 680x0 series). A byte swap is necessary when transmitting non-numeric data while the host processor operates with Little Endian format (like the Intel 80x86 series).

Approach: The MVBC shall be informed whether to perform a byte swap or not. First, an Intel/Motorola bit (IM in SCR, see section 3.4.7) is available to enable byte swapping. If the MVBC operates in "Intel" mode, byte swapping is permitted (does not mean "enabled"). Otherwise, "Motorola" allows no swapping at all. Byte swapping is performed only if the data to be transferred is declared as "non-numeric data" (See PCS, section 2.3.1).

In the normal case, all data being transferred are considered as numeric data except messages (see section 0). Word order for 32-bit or bigger numbers is not handled by the MVBC. The software shall assure that the upper 16-bit word is stored at address *i* and the lower 16-bit word at address *i*+2 (*i* = an even address).

Attention: In class '1' mode, all data being transferred is considered as numeric data. No byte swapping will take place at all. If 8-bit data are exchanged (i.e. between MVBC and an A/D-converter), the user shall make a decision himself whether to use the upper or lower eight bits and declare the respective data as numeric or non-numeric in MVBCs of the other bus participants.

1.5.5 Class 1 Mode Addressing

While the MVBC operates in Class 1 Mode, the addressing range is limited to sixteen 16-bit locations. Sixteen bits ($A_{15..1}$ and A_{16}) of the address bus are decoded into active-low *chip-select* signals. The remaining three bits will stay at '1' permanently. Details about operation in Class 1 Mode are given in section 5.

2 TRAFFIC MEMORY ORGANIZATION

All information and data pertaining to the MVBC are found in the Traffic Memory address space. This space is visible to both host CPU and MVBC. The Traffic Memory is divided into following partitions:

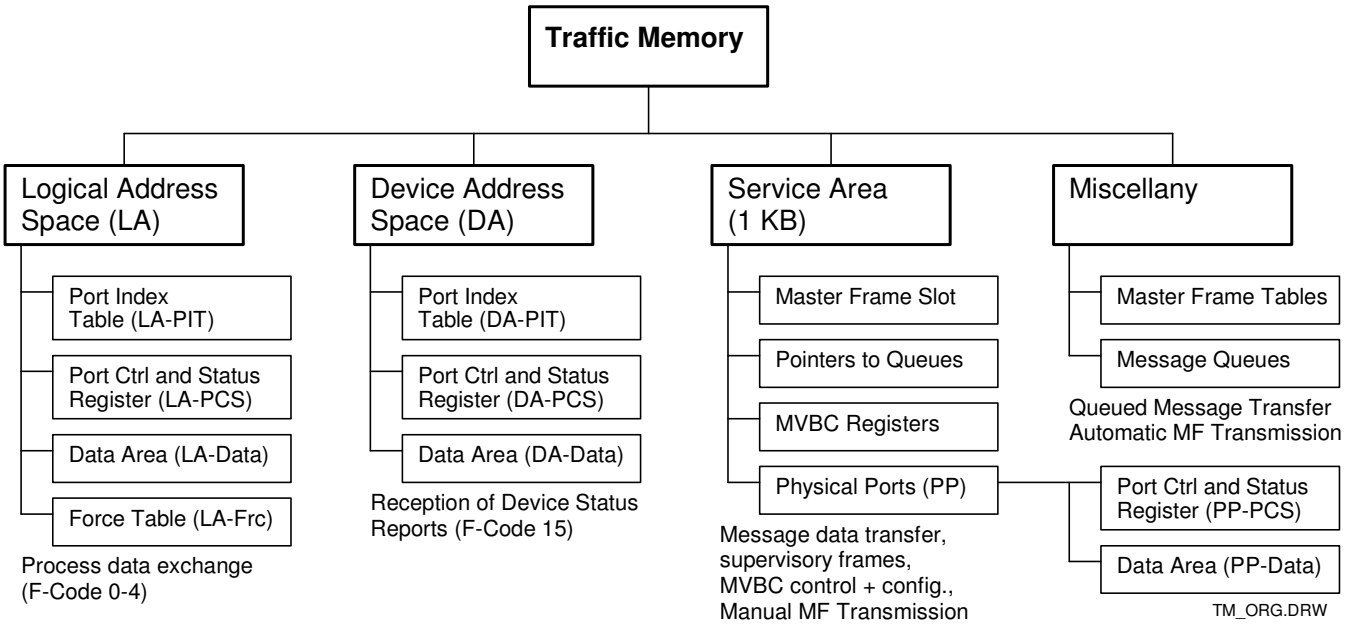


Figure 2.1: TM Organization

Depending on the hardware application, the user may consider to choose a Traffic Memory with a specific size. In order to utilize the Traffic Memory efficiently, five Memory Configuration Modes (MCM) have been introduced.

MCM	TM Size	LA Ports	DA Ports	Unused	Service Area (address range)
Class 1	-	16	0	-	No Service Area
0	16 KB	256	0	1 KB	03C00H - 0x03FFFH
1	32 KB	256	256	7 KB	07C00H - 0x07FFFH
2	64 KB	1024	256	1 KB	0FC00H - 0x0FFFFH
3	256 KB	4096	2048	31 KB	0FC00H - 0x0FFFFH
4	1 M	4096	4096	751 KB	0FC00H - 0x0FFFFH
4 (see [1])	256 KB	4096	3008	8 KB	0FC00H - 0x0FFFFH

[1] MCM=4 operating with 256 KB TM: The DA Data Area at location 40000H-50000H maps into 00000H-100000H. In order to avoid overlapping into the Port Index Tables and Service Area, the range is limited to 47 KB (04000H-0FC00H). Consequently, only 3008 DA ports can be supported. The vacant 8 KB region originates from the PCS space due to 1088 unused ports.

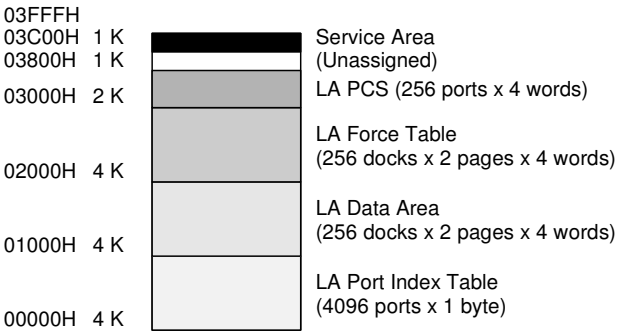
Table 2.1: Memory Configuration Modes (MCM)

2.1 Traffic Memory Maps

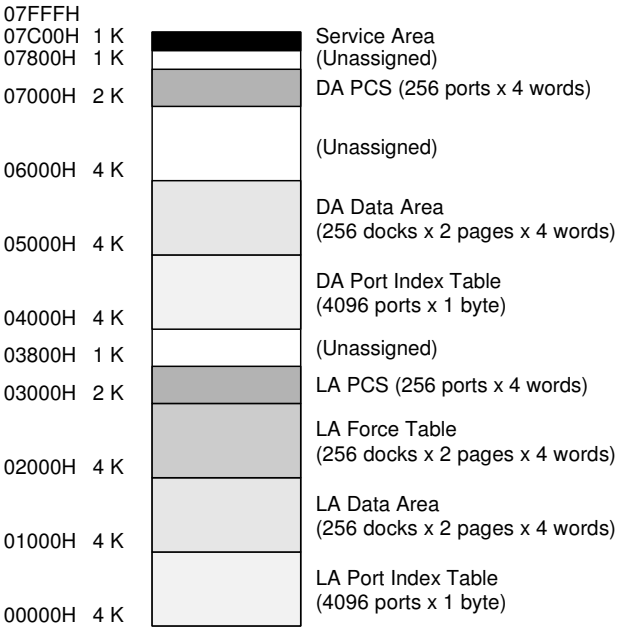
The following pages illustrate the Traffic Memory Maps for all Memory Configuration Modes. All *unused* memory fragments can be used for data structures which are not bound to any specific location: Message Queues and Master Frame Tables. Despite this, the MVBC is capable to address 1 MB memory independent of used MCM.

Mode 0 is effective after power-up or an asynchronous or synchronous reset has been issued, given the MVBC does not operate in class 1 mode. The start address to the Service Area is 03C00H. Mode 0 supports no device-addressable ports which are necessary to receive Device Status Reports.

Memory Configuration Mode 0 (16 KB)



Memory Configuration Mode 1 (32 KB)



Memory Configuration Mode 2 (64 KB)

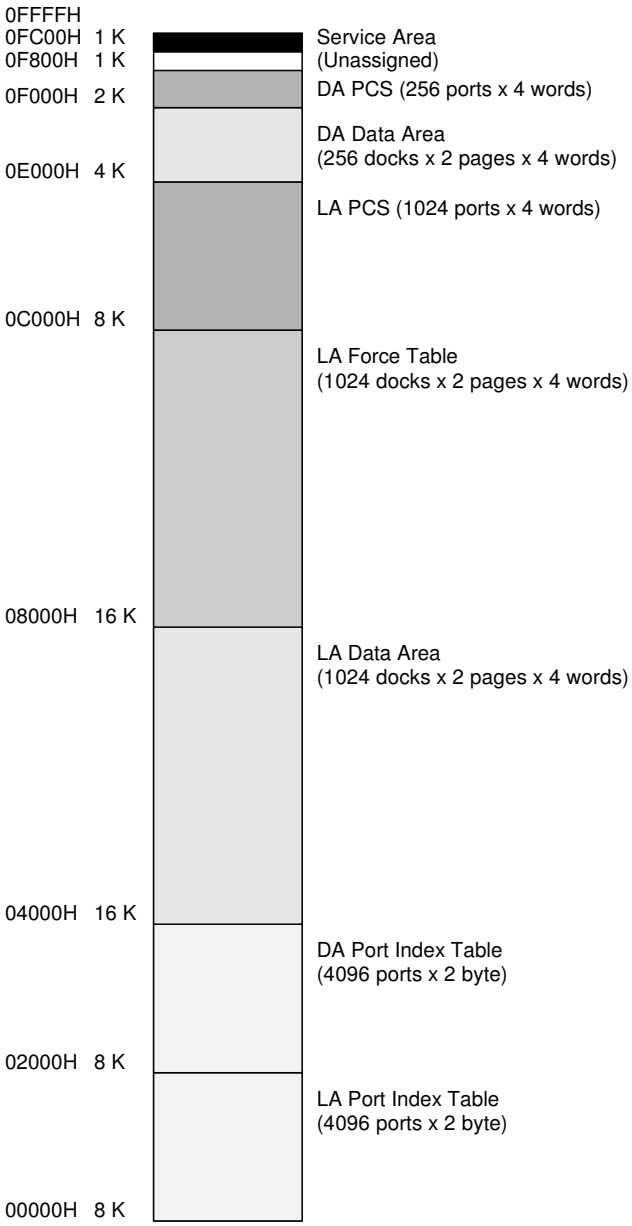
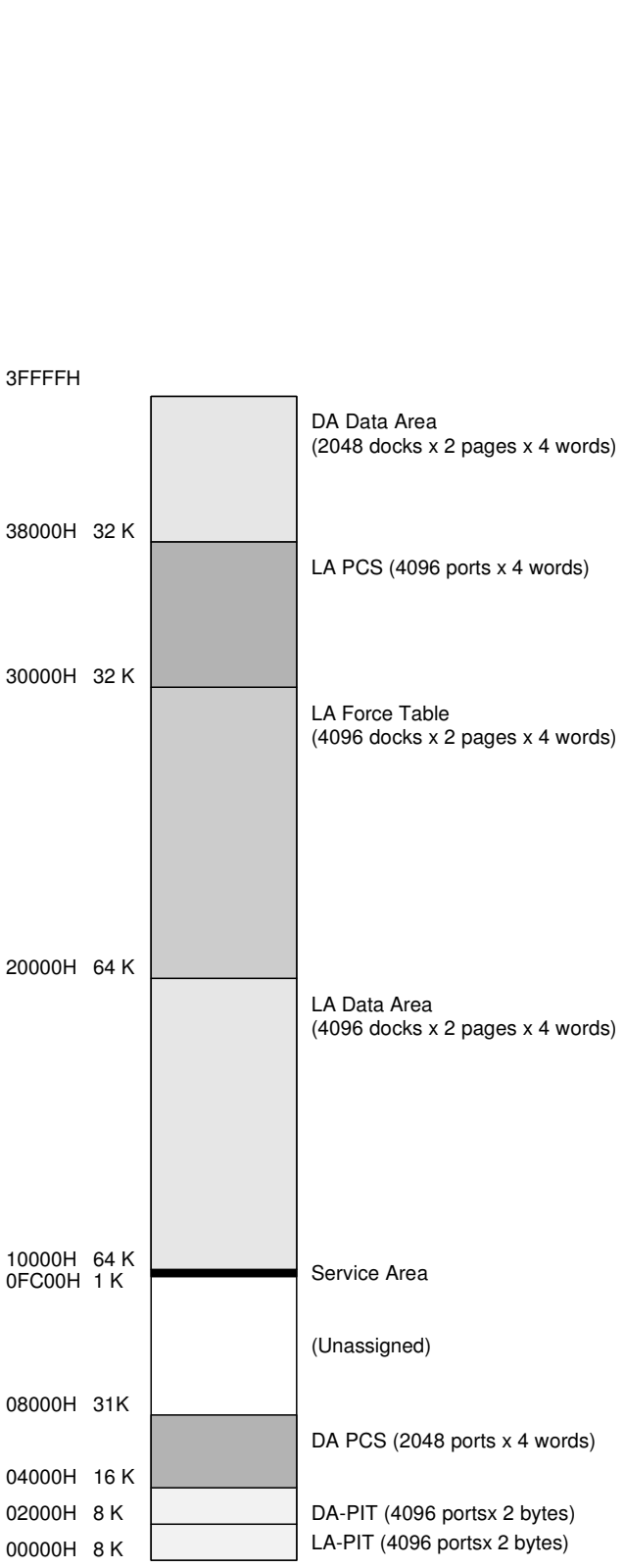


Table 2.2: Traffic Memory Maps (continued on next page)

Memory Configuration Mode 3 (256 KB)



Memory Configuration Mode 4 (1 MB)

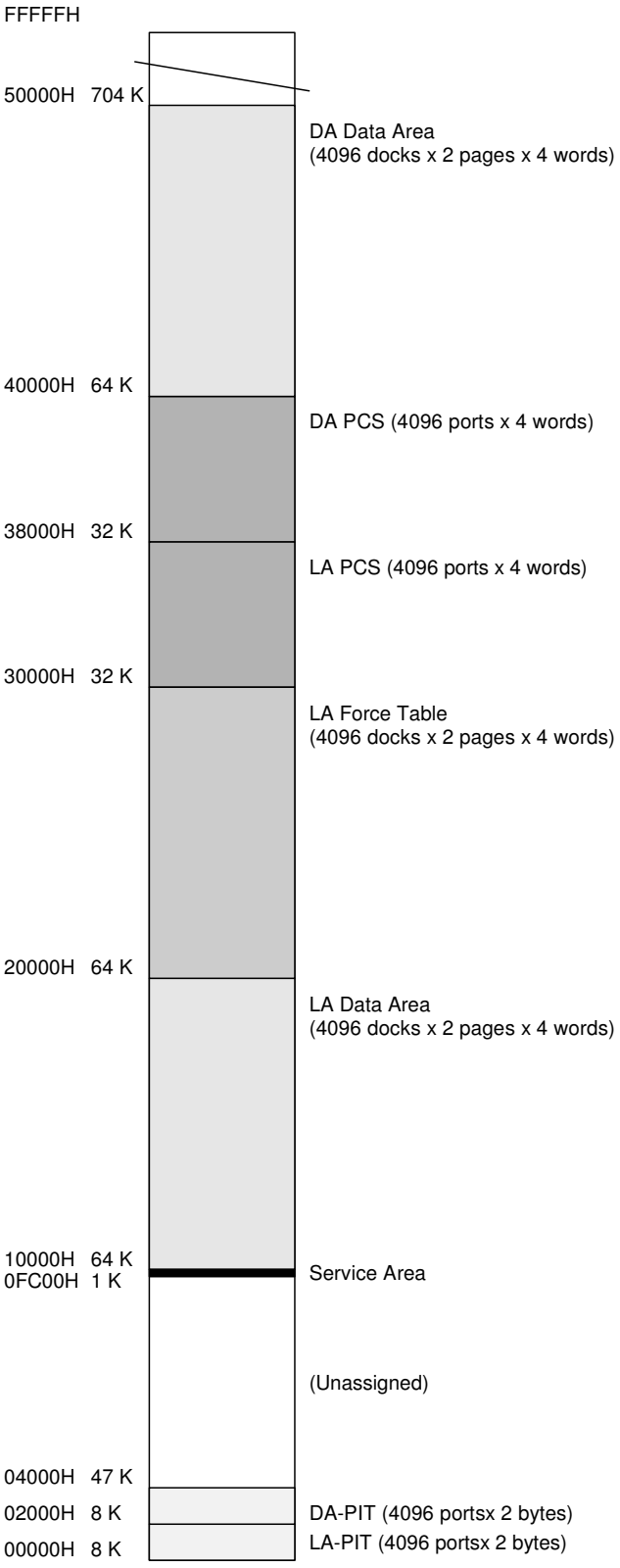


Table 2.4: Traffic Memory Maps (continued)

2.2 Data Area Ports, Addressing Mechanism using Port Index Tables (PIT)

The Traffic Memory provides two Port Index Tables, one for

- Logical Addressed Data (Used for Process Data)
- Device Addressed Data (Used to receive Device Status Reports)

The Port Index Tables link the Ports to the Logical and Device Addresses which are specified in the Master Frames. Port Index PI=000_{hex} is used to assign all unused Logical and Device Addresses.

- If the Memory Configuration Mode (MCM) is zero, then no device addressable Port Index Table and Ports exists.

- If MCM={0,1}, every 16-bit word in the Port Index Table contains two 8-bit Port Indexes. The low address bytes contain even numbered Port Indexes, accordingly the high address bytes contain odd numbered Port Indexes. Since the native byte order of the host CPU is used, the MVBC must be informed about the selected byte order (see SCR, IM-bit, section 3.4.7).

PIT Word Format for MCM ≤ 1:

Motorola Mode:

15 … 8	7 … 0
Port 4094 :	Port 4095 :
Port 0	Port 1

Intel Mode:

15 … 8	7 … 0
Port 4095 :	Port 4094 :
Port 1	Port 0

Figure 2.2: PIT Organization, MCM ≤ 1

If MCM={2,3,4}, then every 16-bit word contains one 12-bit Port Index, covering bits 11..0. Bits 15..12 must be zero.

Start Address:	LA-PIT:	00000H	for all MCM
	DA-PIT:	04000H	if MCM = 1
		02000H	if MCM ≥ 2

2.2.1 Address Evaluation from Port Index

The Port Index is used to compute the effective TM addresses to the following memory blocks:

- PCS
- Data Area
- Force Table (For logical address space only)

Figure 2.3 on the next page shows the algorithm which is used to compute the effective TM addresses.

Address Evaluation Example:

Consider an MF containing 0234H (F-Code=0, Port Address = 234H). The MCM is set to 2 (64 KB Traffic Memory). First, the TM address 0468EH is evaluated from the Port Address to read the Port Index Table (PIT). Assume, the Port Index contains 00FH. The resulting addresses are computed as follows:

Addr(PCS) = Start_addr(PCS) + (00F shl 3) = 0C000 + 078 = 0C078

Map(PI=00F, VP=0) = 00D8H; Map(PI=00F, VP=1) = 00F8H

Addr(Data_Area, VP=0) = 04000H + 00D8H = 040D8H
Addr(Data_Area, VP=1) = 04000H + 00F8H = 040F8H
Addr(Force_Table, Data pattern: VP=0) = 080D8H
Addr(Force_Table, Mask pattern: VP=1) = 080F8H

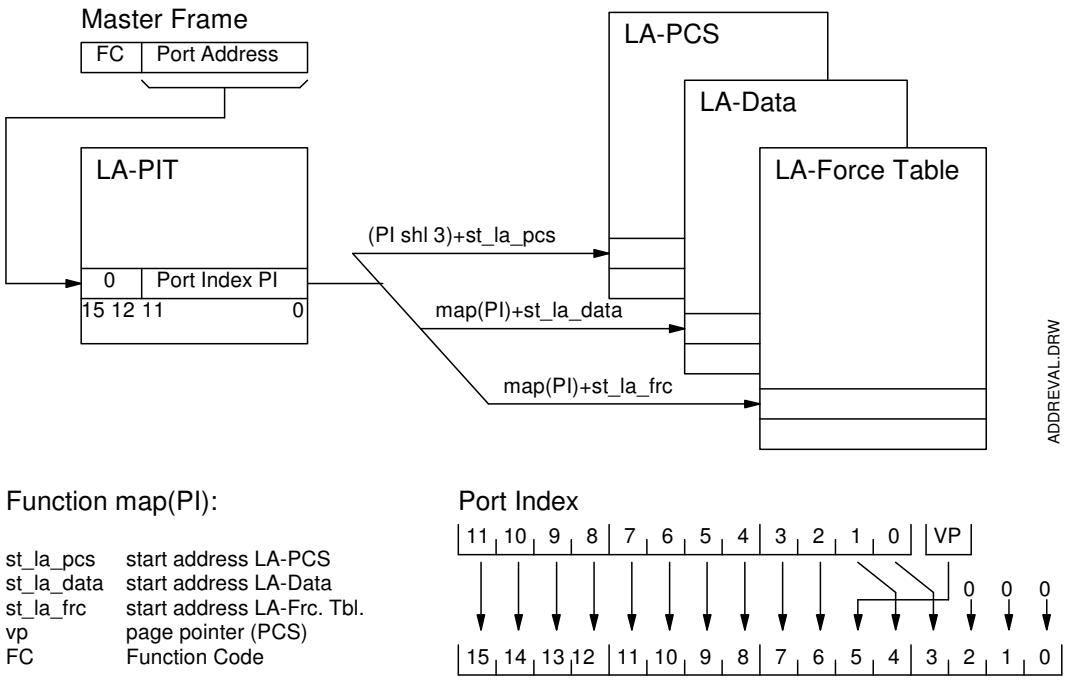


Figure 2.3: Address Evaluation from Port Index

2.3 Port Control and Status Register (PCS)

The Port Control and Status Register contains all the relevant information pertaining to one port. This information is used by MVBC to determine how it should handle the related port. The PCS includes following information in a four-word record:

- Port-related information
  - Function Code
  - Port description (source vs sink port, queuing and forcing en-/disabled)
  - Specifications of interrupts to occur when transfer has completed
  - Event arbitration
- Data consistency check
  - Valid Page pointer
  - Port Disabling mechanism (used to support host systems which do not comply with any real-time requirements)
- Telegram report
  - Indicates type of communication error or timeout occurred
    This may be selected in a standard mode (as with MVBC01) or in an extended line diagnosis mode (if the according bit LD is set in the SCR register
- Transfer acknowledge bits
  - Acknowledges successful data transfer
  - Intended for sink-time supervision
- Check Sequences
  - Used if data is transferred with software-defined Check Sequences

Each PCS is a four-word record:

PCS Word 0:	PCS0	Port Description
PCS Word 1:	PCS1	Telegram Report, Valid Page Pointer, Port Disabling Mechanism
PCS Word 2:	PCS2	Transfer Acknowledge Bits
PCS Word 3:	PCS3	Check Sequences

2.3.1 PCS Word 0: Port Description

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	$F\text{-}Code_{3..0}$				SRC	SINK	TWCS	WA	$IE_{2..0}$			$CPE_{1..0}$		QA	NUM	FE
Init. Value:	This location in the Traffic Memory must be initialized by the host software															
CPU Acc.:	Read and write access															
MVBC Acc.:	Read-only															

The MVBC accesses this port every time after a Master Frame has been received and an appropriate port has been selected.

Symbol	Description
$F\text{-}Code_{3..0}$	Function Code (F-Code) The MVBC compares the F-Code in the PCS with the F-Code received in the Master Frame. If they are identical, then further actions are taken. Otherwise, the frame is ignored and no further action is taken. Description of F-Codes: See appendix A Exception: The F-Code is not checked during event arbitration. Reason: The ports EF0, EF1 and EFS (See appendix A) must be accessible with three different F-Codes: 9, 13 and 14. A value of 9 is suggested.
SRC	Port is active Source 0 Port is passive source 1 Port is active source (regardless if SINK=0 or 1)
SINK	Port is active Sink 0 Port is passive sink 1 Port is active sink (provided that SRC=0)
TWCS	TWCS Transfer with Check Sequence 1 Transfers data with 8-bit Check Sequence between the Traffic Memory and the MVBC. The Check Sequence is loaded/stored in word 3 of the PCS. For transferring queued Message Data: The Check Sequences are not queued. They are handled in the same manner as for any regular data transfer.
WA	Write Always 0 Received Slave Frames with errors will not be written into the Data Area of the TM (or appended to the Message Queue if F-Code=12). VP remains unaffected. This mechanism prevents sink ports from becoming contaminated with erroneous data. 1 All correct Slave Frames, as well as erroneous Slave Frames where no frame size discrepancy has been detected will be stored in the Traffic Memory. This type of erroneous data is known as recoverable data. Erroneous data with mismatching frame size (i.e. due to an signal loss) will not be stored. This feature may be useful for bridges which do intentionally forward erroneous frames (using false CRCs with TWCS=1).

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Symbol	Description
$IE_{2..0}$	Enable Interrupts A general-purpose Data Transfer Interrupt (DTIi) is generated upon successful (no errors, or recoverable data after an error given WA-bit is set) processing of the port. If an error is detected, then no interrupt is asserted because no data transaction is made to the port. The software developer is free to use these interrupts for his application needs. 0 0 0 No interrupt is generated 0 0 1 DTI1 is asserted (see also section 3.7.2) 0 1 0 DTI2 is asserted 0 1 1 DTI3 is asserted 1 0 0 DTI4 is asserted 1 0 1 DTI5 is asserted 1 1 0 DTI6 is asserted 1 1 1 DTI7 is asserted (If DTI7 is enabled and the port is a sink, then an Automatic Comparison Mechanism is enabled. No interrupt occurs if the port is configured as a source. See section 4.8.4 for details.)
$CPE_{1..0}$	Clear Pending Event of Type 1, or 0 1 The announced event of type ET = 1 or 0 is cleared upon any data transfer using this port by setting EAi and PARi (see SCR, section 3.4.7) to zero. These bits are used for event arbitration and event data transfers, regardless if the transfer turned out successfully or not. Exception: If the QA-bit (see below) is active, then EAi will be cleared only if no more messages are left in the queue.
QA	Queue Attached to Port 1 Message Queues are attached. If SINK=1, the Receive Queue is attached. If SRC=1 and SINK=0, the Transmit Queues are attached. Transmit Queue 0 will be checked before Transmit Queue 1. 0 No queue is attached. All data transfers are made with Data Area (inside Traffic Memory) instead. This bit applies for message transfers only (F-Code=12). However, the user is required to keep this bit at zero in PCS with other F-Codes.
NUM	NUM Numeric Data 1 The port contains 16-bit or longer numeric data. This information is required in order to transmit numeric data in the correct byte sequence (see section 1.5.4). 0 The port contains non-numeric data (i.e. character sequences, messages) NUM has no effect if the MVBC is running in Motorola-Mode (see section 1.5.4), but the user is strongly recommended to declare numeric data anyway. Reason: The byte ordering is correct for both numeric and non-numeric data. Attention: The MVBC handles byte order of 16-bit words only. It does not handle word order of 32-bit or larger words.
FE	Data Forcing Enabled 0 Data Forcing is disabled. The MVBC does not access the Force Table. 1 Forcing is enabled. Access to Force Mask and Data Area are made before transmission or reception of every Process Data word. Attention: Forcing requires two additional TM accesses for each data word.

Table 2.3: PCS Word 0: Port Description

2.3.2 PCS Word 1: Telegram Report, Page Pointer

This register contains different information depending on state of the “Extended Line Diagnosis” bit LD in the Status and Control Register (SCR, refer to section 3.4.7).

- In standard mode (equivalent to MVBC01, LD = 0)), only line diagnosis of active line is reported (bit LAA of decoder register DR is pointing to; see DR, section 3.3.5). The Port Temporarily Disable – feature is supported.
- In the Extended Line Diagnosis mode, telegram report of both, the active line and the redundant line, is stored in PCS1. Therefore, no Port Temporarily Disable – mechanism is supported.

2.3.2.1 PCS Word 1: No Extended Line Diagnosis

This word is updated every time a data transfer has taken place (both successful or erroneous), or a Reply Timeout has occurred (default value: 42.7 µs). This word is not updated if a Master Frame has been received while expecting a Slave Frame, or if the port is inactive. The six error bits CRC through STO are not cumulative. If the next data transfer was successful, then all of these bits return to '0'.

Bit Number	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	$DEC_{7..0}$								PTD	VP	CRC	SQE	ALO	BNI	TERR	STO
Init. Value:	This location in the Traffic Memory must be initialized by the host software															
CPU Acc.:	Read and write access															
MVBC Acc.:	Read-only								rw	rw	w	w	w	w	w	w

Symbol	**Description**
$DEC_{7..0}$	Disable / Enable Counter. See 3.9.2. This counter is used in association with the PTD (Port Temporarily Disabled) bit to disable data reception in order to allow host computers, which do not fulfill real-time requirements, to retrieve data from this port. = 0 The port remains active according to the information’s given in PCS Word 0. Whenever the MVBC writes PCS Word 1 back to the Traffic Memory, PTD will be set to '0' if this is not yet done so. > 0 The port will disable automatically after the next transfer. Whenever the MVBC writes PCS Word 2 back to the Traffic Memory, PTD will be set to '1'.
PTD	Port Temporarily Disabled. See 4.8.2 0 The port is enabled. The MVBC will set PTD to '0' if it detects a zero Disable/Enable Counter. 1 The port is disabled Attention: PTD applies to sink ports (SINK=1, SRC=0) only. It is ignored when the port is used as a source.
VP	Valid Page Pointer The Page Pointer indicates which page of the Traffic Memory data section is active. This pointer is used to maintain data consistency. If the port is active source (SRC='1', SINK=don't care): The MVBC reads data from the page pointed to by VP. The MVBC does not change the value of VP, but attention to the note at the end of this section 2.3.2! The host must write data to the page not pointed to by VP. After data has been written, the host must invert VP in order to make new data visible to the MVBC.

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VP (continuing)	If the port is active sink (SRC='0', SINK='1'): The host reads data from the page pointed to by VP. The host must not change the value of VP. The MVBC writes all incoming data to the page not pointed to by VP. After all words of the telegram have been written, the MVB inverts VP in order to make the new data visible to the host. Attention: VP is not inverted if erroneous data has been received and the MVBC will therefore not store the received data. Exceptions apply when the WA-bit is active. See WA-bit in PCS Word 0.
CRC	Mismatching Check Sequence 1 Frame with mismatching CRC has been detected. If WA=1, and the port is a sink, then the erroneous frame is written to the Traffic Memory. If this bit is active, then TERR will also be active.
SQE	Signal Quality Error 1 Bad signal quality has been detected. This bit is enabled by the Decoder Unit (see 3.3) if the double-sampling on the incoming line gives different results. If this bit is active, then TERR will also be active.
ALO	Active Level Overbalance, commonly found when collisions have occurred. 1 This signal is active if four or more signal-transitions have occurred on the transmission line (starting reception from idle). ALO is not set to '1' after successful data transfers.
BNI	Bus not Idle 1 This signal is active if seven or more signal-transitions have occurred on the transmission line (starting reception from idle). BNI is affected when port is active source or active sink. Exception: BNI is not set to '1' after successful data transfers. If this bit is active, then TERR and/or STO will also be active.
TERR	Telegram Error Bit 1 Frame error has been detected. This bit can only become active if a valid Master or Slave Delimiter has been received and missing or garbled data follows. The following error types can set this bit to '1': ▪ Mismatching CRC (CRC bit will also be active) ▪ Bad Manchester bit ▪ Signal quality error (SQE bit will also be active) ▪ Frame length error ▪ Active Level Overbalance (ALO bit will also be active) TERR is affected when port is active source or active sink.
STO	Slave Frame Reply Timeout If no valid Slave Delimiter (SD) is received within reply time (default value: 42.7 µs) of receiving a valid Master Delimiter (MD), this timeout bit is set.

Table 2.4: PCS Word 1: Telegram Status, Page Pointer (no Extended Line Diagnosis)

2.3.2.2 PCS Word 1: Extended Line Quality Reporting

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	-	LR	OCRC	OSQE	OALO	OBNI	OTERR	OSTO	-	VP	CRC	SQE	ALO	BNI	TERR	STO
Init. Value:	This location in the Traffic Memory must be initialized by the host software															
CPU Acc.:	Read and write access															
MVBC Acc.:	w0	rw	w	w	w	w	w	w	w0	rw	w	w	w	w	w	w

This word is updated every time a data transfer has taken place (both successful or erroneous), or a Reply Timeout has occurred. This word is not updated if a Master Frame has been received while expecting a Slave Frame, or if the port is inactive. The twelve error bits CRC through STO, OCRC through OSTO are not cumulative. They are updated after each data transfer to this port.

The flags STO, TERR, BNI, ALO, SQE, CRC are reporting line reception status of the “active line”, to which the LAA – bit in the decoder register is pointing to while OSTO, OTERR, OBNI, OALO, OSQE, OCRC are referring to the line reception status of the “other” line (the redundant line, the LAA – bit of decoder register not pointing to).

Symbol	Description
LR	Line Reception Points to line from which slave frame has been taken. 1 Slave frame has been received on line A. Bits 5 … 0 relate to line A, bits 13 … 8 relate to line B (the observed line) 0 Slave frame has been received on line B. Bits 5 … 0 relate to line B, bits 13 … 8 relate to line A (the observed line)
OCRC	same as CRC, but reported for the “other” (redundant) line
OSQE	same as SQE, but reported for the “other” (redundant) line
OALO	same as ALO, but reported for the “other” (redundant) line
OBNI	same as BNI, but reported for the “other” (redundant) line
OTERR	same as TERR, but reported for the “other” (redundant)”) line
OSTO	same as STO, but reported for the “other” (redundant) line
VP	Valid Page Pointer The Page Pointer indicates which page of the Traffic Memory data section is active. This pointer is used to maintain data consistency. If the port is active source (SRC='1', SINK=don't care): The MVBC reads data from the page pointed to by VP. The MVBC does not change the value of VP, but attention to the note at the end of this section 2.3.2! The host must write data to the page VP not pointing to. After data has been written, the host must invert VP in order to make new data visible to the MVBC. If the port is active sink (SRC='0', SINK='1'): The host reads data from the page pointed to by VP. The host must not change the value of VP. The MVBC writes all incoming data to the page VP not pointing to. After all words of the telegram have been written, the MVB inverts VP in order to make the new data visible to the host. Attention: VP is not inverted if erroneous data has been received and the MVBC will therefore not store the received data. Exceptions apply when the WA-bit is active. See WA-bit in PCS Word 0.
CRC	Mismatching Check Sequence 1 Frame with mismatching CRC has been detected. If WA=1, and the port is a sink, then the erroneous frame is written to the Traffic Memory. If this bit is active, then TERR will also be active.

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Symbol	Description
SQE	Signal Quality Error 1 Bad signal quality has been detected. This bit is enabled by the Decoder Unit (see 3.3) if the double-sampling on the incoming line gives different results. If this bit is active, then TERR will also be active.
ALO	Active Level Overbalance, commonly found when collisions have occurred. 1 This signal is active if four or more signal-transitions have occurred on the transmission line (starting reception from idle). ALO is not set to '1' after successful data transfers.
BNI	Bus not Idle 1 This signal is active if seven or more signal-transitions have occurred on the transmission line (starting reception from idle). BNI is affected when port is active source or active sink. Exception: BNI is not set to '1' after successful data transfers. If this bit is active, then TERR and/or STO will also be active.
TERR	Telegram Error Bit 1 Frame error has been detected. This bit can only become active if a valid Master or Slave Delimiter has been received and missing or garbled data follows. The following error types can set this bit to '1': ▪ Mismatching CRC (CRC bit will also be active) ▪ Bad Manchester bit ▪ Signal quality error (SQE bit will also be active) ▪ Frame length error ▪ Active Level Overbalance (ALO bit will also be active) TERR is affected when port is active source or active sink.
STO	Slave Frame Reply Timeout If no valid Slave Delimiter (SD) is received on active line within reply time (default value: 42.7 µs) of receiving a valid Master Delimiter (MD), the timeout bit is set.

Table 2.5: PCS Word 1: Telegram Status, Page Pointer (Extended Line Quality Reporting)

Attention: Since MVBC updates also status of an active source port (where it is not allowed to modify the page pointer VP), it reads PCS word 1 prior to writing updated status with same VP value. Since this MVBC access is not a locked read - modify - write – access, it can happen, that CPU modifies the PCS word 1 value in between, and MVBC restores the old value when writing updated status.
Application has to care checking the VP value of an active source port after modifying it, if it is not accidentally restored by MVBC, or writing the PCS word 1 value a second time (of course MVBC status update is lost then). MVBC write access takes typically four CLK-cycles (+ wait states + TM not ready states), refer to timing diagram Figure 9.7.

2.3.3 PCS Word 2: Transfer Acknowledge Bits

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	$TACK_{15..0}$															
Init. Value:	This location in the Traffic Memory must be initialized by the host software															
CPU Acc.:	Read and write access															
MVBC Acc.:	Read and write access															

This word is updated every time data has been transferred from the MVBC to Traffic Memory or vice versa.

The Transfer Acknowledge bits $TACK_{15..0}$ will be set after a valid transfer from the MVBC to the TM or in the other direction. The complete word is set to FFFFH when this transfer is complete. The software or the Sink-Time Supervision Logic on the MVBC (see section 3.9) can decrement this counter in order to perform sink time supervision. TACK is not affected when the port is inactive.

Table 2.6: PCS Word 2: TACK Bits

2.3.4 PCS Word 3: Check Sequences

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	$CS1_{7..0}$								$CS0_{7..0}$							
Init. Value:	This location in the Traffic Memory must be initialized by the host software															
CPU Acc.:	Read and write access															
MVBC Acc.:	Read-only (source ports) or write access (sink ports)															

Symbol	Description
$CS0_{7..0}$, $CS1_{7..0}$	8-bit Check Sequence for data page 0 (CS0) and for page 1 (CS1) If TWCS (Transfer with Check Sequence) equals '1', then the Check Sequence (CS) corresponding to the data stored in pages 0 and 1 located in the Data Area are stored in CS0 and CS1 respectively. The page is pointed to by VP. If the frame size exceeds 4 words so that multiple Check Sequence are required (up to 4), the other Check Sequence pairs are found in the corresponding PCS word 3 of the next higher (unused) port addresses. The following examples illustrates CS-storage for a 16-word PD variable:

Dock Nr.	Addr.	Contents	Usage
	i+1EH	PCS Word 3	CRC's for words 12-15
	i+1CH	PCS Word 2	(not used)
	i+1AH	PCS Word 1	(not used)
Dock 3	i+18H	PCS Word 0	(not used)
	i+16H	PCS Word 3	CRC's for words 8-11
	i+14H	PCS Word 2	(not used)
	i+12H	PCS Word 1	(not used)
Dock 2	i+10H	PCS Word 0	(not used)
	i+0EH	PCS Word 3	CRC's for words 4-7
	i+0CH	PCS Word 2	(not used)
	i+0AH	PCS Word 1	(not used)
Dock 1	i+08H	PCS Word 0	(not used)
	i+06H	PCS Word 3	CRC's for words 0-3
	i+04H	PCS Word 2	TACK Bits
	i+02H	PCS Word 1	Telegram Status, VP, etc
Dock 0	i+00H	PCS Word 0	Port Description

Table 2.7: PCS Word 3: Check Sequences

2.4 Data Areas

The Data Areas contain the data to be transmitted to or received from the MVB. Data Areas are available for logical addressed ports, device addressed ports and Physical Ports (located inside Service Area). The Data Area provides memory space for a specified number of docks. 2 pages of 4 words are assigned to each dock. For 1, 2 and 4-word telegrams, one dock is assigned to one port. For 8 and 16-word telegrams, two (or four) docks are grouped into one port. The page is pointed to by the VP bit in the PCS.

Address	**1 / 2 / 4 words:** **1 Dock / Port**	**8 words:** **2 Docks / Port**	**16 words:** **4 Docks / Port**
+38H ... +3FH	Port i+3, Page 1	(Dock 3)	(Dock 3)
+30H ... +37H	Port i+2, Page 1	Port i+2, Page 1	(Dock 2)
+28H ... +2FH	Port i+1, Page 1	(Dock 1)	(Dock 1)
+20H ... +27H	Port i+0, Page 1	Port i+0, Page 1	Port i+0, Page 1
+18H ... +1FH	Port i+3, Page 0	(Dock 3)	(Dock 3)
+10H ... +17H	Port i+2, Page 0	Port i+2, Page 0	(Dock 2)
+08H ... +0FH	Port i+1, Page 0	(Dock 1)	(Dock 1)
+00H ... +07H	Port i+0, Page 0	Port i+0, Page 0	Port i+0, Page 0

Table 2.8: TM Data Area

2.5 Force Table

The Force Table is used to override transmitted or received Process Data with forced data. The Force Table consists of two parts: Force Data bit pattern (FD) and Force Mask bit pattern (FM). The Force Data Pattern contains the data image (similar format as in a single page inside the Data Area entry) which will be partly or entirely used when forcing is enabled (See FE-bit inside PCS).

Attention: Forcing is not allowed on Message Data and Supervisory Data.

For every active Force Mask Bit ('1'), the corresponding bit to be transmitted or received is obtained from the local Force Data word. For every passive Force Mask Bit ('0'), the corresponding bit to be transmitted is obtained from the selected page (pointed to by VP in PCS) in the Data Area. For data reception: If the corresponding Force Mask Bit is '0', then the data bit is obtained from the MVB.

Data-to-xmit = (DT[VP] & not FM) or (FD & FM)
Data-to-rcve = (MVB & not FM) or (FD & FM)

DT Data Area, pointed to by Page Pointer VP

MVB Current word retrieved from MVB

The organization of the Force Table is similar to that of the Data Area. 4 words are assigned to each dock. For 1, 2 and 4-word telegrams, one dock is assigned to one port. For 8 and 16-word telegrams, two (or four) docks are grouped into one port. The page is pointed to by the VP bit in the PCS. See table on next page.

Address	1 / 2 / 4 words: 1 Dock / Port	8 words: 2 Docks / Port	16 words: 4 Docks / Port
+38H ... +3FH	Port i+3, Mask	(Dock 3)	(Dock 3)
+30H ... +37H	Port i+2, Mask	Port i+2, Mask	(Dock 2)
+28H ... +2FH	Port i+1, Mask	(Dock 1)	(Dock 1)
+20H ... +27H	Port i+0, Mask	Port i+0, Mask	Port i+0, Mask
+18H ... +1FH	Port i+3, Data	(Dock 3)	(Dock 3)
+10H ... +17H	Port i+2, Data	Port i+2, Data	(Dock 2)
+08H ... +0FH	Port i+1, Data	(Dock 1)	(Dock 1)
+00H ... +07H	Port i+0, Data	Port i+0, Data	Port i+0, Data

Table 2.9: TM Force Table

Attention: Activating TWCS (in PCS Word 0) and FE when the port is used as a sink makes no sense. In this case, the received Check Sequence will no longer match with the data written into Traffic Memory.

2.6 Service Area

Depending on the selected Memory Configuration Mode MCM, the Service Area can take one of the following address spaces:

MCM = 0	03C00H - 03FFFH	(16 K Traffic Memory)
MCM = 1	07C00H - 07FFFH	(32 K Traffic Memory)
MCM = 2 / 3 / 4	0FC00H - 0FFFFH	(64 K / 256 K / 1 M Traffic Memory)

Attention: For improved clarity, the addresses to the Service Area are referred with 0yC00H - 0yFFFH where 'y' stands for 3, 7 or F (hex) respectively.

The Service Area is divided into following sections:

- Physical Ports (PP)
  - Port Control and Status Registers
  - Data Area
- MVBC External Registers
  - Master Frame Slot to send individual Master Frames
  - Queue Descriptor Table
- MVBC Internal Registers
  - Physically located inside the MVBC.

The following table specifies two addresses. Address 03xxxH applies if MCM=0 (y=3), otherwise 0FxxxH applies (y=F).

Address	Size	Description	Comments
0yFFFH			
0yF80H	128 Bytes	MVBC: Max. 32 internal regs.	Located inside MVBC (32-bit word-aligned)
0yF00H	128 Bytes	MVBC: Max. 32 external regs.	Located in Traffic Memory (16-bit word-aligned)
0yE00H	256 Bytes	Physical Ports: PP-PCS	32 ports x 4 words (16 of them are in use)
0yC00H	512 Bytes	Physical Ports: PP-Data	32 ports x 4 words (16 of them are in use)

Table 2.10: Service Area

2.6.1 Physical Ports

The following table summarizes the available Physical Ports:

Port	F-Code	Direction	Description
FC8	8	Source	Mastership Offer Source Port This port is used to send 1-word Mastership Offer Frames.
MOS	8	Sink	Mastership Offer Sink Port This port is used to receive 1-word Mastership Offer Frames.
EF0	9, 13, 14	Source	Event Frame Source Port for Event Type 0 This port is used to send 1-word Event Frames if Event Type ET=0 is specified in the incoming Master Frame.
EF1	9, 13, 14	Source	Event Frame Source Port for Event Type 1 This port is used to send 1-word Event Frames if Event Type ET=1 is specified in the incoming Master Frame.
EFS	9, 13, 14	Sink	Event Frame Sink Port This port is used to receive 1-word Event Frames
FC15	15	Source	Device Status Port This port is used to send 1-word Device Status Reports.
MSRC	12	Source	Message Source Port This port is used to transmit Message Data. If queuing is enabled, then the Message Queue will be used instead of the MSRC Data Area.
MSNK	12	Sink	Message Sink Port This port is used to receive Message Data. If queuing is enabled, then the Message Queue will be used instead of the MSRC Data Area.

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Port	F-Code	Direction	Description
TSRC	any	Source	Test Source Port This port is used instead of any other port as the source if the UTQ-bit is set (see SCR, section 3.4.7). This port shall be used for internal loop-back tests only. Attention: Memory location of MSRC and TSCR are the same.
TSNK	any	Sink	Test Sink Port This port is used instead of any other port as the sink if the UTS-bit is set (see SCR, section 3.4.7). This port shall be used for internal loop-back tests only. Attention: Memory location of MSNK and TSNK are the same.

Table 2.11: Physical Ports: Description

2.6.1.1 Physical Ports, PCS Table

Address	Contents
0yE7FH	
	Message Sink Port / Test Sink Port (MSNK / TSNK) (size: 16 words; covers 4 docks)
0yE60H	
	Message Source Port / Test Source Port (MSRC / TSRC) (size: 16 words; covers 4 docks)
0yE40H	
0yE38H	Device Status Port (FC15)
0yE30H	Mastership Offer Sink Port (MOS)
0yE28H	Event Frame 1 Source Port (EF1)
0yE20H	Event Frame 0 Source Port (EF0)
0yE18H	(Reserved)
0yE10H	(Reserved)
0yE08H	Event Frame Sink Port (EFS)
0yE00H	Mastership Offer Source Port (FC8)

Table 2.12: Physical Ports: PCS

Attention: Locations 0yE80H-0yEFFH are reserved for future use.

Attention: The Test Ports TSRC and TSNK overlay the Message Ports MSRC and MSNK. For clarity reasons, separate names are maintained throughout this document.

2.6.1.2 Physical Ports, Data Area

The Data Area of the Physical Ports is organized similarly as the data for logical addressed and device addressed ports. A similar memory assignment as found in the other Data Area is used.

Address	Contents
0yCFFH	
	Message Sink Port / Test Sink Port (MSNK / TSNK) Page 1 (size: 16 words; covers 4 docks)
0yCE0H	
	Message Sink Port / Test Sink Port (MSNK / TSNK) Page 0 (size: 16 words; covers 4 docks)
0yCC0H	
	Message Source Port / Test Source Port (MSRC / TSRC) Page 1 (size: 16 words; covers 4 docks)
0yCA0H	
	Message Source Port / Test Source Port (MSRC / TSRC) Page 0 (size: 16 words; covers 4 docks)
0yC80H	
0yC78H	Device Status Port (FC15), Page 1
0yC70H	Mastership Offer Sink Port (MOS), Page 1
0yC68H	Event Frame 1 Source Pt. (EF1), Page 1
0yC60H	Event Frame 0 Source Pt. (EF0), Page 1
0yC58H	Device Status Port (FC15), Page 0
0yC50H	Mastership Offer Sink Port (MOS), Page 0
0yC48H	Event Frame 1 Source Pt. (EF1), Page 0
0yC40H	Event Frame 0 Source Pt. (EF0), Page 0
0yC38H	(Reserved)
0yC30H	(Reserved)
0yC28H	Event Frame Sink Port (EFS), Page 1
0yC20H	Mastership Offer Source Pt. (FC8), Page 1
0yC18H	(Reserved)
0yC10H	(Reserved)
0yC08H	Event Frame Sink Port (EFS), Page 0
0yC00H	Mastership Offer Source Pt. (FC8), Page 0

Table 2.13: Physical Ports: Data Area

Attention: Locations 0yD00H-0yDFFH are reserved for future use.

Attention: The Test Ports TSRC and TSNK are equivalent to the Message Ports MSRC and MSNK. For clarity reasons, separate names are maintained throughout this document.

2.6.2 MVBC External Registers

The External Registers are located in the Traffic Memory and are accessed by both CPU and MVBC:

Name	Description	Symbol	Address
Master Frame Slot	Used for outgoing Master Frames	MFS	0yF00H
Queue Descriptor Table (QDT), see 2.7.1.1	Pointer to Transmit Queue 0 Pointer to Transmit Queue 1 Pointer to Receive Queue	QDT[0] QDT[1] QDT[2]	0yF10H 0yF12H 0yF14H

Table 2.14: External Registers

MFS: The Master Frame is a 16-bit word which consists of an F-Code (4 bits) and an address (12 bits).

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	F-Code$_{3..0}$				Address $_{11 ...0}$											

Attention: The remaining locations 0yF02H … 0yF0FH, 0yF16H … 0yFFFH are not used.
They are reserved for future use and shall not be used as general-purpose data storage.

2.6.3 MVBC Internal Registers

The register addresses are 32-bit word aligned in order to simply operating with 32-bit processors.

MVBC Functional Unit	Register Name	Symbol	Address	Section
Status Control Register	Status Control Register	SCR	0yF80H	3.4.7
Address Logic	Memory Configuration Register	MCR	0xF84H	3.6.1
Decoder	Decoder Register	DR	0yF88H	3.3.5
Sink-Time Supervision	Sink-Time Supervision Register	STSR	0yF8CH	3.9.1
Telegram Analysis Unit	Frame Counter Error Counter Master Frame Register Master Frame Reg. Duplicate Exception	FC EC MFR MFRE	0yF90H 0yF94H 0yF98H 0yF9CH	3.4.5 3.4.5 3.4.4 3.4.4
Main Control Unit	Master Register Secondary Master Register Dispatch Pointer Register Secondary Dispatch Pointer Register	MR MR2 DPR DPR2	0yFA0H 0yFA4H 0yFA8H 0yFACH	3.5.1 3.5.1 3.5.3 3.5.3
Interrupt Logic	Interrupt Pending Register 0 Interrupt Pending Register 1 Interrupt Mask Register 0 Interrupt Mask Register 1 Interrupt Status Register 0 Interrupt Status Register 1 Interrupt Vector Register 0 Interrupt Vector Register 1	IPR0 IPR1 IMR0 IMR1 ISR0 ISR1 IVR0 IVR1	0yFB0H 0yFB4H 0yFB8H 0yFBCH 0yFC0H 0yFC4H 0yFC8H 0yFCCH	3.7.3 3.7.4 3.7.5 3.7.6
Line Error Counters	Error Counter Line A Error Counter Line B	ECA ECB	0yFD0H 0yFD4H	3.4.8
Device Address	Device Address Override Register Device Address Override Key	DAOR DAOK	0yFD8H 0yFDCH	3.5.5.1
Special Function	Special Function Register	SFR	0yFE4H	3.2.5

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Universal Timer	Timer Control Register Timer Reload Register 1 Timer Reload Register 2 Timer Counter Register 1 Timer Counter Register 2	TCR TR1 TR2 TC1 TC2	0yFE0H 0yFF0H 0yFF4H 0yFF8H 0yFFCH	3.8.1

Table 2.15: Internal Registers

Attention: The remaining addresses 0yFE8H, 0yFECH are reserved for future use.

Attention: For register access, the MVBC will not decode address bits 0 and 1. Therefore, the same register is accessed without any word realignment if address 0yXXXXH, 0yXXXXH+1, 0yXXXXH+2 or 0yXXXXH+3 is used.

Example: A CPU attempt to access a 32-bit word from address 0yFFCH where the host-side logic splits it into two 16-bit accesses will automatically lead to fitting the 16-bit counter value twice into the 32-bit word.

2.7 Miscellany Memory Space

2.7.1 Message Queues

The MVBC supports three Message Queues: two Transmit Queues with different priorities and one Receive Queue. The queues are organized as linked lists and may be located in any unused region in the Traffic Memory.

The Message Queues are used when the QA-bit in the PCS is active. The SRC and SINK-bits indicate whether the Transmit or Receive Queues are used. The following table summarizes the queue assignment:

SINK	SRC	QA	Description
X	X	0	No queue attached (set and reset by user only)
1	0	1	Receive Queue attached
X	1	1	Transmit Queues attached. Queue 0 (high priority) is always checked before queue 1 (low priority). Queue 1 is serviced only if queue 0 is empty or nonexistent.

Table 2.16: Conditions to Select Message Queues

Attention: High and low priority queues have nothing in common with the priorities related to different Event Types used in Event Arbitration.

If both QA and TWCS bits are active in the PCS, then the Check Sequences will still be read or written to their usual locations, namely PCS Word 3.

2.7.1.1 Queue Descriptor Table (QDT)

All three queues are accessible via the Queue Descriptor Table (QDT). The QDT lies in the Service Area of the Traffic Memory (Address 0yF10H, 0yF12H, 0yF14H) and contains the pointers to all three queues. A zero pointer indicates a *nonexistent queue*.

2.7.1.2 Queue Address Evaluation

The 19-bit (No A_0) address to the Traffic Memory is computed from any 16-bit queue pointer by shifting it 2 bits to the left and adding an offset (Valid offset values: 00000H, 40000H, 80000H or C0000H). The Queue Offset ($QO_{1..0}$) is defined in the Memory Configuration Register. Hence, the QDT, LLR and queue data blocks must be located within a selected 256 K block.

2.7.1.3 Linked List Records (LLR)

The pointer from the QDT points to the first Linked List Record (LLR) . Each LLR consists of two 16-bit pointers: Data Pointer (DP) and Next Pointer (NP). The DP points to a 16-word message block. This data structure allows packet generation without physical data movement as long the data is already stored in the Traffic Memory. The NP points to the next LLR. *End of queue* is indicated with DP=NULL and NP=*Don't Care*. An *empty queue* consists of one LLR with DP = NULL. The following Figure 2.4 illustrates the data structure. DP must be aligned to 16-word blocks.

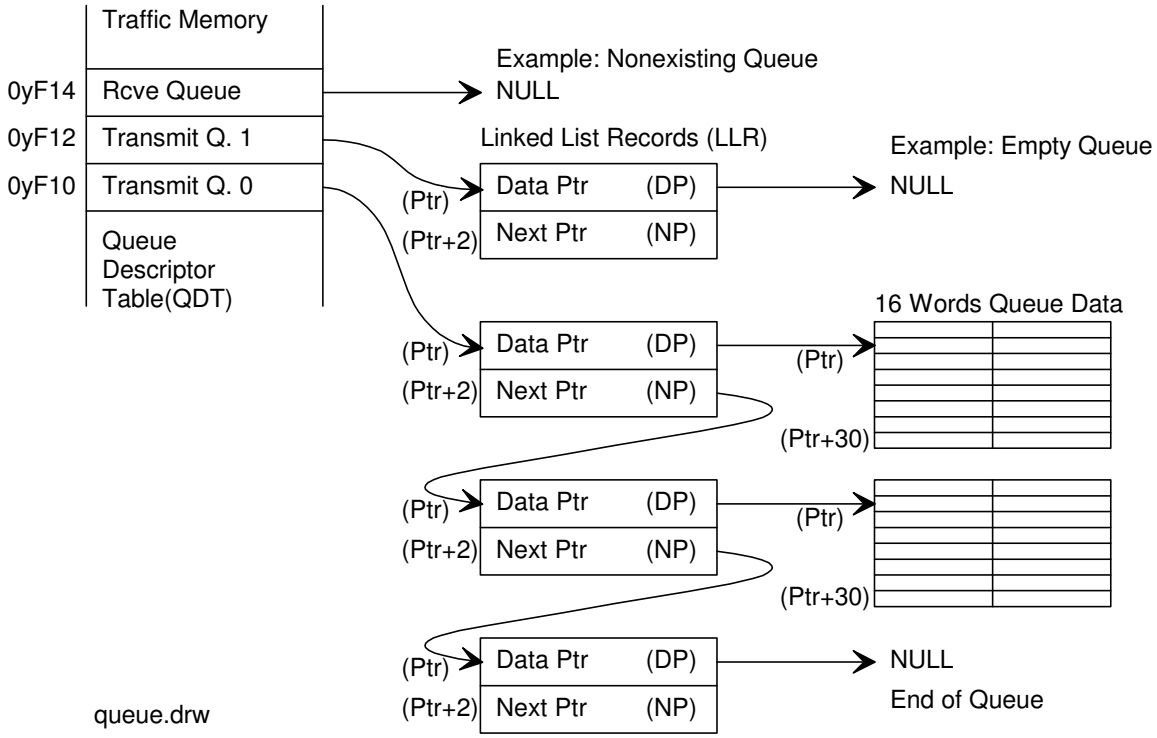


Figure 2.4: Queue Data Structure

The MVBC does not create any queue data structures by itself. The user must install a linked list structure of sufficient size for all three queues before queuing can be activated. The queue data records have a fixed size of 16 words. Following rules must be observed when installing a linked list for queuing:

- The queue structure must not overlap into any active TM regions (i.e. active port data, PCS, Service Area, Master Frame Tables)
- The start address to an LLR must be aligned to a 4 byte block (2 word block).
- The start address to a Data Record must be aligned to a 32 byte block (16 word block).
- The entire linked-list structure must be located within an aligned 256 KB block which is selected by the Queue Offset ($QO_{1..0}$).

2.7.2 Master Frame Tables (MF-Tables)

The MVBC provides an automatic Master Frame Dispatcher. Details about its operation are specified in section 4.9. Each Master Frame Table contains between 1 and 32 Master Frame Words. The Master Frame Tables may be stored in any yet unused location in the Traffic Memory. The user is responsible not to let the MF-Tables overlap

any active TM areas (i.e. Port Index Table, active ports (PCS/Data/Force Table), Service Area, Message Queues).

The Master Frame Table is pointed to by the 16-bit Dispatch Pointer Register (DPR) where the lower two bits are tied to zero. The table size is specified in the Master Register (MR). The pointer is shifted 2 bits to the left and a Master Frame Offset is added. Valid offset values are 00000H, 40000H, 80000H or C0000H. The Master Frame Offset ($MO_{1..0}$) is defined in the Memory Configuration Register. Following rules must be observed when defining Master Frame Tables:

- The Master Frame Tables must not overlap into any active TM regions (i.e. active port data, PCS, Queues)
- The start address to any Master Frame Table must be aligned to a 16 byte block (8 word block) if the Master Frame Table contains not more than 8 words.
- The start address to any Master Frame Table must be aligned to a 32 byte block (16 word block) if the Master Frame Table contains not more than 16 words.
- The start address to any Master Frame Table must be aligned to a 64 byte block (32 word block) if the Master Frame Table contains not more than 32 words.
- All Master Frame Tables must be located within an aligned 256 KB block which is selected by the Master Frame Offset ($MO_{1..0}$).

  In other words, smaller Master Frame Tables with 8, 16 or 24 Master Frame bodies may be defined in order to use the Traffic Memory more efficiently.

WRONG:

Address	**Contents**
0y1050H	
0y1040H	Table 2 (overrun)
0y1010H	
0y1000H	Table1

RIGHT:

Address	**Contents**
0y1050H	
0y1040H	Table 1
0y1010H	Table 2
0y1000H	

Best software approach: The Bus Administrator Software (BAS) should initialize the tables during start-up and assign pointers every time the next cyclic Master Frames are to be sent out. The plausibility of the tables can be tested with a common CRC algorithm which is typically used to test read-only memories.

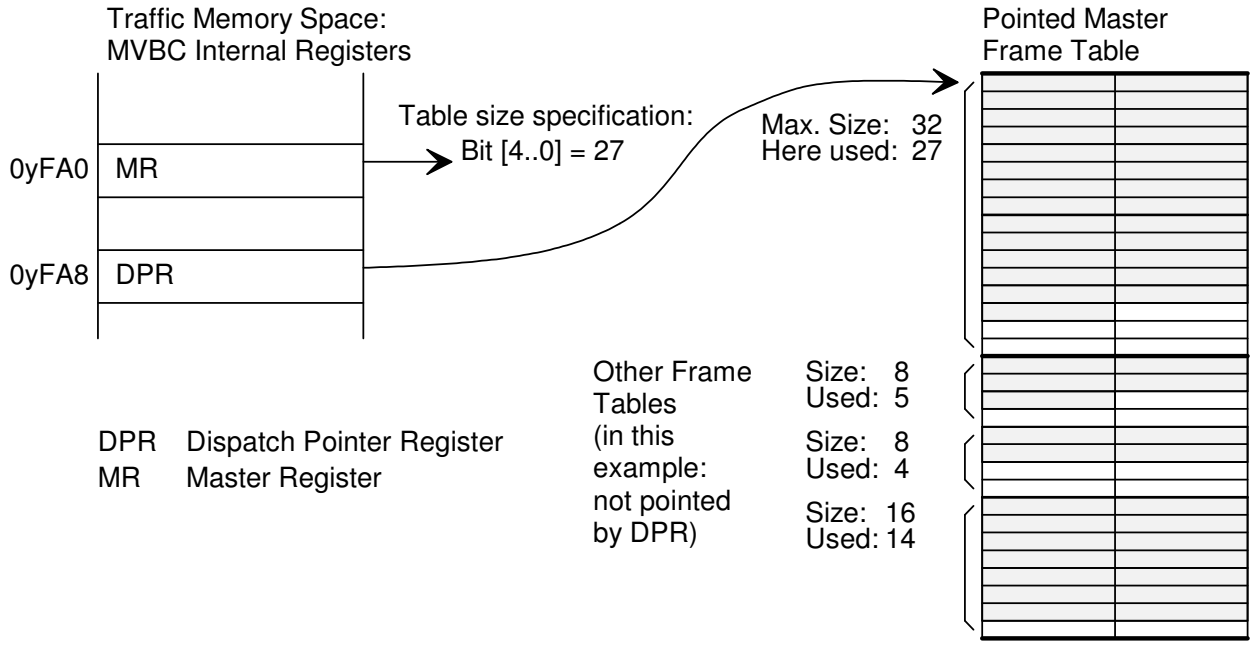


Figure 2.5: Master Frame Table Structure

2.8 Summary: Address Generation Tables

The following tables summarize the layout of the Traffic Memory by specifying the address bits.

Symbol	Description
$LA_{11..0}$	Logical Address (For MCM=0-1, the same word in PIT is accessed regardless if LA is even or odd)
$DA_{11..0}$	Device Address (For MCM=1, the same word in PIT is accessed regardless if DA is even or odd)
$PI_{11..0}$	Port Index
VP	Valid Page Pointer
$C_{4..0}$	Word Counter
$R_{6..1}$	Addresses Internal Registers (Service Area)
$QO_{1..0}$	Queue Offset (From Memory Configuration Register (MCR))
$MO_{1..0}$	Master Frame Offset (From Memory Configuration Register (MCR))
$P_{15..0}$	Master Frame and Queue Pointer bits
$T_{1..0}$	2-bit arithmetic sum of Port Index (PI) and Counter (C): $(T_1,T_0) = (PI_1,PI_0) + (C_3,C_2)$;
$X_{1..0}$	2-bit arithmetic sum of Pointer (P) and Counter (C): $(X_1,X_0) = (P_3,P_2) + (C_4,C_3)$;

Type	MCM	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1
LA-PIT	0,1	0 0 0 0	0 0 0 0	LA_{11} LA_{10} LA_9 LA_8	LA_7 LA_6 LA_5 LA_4	LA_3 LA_2 LA_1
	2,3,4	0 0 0 0	0 0 0 LA_{11}	LA_{10} LA_9 LA_8 LA_7	LA_6 LA_5 LA_4 LA_3	LA_2 LA_1 LA_0
DA-PIT	1	0 0 0 0	0 1 0 0	DA_{11} DA_{10} DA_9 DA_8	DA_7 DA_6 DA_5 DA_4	DA_3 DA_2 DA_1
	2,3,4	0 0 0 0	0 0 1 DA_{11}	DA_{10} DA_9 DA_8 DA_7	DA_6 DA_5 DA_4 DA_3	DA_2 DA_1 DA_0
LA-Data	0,1	0 0 0 0	0 0 0 1	PI_7 PI_6 PI_5 PI_4	PI_3 PI_2 VP T_1	T_0 C_1 C_0
	2	0 0 0 0	0 1 PI_9 PI_8	PI_7 PI_6 PI_5 PI_4	PI_3 PI_2 VP T_1	T_0 C_1 C_0
	3,4	0 0 0 1	PI_{11} PI_{10} PI_9 PI_8	PI_7 PI_6 PI_5 PI_4	PI_3 PI_2 VP T_1	T_0 C_1 C_0
DA-Data	1	0 0 0 0	0 1 0 1	PI_7 PI_6 PI_5 PI_4	PI_3 PI_2 VP T_1	T_0 C_1 C_0
	2	0 0 0 0	1 1 1 0	PI_7 PI_6 PI_5 PI_4	PI_3 PI_2 VP T_1	T_0 C_1 C_0
	3	0 0 1 1	1 PI_{10} PI_9 PI_8	PI_7 PI_6 PI_5 PI_4	PI_3 PI_2 VP T_1	T_0 C_1 C_0
	4	0 1 0 0	PI_{11} PI_{10} PI_9 PI_8	PI_7 PI_6 PI_5 PI_4	PI_3 PI_2 VP T_1	T_0 C_1 C_0
LA-Force Table	0,1	0 0 0 0	0 0 1 0	PI_7 PI_6 PI_5 PI_4	PI_3 PI_2 VP T_1	T_0 C_1 C_0
	2	0 0 0 0	1 0 PI_9 PI_8	PI_7 PI_6 PI_5 PI_4	PI_3 PI_2 VP T_1	T_0 C_1 C_0
	3,4	0 0 1 0	PI_{11} PI_{10} PI_9 PI_8	PI_7 PI_6 PI_5 PI_4	PI_3 PI_2 VP T_1	T_0 C_1 C_0
LA-PCS	0,1	0 0 0 0	0 0 1 1	0 PI_7 PI_6 PI_5	PI_4 PI_3 PI_2 T_1	T_0 C_1 C_0
	2	0 0 0 0	1 1 0 PI_9	PI_8 PI_7 PI_6 PI_5	PI_4 PI_3 PI_2 T_1	T_0 C_1 C_0
	3,4	0 0 1 1	0 PI_{11} PI_{10} PI_9	PI_8 PI_7 PI_6 PI_5	PI_4 PI_3 PI_2 T_1	T_0 C_1 C_0
DA-PCS	1	0 0 0 0	0 1 1 1	0 PI_7 PI_6 PI_5	PI_4 PI_3 PI_2 T_1	T_0 C_1 C_0
	2	0 0 0 0	1 1 1 1	0 PI_7 PI_6 PI_5	PI_4 PI_3 PI_2 T_1	T_0 C_1 C_0
	3	0 0 0 0	0 1 PI_{10} PI_9	PI_8 PI_7 PI_6 PI_5	PI_4 PI_3 PI_2 T_1	T_0 C_1 C_0
	4	0 0 1 1	1 PI_{11} PI_{10} PI_9	PI_8 PI_7 PI_6 PI_5	PI_4 PI_3 PI_2 T_1	T_0 C_1 C_0

Service Area (Start Address, Physical Ports, Master Frame Slot, Queue Descriptor Table, Int. Registers):

Type	MCM	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1
Start Address	0	0 0 0 0	0 0 1 1	1 1 * *	* * * *	* * *
	1	0 0 0 0	0 1 1 1	1 1 * *	* * * *	* * *
	2,3,4	0 0 0 0	1 1 1 1	1 1 * *	* * * *	* * *
PP-Data	all	* * * *	* * * *	* * 0 0	PI_3 PI_2 VP T_1	T_0 C_1 C_0
PP-PCS	all	* * * *	* * * *	* * 1 0	0 PI_3 PI_2 T_1	T_0 C_1 C_0
MFS	all	* * * *	* * * *	* * 1 1	0 0 0 0	0 0 0
QDT[0]	all	* * * *	* * * *	* * 1 1	0 0 0 1	0 0 0
QDT[1]	all	* * * *	* * * *	* * 1 1	0 0 0 1	0 1 0
QDT[2]	all	* * * *	* * * *	* * 1 1	0 0 0 1	1 0 0
Int.Regs	all	* * * *	* * * *	* * 1 1	1 R_6 R_5 R_4	R_3 R_2 0

Port Index Assignment (PI3..0) for Physical Ports (PP-Data/PP-PCS):

0	FC8	1	EFS	2	*Reserved*	3	*Reserved*
4	EF0	5	EF1	6	MOS	7	FC15
8	MSRC/TSRC	(4 docks)		C	MSNK/TSNK	(4 docks)	

Miscellaneous Assignment, Class 1 Mode:

Pointer / Mode	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1
LLR	QO_1 QO_0 P_{15} P_{14}	P_{13} P_{12} P_{11} P_{10}	P_9 P_8 P_7 P_6	P_5 P_4 P_3 P_2	P_1 P_0 0
Queue Data	QO_1 QO_0 P_{15} P_{14}	P_{13} P_{12} P_{11} P_{10}	P_9 P_8 P_7 P_6	P_5 P_4 X_1 X_0	C_2 C_1 C_0
MF-Tables	MO_1 MO_0 P_{15} P_{14}	P_{13} P_{12} P_{11} P_{10}	P_9 P_8 P_7 P_6	P_5 P_4 X_1 X_0	C_2 C_1 C_0
Class 1 Mode	1 1 1 S_0	S_{15} S_{14} S_{13} S_{12}	S_{11} S_{10} S_9 S_8	S_7 S_6 S_5 S_4	S_3 S_2 S_1

$S_{15..0}$ are active low decoded select signals. Only one signal may be active at a time.

Table 2.17: Address Generation Tables

3 HARDWARE OVERVIEW

The MVBC consists of the following functional blocks:

- Encoder - Generation of Manchester code and transmission of frames
- Transmission Buffer - 16 Words + 4 Check Sequences
- Decoder - Reception, Manchester decoding, data extraction and error checking
- Receive Buffer - 16 Words + 4 Check Sequences
- Telegram Analysis Unit
  - Detects Master Frame (MF) and Slave Frame (SF) timeouts
  - Frame level errors (duplicate/missing MF, SF), error statistics
- Status Control Registers - MVBC configuration: No. wait states, initialization level, etc.
- Main Control Unit
  - Supports MVBC functions to operate both as Master and Slave
  - Supports queued message transfers
- Dev. Addr Read & Store Unit- hardware-defined Device Address can be overridden by different value
- Address Logic
  - Decoder of CPU addresses applied to MVBC to select int. registers
  - Encoder to generate outgoing addresses to Traffic Memory
- Arbitration Controller
  - Governs access to Traffic Memory between MVBC and host CPU
  - Different arbitration modi are supported to assure data consistency
- Traffic Memory Controller
  - Controls access from CPU and MVBC to Traffic Memory
  - Built-in waitstate logic
- Bus Multiplexer / Forcing
  - Handles all internal data transfers in the MVBC
  - Enables data forcing, byte swapping
- Class 1 Logic
  - Permits operation without assistance of CPU or microcontroller
  - 16 ports à 16 bits are provided for Process Data
- Interrupt Logic
  - Interrupt vectors are provided for convenience
  - Generates interrupts on user-specified data transfers
  - Reports exceptions (data transfer errors)
  - Supports external incoming interrupt signals
- Two Universal Timers
  - Timer 1: 10 µs up to 650 ms, 10 µs resolution
  - Timer 2: 125 ns up to ca 8 ms, 125 ns resolution
  - Timer output signal (TMR1\,TMR2\) and interrupt capability
  - Multi-MVBC synchronization capabilities
- Sink-Time Supervision
  - Helps to detect irregularities while transferring Process Data
  - Any number of ports from 0 through 5096 can be supervised
  - Selectable supervision period from 1 ms, 2, 4, 8, ... 256 ms
- Clock Generator - Generates all clock and counter signals for the MVBC
- Test Support
  - Ad-Hoc: Internal loop-back, high degree of functional observability
  - JTAG Boundary Scan; Internal Scan; MUX-Isolation of internal RAMs

3.1 Block Diagram

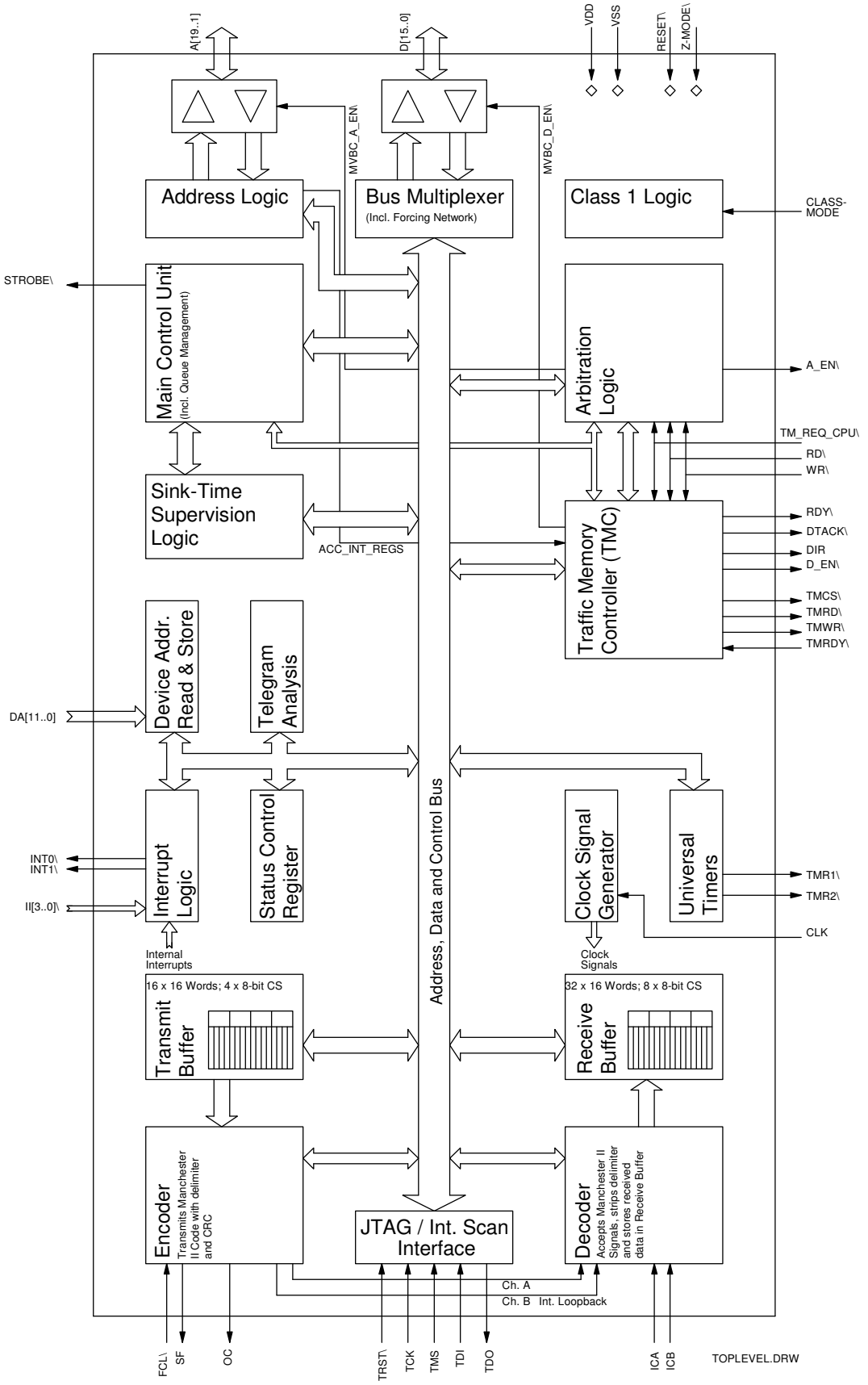


Figure 3.1: MVBC Top-Level Block Diagram

3.2 Encoder

The Encoder converts 16-bit data into a 1.5 Mbit/s serial Manchester Biphase L encoded data stream and transmits it over the common output pin OC. The data is supplemented with a start bit, Master or Slave Delimiter and with one or more 8-bit Check Sequences. The code complies with the IEC TCN Standard [1].

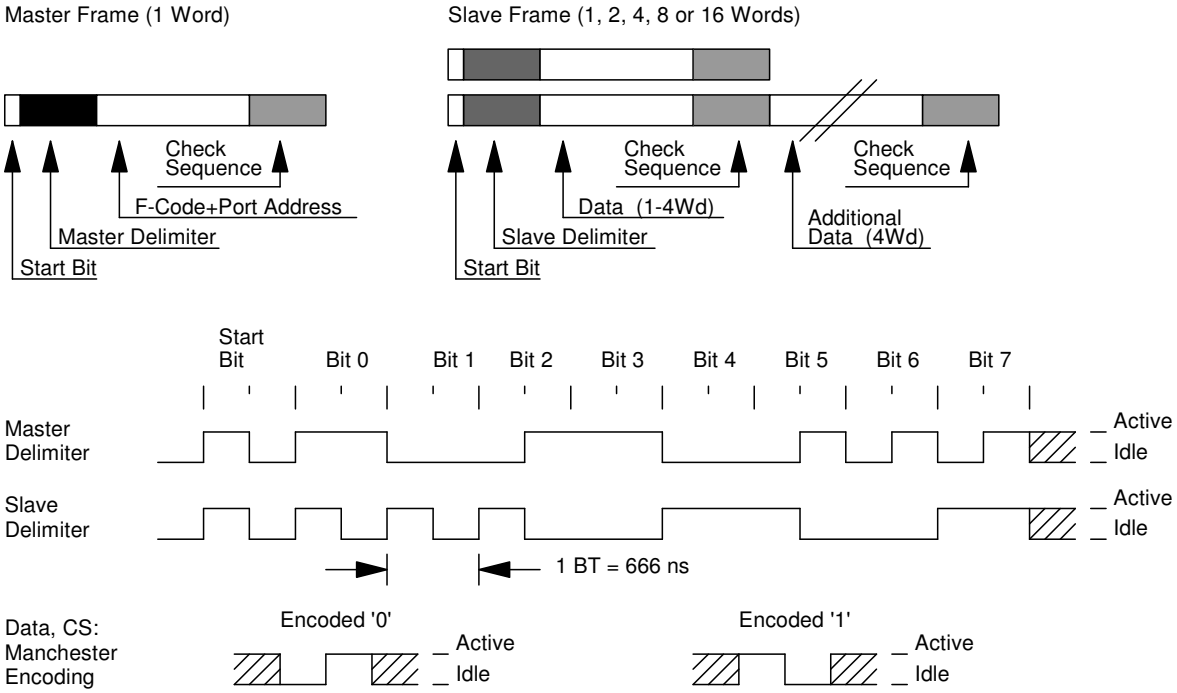


Figure 3.2: Manchester Coding Scheme

The CRC is evaluated from the generator polynomial shown below:

$$G(x) = X^7 + X^6 + X^5 + X^2 + 1$$

This polynomial guarantees a Hamming distance of 4. The overall Hamming distance of 8 is achieved by combining Manchester Biphase coding and CRC. The user can request to transmit user-supplied Check Sequences in the Slave Frames by activating TWCS in the PCS for selected ports. In this case, the same algorithm must be applied in order to assure correct data transfers. If the CRC mismatches, then the MVBC assumes that the user intends to forward garbled data intentionally.

Attention: All types of communication errors, including plain CRC mismatches, are treated as if they occurred on the MVB. Therefore, the bus participants may take actions such as line switchover.

3.2.1 Control Signals for Physical Layer Drivers

The encoder supports EMDB and ESDB interface to the medium. This is selected with the control bit “Trafo” in the decoder register (see section 3.3.7).

The serial data is output via the OC pin. The active high signal "Send Frame" (SF) stays active from 125 ns before the beginning and until the end of the transmitted frame in the ESDB mode where in EMDB mode it is synchronously active with the beginning of start bit until end of frame bit delimiter (see Figure 3.3 and Figure 3.4).

An external input pin "Force Constant Light" (FCL\) is available to tie the output signal to high level in order to adjust signal driver strengths when using fiber optical medium.

A jabber-hold mechanism is available to suppress the serial outputs and keep the SF-signal disabled if the Encoder starts transmitting permanently due to a hardware fault. This mechanism is activated if the QUIET-bit in the SCR (see section 3.4.7) is active.

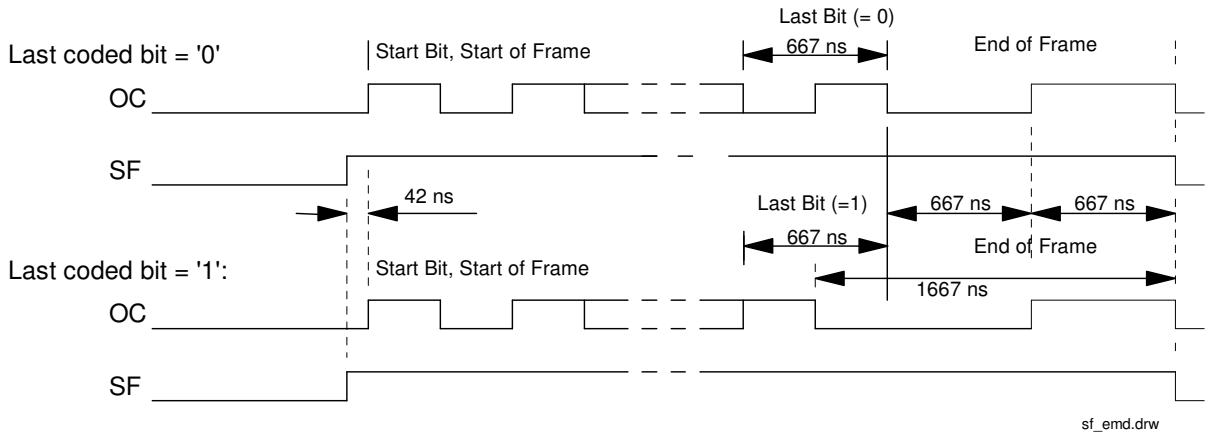


Figure 3.3: OC and SF signals for EMDB interface

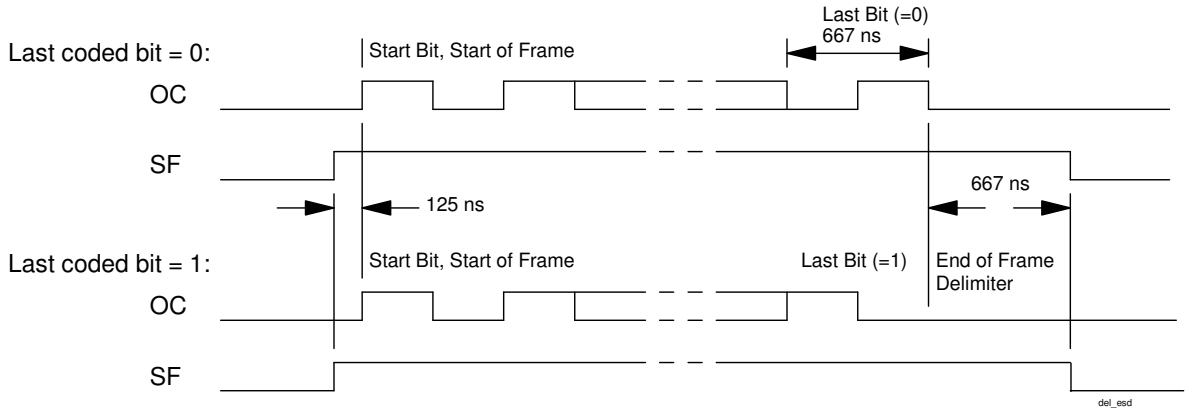


Figure 3.4: OC and SF signals for ESDB and OGF interface

3.2.2 Adjustable Interframe Spacing

The MVBC02C supports configurable interframe spacings: 4, 6, 8 and 12 µs. Only the smallest interframe spacing, namely 4 µs, complies with the TCN standard. This spacing is bigger than in MVBC01.

In Class1 mode interframe spacing is selected by configuring TMR2, TMR1 which serve as inputs in this mode. The default setting for an MVBC02C in Class1 mode will be set to 6 us (terminals TMR2, TMR1 left open).

In Class2,3,4 mode interframe spacing is selected by setting two bits in the Timer Control Register (TCR, see section 3.8.1).

Interframe	**Class 1 Mode: Inputs**		**Timer Ctrl. Register**		
Spacing	**TMR2**	**TMR1**	**IFS_1**	**IFS_0**	**Remarks**
4 µs	Open (1)	Vss (0)	0	0	Default setting for Class2,3,4 Devices
6 µs	Open (1)	Open (1)	0	1	Default setting for Class1 Devices
8 µs	Vss (0)	Open (1)	1	0	
12 µs	Vss (0)	Vss (0)	1	1	

Table 3-2: Interframe Spacing Configuration

3.2.3 Clocked Transmitter Output mode

In applications with potential isolation to the bus line by means of optocouplers an asymmetric duty cycle of biphase line code results due to asymmetric switching behavior of optocouplers. Most optocouplers have a much faster “on” – switching than “off” – switching characteristic.

Here the encoder supports reshaping of biphase code symmetry by means of clocked outputs OC, SF. Figure 3.5 shows the principle of operation.

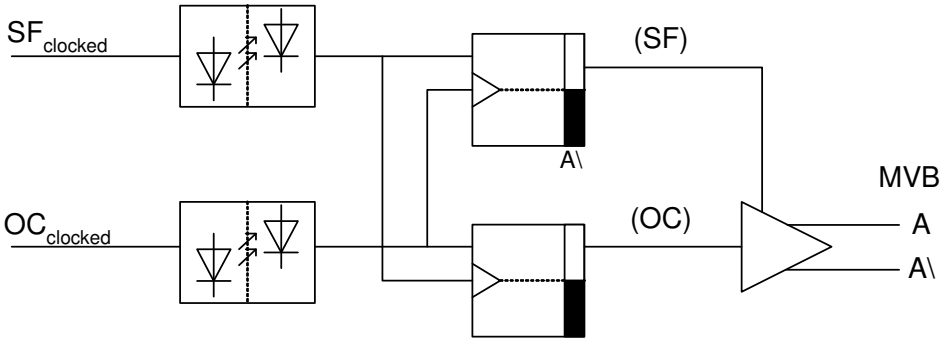


Figure 3.5: Clocked Transmitter Output mode reshaping line code symmetry

In this mode the MVBC outputs SF, OC become clocked outputs $SF_{clocked}$, $OC_{clocked}$, while the driver feeding signals SF, OC are generated using flipflops behind the optocoupler stage. To save output pins and optocoupler, the signals $SF_{clocked}$, $OC_{clocked}$ are coded this way to serve the own logic state for latching and the clock edge for latching the other signal. Figure shows the timing behavior of this interface for example for ESDB. Resulting timing behavior of OC, SF is as described in section 3.2.1.

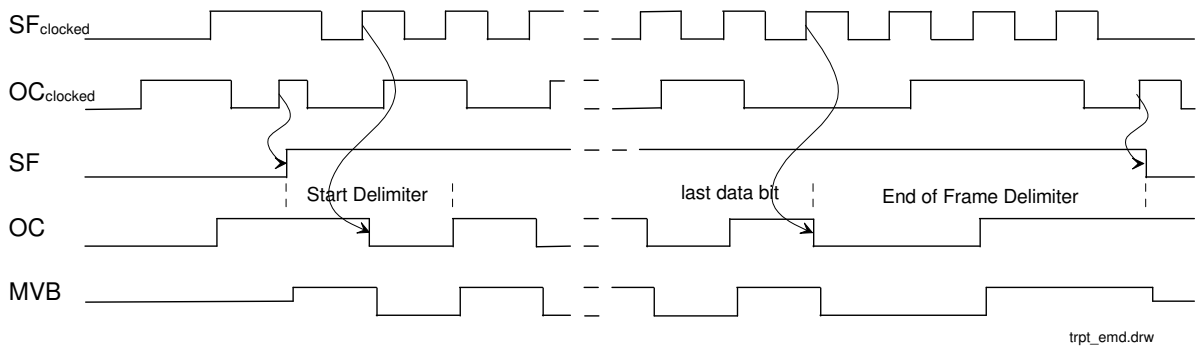


Figure 3.6: Timing of Clocked Transmitter Output mode, EMDB

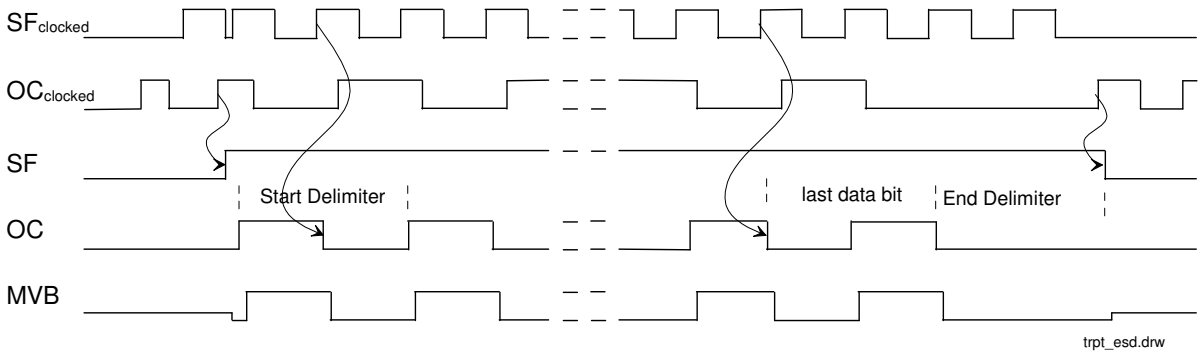


Figure 3.7: Timing of Clocked Transmitter Output mode, ESDB

This Clocked Transmitter Output mode supports both ESDB and EMDB line mode, thus building of one hardware line interface for both, ESDB and EMDB, is possible, without need of transformer.

This function is enabled by setting TRP = 1 in the SFR – register (see chptr. Special Function Register (SFR)3.2.5). In class1 – mode, the output Int1\ serves as an input and controls the Transmitter Output mode: Int1\ = 0 (tied to VSS) enables this mode, this input left open enables traditional behavior of SF, OC.

3.2.4 Transmission Buffer (TXB)

The Transmission Buffer (TXB) serves as an intermediate buffer to store the next frame to be transmitted. This buffer is not visible to the user and is exclusively controlled by the Main Control Unit (MCU).

Capacity: 16 x 16-bit data words plus 4 x 8-bit Check Sequences

3.2.5 Special Function Register (SFR)

The Special Function Register contains additional MVBC configuration information. Control bits not specified are subject to future use.

Special Function Register (SFR): Address 0yFE4H

Bit Number	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol																TRP
Init. Value:																0
CPU Acc.:																RW
MVBC Acc.:																r

Symbol	**Description**	
TRP	TRP	Encoder Output Behavior (refer to section 3.2.3)
	0	OC, SF working in traditional NRZ – mode, see section 3.2.1
	1	clocked transmitter output mode (OC, SF outputs become behavior of $OC_{clocked}$, $SF_{clocked}$, refer to section 3.2.3)

3.3 Decoder

As an essential enhancement compared to the MVBC01 the MVBC02C incorporates a fully redundant decoder. The MVBC receives incoming Manchester biphase L signals over both lines via individual decoder sections for line A / B and selects after complete frame reception from which line to take the received data. Contrarily to this the MVBC01 has to decide prior to reception to which line to trust and switch its decoder.

While frames are received, the Decoder identifies frame type (Master or Slave Frame) from the delimiter and stores the data and 8-bit CRC in the Receive Buffer (RXB). The built-in error detection mechanism guarantees a Hamming Distance of 8.

3.3.1 Signal Detection

The MVBC02C complies with the behavior of the MVBC01,receiving frames with a minimum pause space after data bits, though it support end delimiter coding as specified in the encoder section (see chptr. 3.2.1).

A valid start bit, which occurs after a pause of at least 500 ns (0.75 bit times (BT)), must be detected in order to receive a frame. Shorter pauses cannot be detected. The start bit is recognized as long its duration (*d*) complies with the following limits:

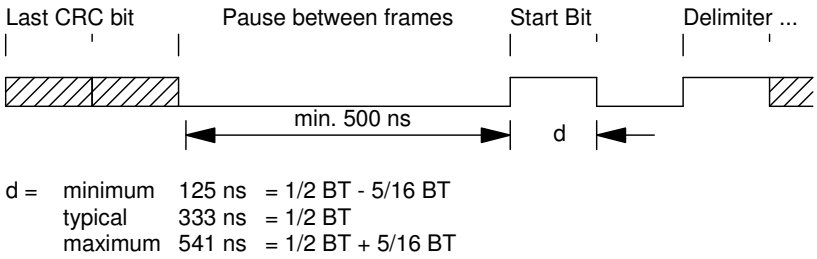


Figure 3.8: Start Bit Detection

Frames with invalid start bits will be ignored and treated as noise. The Decoder synchronizes into the falling edge of the start bit and starts decoding the signal using mid-step signal detection and a sampling rate 16 x the data rate. At every transition, the Decoder performs self-synchronization and is able to adjust to jitter (± 125 ns, or ± 3/16 BT) and data rate deviations between sending and receiving devices (± 41.7 ns, or 1/16 BT). The shaded regions, as shown in Figure 3.9, illustrate the regions where transitions are allowed. Outside these regions, known as *forbidden zones*, the signal will be sampled twice (rhombus symbols). This dual method assures reliable sampling and signal quality monitoring. If the edge is detected within forbidden zones (outside shaded areas), then a false sampling is made and a Signal Quality Error (SQE) will be reported.

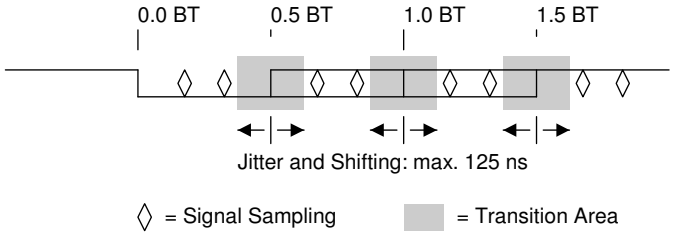


Figure 3.9: Signal Detection

3.3.2 Signal Monitoring

The Decoder monitors the incoming signals for following irregularities:

- Signal Quality Errors (SQE), see section 3.3.1.
- Manchester Code Violation
- Active Level Overbalance (ALO)
- Mismatching CRC
- Frame too short or too long
- Slave Frame Reply Timeouts

A Manchester Code Violation is reported when no transition is found in the middle of a received bit. However, the Decoder tolerates the violations defined in the Master and Slave delimiters (signal is stable for 3/2 BT).

The Manchester biphase L signal foresees a balance between "Low" and "High" signal level.

Active Level Overbalance (ALO) is reported if four or more signal transitions occurred since starting reception (e.g. some noise / collisions on the bus line) and the reception is reported as erroneous or timed out (PCS). **Note:** This function is different compared to the implementation in the MVBC01!

The Decoder evaluates the CRC of the incoming frames according to the CRC algorithm specified in [1]. A CRC error is issued if the reconstructed CRC differs from the received CRC.

Frame size checking: The Decoder knows the expected frame length at the moment a valid delimiter has been received. Master Frames contain one word only. The expected size of a Slave Frame is derived from the F-Code of the previously received Master Frame.

If an error is detected inside the delimiter, then the Decoder ignores the frame (timeout!) and tries to re-synchronize on the start bit of the next frame. If an error is detected inside the data or CRC fields after receiving a correct delimiter, the Decoder reports the error to the PCS. If an error occurs, but the frame size remains unchanged, then the Decoder tries to recover the data if requested (active WA bit in the PCS, “write always”).

3.3.3 Redundant Line Supervision

The trusted line is indicated by the LAA bit (Line A Active) in the Decoder Register (DR), where the received data is taken from. Unless the Decoder operates in Single Line Mode (SLM bit in DR active), both ICA - and ICB – decoder-sections are active and line switchover is enabled. Otherwise, if the user sets the SLM bit, the Decoder considers the trusted line (ICA or ICB, whichever is active at the moment) as the single input and line switchover is disabled. If ICB (or ICA) is the only connected line and LAA is active (or inactive), then the user must invoke a manual line switch before setting SLM.

The observed line (for the redundant decoder it is the line which is not indicated by LAA – bit in the DR – register) is monitored for the same types of errors as the trusted line, because of the fully doubled redundant decoder.

The RLD-bit (Redundant Line Disturbed) in the DR is set if one of the errors occurs.

The Decoder will always wait until the complete frame has been received on both lines except when at least one of the following items apply:

- RLD-bit is set
- SLM-bit is set
- The observed line remained silent throughout the period the entire frame has been received over the trusted line.
- Permanent signal reception on the observed line

Line Switchover (applies if SLM = '0'):

A switch from the trusted line to the observed line takes place if one of the following conditions are met:

1. Erroneous frame or Reply Timeout on the trusted line, regardless if valid data has been detected on the observed line. Exception: No line switch will take place during Event Arbitration (F-Codes 9, 13, 14). The line switch takes place when nothing is received at the moment or at the next pause. RLD is set.

2. Silence: No valid Master Frame has been received within 1.4 ms. If both lines are silent, the MVBC will switch lines at 1.4 ms intervals until a Master Frame has been received again. RLD bit is set.

3. A Master Frame containing a Device Status Poll (F-Code=15) has been received and the Device Address matches. The addressed MVBC performs following steps:

   - If RLD is not set, then a line switch will be invoked
   - The RLD will be cleared
   - The Device Status Report will be transmitted (Class 1 Mode: contains old RLD)

4. User-invoked Line Switchover

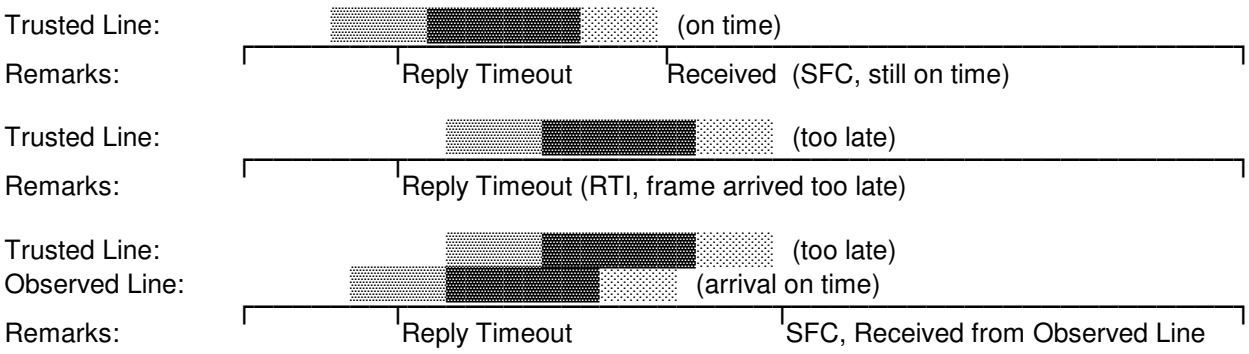
If the user activates the LS-Bit (inside DR), then the line switch will take place at the next pause or when the MVB is silent. The MVBC resets LS to zero after the line switch has taken place.

Attention: If RLD is active, then line switchover is restricted to the conditions stated in item 2.

3.3.4 Frame Reception Scenarios

The following diagrams illustrate the behavior of the Decoder for different scenarios while both lines are active (SLM=0).

<u>Timeouts:</u>



<u>Valid reception with skew:</u>

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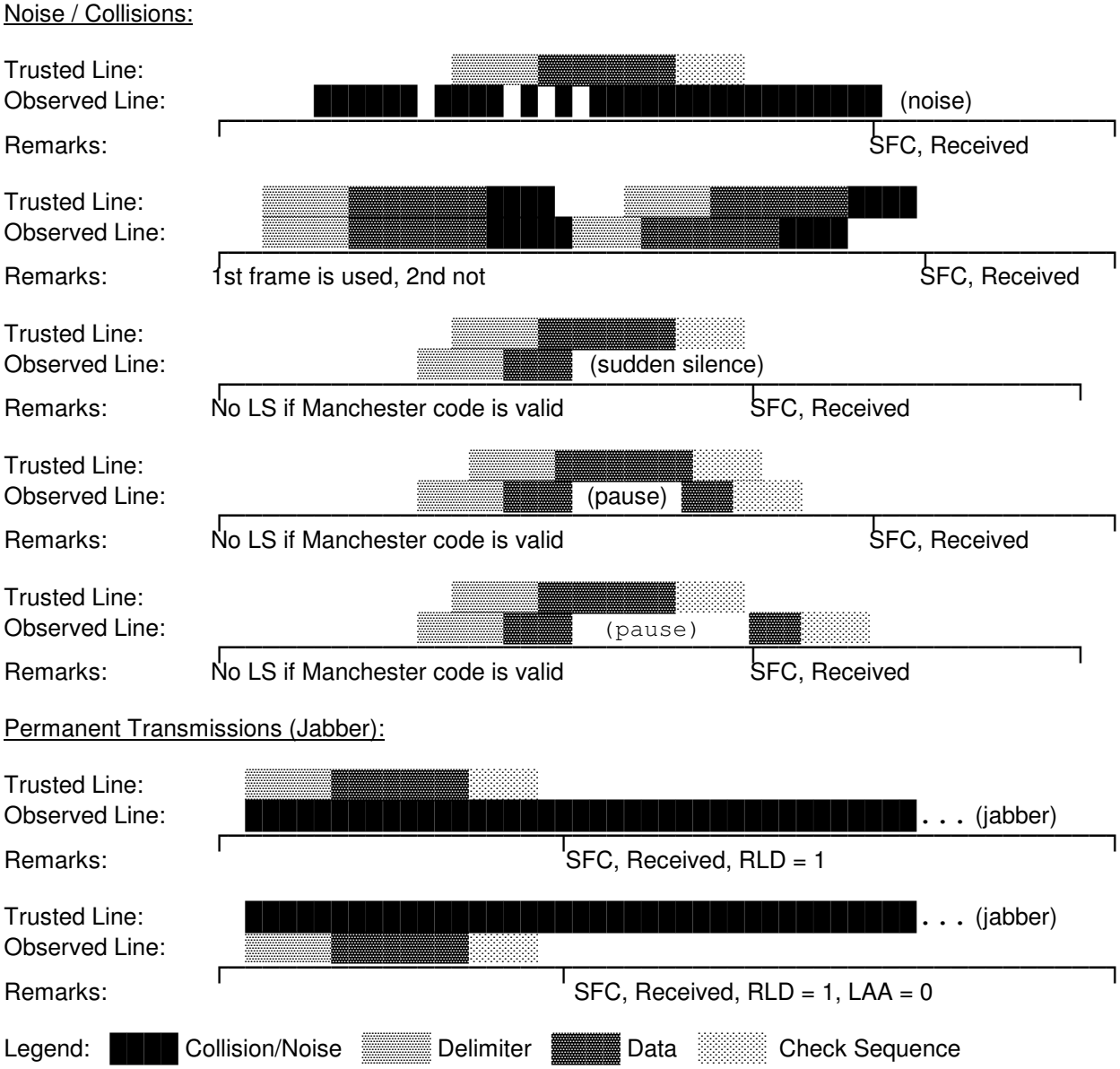

Figure 3.10: Communication Scenarios

3.3.5 Late Transmit Enable

During arbitration mode – applies to bus administrators only – a mechanism was added to prevent collisions and wrong status, if a 2nd delayed answer from a Slave which lasts longer than the STO is being received. Normally when “late_tx_enable” is NOT set, the next MF will be transferred after the STO is being recognized during event arbitration. This can collide with a late arriving SF. To prevent this two possible solutions have been worked out:

1.) Increase the SlaveFrameReplyTimeout. This will decrease the available bandwidth for all others transfers as well, but might be the only solutions, if the bus is noisy.

2.) Set the flag “Late Tx Enable” LTE = ‘1’ in the decoder register (see chptr. 3.3.7). This will ‘delay’ the transmission of the next MF until the line is idle, even after STO has already been expired.

3.3.6 Late Delimiter Hunting

It was found that - caused by noise and by reflections - it is possible that a ‘wrong’ delimiter is recognized prior to the real delimiter normally following some bits later. This behavior produces unnecessary bad reception of frames and loss of the real frame. A new mechanism – so called Delimiter Hunting – is now introduced to the decoder.

After reception of a delimiter and detected manchester code violation in the following data bits, the decoder checks again for a valid delimiter pattern. If found, the decoder considers the very first delimiter as fake and resynchronizes on the second found.

After reset this mechanism is active. It can be disabled by setting the flag “No Delimiter Hunting” NDH = ‘1’ in the decoder register (see chptr. 3.3.7).

3.3.7 Decoder Register (DR)

Decoder Register (DR) : Address 0yF88H

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	LTE	NDH	ATO	RLDS	BLVL	BCHG	ALVL	ACHG	Turbo	Opto	Trafo	WTR	LAA	RLD	LS	SLM
Init. Value:	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
CPU Acc.:	RW	RW	RW	RW0	R	RW0	R	RW0	RW	RW	RW	RW	R	RW0	RW1	RW
MVBC Acc.:	r	r	r	w1	w	w1	w	w1	r	r	r	r	rw	rw	rw	r

Symbol	Description
LTE	“Late Tx Enable” Late Transmit Enable, affects only bus administrator behavior. 0 Transmit enable after STO occurs. (like in MVBC01) 1 Transmit enable after STO occurs and line is idle (no late reception found).
NDH	No Delimiter Hunting. 0 Allow resynchronization, if second delimiter found (reset state) 1 No delimiter hunting. (like in MVBC01)
ATO	“ALLOW_TMO” Allow Timeout. 0 No timeout status report, if no delimiter detected (like in MVBC01, reset state) 1 Enable a reply timeout status, if the Slave Frame Reply Timeout has been expired, and no valid frames other than noise has been received so far (no delimiter has been detected). Up to now, if the line is not idle (only some noise, no delimiter detected) no status with an STO will be produced. In a noisy environment the MVBC will wait until the noise disappears and silence on the line is recognized, or the Jabber Control Logic forces a status after ~1.25 ms. This decreases the effective available bandwidth.
RLDS	RLD Static. This bit holds RLD status until cleared by CPU. It is not cleared automatically as done with RLD bit (compare to bit 2, RLD). 0 No RLD occurred since last reset by CPU. 1 RLD = 1 occurred since last time this status bit was reset by CPU
BLVL	Current signal level detected in input channel B (ICB or local test loop-back in test mode or OR-gate of both if OPTO=‘1’) 0 Logic ‘0’ 1 Logic ‘1’
BCHG	At least one signal transition has taken place as detected in BLVL since last time BCHG has been cleared. Read access: 0 Logic ‘0’ 1 Logic ‘1’ Write access: 0 Clears BCHG 1 No action

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Symbol	Description
ALVL	Current signal level detected in input channel A (ICA or local test loop-back in test mode or OR-gate of both if OPTO='1') 0 Logic '0' 1 Logic '1'
ACHG	At least one signal transition has taken place as detected in ALVL since last time ACHG has been cleared. Read access: 0 Logic '0' 1 Logic '1' Write access: 0 Clears BCHG 1 No action
TURBO	Selects communication speed (applies to both MVBC encoder and decoder) 0 1.5 Mbit/s (MVB standard) 1 3.0 Mbit/s (double speed)
OPTO #	Enables local loop-back in order to facilitate use of fiber-optical communication medium. If enabled, input channel A = OC or ICA, and input channel B = OC or ICB. 0 No local loop-back (like in MVBC01) 1 Local loop-back enabled
TRAFO #	Enables trafo line mode (controls end delimiter reception and transmission), 0 MVB ESDB (opto) mode 1 MVB EMDB (trafo) mode
WTR	Enable waiting till MVBC has given timeout signal (typical 42.7 us), applies for BA only 0 Disabled (like in MVBC01). Only done in arbitration polls. 1 Enabled for all F-Codes. MVBC will await reply timeout (RTO), if not elapsed so far, until it processes received SF.
LAA	Line A Active (trusted), inverted at every line switch 0 Line B active (Line A is observed) 1 Line A active (Line B is observed)
RLD	Redundant Line Disturbed 0 Observed line is O.K. 1 Bad data or silence detected on observed line Attention: This bit is cleared automatically when a Device Status Poll (F-Code 15) addresses this MVBC
LS	Activate Line Switchover 0 No line switchover in progress or filed 1 Line switchover in progress or filed
SLM	SLM Single Line Mode 0 Line switchover by MVBC is allowed 1 Only the line selected by LAA will be used to receive data. Line switchovers are suppressed.

in class 1 mode controlled by hardware means, see section 5.4.4

Table 3.1: Decoder Register (DR)

3.3.8 Receive Buffer (RXB)

The Receive Buffer (RXB) serves as an intermediate buffer to store the last received frame of both lines. This buffer is not visible to the user and is exclusively controlled by the Main Control Unit (MCU).

Capacity: 2 x 16 x 16-bit data words plus 2 x 4 x 8-bit Check Sequences

3.4 Telegram Analysis Unit

The Telegram Analysis Unit pursues following tasks:

- Reporting incoming Slave Frames Section 3.4.1
- Timeout Mechanisms Section 3.4.2
- Telegram Error Handling Section 3.4.3
- Master Frame Registers Section 3.4.4
- Telegram Error Record-keeping Section 3.4.5

3.4.1 Incoming Slave Frames

At the moment the Decoder reports that a valid or erroneous Slave Frame has arrived (at least the Slave Delimiter is valid) has been received, the interrupt

"Slave Frame Checked" (SFC)

is asserted.

3.4.2 Timeout Mechanisms

The Telegram Analysis Unit generates three different Timeout signals, as long the MVBC is operating in full-functional or loopback mode (Initialization Level 2 or 3, see SCR, section 3.4.7):

- Reply Timeout See below
- Bus Timeout 1.30 ms
- Line Timeout 1.42 ms

The Slave Frame Reply Timeout signal is used to signal a timeout if no Slave Frame arrives, or if the delay is too large. The signal is passed to the Decoder which checks whether a Frame is currently received or not. If not, then the interrupt

"Reply Timeout Interrupt" (RTI)

is asserted. This interrupt does not occur more than once after a Master Frame. The Timeout Coefficient is adjustable with the SCR bits TMO1..0. The initial value is 42.7 µs and complies with the MVB Specification [1]. All other values do not comply with the specifications and must not be used in open MVB systems.

- 21.3 µs (50% less)
- 42.7 µs (default value)
- 64.0 µs (50% more)
- 85.4 µs (100% more)

RTI can occur during a true timeout or a strong-overlapping collision where the delimiters have been garbled. If an active port is affected, then the PCS Word 1 will be updated with STO=1. BNI may be active if the line was not silent. The Bus Timeout occurs 1.3 ms after the end of the last Master Frame. If no Master Frame has been received within this period, then the interrupt

"Bus Timeout Interrupt" (BTI)

will be asserted. This timeout does not occur more than once after a Master Frame. The Line Timeout occurs 1.42 ms after the end of the last Master Frame. This timeout forces a line switch at the Decoder, given the Decoder does not operate in Single Line Mode (SLM=1). As long no Master Frame has been received, this timeout signal at 1.42 ms intervals in order to poll both signal inputs.

3.4.3 Telegram Error Handling

Error information are obtained from the Decoder, processed and suggestions for further actions are passed to the Main Control Unit (MCU). If the delimiter has been recognized, but the received frame contains an error, then one of the following interrupts can occur:

"Erroneous Master Frame" (EMF)
"Erroneous Slave Frame" (ESF)

If ESF occurs and an active port is affected, then the PCS Word 1 will be updated with TERR=1 and BNI=1. SQE, ALO and CRC contain detailed error information. If EMF occurs, then no port will be affected. If two or more subsequent Master Frames are received before Reply Timeout occurs, then the last Master Frame applies. The previous Master Frames will be ignored. The interrupt

"Duplicate Master Frame" (DMF)

will be asserted. If two or more subsequent Slave Frames are received, the first Slave Frame will be handled. All other frames are ignored. This case also occurs if a valid Slave Frame is received after a Reply Timeout. The interrupt

"Duplicate Slave Frame" (DSF)

will be asserted.

3.4.4 Master Frame Registers (MFR, MFRE)

Two registers are foreseen for capturing the Master Frame:

- Master Frame Register (MFR)
- Master Frame Register Duplicate on Exception occurrence (MFRE)

The MFR contains the last Master Frame received. It also applies to Master Frames sent by this MVBC which returns back into the Decoder. The MFR serves for following purposes:

- F-Code Checking, Comparison of 12-bit address, Port Selection
- Frame size Comparison for the next arriving Slave Frame
- Evaluation of various Traffic Memory Addresses

If an interrupt due to an exception is generated, then the contents in MFR are copied into MFRE. Then, MFRE will be frozen until the interrupt has been serviced (corresponding Interrupt Status bits in ISR are cleared, see Interrupt Logic, section 3.7). MFRE will not be frozen if the affected interrupt is masked.

Following interrupts are considered as exceptions: EMF, ESF, DMF, DSF, RTI, BTI

Both MFR and MFRE use the same 16-bit Master Frame Format:

Master Frame Registers (MFR): Address 0yF98H

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	$F\text{-}Code_{3..0}$				$Addr_{11..0}$											
Init. Value:	all 0				all 0											
CPU Acc.:	R				R											
MVBC Acc.:	rw				rw											

Master Frame Register Duplicate Exception (MFRE): Address 0yF9CH

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	$F\text{-}Code_{3..0}$				$Addr_{11..0}$											
Init. Value:	all 0				all 0											
CPU Acc.:	R				R											
MVBC Acc.:	w				w											

Symbol	Description
$F\text{-}Code_{3..0}$	Function Code. See "Appendix A: Function Code Summary" for details.
$Addr_{11..0}$	Address as specified in the Master Frame. It depends on the F-Code: F-Code 0 – 4: Logical Address 8,12,14,15: Device Address 9: Parameters 13: Device Group Address

Table 3.2: Master Frame Registers (MFR, MFRE)

Attention: Whenever messages are received, the MFR is loaded with the first word of the Message Data. The first word contains the destination Device Address and the Communication Mode bits.

Attention: At EMF and DMF, the MFRE contains the previous Master Frame and not the one which caused the error.

3.4.5 Telegram Error Record-keeping, Error Counter

In order to obtain quantitative results regarding the quality of the bus, the number of frames sent and received are recorded in the Frame Counter Register (FC). The number of erroneous frames (or Reply Timeouts) sent or received are recorded in the Error Counter Register (EC). When 65,535 frames have been received, the interrupt

"Frames Evaluated Interrupt" (FEV)

will be asserted. The user can retrieve the error count from the EC and reset the FC. The EC will be frozen when the FC has reached the maximum value of 65,535 (216-1). FC and EC will remain unchanged during event polls since these polls allow collisions and Reply Timeouts.

The following frames affect FC and EC:

- All Master Frames (including F-Codes 9, 13 and 14)
- Slave Frames (or Reply Timeouts) followed after Master Frames with all F-Codes except 9, 13 and 14.

The following frames do not affect FC and EC:

- Slave Frames followed after valid Master Frames with F-Code 9, 13 and 14: Arrival of good and erroneous frames (collisions) and timeouts.

Frame Counter (FC): Address 0yF90H

Bit Number	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	$FC_{15..0}$															
Init. Value:	all 0															
CPU Acc.:	RW															
MVBC Acc.:	rw															

The Error Counter counts the number of erroneous frames as described above. This value shall be reset by the user.

Error Counter (EC): Address 0yF94H

Bit Number	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	$EC_{15..0}$															
Init. Value:	all 0															
CPU Acc.:	RW															
MVBC Acc.:	rw															

3.4.6 Error Models

The table shown on the next page illustrates the error models and the actions taken:

Brief description of the column headers:

Counter: FC Frame Counter is incremented. Not affected during Event Polls (F-codes 9,13,14).

Counter: EC Error Counter is incremented. Not affected during Event Polls (F-Codes 9, 13, 14).

Counter: ECA, ECB
Error Counter is incremented. Not affected during Event Polls (F-Codes 9, 13, 14) and if STO occurs.

TACK: Transfer Acknowledge set to FFFFH (PCS Word 2)

CRC, SQE, ALO, BNI, TERR, STO:
Telegram Status Bits affected (PCS Word 1) if active port is processed

LS: Line switched (if RLD=0, SLM=0). No line switchover takes placing during Event Polls.

VP: Valid Page Pointer (PCS Word 2) toggled or unchanged if active port is processed

Interrupts: See section 3.7.

Error Situation, Possible Causes	Counter				Influences on the PCS, Word 1 (Telegram Status)								PCS Wd 1	Interrupts
	FC	EC	ECA	ECB	TACK	CRC	SQE	ALO	BNI	TERR	STO	LS	VP	(if enabled)
Valid Master Frame (no DMF):	+1	+0	+0	+0	-	-	-	-	-	-	-	No	-	- [3]
Valid Slave Frame (no DSF):	+1	+0	+0	+0	FFFFH	0	0	0	0	0	0	No	toggle	SFC+DTI*i* [2]
Entire Telegram (Valid MF + SF):	+2	+0	+0	+0	FFFFH	0	0	0	0	0	0	No	toggle	SFC+DTI*i* [2]
Erroneous Master Frame (EMF) detected (delimiter OK):	+1	+1	+1	+1	-	-	-	-	-	-	-	Yes	-	EMF [3]
Erroneous Slave Frame (ESF) detected (delimiter OK):														
Due to Signal Quality Error (SQE)	+1	+1	+1	+1	unchgd	0	1	0	1	1	0	Yes	See [1])	ESF
Due to Manchester Code Violation	+1	+1	+1	+1	unchgd	0	0	0	1	1	0	Yes	See [1])	ESF
Due to Invalid Check Sequence (CRC)	+1	+1	+1	+1	unchgd	1	0	0	1	1	0	Yes	See [1])	ESF
Frame Size Error (but correct transfer over the bus)	+1	+1	+1	+1	unchgd	0	0	0	1	1	0	Yes	unchgd	ESF
External Noise (notice combination of errors allowed)	+1	+1	+1	+1	unchgd	0 or 1	0 or 1	0 or 1	1	1	0	Yes	unchgd	ESF
Reply Timeouts (RTI):														
Late Slave Frame (SF is treated as DSF afterward)	+1	+1	+0	+0	unchgd	0	0	0	0	0	1	Yes	unchgd	RTI
Timeout due to missing Slave Frame (Silence)	+1	+1	+0	+0	unchgd	0	0	0	0	0	1	Yes	unchgd	RTI
Noisy bus, no delimiter detectable	+1	+0	+0	+0	unchgd	0	0	0 or 1	1	0	1	Yes	unchgd	RTI
Reception of two consecutive Master Frames (DMF):														
1st frame is ignored, 2nd frame is processed	+1	+1	+1	+1	-	-	-	-	-	-	-	No	unchgd	DMF [3]
Reception of two consecutive Slave Frames (DSF):														
1st frame is processed as good Slave Frame	+2	+0	+0	+0	FFFFH	0	0	0	0	0	0	No	toggle	SFC+DTI*i* [2]
2nd SF causes error	+1	+1	+1	+1	-	-	-	-	-	-	-	No	unchgd	DSF
Collisions:														
Strong overlapping: Both delimiter and data garbled:	+1	+1	+1	+1	unchgd	0	0	0 or 1	1	0	1	Yes	unchgd	RTI
Weak overlapping: 1 Delimiter OK, data and CRC garbled	+1	+1	+1	+1	unchgd	0 or 1	0 or 1	0 or 1	1	0 or 1	0	Yes	unchgd	ESF
No overlapping: 2 consecutive Slave Frames: At 1st Frame:	+1	+0	+0	+0	FFFFH	0	0	0	0	0	0	No	toggle	SFC+DTI*i* [2]
At 2nd Frame: DSF occurs	+1	+1	+1	+1	-	-	-	-	-	-	-	No	unchgd	DSF
Mixup: 1 good SF followed by 1 erroneous SF: At 1st Frame:	+1	+0	+0	+0	FFFFH	0	0	0	0	0	0	No	toggle	SFC+DTI*i* [2]
At 2nd Frame: ESF+DSF occur	+1	+1	+1	+1	-	-	-	-	-	-	-	Yes	unchgd	DSF+ESF
Bus Timeout (BTI):	+0				-	-	-	-	-	-	-	Yes	unchgd	BTI
Frame spacing too small: (less than 500 ns)	-				Previous and current frames are treated as one large frame with illegal frame size, see *Frame Size Error*									

[1] Toggles if TWCS=='1' and an entire frame has been received (no frame size error)

[2] DTIi means "Data Transferred" interrupt, see section 3.5.

[3] MFC "Master Frame Checked" is not included since it applies to sending Master Frames only. See section 3.5.

Table 3.3: Telegram Analysis Results

3.4.7 Extended Line Diagnosis, Line Quality Reporting

For improved line diagnostic, also related to the source of a frame, an extended port related line diagnosis is provided. Information on the line quality is made available in the Port Control and Status Register (PCS, Word 1) for every telegram transfer. Therefore problems related to individual telegrams or source devices can be tracked down.

In normal operation (as with MVBC01) the telegram status bits CRC, SQE, ALO, BNI, TERR, STO are reported in the PCS1 register order to maintain backward compatibility to existing MVBC chips.

However, if “Line Diagnosis” (LD) in the Status and Control Register (SCR, see section 3.5.1) is activated, the telegram status bits of both, the trusted line and observed line, are reported in the PCS1 (see details in PCS section 2.3.2.2) .

3.4.8 Individual Line Error Counters

Though the existing counters “Frame Counter” (FC) and “Error Counter” (EC) are suitable to collect information on the success of received frames, they are not suitable to obtain a plausible statistical value on the quality of a particular MVB line. Actually reception errors recognized in the observed line are not taken into account.

Two additional error counters “Error Counter line A / B” (ECA, ECB) help to solve this problem.

Attention: Slave Frame Reply Timeout Signal does not increment the appropriate Line Error Counter ECA, ECB (but increments EC).

Line Error Counter A (ECA): Address 0yFD0H

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	$ECA_{15..0}$															
Init. Value:	all 0															
CPU Acc.:	RW															
MVBC Acc.:	RW															

Line Error Counter B (ECB): Address 0yFD4H

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	$ECB_{15..0}$															
Init. Value:	all 0															
CPU Acc.:	RW															
MVBC Acc.:	RW															

Table 3.4: Error Counter for line A and B (ECA, ECB)

3.5 Main Control Unit (MCU)

The Main Control Unit (MCU) orchestrates all data transfers between the MVB and the Traffic Memory. The MCU handles following functions:

- Slave Functions:

  Received Master Frames are checked for their F-Code and address and a decision is made whether ports are to be processed or not. If a source port is encountered, then data is transmitted. If a sink port is encountered, then the MVBC will store the contents of the received Slave Frame in the port. All F-Codes, which are defined in the IEC TCN Standard [1], are supported.

- Master Functions:

  The MCU can transmit individually assigned Master Frames or Master Frames retrieved from Master Frame Tables. The Master Frames which are transmitted here will also be received and processed by the MVBC in the same manner as if they originated from a remote MVB participant. This feature allows one CPU to run both Bus

Administrator software and application software which depend on the MVB. The MAS-bit in the SCR must be active in order to pursue Master Functions.

- Event Arbitration Mechanism

  The MCU is in charge of handling event arbitration.

- Interrupts

  The MCU can assert following interrupts:

  "Master Frame Checked" (MFC)

  "All Master Frames Transmitted" (AMFX)

  "Data Transfer Interrupts" (DTI1..DTI7)

  MFC is asserted after the MCU has retrieved a MF from the TM and passed to the Transmit Buffer in order to send it. AMFX indicates that a Master Frame Table has been processed entirely. $DTI_{1..7}$ are user-definable interrupts which occur after the data transfer and after the ports have been processed.

The MCU is closely coupled with the Status Control Register (SCR), Telegram Analysis Unit and Sink Time Supervision. Details about communication behavior are handled in chapter 4.

The MCU provides four control registers which are described in the following sections:

- Master Register (MR)
- Secondary Master Register (MR2), lower 8 bits only
- Dispatch Pointer Register (DPR)
- Secondary Dispatch Pointer Register (DPR2)

3.5.1 Status Control Register (SCR)

The Status Control Register contains MVBC configuration information. This register is used to force the MVBC into various operation and test modes. The test modes allow extensive testing of MVBC functionality without interfering with MVB traffic.

Status Control Register (SCR): Address 0yF80H

Bit Number	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	IM	QUIET	MBC	LD	$TMO_{1..0}$		$WS_{1..0}$		$ARB_{1..0}$		UTS	UTQ	MAS	RCEV	$IL_{1..0}$	
Init. Value:	0	0	0	0	01		11		00		0	0	0	0	00	
CPU Acc.:	RW	RW	RW	RW	RW		RW		RW		RW	RW	RW	RW	RW	
MVBC Acc.:	r	r	r	r	r		r		r		r	r	r	r	r	

Symbol	**Description**
IM	Intel/Motorola Mode (Assures correct order of data transmitted/received) 0 Motorola Mode (Big Endian type CPU connected to MVBC, i.e. Motorola 680x0 series) 1 Intel Mode (Little Endian type CPU connected to MVBC, i.e. Intel 80x86 series) IM affects byte order when transferring non-numeric data (see section 2.3.1, PCS bit "NUM" inactive) over the MVB and byte order of Port Index Tables when using MCM=0 or 1 (see section 2.2).

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Symbol	Description
QUIET	Disables data transmission immediately (Jabber-Hold Protection), used by Encoder If the software got information that its own MVBC acts as a permanent transmitter (jabber activity), the Encoder can be shut off by activating this bit. The MVBC will still be able to receive frames and update sink ports. 0 Transmitter is active 1 Transmitter is shut off
MBC	Message Broadcall: Used by Main Control Unit 0 Messages (F-Code=12) are received only if target address matches with own DA. 1 All messages with valid CM values are received (suitable for bus monitoring).
LD	Line Diagnosis 0 No extended Line diagnosis in Port Control Register (PCS1) 1 Enable extended Line diagnosis in Port Control Register (PCS1), see section 3.4.7 and section 2.3.2.2
$TMO_{1..0}$	Timeout Coefficient: Used by Telegram Analysis Unit 0 0 21.3 µs (50% less) 0 1 42.7 µs (Default and Initial value) 1 0 64.0 µs (50% more) 1 1 85.4 µs (100% more)
$WS_{1..0}$	Minimum number of Waitstates: Used by Traffic Memory Controller for all TM accesses made by host CPU and MVBC, as well as accesses to Internal Registers 0 0 0 waitstates inserted 0 1 1 waitstates inserted 1 0 2 waitstates inserted 1 1 3 waitstates inserted
$ARB_{1..0}$	Arbitration Strategies: Used by the Arbitration Controller 0 0 The CPU has the highest priority (recommended operation) 0 1 The MVBC has the highest priority 1 0 Traffic Memory is locked to allow CPU accesses only 1 1 The CPU has the highest priority except when contents of Transmission or Receive Buffer of the MVBC are transferred from/to the Traffic Memory.
UTS	Use Test Sink Port (TSNK) 1 The MVBC checks TSNK and no other port when a Slave Frame is received. Used for testing and diagnostics, i.e. transferring Process Data over internal loop-back. 0 Normal operation Attention: TSNK is equivalent to MSNK
UTQ	Use Test Source Port (TSRC) 1 The MVBC checks TSRC and no other port when a Slave Frame is sent. Used for testing and diagnostics, i.e. transferring Process Data over internal loop-back. 0 Normal operation Attention: TSRC is equivalent to MSRC

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Symbol	Description
MAS	MVBC is permitted to send Master Frames 1 The MVBC is allowed to send Master Frames 0 The MVBC is not allowed to send Master Frames (Slave device only) Attention: If MAS is set from '1' to '0' while the MVBC is busy sending a manually initiated Master Frame (SMFM bit, see MR, section 3.5.1), the current Master Frame will still be sent. If automatic sending is in progress (SMFA or SMFT), then the current Master Frame will be transmitted and sending the remaining frames will be suspended until MAS changes back to '1'. Canceling sending Master Frames is accomplished by writing '1' to the CSMF-Bit in the MR.
RCEV	Receive Event Frames (allow participation) 1 The MVBC reacts to all MF containing Event Polls (F-Code=9,13,14). To avoid continuous message transmission, the bits EA0 and EA1 (See Master Register MR) shall be set to '0' and the event ports EF0 and EF1 shall be declared as sinks or passive before activating RCEV. 0 The MVBC does not react to Event Polls. Attention: If RCEV is set from '1' to '0' while the MVBC is participates on event arbitration, then participation will be suspended until RCEV changes back to '1'. Canceling participation on event arbitration is accomplished by writing '1' to the corresponding EC-bits found in the MR.
$IL_{1..0}$	Initialization Level 0 0 Software reset of MVBC, all relevant bits are set to initial state. Data communication stops. If a frame is still transmitted, then the transmission will be completed. See Appendix E: Reset Behavior. 0 1 Configuration Mode: The MVBC does not participate at or listen to MVB traffic. The timeout mechanisms in the Telegram Analysis Unit stay disabled. This level is useful to configure MVBC registers without affecting bus traffic. 1 0 Self test Mode: In this mode, local loop-back between the two outgoing and incoming serial bus lines is established. In this mode, the pins OC and SF remain inactive in order to prevent interfering bus traffic. 1 1 Full operation mode

Table 3.5: Status Control Register (SCR)

3.5.2 Master Registers (MR, MR2)

The Master Register (MR), along with the Dispatch Pointer Register (DPR) provides dashboard type functions to pass instructions to the MCU. It is organized in such a way so multiple independent software tasks can access this register without interfering among each other. Its principal functions include

- Signing up and canceling participation on Event Arbitration
- Dispatching Master Frames (Bus Administrator function)
- BUSY-Indicator (MCU is busy processing ports)

Master Register (MR): Address 0yFA0H

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	$PAR_{1..0}$		$EA_{1..0}$		$EC_{1..0}$		BUSY	CSMF	$SMF_{1..0}$		SMSM	$C_{4..0}$				
Init. Value:	00		00		00		0	0	00		0	all 0				
CPU Acc.:	R		RW1		R0W1		R	R0W1	RW1		RW1	RW				
MVBC Acc.:	rw		rw0		r		w	rw0	rw0		rw0	rw				

Symbol	Description
$PAR_{1..0}$	Indicates that MVBC is participating on Event Arbitration; Bit 1 = Related to Event type 1 Bit 0 = Related to Event type 0 0 No participation 1 Participation
$EA_{1..0}$	Event Announced by software Bit 1 = Related to Event type 1 Bit 0 = Related to Event type 0 0 No effect 1 Event announced. The MVBC participates at the next event round for selected Event Type
$EC_{1..0}$	Event Announcement Cancellation Bit 1 = Related to Event type 1 Bit 0 = Related to Event type 0 0 No effect 1 Cancels announced event and any form of participation. EA*i* and PAR*i* will be cleared. (*i* = selected Event Type) Read: Always zero
BUSY	Busy Sending Master Frame and waiting for its Slave Frame 0 Indicates that no data transfer is in progress and the MVBC is ready to send next Master Frame immediately. 1 MVBC is not yet ready to send next Master Frame. Either, the previous Master Frame has not yet been sent, or the Slave Frame has not yet arrived, or automatic dispatching is still in progress. If no Slave Frame is received, the MVBC times out and clears this bit. Exceptions: If, for any technical problems, the transmitted Master Frame does not arrive at the Decoder, then the Telegram Analysis Unit will automatically assert BTI after 1.3 ms. This signal will clear the BUSY-Bit. On the other hand, if the Master Frame is corrupted, then the EMF (Erroneous Master Frame) Interrupt is asserted and the BUSY-Bit is cleared automatically.

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Symbol	Description
CSMF	Cancel Sending Master Frames 0 No action 1 Clears pending SMFE, SMFT, SMFM and SMFA requests. This mechanism cancels any scheduled MF-transmission or MF-transmission already in progress. If a telegram is transferred meanwhile, then the MVBC completes the transfer and sends no MF afterward. Read: Always zero
$SMF_{1..0}$	Send Master Frames Automatically from MF-Tables (3 options): Write access: Actions 0 0 No action 0 1 SMFA issued (Automatic Mechanism): Start processing MF-Table pointed to by the DPR immediately. The bits C4..0 indicate table size. Attention: This bit can be activated by the MVBC when the Universal Timer 1 reaches zero (given it is active) and SMFT is set to '1', or when the contents of MR2 are moved to MR when the AMFX-Interrupt occurs. End of MF-Table is indicated with the AMFX-Interrupt. The interrupt leads to a transfer from DPR2 to DPR and from MR2 to MR in order to process the next MF-Table if assigned. 1 0 SMFT issued (Timed Mechanism): Start processing MF-Table pointed to by DPR at the moment the Universal Timer 1 reaches zero (precondition: Timer 1 must be active). At that moment, SMFT changes to SMFA and processing starts as if an SMFA has been issued. This command is suitable for precisely timed MF-distribution. 1 1 SMFE issued (Empty MF-Table declared): The MVBC transmits no Master Frames, but waits until the Universal Timer 1 reaches zero. At that instance, the interrupt AMFX is issued. This interrupt leads to an Internal Register transfer from MR2 to MR and DPR2 to DPR in order to process the next MF table. It is useful to handle empty time slots. Attention: Only one of the three request can be submitted. A different request will be ignored until the request has been processed or canceled. Read access: Information on type of request submitted: 0 0 No request pending 0 1 SMFA requested 1 0 SMFT requested 1 1 SMFE requested
SMFM	Send Master Frame Manually Write access: 0 No action 1 Send Master Frame manually. The Master Frame body to be sent will be retrieved from TM location 0yE00H (Master Frame Slot). The automatic Master Frame Dispatcher is still active, then the manual Master Frame will be sent after the Master Frame Table has been completed. Read access: Information on request submitted 0 No SMFM request pending 1 SMFM requested

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Symbol	Description
$C_{4..0}$	Size of Master Frame Table. Write access: 1..31 Specifies Master Frame Table of size 1..31 respectively 0 Specifies Master Frame Table of size 32 Attention: Use SMFE to specify an empty Master Frame Table (0 entries). Attention: This value will only apply if SMFA or SMFT is requested with the same write access. $C_{4..0}$ will also be updated to the value written if SMFE is requested, but in this case, the value is ignored. All other accesses, where $SMF_{1..0}$ equals '00' will keep $C_{4..0}$ unchanged. Read access: Number of Master Frames to be sent out. With every Master Frame sent, the value will be decremented by 1. If 0 is specified for 32 Master Frames, then the first decrement leads to a value of 31.

Table 3.6: Master Register (MR)

The secondary Master Register (MR2) is used along with the corresponding Dispatch Pointer Register (DPR2) to place *advance requests* to send Master Frames while MF-transmission is in progress. Details are handled in section 4.9. At the moment the AMFX Interrupt occurs, then the contents of MR2 are transferred to MR7..0 and MR2 returns to zero. The upper halfword of MR2 is not used.

Secondary Master Register (MR2): Address 0yFA4H

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	-								$SMF_{1..0}$		SMSM	$C_{4..0}$				
Init. Value:	-								00		0	all 0				
CPU Acc.:	all 0								RW1		RW1	RW				
MVBC Acc.:	-								rw0		rw0	rw				

See MR (Table 3.6) for bit descriptions.

Table 3.7: Secondary Master Register (MR2)

3.5.3 Dispatch Pointer Register (DPR, DPR2)

The DPR contains the pointer to address the MF-Table when a MF-Table is to be processed. The table size is specified in MR.

Dispatch Pointer Register (DPR): Address 0yFA8H

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	$DPR_{15..2}$														-	
Init. Value:	0														all 0	
CPU Acc.:	RW														-	
MVBC Acc.:	rw0														-	

The contents of the Secondary Dispatch Pointer Register (DPR2) are transferred to DPR when the AMFX interrupt occurs.

Secondary Dispatch Pointer Register (DPR2): Address 0yFACH

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	$DPR2_{15..2}$														-	
Init. Value:	0														all 0	
CPU Acc.:	RW														R0	
MVBC Acc.:	rw0														-	

Symbol	Description
$DPR_{15..2}$ $DPR2_{15..2}$	Dispatch and Secondary Dispatch Pointer Value The start address to the Master Frame Tables are always aligned in a way so the lower two bits are zero. If the whole 16-bit word ($DPR_{15..0}$) is considered, then this whole word represents the pointer to the Master Frame Table, in units of 4 bytes. See also section 2.7 for more information on the pointer format.

Table 3.8: Dispatch Pointer Register (DPR)

3.5.4 Queue Management

The Queue Management is responsible for Message Queues. Queues are referenced when the QA-bit in the PCS is active. The queue is retrieved by accessing the Queue Descriptor Table. Then, a Linked List Record (LLR) is retrieved in order to access the Message Data block and the pointer to the next LLR.

Following interrupts are available to report queued data transfers and exceptions: If all records of one of the two Transmit Queues have been sent, then one of the following interrupts may occur:

"Transmit Queue 0 Complete" (TQ0C)

"Transmit Queue 1 Complete" (TQ1C, along with TQ0C)

If TQ1C is asserted, then TQ0C is asserted, too. Reason: The MCU checks Queue 0 before Queue 1. If both Transmit Queues are empty or do not exist, then the interrupt

"Transmit Queue Exception" (TQE)

is asserted. The MVBC cannot send any data. If the Receive Queue is full after receiving the message, then the interrupt

"Receive Queue Complete" (RQC)

is asserted. However, if the queue is already full before the reception, then the data gets lost and following interrupt occurs:

"Receive Queue Exception" (RQE).

3.5.5 Device Address Read & Store Unit

The Device Address is supplied via the 12-bit Device Address ($DA_{11..0}$) pins into the MVBC. This Device Address must stay constant since the MVBC references these pins throughout its operation. The Telegram Analysis Unit compares the Device Address with the address given in the Master Frame and passes the results to the MCU. The effective Device Address can be read from the Device Address Override Register (DAOR).

An override mechanism allows the user to let a software-defined value override the original Device Address. Overriding is enabled if a protection key is written to the Device Address Override Key (DAOK).

Enabling DA override:

- Write a value to DAOR. When DAOR is read, then the contents of the DA11..0 pins are still returned.
- Write 94H to DAOK. Reading DAOR now returns the new DA.

Disabling DA override:

- Write 49H to DAOK. Reading DAOR now returns the hardware DA.

3.5.5.1 Device Address Registers (DAOR, DAOK)

Device Address Override Register (DAOR): Address 0yFD8H

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	-				$DA_{11..0}$											
Init. Value:	all 0				all 0											
CPU Acc.:	R0				RW											
MVBC Acc.:	-				r(w)											

Symbol	Description
$DA_{11..0}$	Device Address Write access: New device address is written into DAOR, regardless of value of DAOK. Read access: If SW-overriding is not set, then the written device address stays hidden and the effective hardware device address (supplied via pins $DA_{11..0}$) is issued. If SW-overriding is set, then the written device address is returned.

Table 3.9: Device Address Override Register (DAOR)

Device Address Override Key (DAOK): Address 0yFDCH

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	-								$K_{7..0}$							
Init. Value:	all 0								00H (disabled)							
CPU Acc.:	R0								RW							
MVBC Acc.:	-								r							

Symbol	Description
$K_{7..0}$	Override Key Write access: 94H Enables SW-overriding on Device Address: $DA_{eff} \Leftarrow$ DAOR(written) 49H Disables SW-overriding on Device Address: $DA_{eff} \Leftarrow$ DA(Input Pins) other: No effect Read access: FFH Indicates DA overriding enabled 00H Indicates DA overriding disabled

Table 3.10: Device Address Override Key (DAOK)

3.5.6 Address Logic

The Address Logic consists of two parts:

- Address Encoder
- Address Decoder

The Address Encoder uses the tables summarized in section 2.8, the parameters issued by the MCU and the Memory Configuration Register to generate addresses for MCU accesses to the Traffic Memory.

The Address Decoder analyzes the addresses issued by the CPU to the MVBC and Traffic Memory. If the address points to an Internal Register inside the Service Area, then the corresponding Internal Register is selected. Otherwise, the Traffic Memory Controller will be instructed to forward the access control signals to the TM. The address ranges for the Internal Registers are summarized in section 2.6.3.

3.6 Parallel Interface Configuration

3.6.1 Memory Configuration Register (MCR)

Memory Configuration Register (MCR): Address 0yF84H

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	$VERSION_{4..0}$					DMAD	$PO_{1..0}$		ICD	$MO_{1..0}$		$QO_{1..0}$		$MCM_{2..0}$		
Init. Value:						0	all 0		1	all 0		all 0		all 0		
CPU Acc.:	R					RW	RW		RW	RW		RW		RW		
MVBC Acc.:	constant value					R	r		r	r		r		r		

Symbol	Description
$VERSION_{4..0}$	MVBC Version 00H MVBC01 02H MVBC02A 03H MVBC02B 04H MVBC02C
DMAD	DMA Direct Function. The MVBC will activate address and data bus output drivers only if TMRDY\ becomes zero. 0 DMAD disabled (functionality like in MVBC01) 1 DMAD enabled.
$PO_{1..0}$	Port Memory Map Table Offset (affects all fixed locations) 0 0 Range 00000H - 3FFFFH 0 1 Range 40000H - 7FFFFH 1 0 Range 80000H - BFFFFH 1 1 Range C0000H - FFFFFH
ICD	Inter-Cycle Delay 0 ICD disabled (functionality like in MVBC01) 1 ICD enabled (this is the initial value)
$MO_{1..0}$	Master Frame Table Offset (affects MF-Tables) 0 0 Range 00000H - 3FFFFH 0 1 Range 40000H - 7FFFFH 1 0 Range 80000H - BFFFFH 1 1 Range C0000H - FFFFFH
$QO_{1..0}$	Queue Offset (a selects LLR's and Queue Data blocks) 0 0 Range 00000H - 3FFFFH 0 1 Range 40000H - 7FFFFH 1 0 Range 80000H - BFFFFH 1 1 Range C0000H - FFFFFH
$MCM_{2..0}$	Memory Configuration Mode 000 Mode 0 (16 K Bytes) 001 Mode 1 (32 K Bytes) 010 Mode 2 (64 K Bytes) 011 Mode 3 (256 K Byte) 100 Mode 4 (1 M Byte) Attention: All other modes are illegal.

Table 3.11: Memory Configuration Register (MCR)

Attention: If the user intends to move the Service Area by modifying MCR, the relocation will take place 41 ns after the write access has been completed (WR\ returning from '0' to '1'). A brief pause (1 clock cycle or 1 instruction) should be introduced in order to avoid accesses in the old MCM.

3.6.2 DMA Direct Mode

The MVBC02 can be connected to a bus system shared with other masters, e.g. a microprocessor. This mode must be activated by the CPU before allowing the MVBC to make any accesses to the bus. A small custom logic (PLD) is necessary to handle bus arbitration between a host CPU and the MVBC.

Advantages of DMA-Direct Mode (for smart I/O systems and small CPU systems):

- No dedicated memory chips needed for Traffic Memory (saves typically 2 chips).
- No address or data buffers needed to attach two bus systems (saves typically 5 chips)

This mode is only suitable for memory modules with fixed timing (e.g. SRAM, DRAM, etc)

If DMA-Direct-Mode is enabled, following applies if the MVBC (not CPU) accesses the Traffic Memory:

- The address and data bus pins are kept in high-impedance state as long TMRDY\ = '1'. Once this signal changes to '0', then the address and data bus pins are activated immediately.
- The wait-state counter inside the MVBC will start counting after TMRDY\ has changed to '0'. In the normal case, where DMA-Direct-Mode is inactive, the wait-state counter already starts counting at the beginning of an access.
- While TMRDY\ = '1', the MVBC will not time out after 64 clock cycles. Careful HW design is necessary to make sure that the external bus arbiter issues a correct TMRDY\-signal.

The following block diagram shows an example of the MVBC where DMA-Direct-Mode is utilized.

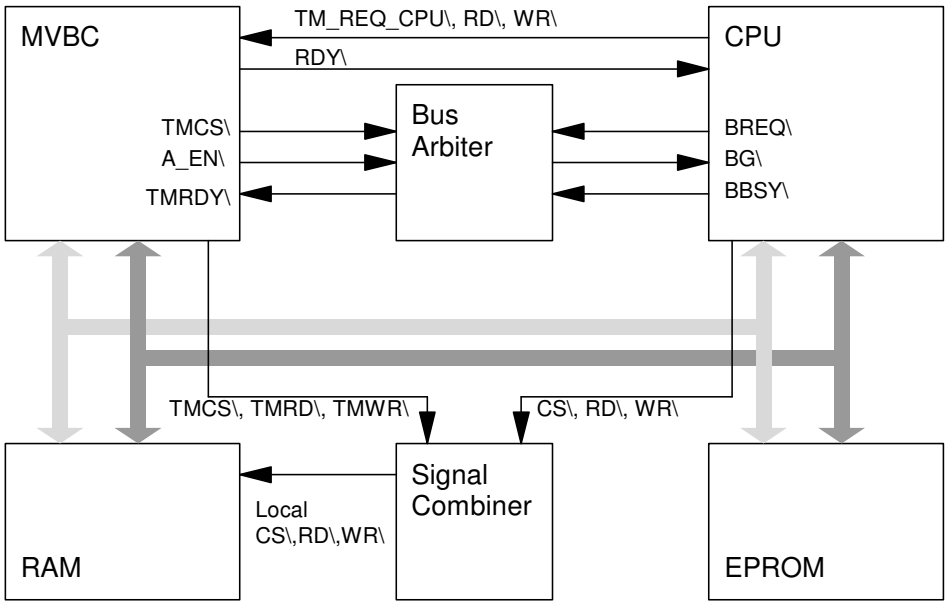


Figure 3.11: DMA Direct Mode Principle

The bus arbiter needs following signals:

TMCS\	Chip Select by MVBC
A_EN\	Distinguishes between CPU and MVBC mode to make sure only MVBC's accesses are considered.
TMRDY\	Bus acknowledge signal to MVBC
BREQ\	CPU Bus Request
BG\	CPU Bus Grant
BBSY\	CPU Bus Busy

When the external arbiter grants access to the MVBC, then following takes place:

At next rising clock edge, address and data bus are activated.

At following rising clock edge, TMRD\ or TMWR\ are activated.

At the end of the access sequence, TMWR\ is deactivated 1/2 clock cycles earlier in order to assure valid address and data bus at both rising and falling edge of TMWR\.

The fixed port arrangement to the Traffic memory (PCS, data areas, force tables, service area) as seen from the MVBC can be relocated in steps of 256 KB blocks, as long MCM is set to 3 or less. The same mechanism is used for assigning 256 KB blocks for message data queues and Master Frame tables. (Please check perspective of CPU accesses over again).

3.6.3 Port Assignment Offset

All MVBC accesses to fixed locations in the Traffic Memory (includes Port Index Tables, PCS, data area, force tables, also the Queue Descriptor table and Master Frame Slot) can be shifted up / down in steps of 256 KB within the full 1 MB addressing range. This functionality applies only if MCM is not equal to 4 (1 MB TM space).

This is useful if the same memory chip foreseen for the Traffic Memory shall also store some non-MVB-related information, e.g. program code (including boot code starting at address zero) and local data.

The shifting is controlled by $PO_{1..0}$ in the Memory Control Register and functions similarly as the MO or QO bits.

The internal MVBC registers, for example SCR, MCR, etc., are not affected by PO. They will always be located between 0xyF80 where y = { 3 for MCM=0, 7 for MCM=1 and F for MCM≥2 }.

The following figure illustrates the memory map. It also includes an example where a 1 MB memory area is filled up with huge MF-tables, message queues and a 256 KB port region (given MCM=3).

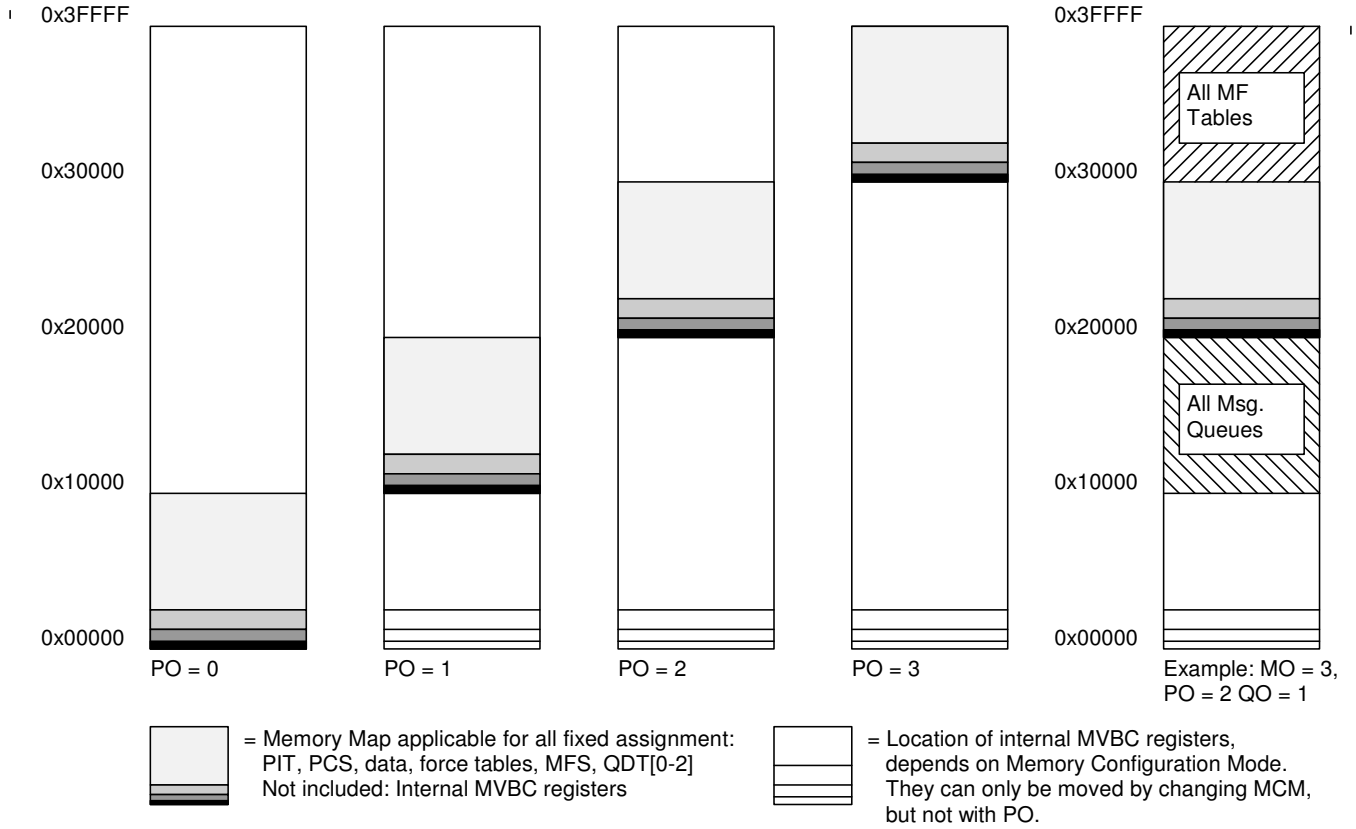


Figure 3.12: Mapping of Port Assignment Offset

3.6.4 Inter-Cycle Delay

An intercycle delay (ICD) has been introduce to maintain minimum of 2 rather than 1 clock cycle between any two consecutive MVBC accesses to Traffic Memory. This function is useful to handle very slow Traffic Memories which require a significant passive or precharge time. The ICD is configurable in both class 1 and 2/3/4 mode.

3.6.5 Arbitration Controller

The Arbitration Controller governs access rights to Traffic Memory between the CPU and the MVBC. The Arbitration Strategy is configurable with the ARB-bits found in the SCR (see section 3.5.1). The Arbitration Controller assures that the last TM access will be completed properly before the switch (from CPU to MVBC or vice versa) takes place.

The Arbitration Controller operates in one state at a time:

State	Description and Signals
CPU State	CPU accesses TM or Internal Registers. This is the initial state for class 2/3/4 mode. Signals: A_EN\ = 0 (active), MVBC address bus is inactive.
MVBC State	MVBC accesses TM. This is the initial state for class 1 mode. Signals: A_EN\ = 1 (inactive), MVBC address bus is active.

Table 3.12: Arbitration Modes

The following Arbitration Strategies are supported:

$ARB_{1..0}$ (see 3.5.1)	Description and Signals
0	CPU has highest priority all time Every time the CPU requests to access the TM or Internal Registers by activating TM_REQ_CPU\, the Arbitration Controller will switch from MVBC to CPU Mode immediately. The CPU can interrupt a series of subsequent TM accesses[1] made by the MVBC (i.e. transferring 16 data words). The MVBC cannot suspend a series of subsequent accesses made by the CPU. This is the recommended operation mode for fast CPUs.
1	MVBC has highest priority Every time the CPU requests to access the TM or Internal Registers, it must wait until the MVBC has completed accessing the TM. This does even apply if the MVBC makes a series of subsequent TM accesses. If the CPU makes a series of subsequent accesses, and the MVBC requests the TM, then the accesses will be suspended until the MVBC has finished.
2	CPU locks Traffic Memory for Memory Test Using this strategy, the MVBC can not make any accesses to TM. This strategy must not be active for a too big time period if the MVBC handles data communication at that time. This strategy guarantees full data consistency on the TM, so on-line back-ground tasks, which run RAM-test software, can make use of this strategy.
3	Mixed Priority Strategy CPU has highest priority (Strategy 0 applies) except when the MVBC transfers data between the Traffic Memory and Transmit as well as Receive Buffer (Strategy 1 applies). CPU accesses cannot break apart any such transfers. This strategy has been introduced to guarantee data consistency while data is sent or received.

[1] The term *subsequent accesses* means holding TMCS\ active while reading or writing with TMRD\ or TMWR\. The CPU must hold TM_REQ_CPU\ active during multiple accesses in order to perform subsequent accesses.

Table 3.13: Arbitration Strategies

Attention: If strategy 0 is selected, then the user must be aware not hold the TM by keeping TM_REQ_CPU\ active over long time periods. In this case, data may arrive from the MVB and cannot be stored in the TM. This may result to loss of received data.

If strategy 2 is selected during normal system operation in order to run on-line RAM tests in a background task, the lock time must be kept to a minimum (i.e. for max. 6 consecutive TM accesses).

Whenever an arbitration switch takes place, A_EN\ and the address or data pin drivers will never be active at the same time. A guard time of 1-2 clock cycles is introduced to disable A_EN\ and enable the drivers and vice versa.

3.6.5.1 Data Transfer Mode

If Arbitration Mode 3 is selected, then the MVBC calls for high priority when following accesses to the TM are made:

- Data transfer (Data Area, queued data), including accesses to PCS words which take place immediately (no pauses) before and after the data transfer
- Queue pre- and postprocessing
- One access pair for sink-time supervision: read + write TACK

3.6.5.2 Voluntary Action

If the MVBC does not operate in class 1 mode, and has completed a series of TM accesses, it will instruct the Arbitration Controller to commit a voluntary action, namely to return to CPU mode. This mechanism helps saving access time since the CPU does not need to wait until a switchover has taken place.

3.6.6 Traffic Memory Controller (TMC)

The Traffic Memory Controller TMC operates closely with the Arbitration Controller and Address Logic. The Traffic Memory Controller handles the following accesses:

- CPU accesses to Traffic Memory
- CPU accesses to Internal Registers inside MVBC
- MVBC accesses to Traffic Memory

The principal functions of the TMC are:

- Forwarding CPU memory access signals to the TM when the CPU accesses the TM
- Processing CPU signals when accessing Internal Registers
- Generating control signals to TM when the MVBC accesses the TM
- Maintaining minimum specified waitstate count for all accesses
- Proper control signal handling while the Arbitration Controller switches between CPU and MVBC mode.

Timing Diagrams:

The TMC follows the specifications given on the attached timing diagrams (see section 9.2).

3.6.6.1 CPU Signals

If the Arbitration Controller resides in CPU mode, then the memory control signals originating from the CPU are directly forwarded to the Traffic Memory, given the address does not point to the address space reserved for Internal Registers:

Always:	TM_REQ_CPU\	→	TMCS\ and D_EN\
If TM_REQ_CPU\ is active:	RD\	→	TMRD\
	WR\	→	TMWR\ and DIR
	A_EN\	→	is always active in CPU Mode
	RDY\	→	0 → 1 immediately at begin of access
			1 → 0 when access has been completed

RDY\ exhibits a "Normally Ready" behavior: The MVBC is *ready* until an access is made. The MVBC becomes *not ready* until the data is available. When the following conditions are met, then the MVBC becomes *ready* again:

- The CPU has waited until the Arbitration Controller switched to CPU mode (if this has not yet taken place)
- The minimum number of waitstates (specified by WS1..0, see SCR) has elapsed
- TMRDY\ has turned active (not applicable if Internal Registers are accessed).

TMRDY\ must conform with the "Normal Ready" behavior. If the incoming Ready-signal TMRDY\ is tied to zero, then the outgoing RDY\-signal is generated explicitly by the waitstate counter in order to abide the waitstate requirements. If TMRDY\ is connected to a memory system (i.e. DRAM controller, Dual-Port RAM), then the RDY\-

signal will be forwarded to the CPU as long the minimum waitstate count has elapsed.

If TM_REQ_CPU\ is inactive, then RD\ and WR\ do not affect the MVBC nor the Traffic Memory. If Internal Registers are accessed, then TMCS\, TMRD\ and TMWR\ remain passive. The MVBC recognizes the access, performs the necessary Internal Register read or write operation, and obeys the specified waitstate requirements.

Following signaling methods are legal to start read and write accesses:

TM_REQ_CPU\	RD\	WR\	Access Started	TMCS\ [1]	TMRD\ [1]	TMWR\ [1]	D_EN	DIR\
1	X	X	No access	1	1	1	1	1
↓	1	1	Chip select	↓	1	1	↓	1
0	↓	1	Read access	0	↓	1	0	1
↓	↓	1	Read access	↓	↓	1	↓	1
↓	0	1	Read access	↓	↓	1	↓	1
0	1	↓	Write access	0	1	↓	0	↓
↓	1	↓	Write access [2]	↓	1	↓	↓	↓
↓	1	0	Write access [2]	↓	1	↓	↓	↓
0	↓	0	Illegal	0	-	-	0	-
0	0	↓	Illegal	0	-	-	0	-
0/↓	↓	↓	Illegal	0	-	-	0	-

1 Inactive if Internal Registers are accessed
2 Activating TMCS\ and TMWR\ simultaneously may violate setup timing specifications of available RAM chips. Consult the data sheets first.

Table 3.14: Starting TM Accesses

If the CPU initiates an access and MVBC mode is still effective, then the TMC waits until the arbitration switch has taken place. During the arbitration switch, the MVBC guarantees that TMCS\ and D_EN\ become active 1 clock cycle before TMRD\ or TMWR\ becomes active.

The access to TM (or Internal Registers) is complete when RDY\ returns from '1' back to '0'. Following signaling methods are legal to stop or cancel read and write accesses:

TM_REQ_CPU\	RD\	WR\	Access Started	TMCS\ [1]	TMRD\ [1]	TMWR\ [1]	D_EN	DIR\
↑	0/↑	1	Stops read access	↑	↑	1	↑	1
0	↑	1	Stops read access	0	↑	1	0	1
↑	1	0/↑	Stops write access	↑	1	↑	↑	↑
0	1	↑	Stops write access	0	1	↑	0	↑
0	↑	↓	Illegal [2]	0	↑	↓	0	↓
0	↓	↑	Illegal [2]	0	↓	↑	0	↑

1 Inactive if Internal Registers are accessed
2 See restrictions listed below

Table 3.15: Stopping TM Accesses

Restrictions:

- Between any two accesses made to the Traffic Memory, the CPU must stop the first access according to the table shown above and wait for at least 41 ns (1 clock cycle) before the next access can be started.
- RD\ must not be activated while deactivating WR\ or vice versa during the period TM_REQ_CPU\ is active.

- A block access consisting of multiple read or write accesses can be realized by holding TM_REQ_CPU\ active while all accesses are performed with toggling RD\ and WR\. The same block access may cover Traffic Memory and Internal Registers. It is forbidden to keep RD\ or WR\ active while changing the address every few clock cycles. This access mechanism exists in common RISC processors and must be deactivated for the TM.

3.6.6.2 Waitstate Generator

The waitstate generator is available to handle slower or variable-timed Traffic Memory RAMs (i.e. DPRAMs) or slow data paths between CPU and MVBC. The waitstates affect

- CPU accesses to Traffic Memory
- CPU accesses to Internal Registers inside MVBC
- MVBC accesses to Traffic Memory

The minimum number of waitstates can be configured with the WS-bits found in the SCR. Allowed values are 0, 1, 2 and 3 waitstates. Each waitstate means prolonging the access by one 24 MHz clock cycle.

For accesses to the TM, the number of waitstates can be extended to 64 cycles by holding TMRDY\ at '1'. The limit of 64 cycles is necessary since Slave Frame data must be transmitted within 4 µs after the Master Frame has been received. It also prevents deadlock situations at the CPU or MVBC. When this limit has been reached, the MVBC assumes that it accessed a bad memory location and completes the access sequence, regardless if the access turned out successfully or not.

Attention: 64 Waitstates is acceptable for data sources. For sinks however, the overall time required to make all write accesses must not exceed the duration of one 16-bit frame. Otherwise, the next Master Frame arrives while the MVBC is still busy processing the last port.

Attention: In Class 1 Mode, it is legal to tie the TMRDY\-signal to +VDD if the attached peripherals require a very long access time.

The $WS_{1..0}$ bits, in conjunction with the TMRDY\ pin shall be used as follows to configure the number of waitstate to be generated:

$WS_{1..0}$	TMRDY\	Number of waitstates inserted	TMRDY\	Number of waitstates inserted[1]
00	0	0	1	64 or at least 0 if TMRDY\→0
01	0	1	1	64 or at least 1 if TMRDY\→0
10	0	2	1	64 or at least 2 if TMRDY\→0
11	0	3	1	64 or at least 3 if TMRDY\→0

[1] The minimum number of waitstates is always inserted regardless of the TMRDY\ level.

Table 3.16: Waitstate Settings

3.6.6.3 TM Accesses made by MVBC

While MVBC Mode is effective, the TMC will handle TM read and write accesses instructed by the MCU and sink-time supervision logic. A_EN\ and D_EN\ are held at '1' and DIR at '0'.

3.6.7 Bus Multiplexer, Data Forcing Network

The Bus Multiplexer handles internal bus traffic and routing in the MVBC. In addition, the bus multiplexer supports

- Byte swapping (needed to access CS, 8-bit Port Indexes, byte order compensation)
- Forcing Process Data

Forcing data is performed one word at a time:

- One Force Mask word is read from the Force Table
- One Force Data word is read from the Force Table
- The outgoing data is read from the Traffic Memory, forced and forwarded to the Transmit Buffer (TXB)

or

- The incoming data is retrieved from the Receive Buffer (RXB), forced and then written to the Traffic Memory.
- The remaining words are processed

The Boolean formula applied for forcing is found in section 2.5.

3.7 Interrupt Logic

The Interrupt Logic can handle up to 32 interrupts which originate from functional units inside the MVBC and from external interrupt pins. The Interrupt Logic has been designed in order to allow efficient cooperation with software. The programmer can choose whether to use fixed-priority interrupt vectors, check the bits in the Interrupt Status Register, or use a combination of both.

The Interrupt Logic consists of two parts which operate independently. Each part is equipped to handle 16 interrupts, provides their own output pins INT0\ and INT1\, and one set of four registers described below:

- Interrupt Mask Registers (IMR0, IMR1)
- Interrupt Pending Registers (IPR0, IPR1)
- Interrupt Status Registers (ISR0, ISR1)
- Interrupt Vector Registers (IVR0, IVR1)

The Interrupt Pending Register (IPR*i*) captures the interrupt request signals from the outside (II3..0 pins) and MVBC functional units. The Interrupt Mask Register (IMR*i*) is used to keep interrupt signals from penetrating from the (IPR*i*) to the Interrupt Status Register (ISR*i*) and to the Interrupt Vector Register (IVR*i*). Any active bit inside the ISR*i* will trigger the outgoing interrupt signal INT*i* \.

Attention: Each part of the Interrupt Logic also contains a hidden state variable: *frozen* or *not frozen* (released). Details about this mechanism is described in section 3.7.1. Freezing Interrupt Logic 0 has no effect on Interrupt Logic 1 or vice versa.

3.7.1 Interrupt Handling Mechanism

Following operation occurs on the falling edge of an incoming interrupt signal:

- The interrupt request *k* is registered in bit *k* in IPR*i* (notation: IPR*i* [*k*] = '1').

- If (ISR*i* is *not frozen*) then
  if (IMR*i* [*k*] = '1' (*not masked*)) then
  the interrupt is forwarded to the ISR*i* [*k*]. At the same time, IPR*i* [*k*] is reset.
  else if (IMR*i* [*k*] = '0' (*masked*)), then
  IPR*i* [*k*] is reset and the Interrupt Logic forgets the interrupt request.
  else, (if ISRi is *frozen*), then
  the value is held in the IPR*i* [*k*] until the ISRi is no longer *frozen*. If the same interrupt occurs for the second time and ISR*i* is still *frozen*, then the second interrupt is *swallowed*. Avoiding this case is a software responsibility.

- If ISR*i* [*k*] becomes active, then the outgoing interrupt signal INT*i* \ changes to '0'. At the same time, the interrupt vector is computed from the ISR*i* and made visible in IVR*i*

- The software can check the interrupts using two methods:
  a. by reading the interrupt vector from IVR*i*, or
  b. by examining the ISR*i* directly.

  Read accesses to the IVR*i* as well as to the ISR*i* will automatically *freeze* the ISR*i* and deactivate the outgoing INT*i* \-pin.

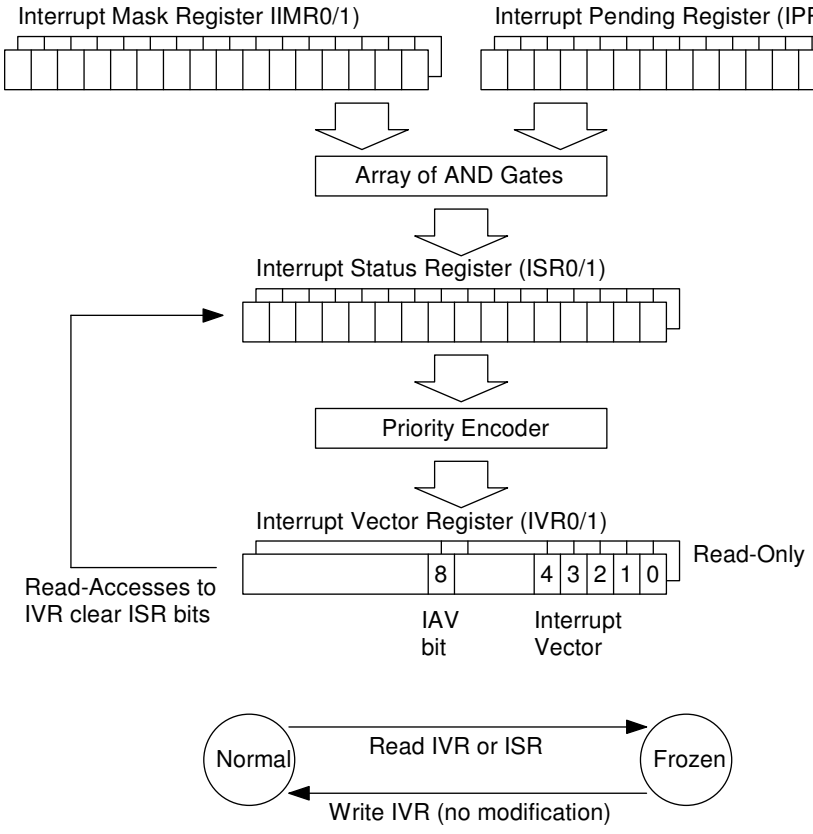
  In case (a.), the ISR*i* -bit pointed to by the vector is automatically cleared when reading the interrupt vector. After this, the IVR*i* will automatically provide the vector to the next lower priority interrupt found in the ISR*i* or indicate that no more interrupts are to be serviced.

  In case (b.), the user shall write a bit pattern to ISR*i* in order to clear one or more interrupts simultaneously. This write access will not touch the operational state of the ISR*i* (*frozen* or *not frozen*).

- The ISR*i* can be released by writing any value to IVR*i* (regardless which value is written, the value is ignored). This release operation shall be undertaken when the CPU has serviced all interrupts which appeared in the ISR*i*. After releasing, the ISR*i* is no longer frozen and the new interrupts, which accumulated in the IPR*i*, propagate into the ISR*i*. If interrupts are present again, the output signal INT*i* \ becomes active again.

Though this mechanism uses a fixed priority scheme, the priority rules the order how the interrupts are to be serviced. None of the lower priority interrupts can be overrun by higher priority interrupts.

Interrupt Signal path:



Two independent "Frozen" flags exist for both controller 0 and 1

Figure 3.13: Interrupt Control Data Flow Structure

3.7.2 Interrupt Sources

Abbre-viation	Name	Brief Description, (MVBC Functional Unit)
TI1	Timer Interrupt 1	Indicates that the Timer 1 has reached zero. (Universal Timer)
TI2	Timer Interrupt 2	Indicates that the Timer 2 has reached zero. (Universal Timer)
MFC	Master Frame Checked	Indicates Master Frame being retrieved from TM (MF Slot or MF Table) and clearance is given to transmit it. This interrupt may occur before actual transmission starts. Usage: Information to Bus Administrator Software that next MF can be sent. (Main Control Unit)
SFC	Slave Frame Checked	Indicates completed transfer of a Slave Frame, regardless if an error has occurred or not. This interrupt does not occur if a SF Reply Timeout occurs. RTI would occur instead. (Telegram Analysis Unit)
EMF	Erroneous Master Frame	Indicates that an erroneous Master Frame has been received. This interrupt may occur at any device, even at the device which has sent the Master Frame. (Telegram Analysis Unit)
ESF	Erroneous Slave Frame	Indicates that an erroneous Slave Frame has been received. This interrupt may occur at any device, even at the device which has sent the Slave Frame. (Telegram Analysis Unit)
DMF	Duplicate Master Frame	Indicates that two duplicate Master Frames have been received within Slave Frame reply time (default value: 42.7 µs). (Telegram Analysis Unit)
DSF	Duplicate Slave Frame	Indicates that two duplicate Slave Frames have been received within the time a Slave Frame has been expected within Slave Frame reply time (default value: 42.7 µs). This is one possible outcome of a collision. (Telegram Analysis Unit)
BTI	Bus Timeout Interrupt	Indicates that no Master Frame has been received within 1.3 ms. Usage: Informs Bus Administrator Software to attain Master privileges in order to transmit a Master Frame itself. (Telegram Analysis Unit)
RTI	Reply Timeout Interrupt	Indicates that, after reception of a Master Frame, a Reply Timeout has occurred, meaning no Slave Frame has been received within the specified Reply Timeout period (default value: 42.7 µs). (Telegram Analysis Unit)
FEV	Frames Evaluated Interrupt	Indicates that 65,536 frames have been checked and that the total number of erroneous telegrams can be found in the Error Counter Register (EC). (Telegram Analysis Unit)
DTI*i* *(i=1..7)*	Data Transfer Interrupt *i*	Interrupt is asserted upon successful data transfer. The interrupts are specified in the PCS of the affected ports. (Main Control Unit)
XQE	Transmit Queue Exception	Indicates that both Transmit Queues are either empty or nonexistent. No message is sent. (MCU Queue Management)
RQE	Receive Queue Exception	Failed attempt to receive a message into a full or non-existent Receive Queue. The received message is lost. (MCU Queue Management)
XQ0C	Transmit Queue 0 Complete	Indicates that the end of the queue 0 has been reached and all the contents have been successfully sent to the MVBC for transmission. It occurs after message transfer. (MCU Queue Management)
XQ1C	Transmit Queue 1 Complete	Indicates that the end of the queue 1 has been reached and all the contents have been successfully sent to the MVBC for transmission. It occurs after message transfer. (MCU Queue Management)
RQC	Receive Queue Complete	Indicates that the Receive Queue is now full. No data has been lost yet. (MCU Queue Management)
XI*i* (i=0..3)	External Interrupts	Four external interrupt inputs (II3..0 pins). Incoming interrupts are recognized by the falling edge. (Interrupt Logic)
AMFX	All Master Frames	Indicates that the last Master Frame has been retrieved from the Traffic Memory is now subject to be transmitted. At the moment Interrupt MFC occurs, the last Master Frame has been sent into the bus. (Main Control Unit)

Table 3.17: Interrupt Sources

3.7.3 Interrupt Pending Register (IPR0, IPR1)

All internal and external interrupts are collected in one of the Interrupt Pending Registers (IPR*i*). One bit is assigned to each interrupt. If the ISR*i* is frozen, then the interrupts accumulate in the IPR*i* until the ISR*i* is released. Writing '1's to IPR*i* will cause interrupts intentionally in order to test the interrupt controller.

Interrupt Pending Register (IPR0): Address 0yFB0H

Bit Number	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	EMF	ESF	DMF	DSF	AMFX	MFC	SFC	RTI	BTI	DTI7	DTI6	DTI5	DTI4	DTI3	DTI2	DTI1
Init. Value:	all 0															
CPU Acc.:	RW															
MVBC Acc.:	rw															

Interrupt Pending Register 1 (IPR1): Address 0yFB4H

Bit Number	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	TI2	XI3	XI2	XQE	RQE	XQ1C	XQ0C	RQC	FEV	Not used				TI1	XI1	XI0
Init. Value:	all 0									0				all 0		
CPU Acc.:	RW									R0				RW		
MVBC Acc.:	rw									-				rw		

Symbol	**Description**
All Interrupts	Read Access: 0 Affected interrupt is not pending 1 Affected interrupt is pending Write Access: 0 Remove pending interrupts (used to test interrupt mechanism) 1 Apply pending interrupts (used to test interrupt mechanism)

Table 3.18: Interrupt Vector Registers (IPR*i*)

3.7.4 Interrupt Mask Registers (IMR0, IMR1)

The Interrupt Mask Registers (IPR*i*) allow masking any interrupt source. If a bit in the IMR*i* is '1', then the corresponding interrupt will propagate from the IPR*i* to the ISR*i*, given that ISR*i* is not frozen. Otherwise, if the bit equals to '0', then the interrupt will be filtered away. The Interrupt Mask Registers allow read and write accesses, but are not altered by the MVBC.

Interrupt Mask Register (IMR0): Address 0yFB8H

Bit Number	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	EMF	ESF	DMF	DSF	AMFX	MFC	SFC	RTI	BTI	DTI7	DTI6	DTI5	DTI4	DTI3	DTI2	DTI1
Init. Value:	all 0															
CPU Acc.:	RW															
MVBC Acc.:	r															

Interrupt Mask Register 1 (IMR1): Address 0yFBCH

Bit Number	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	TI2	XI3	XI2	XQE	RQE	XQ1C	XQ0C	RQC	FEV	Not used				TI1	XI1	XI0
Init. Value:	all 0									all 0				all 0		
CPU Acc.:	RW									R0				RW		
MVBC Acc.:	r									-				r		

Symbol	Description
All Interrupts	Read Access: 0 Interrupt is masked away (disabled) 1 Interrupt is not masked (enabled) Write Access: 0 Apply masking (Affected interrupt(s) will no longer penetrate into ISR*i*.) 1 Remove masking (Affected interrupt(s) will no longer penetrate into ISR*i*.)

Table 3.19: Interrupt Vector Registers (IMR*i*)

3.7.5 Interrupt Status Registers (ISR0, ISR1)

The Interrupt Status Registers provide information about the sources which have generated an outgoing interrupt. A read access to an ISR*i* will automatically freeze the affected ISR*i*. Writing '0's to the affected bits will clear the bit. Writing '1's will cause no action.

Interrupt Status Register (ISR0): Address 0yFC0H

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	EMF	ESF	DMF	DSF	AMFX	MFC	SFC	RTI	BTI	DTI7	DTI6	DTI5	DTI4	DTI3	DTI2	DTI1
Init. Value:	all 0															
CPU Acc.:	RW0															
MVBC Acc.:	rw															

Interrupt Status Register 1 (ISR1): Address 0yFC4H

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	TI2	XI3	XI2	XQE	RQE	XQ1C	XQ0C	RQC	FEV	Not used				TI1	XI1	XI0
Init. Value:	all 0									0				all 0		
CPU Acc.:	RW0									R0				RW0		
MVBC Acc.:	rw									-				rw		

Symbol	Description
All Interrupts	Read Access: 0 Interrupt is set. 1 Interrupt is not set. Attention: Read accesses will freeze the corresponding interrupt controller, regardless of the value read. Write Access: 0 Clear interrupt. 1 No effect on contents. Attention: Any modification in the ISR*i* has immediate effect on the interrupt vector found in the Interrupt Vector Register IVR*i*.

Table 3.20: Interrupt Vector Registers (ISR*i*)

3.7.6 Interrupt Vector Register (IVR0, IVR1)

The Interrupt Vector Registers return the interrupt vector and provide a mechanism to freeze and release the ISR*i*. The IVR*i* is connected directly via a priority encoder (combinational logic) to the corresponding ISR*i*.

Interrupt Vector Register (IVR0): Address 0yFC8H

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	Not used							IAV	Not used				$VEC_{3..0}$			
Init. Value:	all 0							0	all 0				all 0			
CPU Acc.:	-							R	-				R			
MVBC Acc.:	-							w	-				w			

Interrupt Vector Register 1 (IVR1): Address 0yFCCH

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	Not used							IAV	Not used				$VEC_{3..0}$			
Init. Value:	all 0							0	all 0				all 0			
CPU Acc.:	-							R	-				R			
MVBC Acc.:	-							w	-				w			

Symbol	Description
IAV	Interrupt Available Indicates that at least one bit is set in the corresponding ISR*i* and that $VEC_{3..0}$ is an applicable interrupt vector.
$VEC_{3..0}$	Interrupt Vector. Read Access: If IAV=0, then $VEC_{3..0}$ = '0000'. Otherwise: Returns interrupt vector and automatically clears bit 2^($VEC_{3..0}$) in the ISR*i*. Consequence: The IVR*i* will be updated thereafter. Examples of data read: 0000 ISRi [15..1] = '0', ISRi [0] = '1' 0001 ISRi [15..2] = '0', ISRi [1] = '1', ISRi [0] = Don't Care : : : : 0010 ISRi [15..3] = '0', ISRi [2] = '1', ISRi [1..0] = Don't Care 1110 ISRi [15] = '0', ISRi [14] = '1', ISRi [13..0] = Don't Care 1111 ISRi [15] = '1', ISRi [14..0] = Don't Care Attention: Read accesses will freeze the corresponding interrupt controller, regardless of the value read. Write Access: Releases frozen state of affected interrupt controller (if frozen). The written value is ignored.

Table 3.21: Interrupt Vector Registers (IPR*i*)

3.7.7 Designers' Responsibilities

The HW designer must be aware that this Interrupt Logic uses quasi edge-driven inputs. The incoming interrupt signals are latched at the rising clock edge and double-sampled to detect a '1' to '0' transition. Therefore, these two levels shall be stable for at least 41.7 n (1 clock cycle).

Interrupts resulting from data transfer exceptions (EMF, ESF, DMF, DSF, RTI, BTI) will generate a copy of the Master Frame, too, but is stored in a separate register.

3.8 Universal Timers

The MVBC provides two general-purpose Universal Timers. Timer 1 can be used to start sending Master Frames (see Master Register, SMFT bit, section 3.5.1) at precise time intervals. Timer 2 is not directly used by the MVBC except that both timers can pass interrupts to the Interrupt Logic. The two timers have the following characteristics:

Timer 1:	Minimum Time:	10 µs	10 µs = 240 clock cycles
	Maximum Time:	ca 655 ms	10 µs x(216)
	Resolution:	10 µs	
	Interrupt:	TMR1	Timer 1 Interrupt
Timer 2:	Minimum Time:	250 ns	250 ns = 6 clock cycles
	Maximum Time:	ca 8.3 ms	125 ns x(216)
	Resolution:	125 ns	125 ns = 3 clock cycles
	Interrupt:	TMR2	Timer 2 Interrupt

Each timer consists of a 16-bit down-counter with automatic reload and manual reset mechanism. When a counter is active and its value reaches zero, then the output signal (TMR*i*\, *i*={1,2}) becomes active for three clock cycle (125 ns) and an interrupt is generated (TI*i*).

Each timer provides a Timer Counter Register (TC*i*) to hold the actual count value, a Timer Reload Register (TR*i*) to specify the period, and two control bits found in the Timer Control Register (TCR) to pause or reset the counter.

3.8.1 Timer Control Register (TCR)

Compared to the MVBC01, the timer control register of the MVBC02C contains additional control bits to select inter-frame spacing.

Timer Control Register (TCR): Address 0yFE0H

Bit Number	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	Not used						$IFS_{1..0}$		Not used		RS2	TA2	n. used	XSYN	RS1	TA1
Init. Value:	all 0						0	0	all 0		1	0	0	0	1	0
CPU Acc.:	-						RW		-		RW0	RW	-	RW	RW0	RW
MVBC Acc.:	-						r		-		R	R	-	r	r	R

Symbol	**Description**
RS1, RS2	Reset Timer 1, 2 0 The selected timer is set to zero. If the corresponding TA*i*-bit is active, then the output signal TMR*i*\ and the interrupt T*i*I\ is asserted and the counter reloads automatically with the value stored in the Timer Reload Register TR*i* and down-counting will continue. Otherwise, if the corresponding TA*i*-bit is zero, then the output signal and the interrupt are not asserted and the counter stays at zero. The signal and the interrupt will not be asserted if TA*i* is set to '1' afterward in order to restart the counter. 1 No action Read Access: 1 Always returned.
TA1, TA2	Timer Active 1, 2 0 Timer is halted. Output signal TMR*i*\ and generation of interrupts are suppressed. 1 Timer is running.
XSYN	External Synchronization 0 No synchronization 1 Timer 1 is synchronized (if timer is active) Timer 1 issues a pulse (TMR1\) and interrupt immediately (if timer is inactive)

$IFS_{1,0}$	Interframe Spacing 0 0 6 µs 0 1 4 µs 1 0 8 µs 1 1 12 µs

Table 3.22: Timer Control Register (TCR)

The Timer Reload Registers contain the automatic reload values for the respective Timer Counter Registers.

Timer Reload Register 1 (TR1): Address 0yFF0H
Timer Reload Register 2 (TR2): Address 0yFF4H

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	TR1, TR2															
Init. Value:	all 0															
CPU Acc.:	RW															
MVBC Acc.:	r															

These registers can be altered even while the counter is active. The new values become effective at the next re-load.

TRi Reload Value	Period on Timer 1	Period on Timer 2
0	10 us	125 ns (250 ns) [1]
1	20 us	250 ns
2	30 us	375 ns
(k)	(k+1)*10 us	(k+1)*125 ns
65535	655.35 ms	8.191875 ms

[1] Interrupt occurs every 125 ns, Timer signal TMRi \ every 250 ns. Reason: Pulse width = 125 ns.

Table 3.23: Timer Periods

The Timer Counter Registers contain the current count values. The values can be read and modified by the software *on-the-fly*. These registers can be altered while the respective timers are active or not. Writing a zero to one of these registers results to the same behavior as resetting them with writing '0' to the RS*i* -bit in the TCR.

Timer Counter Register 1 (TC1): Address 0yFF8H
Timer Counter Register 2 (TC2): Address 0yFFCH

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	TR1, TR2															
Init. Value:	all 0															
CPU Acc.:	RW															
MVBC Acc.:	rw															

3.8.2 External Synchronization

An external synchronization mechanism is supported for Timer 1. This mechanism can be enabled by setting the XSYN-bit (inside TCR) to 1. If enabled, the incoming interrupt signal II3\ will serve as the synchronization input. In order to prevent II3\ from generating interrupts, the Interrupt Mask Register must be set accordingly (See section 3.7.4). Synchronization takes place at the falling transition from '1' to '0', similarly done as for external interrupts. The synchronization is completed after two clock cycles.

The synchronization pulse invokes following actions:

- If the timer 1 is not active (TA1=0):

  A timer pulse is generated which leads to a Timer Interrupt, TMR1\ active for three cycles and MF dispatching being started if configured to do so.

- If the timer 1 is active (TA1=1):

  Timer Counter 1 (TC1) is set to zero. At the next 10 µs pulse, the reload takes place. Attention: The timer pulse occurs within 10 µs.

Applications:

Synchronized operation of multiple MVBCs which dispatch Master Frames to multiple MVBs at precisely synchronized time instances. Two variations are possible:

- Timer 1 of one MVBC is active and distributes its timer pulse to all other on-board MVBCs. Timer 1 of the other MVBCs is kept inactive
- Timer 1 in all MVBCs are active. After power-up, a synchronization pulse is passed into all MVBCs. This synchronization pulse may originate from an external unit, or from following outputs of one MVBC:

  - STROBE\ (for global synchronization)
  - TMR1\, TMR2\

  The synchronization pulse may be reissued sporadically. As long all MVBCs have been powered up or reset at the same time, the 10 µs pulses appear simultaneously and all MVBCs will operate perfectly synchronously.

3.9 Sink-Time Supervision Logic

The Sink-Time Supervision Logic helps to check whether data has been sent or received within a specified time interval. If the Sink-Time Supervision Logic is activated, then the TACK bits of a specified dock range are decremented by 1 at fixed time intervals. If a TACK value is already zero, then it will stay zero. The Sink-Time Supervision runs like a *background-task* in the MVBC, taking advantage of the idle periods of the MCU waiting for incoming Master or Slave Frames.

For every dock, the following steps are undertaken:

- Read TACK-Value (PCS, Word 3)
- If TACK is nonzero, then it is decremented by 1
- Write TACK-Value back to TM (only if the read TACK was not zero)

The Sink-Time Supervision Logic does not inform the CPU if one or more TACK bits have reached zero. The software is responsible to compare the TACK bits with a threshold value when retrieving (or depositing) data from (or to) the Traffic Memory.

3.9.1 Sink-Time Supervision Register (STSR)

The Sink-Time Supervision Register specifies the range of docks and supervision time interval. The user is responsible to avoid TM access overloading due to supervising too many docks within a too small time interval. See Figure 3.15 for limiting factors.

Sink-Time Supervision Register (STSR): Address 0yF8CH

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	$SI_{3..0}$				$R_{11..0}$											
Init. Value:	all 0				all 0											
CPU Acc.:	RW				RW											
MVBC Acc.:	r				r											

Symbol	Description
$SI_{3..0}$	Supervision Interval 0 = Inactive 2 = 2 ms 4 = 8 ms 6 = 32 ms 8 = 128 ms 1 = 1 ms 3 = 4 ms 5 = 16 ms 7 = 64 ms 9-15 = 256 ms
$R_{11..0}$	Range of docks to be supervised This 12-bit value specifies that all docks from zero to R11..0 are subject to sink-time supervision. The user must assure that this value does not exceed the number of available docks in the LA Data Area assigned by the selected Memory Configuration Mode.

Table 3.24: Sink-Time Supervision Register (STSR)

3.9.2 Traffic Memory Loading

The sink-time supervision takes place in bursts. When the time interval counter has elapsed, then the TM accesses start. In order to avoid bus traffic overflows, the following formula can be applied to find the minimum possible time interval for a given number of ports.

$$t_{acc} = 2\ t_{cp}\ (W + 3) \qquad t_{bc} = N\ t_{acc} \qquad t_{wc} = N\ (t_{acc} + 2\ A\ t_{cp})$$

t_{cp} Clock Period, 41.67 ns
W Number of waitstates
t_{acc} Access time required to read and rewrite one TACK word (ns)
A Average time required to perform one arbitration switch, here: 2 clock cycles
N Number of docks to be supervised
t_{bc} Best-case timing (ns; no arbitration switch required)
t_{wc} Worst-case timing (ns; two arbitration switches required for every access)

t_{bc} and t_{wc} represent fictitious boundaries. In field applications, some value inbetween will apply. Software engineers are urged to base their computations on the worst-case parameters:

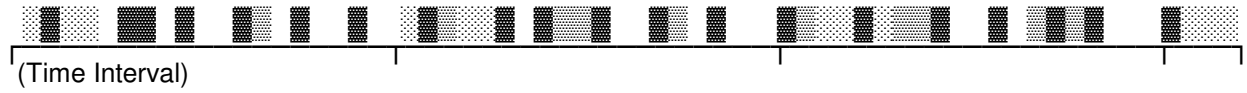
$$L = \frac{t_{wc}}{10^{6}\ I} \times 100$$

I Time Interval (ms)
L Loading ratio (percent)

The loading ratio L represents the worst-case time fraction the Sink-Time Supervision accesses the TM. The two charts shown on the next page provide a better understanding of these formulae. The following diagrams illustrate how the Sink-Time Supervision Logic accesses the TM and how these accesses interact with those originating from the CPU and MCU.

Sink-Time Supervision without any communication:

TM sharing between CPU, MCU and Sink-Time Supervision:



Legend: Data CPU ↔ TM Data MCU ↔ TM Sink-Time Supervision

Figure 3.14: Sink Time Supervision Events

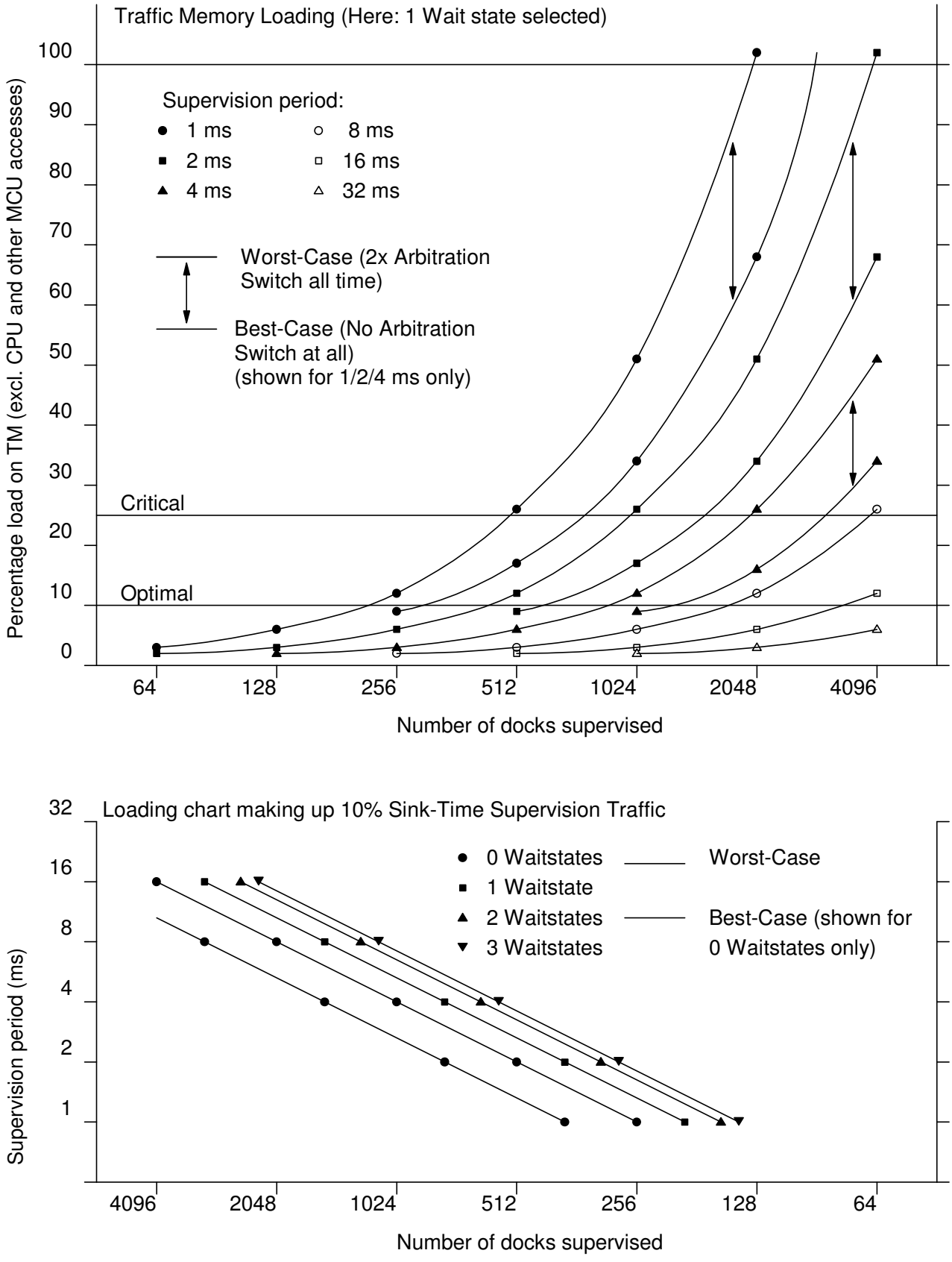


Figure 3.15: Traffic Memory Loading Charts

3.10 Clock Generator

The Clock Generator generates all clock and timing interval pulses for the Decoder, Universal Timers and MCU.

4 BEHAVIORAL OVERVIEW

This chapter summarizes the behavior the MVBC will follow during data transfers. The data transfers can be arranged into following categories:

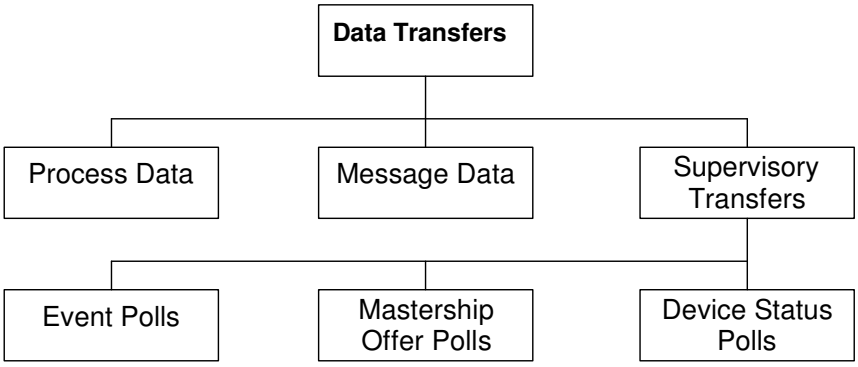


Figure 4.1: Types of Data Transferred

Section 4.1 indicates the preconditions the MVBC must fulfill in order to participate on MVB communication. Section 4.2 summarizes the general procedure the MVBC will undertake while transferring data over the MVB. The different data transfers (Process Data, Message Data, etc.), which may alter or supplement the general procedure, are summarized in the following sections.

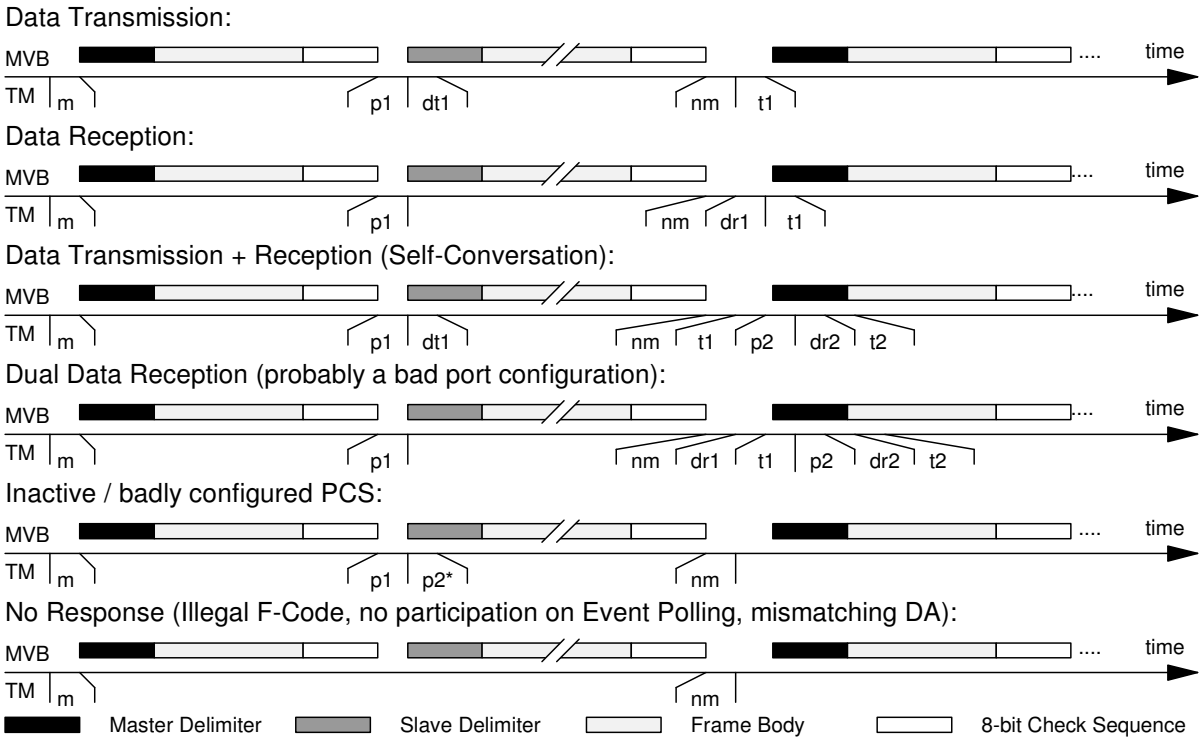
4.1 Preconditions

Following conditions must be met in order to let the MVBC participate on the MVB traffic:

- Initialization Level IL1..0 in the SCR must be set to '11'. If '10' is selected, then the full functionality is restricted to the internal loop-back lines (no outgoing signals). Values '00' and '01' do not permit data communications.
- A valid timeout coefficient TMO1..0 must be specified. The default value is 42.7 µs.
- A valid Device Address must be configured (either over DA11..0 pins or DAOR, see section 3.5.5.1)
- Event polling: In order to participate on event polling rounds, the RCEV-Bit in the SCR must be active.
- Masters only: The MAS-bit in the SCR must be active if the MVBC shall send Master Frames.

4.2 General Procedure

The MVBC makes following TM accesses while one telegram is transferred:



* If a 2nd port must be processed and is active, then it will be processed as if it would be the 1st port

m Master Frame Retrieval — Applies to active Masters only

nm MF Retrieval for next Telegram — Takes place before port processing in order to avoid delays
- Manual Transmission: Retrieve MF from Master Frame Slot (MFS)
- Automatic Transmission: Retrieve MF from MF-Table pointed by DPR

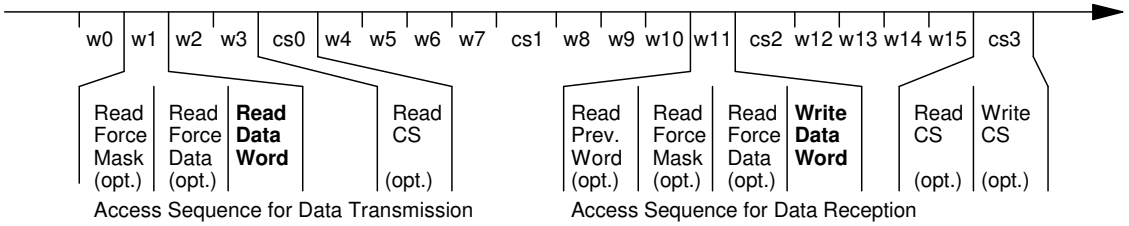
p1 Port Preprocessing - (2 - 8 accesses)
- Read LA-PIT or DA-PIT. No PIT-access for Physical Ports (PP)
- Read LA / DA / PP - PCS Word 0
- Read LA / DA / PP - PCS Word 1
- Queue Preprocessing (optional, max. 5 accesses)

- Processing discontinues if port is inactive, F-Code in PCS mismatches, or port is temporarily disabled (PTD)

dt1 Data Transmission: 1-52 accesses (1-16 words) — (Slave delimiter is already underway while data is retrieved from the TM)

dr1 Data Reception: 0-72 accesses

dr2 Data Reception for 2nd port (in case of self-conv.)



t1 Port Postprocessing - (2 - 8 accesses)
- Write 0xFFFF to TACK bits (applies if data transfer took place without errors)
- Read LA / DA / PP - PCS Word 1
- Write LA / DA / PP - PCS Word 1
- Queue Postprocessing (optional, max. 5 accesses, applies if no errors occurred)

t2 Port Postprocessing for 2nd port (in case of self-conversation)

p2 Port Preprocessing for 2nd port (in case of self-conversation)

Figure 4.2: TM Access Sequences

See also: "Appendix B: Port Processing Overview", "Appendix B: Port Processing Overview" and "Appendix C: Required PCS Settings for all Ports" which are helpful to configure ports.

4.3 Process Data Transfers (F-Codes 0-4)

The MVBC supports Process Data Transfers for all frame sizes specified in [1]. The MVBC handles Process Data in the Logical Address space.

Master Frame:

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	$F\text{-}Code_{3..0} = \{0..4\}$				Logical Address $LA_{11..0}$											

Slave Frame:

F-Code:	0	1	2	3	4	5-7
Frame Size:	1	2	4	8	16	not supported

Applicable Ports:

Port	Condition to process port
Port in LA Space	LA Port Index Table is configured PCS of affected port is configured (active, not temp. disabled)

Table 4.1: Process Data Transfers

Test case: If UTQ (SCR bit) is active, then the Test Source Port (TSRC) is checked before the LA port. If UTS is active, then the Test Sink Port (TSNK) is checked after the LA port. If both UTQ and UTS are active, then TSRC and TSNK are checked, but no LA port.

Allowed Options:

- Forcing Data (see section 4.8.1)
- Supporting non-real-time systems (see section 4.8.2)
- Data Transfer Interrupts (see section 4.8.3)
- Automatic Data Comparison Mechanism (see section 4.8.4)
- Synchro Port (see section 4.8.5)
- Transfer with Check Sequence (see section 4.8.6)
- Transferring non-numeric Data (see section 4.8.7)
- Write Always-Option to recover erroneous data (see section 4.8.8)

Discouraged Options:

- Attaching Message Queues
- Attempting to request Data Comparison Mechanism on source port

Attention: If no port shall be assigned to a specific Logical Address, then the Port Index shall point to a common inactive port (i.e. Port 0) where the PCS defines a passive port (SRC=0, SINK=0).

Attention: Assigning two different Logical Addresses to one common port index is allowed, but not strongly recommended.

During normal operation, the MVBC cannot send Process Data to itself since the same port cannot be declared as a bidirectional port. However, self-conversation can be invoked for self-test purposes by enabling UTS and/or UTQ so the MVBC will always check the Test Port.

4.4 Mastership Offer Poll (F-Code 8)

The MVBC handles Mastership Offer Polls as simple device-addressed polls. The addressed bus participant replies with a 1-word Slave Frame if a Master Frame with F-Code 8 is received. The software, which handles TCN upper layer protocols, is responsible to use this F-Code to handle mastership transfers from one Bus Administrator to another.

Master Frame:

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	$F\text{-}Code_{3..0} = \{8\}$				Device Address $DA_{11..0}$											

Slave Frame: 1 Word

Applicable Ports:

Port	Condition to process port
Mastership Offer Source Port (FC8)	Device Address in MF matches with own Device Address PCS is configured (active source, not temp. disabled)
Mastership Offer Sink Port (MOS)	PCS is configured (active sink, not temp. disabled)

Table 4.2: Mastership Offer Polls

Allowed Options:

- Data Transfer Interrupts (see section 4.8.3)

4.5 Device Status Polls (F-Code 15)

The MVBC supports Device Status Polls for both Class 1 and 2/3/4 Mode. If the MVBC operates in Class 1 Mode, then the Device Status Report is generated inside the MVBC. See section 5.3 for details. Otherwise, the Device Status Report is retrieved from port FC15.

Master Frame:

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	$F\text{-}Code_{3..0} = \{15\}$				Device Address $DA_{11..0}$											

Slave Frame: 1 Word

Applicable Ports:

Port	Condition to process port
Device Status Port (FC15)	Device Address in MF matches with own Device Address PCS is configured (active source, not temp. disabled)
Port in DA Space	DA Port Index Table is configured PCS is configured (active sink, not temp. disabled) Nonzero MCM (if MCM=0, then no DA port space is available)

Table 4.3: Device Status Polls

Allowed Options:

- Data Transfer Interrupts (see section 4.8.3)

4.6 Event Arbitration

The MVBC supports the lower-level protocol for Event Arbitration. Event arbitration is necessary in order to let one MVBC transfer sporadic data (i.e. a message) to another MVBC. Details on the Event Arbitration protocol are discussed in [1]. Three different Event Polls are supported and described next:

- Start Event Polls (F-Code 9)
- Group Event Polls (F-Code 13)
- Individual Event Polls (F-Code 14)

4.6.1 Start Event Polls (F-Code 9)

All Event Polling Rounds must start with a Start Event Poll in order to let MVBCs, which have announced events, to participate.

Master Frame:

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	$F\text{-}Code_{3..0} = \{9\}$				Event Mode $EM_{3..0}$				Event Type $ET_{3..0}$				Reserved			

Slave Frame: 1 Word, known as Event Frame; Collisions or no replies may occur.

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	$F\text{-}Code_{3..0}$				Logical Address $LA_{11..0}$ or Device Address $DA_{11..0}$											

The Event Frame must contain this format since the Bus Administrator returns it as a Master Frame.

Applicable Ports:

Port	Condition to process port
Event Frame Source Ports for both Event Types ET={0,1} (EF0, EF1)	Depends on Event Mode (EM) and Event Type (ET) PCS is configured (active source, not temp. disabled) RCEV bit is active
Event Frame Sink Port (EFS)	PCS is configured (active sink, not temp. disabled) RCEV bit is active

Table 4.4: Start Event Polls

If RCEV is 0, then participating on Event Polling is suspended. The EFS must be used by the Bus Administrator. All other slave devices can keep this port inactive or active for passive monitoring purposes.

Allowed Options:

- Data Transfer Interrupts (see section 4.8.3)

Event Types (ET):

ET	Description
0	Start/continue Event Polling Round events announced for high priority. If events are announced for low-priority polling (ET=1) only, then the MVBC will not participate until the next Start Event Poll (MF: F-Code 9, ET=0). Affected port: EF0. Affected flags: EA0 and PAR0 in the Master Register (MR).
1	Start/continue Event Polling Round events announced for low priority. If events are announced for high-priority polling (ET=0) only, then the MVBC will not participate until the next Start Event Poll (MF: F-Code 9, ET=0). Affected port: EF1. Affected flags: EA1 and PAR1 in the Master Register (MR).
2-15	Illegal. The MVBC will not respond to these values.

Table 4.5: Event Types (ET)

The MVBC *memorizes* the Event Type for all upcoming Group and Individual polls (F-Codes 13 and 14) until the next Start Event Poll (F-Code 9) is made. If ET=0 (or 1), then Port EF0 (or EF1) are used to retrieve the Event Frame. Announced and participating events for the two Event Types behave independently from each other, meaning a poll with ET=0 does not affect any MVBC flags related to ET=1 (i.e. PAR1, EA1, CPE1).

Event Modes (EM):

EM	Replying Allowed	Polling Round	Description (See flow-chart on Figure 4.3)
0	Yes	Continued	All MVBCs, which are currently participating at the current Event Polling Round (PARET='1'), will reply with an Event Frame.
1	Yes	Started	All MVBCs with announced events (EAET='1') will participate (PARET:='1') at this Event Polling Round and reply with an Event Frame
2	No [1]	Continued	All participating MVBCs (PARET='1') will continue to do so. This Event Mode can be used to change Event Type.
3	No [1]	Started	All MVBCs with announced events (EAET=1), will participate (PARET:='1') at this Event Polling Round without replies.
4-15	No	Illegal	The MVBC will not respond to these EM.

[1] For EM=2 and 3, no bus participant may reply and all MVBCs will wait until a Reply Timeout occurs.

Table 4.6: Event Modes (EM)

4.6.2 Group Event Polls (F-Code 13)

The Group Event Polls provide a mechanism to poll 2,4,8,...all 4096 MVB devices. If the Start Event Poll resulted in a collision, then this poll can be used to split the devices into two equal-sized groups (i.e. 2x2048) which are polled accordingly. If collisions continue to occur, then the groups are split again and polled. This group poll can be used until a small enough group of devices has been isolated where only one device replies with an Event Frame. The smallest group covers 2 devices.

Master Frame:

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	$F\text{-}Code_{3..0} = \{13\}$				Device Group Address $DGA_{11..0}$											

Slave Frame: 1 Word, known as Event Frame; Collisions or no replies may occur. See also section 4.6.1.

Applicable Ports:

Port	Condition to process port
Event Frame Source Ports for both Event Types ET={0,1} (EF0, EF1)	Device Group Address (DGA) matches PAR*i* is active, where *i*=ET of last Start Event Poll PCS is configured (active source, not temp. disabled) RCEV bit is active
Event Frame Sink Port (EFS)	PCS is configured (active sink, not temp. disabled) RCEV bit is active

Table 4.7: Group Event Polls

Allowed Options:

- Data Transfer Interrupts (see section 4.8.3)

Device Group Address:

The DGA is a 12-bit pattern which can be used to select a bi-sectional group of 2,4,8,... all 4096 Devices.

$DGA_{11..0}$	**Description**
1111 1111 1110	All devices are addressed (global poll)
1111 1111 110A	Half of them: DAs with matching DA_0 = A
1111 1111 10AA	One quarter of of them: DAs with matching $DA_{1..0}$ = 'AA'
:	:
10AA AAAA AAAA	Four of them are addressed: DA's with matching $DA_{13..0}$
0AAA AAAA AAAA	Two of them are addressed: DA's with matching $DA_{14..0}$

Table 4.8: Device Group Addresses (DGA)

4.6.3 Individual Event Polls (F-Code 14)

The Individual Event Polls address single devices to obtain Event Frames, as long this devices participate on the event polling round for the Event Type defined in the last Start Event Poll.

Master Frame:

Bit Number	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	$F\text{-}Code_{3..0} = \{15\}$				Device Address $DA_{11..0}$											

Slave Frame: 1 Word, known as Event Frame; Collisions or no replies may occur. See also section 4.6.1.

Applicable Ports:

Port	**Condition to process port**
Event Frame Source Ports for both Event Types ET={0,1} (EF0, EF1)	Device Address (DA) matches PAR*i* is active, where *i*=ET of last Start Event Poll PCS is configured (active source, not temp. disabled) RCEV bit is active
Event Frame Sink Port (EFS)	PCS is configured (active sink, not temp. disabled) RCEV bit is active

Table 4.9: Individual Event Polls

Allowed Options:

- Data Transfer Interrupts (see section 4.8.3)

4.6.4 Software Responsibility

Following aspects of Event Arbitration must be covered by software:

All Class 2/3/4 Devices, operating as slaves:

- Following steps must be undertaken by the Link Layer Software to initiate a sporadic data transfer:
  - Choose Event Type ET, 0 or 1.
  - The Event Frame (Master Frame contents which would initiate the transfer) must be copied into the Data Area of the EF*i* (*i*=ET). Example for Message Data transfers: Event Frame contains F-Code 12 and own Device Address.
  - The PCS of EF*i* must be configured as active source. Both CPEi-bits must be inactive.
  - The source port, involved in the sporadic data transfer, must contain valid data and its PCS must be configured accordingly. The CPE*i*-bit (Clear Pending Event) must be active.
  - EA*i* is set to '1' to announce the event.
- Participation on event polling will be cleared when the sporadic data transfer (i.e. Message Data) has taken place. This is accomplished with the active CPE*i* bit.
- Clearing participation: An exception applies for queued messages. See section 4.6.1.
- If required, the software can cancel announced and participating events by writing '1' to EC0 or EC1.

Attention: If CPE0 or CPE1 is not set, then the event will never be signed off and the MVBC continues participating at the next event polling round immediately.

Attention: The user shall not enable any of the CPE*i* bits in the PCS of those ports which are not intended for event-driven data transfers. Otherwise, event arbitration does not function properly.

All Bus Administrators (BA), operating as masters:

- Bisectional algorithm to perform a complete Event Polling Round. This algorithm is part of the BA Software.
- The Bus Administrator Software must copy the Event Frame from the Event Frame Sink Port (EFS) to the Master Frame Slot (MFS) in order to return the Event Frame as a Master Frame.

Third-Party Events:

Technically, device A may announce an event to instruct device B to send data to device C. In this case, device A must still provide a sink port for the transferred data in order to clear the announced event (active CPEi bit!).

Overruns:

A successful transmission of a port with activated CPE*i* will clear the announced event no matter what caused the transmission, i.e. cyclic Process Data transfer. Three cases may occur:

1. The master transferred the affected data before starting the next Event Polling round. The sporadic data transfer has been taken care and the MVBC will not participate on the upcoming Event Polling round.
2. The master received the Event Frame and retransmits it. The affected data transfer takes place twice.
3. The master received the Event Frame and the BA software recognizes that the Event Frame is identical with the previous Master Frame transmitted. Therefore, one transfer can be cut.

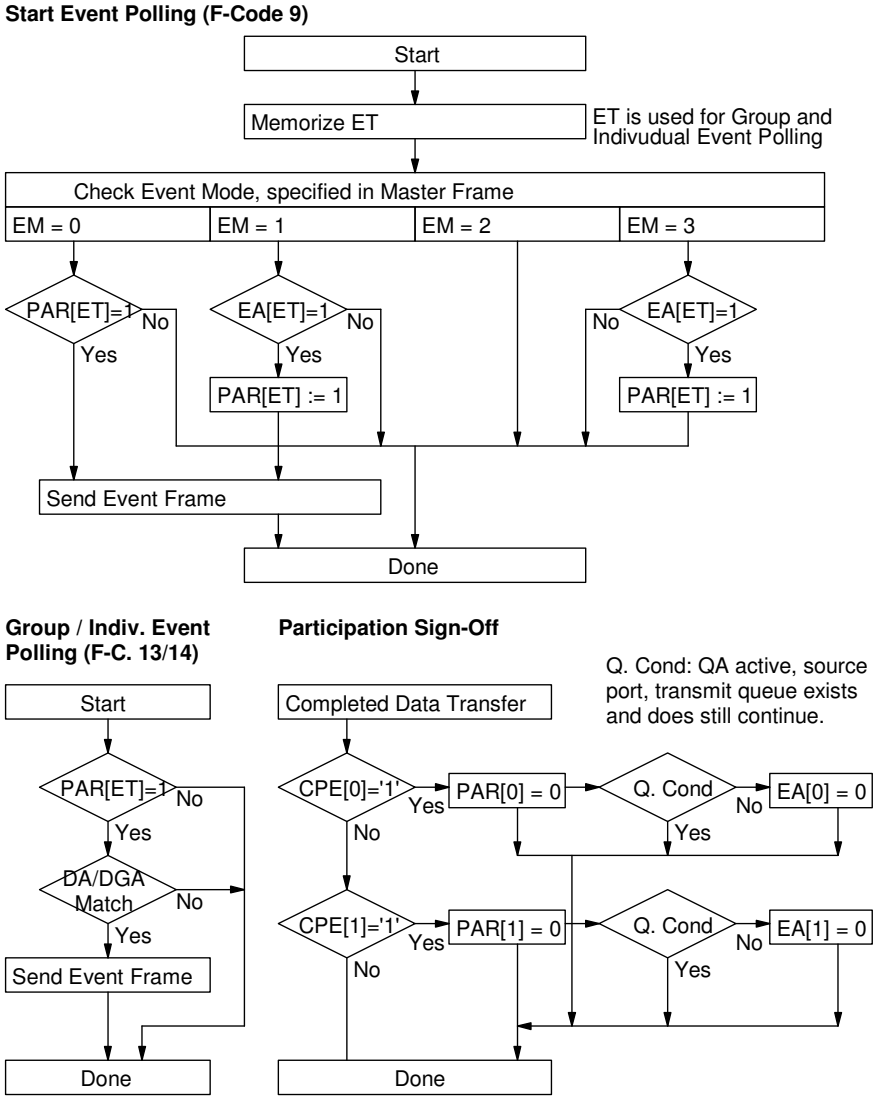


Figure 4.3: Event Polling FlowchartsMessage Data Transfers (F-Code 12)

The MVBC supports queued and nonqueued Message Data transfers. Message transfers are either sent to individual devices or broadcast to all devices.

Master Frame:

Bit Number	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	F-Code$_{3..0}$ = {12}				Device Address DA$_{11..0}$											

Slave Frame: 16 Words, Word 0 must contain following information:

Address *i* (Low Address Byte):

Bit Number	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	Comm. Mode CM$_{3..0}$				DDA$_{11..8}$			

Address *i+1* (High Address Byte):

Bit Number	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	DDA$_{7..0}$							

DDA = Destination Device Address

The format in Word 0 is mandatory since it is inspected by the MVBC. The entire message is considered as a non-numeric byte stream. The MVBC will take necessary actions to transfer the low address byte before the high address byte.

Applicable Ports:

Port	Condition to process port
Message Source Port (MSRC)	Device Address (DA) matches with own device PCS is configured (active source, not temp. disabled, NUM-bit = 0)
Message Sink Port (MSNK)	At least one of following 3 conditions must apply: Device Address matches given CM=1 or CM=15 (Broadcast) or MBC (SCR bit) is active and CM is valid (Broadcall) PCS is configured (active sink, not temp. disabled, NUM-bit = 0)

Table 4.10: Message Data Transfers

Allowed Options:

- Data Transfer Interrupts (see section 4.8.3)
- Transferring non-numeric Data - required! (see section 4.8.7)

Communication Modes (CM):

ET	Description
1	Point-to-Point Message: The receiver may receive the message if Destination Device Address matches with own DA. Exception: Message Broadcalling (MBC, see SCR) is enabled.
15	Broadcast message: The receiver may receive the message.
0, 2-14	Illegal. The MVBC will not receive any messages with these CM.

Table 4.11: Communication Modes (CM)

If no queues are used, then Message Data is stored to and retrieved from the Data Area, using the page pointer (VP) to address the page, as it is done with all other ports. If the queuing mechanism is enabled, then all messages are stored to and retrieved from Message Queues.

4.6.5 Message Queues

Message queueing is enabled if the QA-bits of the message ports (MSRC and/or MSNK) are set to '1'.

Attention: Queuing can only function properly in conjunction with event arbitration using one Event Type. The CPE bit for the chosen Event Type must be active in the Message Source Port.

Message Queues consist of the Linked List Structure (LLR) and the Queue Data area. See section 2.7 for details. Whenever a message is sent or received, the MVBC will perform two additional operations:

- Queue Preprocessing
- Queue Postprocessing

Queue Preprocessing takes place before outgoing data is read from one of the Transmit Queues (XQ0, XQ1), or before incoming data is stored to the Receive Queue (RQ). For outgoing messages, this operation reads the LLR pointer from QDT[XQ0] first. If this pointer is zero, then it assumes that XQ0 is *nonexistent* and will check XQ1. Otherwise, it retrieves the Data Pointer (DP). If DP is zero, then it assumes that XQ0 is *empty*, so XQ1 will be checked. XQ1 will be checked in the same manner as XQ0. If XQ1 is *nonexistent* or *empty*, too, then the interrupt "Transmit Queue Exception" (XQE) is asserted and message transfer will be cancelled. Otherwise, the Message Data ready to be retrieved and sent. For incoming messages, this operations checks the RQ in a similar manner. If the RQ is *nonexistent* or *full*, then the "Receive Queue Exception" (RQE) is asserted. There is no alternative Receive Queue to check.

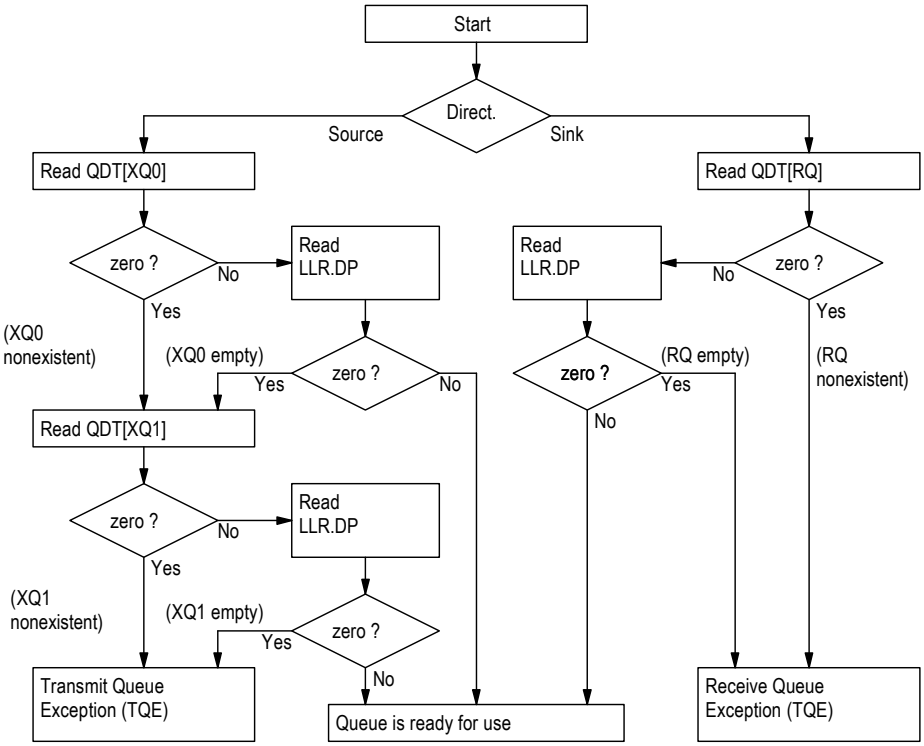


Figure 4.4: Queue Preprocessing

Queue Postprocessing takes place after outgoing data is read from one of the Transmit Queues or stored in the Receive Queue. This operation is needed to update the Queue Descriptor Table so the QDT of the affected queue points to the next entry in the LLR. This algorithm also checks whether the end of a particular queue has been reached or not. In detail, the Next Pointer of the current LLR is copied into QDT. If this pointer is zero, or the Data Pointer in the next LLR is zero, the MVBC assumes that the end has been reached. Concerning Transmit Queues: XQ0 is always checked before XQ1. If the end has been reached, then the interrupts "Transmit Queue 0/1 Complete" (XQ0C, XQ1C) or "Receive Queue Complete" will be asserted.

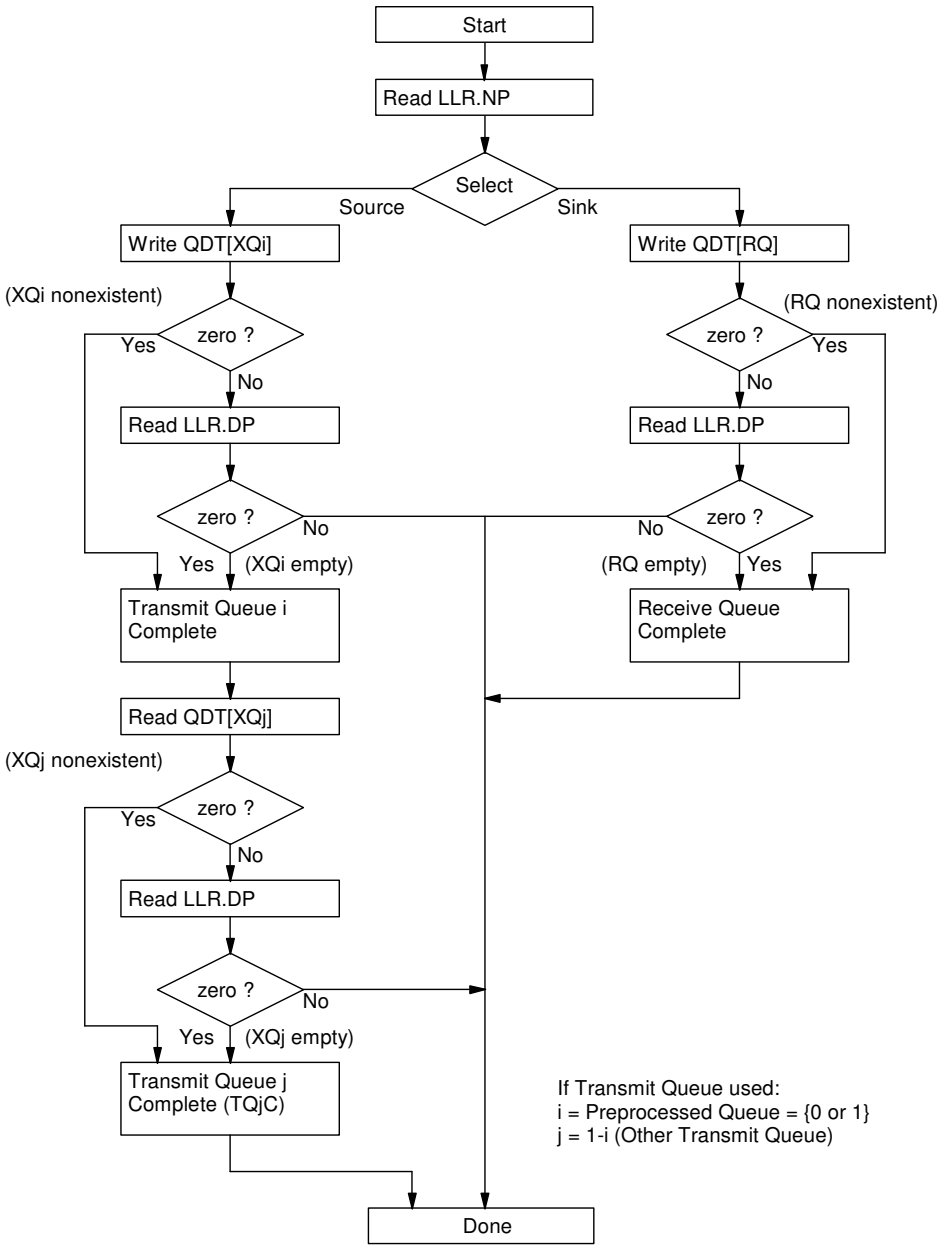


Figure 4.5: Queue Postprocessing

Notice on Event Polling with Queued Messages:

Normally, the CPE*i*-bit (*i*=ET) clears both EA*i* (announced event) and PAR*i* (participation), when the corresponding source port has been processed. If message queues are attached, two cases may occur:

- If at least one of the two Transmit Queues contain one or more outgoing messages, then only PARi is cleared. The event maintains announced for the next Event polling round. However, the MVBC will no longer participate in the current Event Polling round.
- If both Transmit Queues contain no more messages after the transfer, the both PARi and EAi are cleared.

4.7 Yet unsupported Master Frames (F-Codes 5-7, 10-11)

The MVBC will receive these Master Frames properly, but will take no additional actions afterward. All ports remain untouched.

4.8 Special Features

4.8.1 Forcing Process Data

A bitwise forcing mechanism is supported in order to override transmitted or received data with fixed values. Forcing can be enabled portwise by setting the FE-bit in the PCS to '1'. If forcing is enabled, then every access to the TM Data Area is extended by two additional accesses to the Force Table (see sections 2.5 and 3.6.7):

- Read Force Mask Word *i*
- Read Force Data Word *i*
- Read/Write Data Word *i*

Attention: Forcing is restricted to Process Data only. The user is required to keep the FE-bit inactive for all other forms of transfers. Otherwise, undefined behavior may occur.

Attention: Increased traffic between MVBC to TM due to accesses to the Force Table.

4.8.2 Disabling Ports Temporarily

The MVBC provides a reservation mechanism to assure consistent data reception to systems which do not comply with any real-time requirements, even though multi-tasking is supported. The mechanism is realized by temporarily disabling the sink-port while one or more tasks are retrieving data from the corresponding Data Area inside the TM. However, depending on the time required to read the data, one or more successive Process Data frames, which arrive at a later time, may be discarded entirely.

This mechanism uses a counter approach which has been derived from classical SW semaphores used for interprocess communication in multi-tasking operating systems. This feature allows multiple concurrent tasks to reserve and access the same port.

The PCS Word 1 provides a byte for the counter (Disable/Enable Counter, $DEC_{7..0}$) and a PTD-bit (Port Temporarily Disabled). The initial values are zero. The MVBC is responsible for the following work: If DEC is nonzero, then the MVBC will receive one more frame and stores it in *Not*(VP). At the moment PCS Word 1 is written back, VP is inverted as usual and PTD is now active. If both $DEC_{7..0}$ and PTD are nonzero, then no data will be received into the port processed. However, if DEC is zero again, data will be received again and PTD is cleared.

The software must do the following in order to receive consistent data:

1. Increment $DEC_{7..0}$ by 1
   - Read $DEC_{7..0}$ (3 indivisible operations)
   - Increment value
   - Write $DEC_{7..0}$
2. Retrieve data from TM to local host memory
3. Decrement $DEC_{7..0}$ by 1
   - Read $DEC_{7..0}$ (3 indivisible operations)
   - Decrement value
   - Write $DEC_{7..0}$

In/Decrementing DEC must not be interrupted by any other task. However, step 2 may be interrupted or temporarily suspended.

Attention: Not more than 255 tasks may read data from the same port.

4.8.3 Data Transfer Interrupts

Data Transfer Interrupts ($DTI_{7..1}$) can be configured in each port by setting the $IE_{2..0}$ to a nonzero value. A value of 7 will enable the Automatic Comparison Mechanism (see section 4.8.4). Interrupts will be issued after processing the port (data transfer plus TACK bits plus final read and write access to PCS word 1) has been completed.

4.8.4 Automatic Comparison Mechanism

The Automatic Comparison Mechanism is activated if Data Transfer Interrupt 7 (PCS: IE2..0='111') is enabled and the port is declared as an active sink. In this case, the MVBC issues interrupts only if the received data differs from the previously received data. This powerful feature can be used to avoid time-wasting reevaluations if the received data did not change. While data is transferred from the Receive Buffer (RXB), following steps are performed for each word transferred:

1. Read previous word from Data Area, pointed to by VP
2. Check whether they differ
3. Write received data to Data Area, pointed to by *Not*(VP)
4. Remaining words: Proceed with step 1 if no difference is yet found
   Proceed with step 3 if difference have been detected

Since no page mechanism exists for queued data (VP), Comparison is made on the same data block. Check Sequences will not be compared, even if TWCS is active. If Forcing is enabled, then forcing will be performed before the Comparison will be made. The MVBC assumes that the previous data has also been forced. Following TM access pattern is used:

- Read Force Mask Word *i* (if forcing is enabled)
- Read Force Data Word *i* (")
- Read Data Word *i*, pointed to by VP (as long data is still similar)
- Write Data Word *i*, pointed to by *Not*(VP)

Attention: Increased traffic: Two TM accesses are made for each transferred data word. Four accesses are made if Forcing is activated, too.

4.8.5 Synchro Port

The Synchro Port is a particular port which activates the STROBE\-signal if accessed. The Synchro-Port has been reorganized to act as a global and highly-time-accurate synchronization signal. Regardless if the MVBC is in class 1 mode or not, following applies

Logical Address for Synchro Port = 0x0FFF (any F-Code allowed)

The STROBE\-Signal will always be activated, regardless if the Synchro Port is configured as active source or sink, or if the function code matches or not. The address 0x0FFF even applies to class 1 devices which device address does not equal 0xFF0! The arrival of a Master Frame with last 12 bits equal 0xFFF will trigger the STROBE\-signal.

One port in the LA space serves as the Synchro Port if it is declared as a sink port. Any data transfer to a Synchro Port causes the strobe signal "STROBE\" to be activated for three clock cycles (125 ns). This port is useful to trigger external devices (i.e. an A/D-converter) or to synchronize bus participants. Since the Synchro Port is assigned to the highest Port Index, the size of the port is limited to one dock (max. 4 words).

MVBC Mode	MCM	Access to Synchro Port	Max. port size
Class 2/3/4 Mode	0, 1	Port Index 255	4 words (1 dock)
Class 2/3/4 Mode	2	Port Index 1023	4 words (1 dock)
Class 2/3/4 Mode	3, 4	Port Index 4095	4 words (1 dock)
Class 1 Mode	(not applicable)	Port 15 [1]	1 word

[1] No strobe signal is generated when two or more consecutive ports are accessed where the last port coincides with port 15. Example: F-Code on port 14 to access both ports 14 and 15 does not activate the strobe signal.

Table 4.12: Synchro Ports

4.8.6 Transfers with User-Supplied Check Sequences

During normal operation, the Check Sequence is generated inside the Encoder using the polynomial described in section 3.2. The user may configure selected ports where the MVBC shall obtain user-supplied Check Sequence from the TM instead. However, the Decoder will always use the same generator polynomial to check received data. Any deviating Check Sequence results to a CRC error with all its consequences.

Applications: Intentional transmission of erroneous data, i.e. for CRC mechanism tests and Bridges

In the TM, both CS octets (for both corresponding pages in the Data Area) are stored in PCS Word 3. Write accesses use the read-modify-write approach to update one such octet because the MVBC supports 16-bit TM accesses only.

If frames containing 8 or 16 data words are transferred, then the CS is accessed after 4 every words. If the frame contains 4 or less words, then the CS is accessed after all words have been transferred.

Attention: When TWCS is enabled, then the number of TM accesses increases by $max(1,\lfloor n/4 \rfloor)*a$. n = number of words transferred; a = 1 for transmission, 2 for reception.

4.8.7 Transferring Non-Numeric Data

Non-Numeric Data is understood as a character or byte string ordered in ascending address order. In the PCS, Word 0, all data must be declared with the NUM-bit. This will ensure data transfers in the correct byte and word order.

Attention: Messages (see section 0) are always non-numeric and must be declared as non-numeric data.

4.8.8 Write-Always Option

In some applications, i.e. gateways, transferring erroneous data intentionally may make sense. If the Write Always (WA)-bit (PCS, Word 0) is active, then the MVBC will process all erroneous data where the overall frame size has not been changed by noise or MVB failure. If TWCS is active, too, then the received (possibly mismatching) CRC will be stored along with the data.

4.8.9 Self Conversation

Self-Conversations occur when the MVBC processes two ports in the period one telegram is transferred. Typically, the first port is a source and the second port a sink. Only one port can be a source. However, an incorrect PCS configuration would represent a scenario where both ports act as sink ports. In case data is transferred, then both ports receive the data.

Common forms of self-conversations include

- Event Arbitration: An application, which runs on the same system where the Bus Administrator Software is running, announces an event.
- Self-addressed Message Data, broadcasting, broadcalling (F-Code 12)
- Self-addressed Device Status Poll (F-Code 15)
- Self-addressed Mastership Offer Poll (possible, but makes no sense; F-Code 8)
- Using of Test Ports for internal (IL=2) and external loopback test (IL=3, using short-circuited lines)

4.8.10 Test Ports

Under regular operating conditions, no self-conversation with Process Data (F-codes 0-4) can take place since only one port is available and must either be configured as a source or sink port. The test ports allow self-tests with transferring Process Data using internal or external loop-back. The maximum size is 16 words and the is located in the same memory locations where the Message ports (MSRC, MSNK) are located. The Test Source Port (TSRC) and Test Sink Port (TSNK) can be activated by setting the respective SCR-bits UTQ and UTS to '1'.

Appendix B indicates the conditions for every F-Code where Test Ports are referenced. The user is discouraged to use test ports for regular data transfers over the MVB.

Attention: In the current MVBC implementation, the Message and Test Ports are equivalent:
MSRC ⇔ TSRC; MSNK ⇔ TSNK

4.9 Master Frame Dispatcher

The MVBC provides an intelligent mechanism to dispatch individual Master Frames or a finite series of Master Frames from Master Frame Tables. The automatic dispatcher is suitable to send cyclic Process Data at precise time intervals; the manual mechanism is suitable to handle individual frames and sporadic data transfers such as messages.

Prerequisite: MAS-bit (SCR) is active, IL = 3 (full mode) or 2 (internal loopback test)

If the prerequisite is not met, then the MVBC will wait until MAS and IL have been set to the values shown above. The MAS-bit can be used to suspend (not cancel) sending Master Frames. Canceling all MF transmission can be achieved by writing a '1' to the CSMF-bit (Cancel Sending Master Frames, inside MR). Four different dispatching mechanisms are supported:

- SMFM Send Master Frames Manually
- SMFA Send Master Frames Automatically immediately
- SMFT Send Master Frames automatically at next Time Slot
- SMFE Empty Master Frame Table encountered, no MF's sent

For SMFA, SMFT and SMFE, the interrupt AMFX is asserted in order to inform the CPU that the addressed MF-Table has been processed.

4.9.1 Manual Mechanism (SMFM)

The manual mechanism transmits individual Master Frames. This mechanism has a lower priority than the automatic approach, so the BAS can append one Master Frame in advance while the automatic dispatcher is still busy working off a MF-Table. When this table has been finished, then the appended Master Frame will be transmitted, except if:

- No additional MF-table is signed up using advance request (see section 4.9.5) with SMFA (no waiting for next timer pulse)
- The BUSY-bit is still active (data transfer still in progress).
- Minimum spacing requirements between previous Slave Frame and current Master Frame are met (4 µs).

If any of these cases applies, then sending the manually requested MF will be postponed until both conditions are met. The BAS must undertake two steps to send a Master Frame: The MF body must be written into the Master Frame Slot (MFS, inside Service Area) and the transmission must be initiated by activating SMFM in the MR. When the three conditions noted above are met, then the MVBC reads the MF from the MFS and transmits it on the MVB. After the read-access, the interrupt

"Master Frame Checked" (MFC)

is asserted to inform that the BAS can write the next MF into the MFS and announce the next MF transmission with SMFM. The BUSY-bit in the MR will become active immediately and stay active until the entire telegram (Master + Slave Frame) has been transferred or a timeout has occurred. This bit is coupled with the "Slave Frame Checked" interrupt (SFC), however this interrupt will not be triggered if a Reply Timeout occurs due to a missing Slave Frame. Figure 4.6, part 1 illustrates few examples of SMFM.

4.9.2 Automatic Mechanism (SMFA)

The automatic mechanism is able to process MF-Tables containing up to 32 Master Frames. Automatic dispatching has a higher priority over manual dispatching, meaning that manual MF-requests submitted thereafter are postponed until automatic dispatching has been completed.

Two steps must be undertaken in order to transmit all Master Frames from one MF Table: First, the 16-bit pointer (Lower two bits are always zero) to the MF Table is written to the DPR. The pointer format is described in section 2.7.2. Next, the transmission is initiated by simultaneously specifying SMFA (Send Master Frames Automatically) and 5-bit table size in the MR. Allowed sizes are 1-32. A size of zero means 32! See section 4.9.4 to send *empty* MF-Tables instead.

MF-transmission starts at the moment all of the following conditions are met:

- The BUSY-bit (see MR) is zero.
- The minimum frame spacing on the MVB must be reached.

The MFC-Interrupt is asserted for every obtained MF body. When the entire MF-Table has been finished, the interrupt

"All Master Frames Transmitted" (AMFX)

will be asserted. The AMFX-Interrupt is asserted when the last entry from the MF-Table has been retrieved. The BUSY-bit remains active until the last telegram has been processed entirely. Figure 4.6, part 2 illustrates an example of SMFA.

4.9.3 Timed Mechanism (SMFT)

The timed mechanism operates in a similar manner as the automatic mechanism. It allows sending Master Frames at precise time intervals. The MVBC waits until the Universal Timer 1 reaches zero before the MF-Table is processed. The Universal Timer 1 must be configured accordingly (active counter, valid value inside the Timer Reload Register 1).

The procedure to send timed MF's is similar as described in section 4.9.2. However, SMFT must be used instead of SMFA. The BUSY-bit will be activated at the moment the first MF is transmitted. Figure 4.6, part 3 illustrates an example of SMFA.

4.9.4 Empty MF-Tables (SMFE)

SMFE is used to specify empty MF-Tables. The MVBC waits until the Timer reaches zero and issues the AMFX-Interrupt immediately afterward. The AMFX-interrupt is needed to handle advance requests described in the following section. Figure 4.6, part 4 illustrates the SMFE-feature.

(Space below has been left blank intentionally)

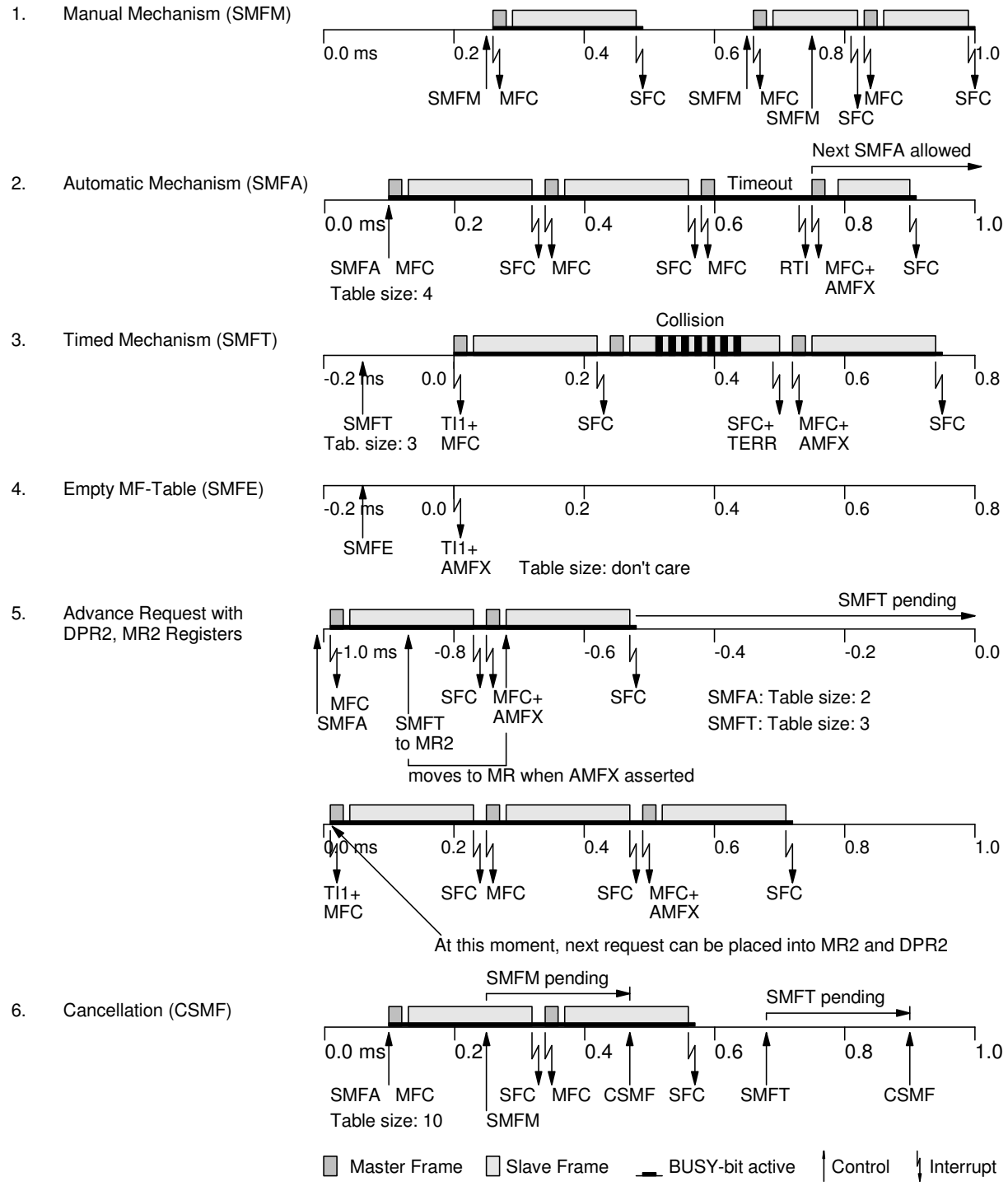


Figure 4.6: Behavior of Master Frame Dispatcher

4.9.5 Advance Requests

The host CPU can submit advance requests to the MVBC in order to transmit MFs on time without struggling with CPU interrupt service latency problems. This mechanism is necessary if the interrupt latency to service the AMFX-interrupt and to initiate the next MF is too big.

Advance request are made into the secondary Master and Dispatch Pointer Registers MR2 and DPR2. The contents of these registers are automatically transferred into MR and DPR when the AMFX-interrupt, originating from the current request, occurs.

Attention: If AMFX is masked, then AMFX will not pass an interrupt to the CPU but still perform the register transaction. The transfer takes place regardless if the Interrupt Logic is frozen or not.

DPR2 contains the pointer to the next MF-Table, and MR2 specifies length of that MF-Table and its transmission

mode (SMFT, SMFA, SMFE) as it should be specified for MR. For obvious reasons, MR2 does not include the upper halfword containing control bits for Event Polling, CSMF and BUSY. MR2 and DPR2 permit full read and write access. The values can be modified if necessary.

At the moment the AMFX-interrupt occurs, the contents of DPR2 and MR2 are moved to DPR and MR respectively. MR2 is cleared afterward in order to avoid repeating the same request. The transfer from MR2 to MR is cumulative, meaning that pending requests inside MR (SMFA, SMFE, SMFM and SMFT) will not be cleared.

Figure 4.6, part 5 illustrates a few examples. First, SMFA is issued to MR to transfer two MFs. While the first telegram is transferred, SMFT is passed to MR2 to transfer three MFs. After the timer reaches zero, the next advance request may be issued.

4.9.6 Cancellations

The CSMF-bit (Cancel Sending Master Frames) cancels any current dispatching request. Any manual dispatching request (SMFM) can be cancelled before the MVBC has started accessing the Master Frame Slot (MFS) to transmit the MF. If an automatic dispatching request (SMFA) is cancelled, then the current telegram is processed entirely and no additional MF will be dispatched. Timed requests (SMFT) can be completely cancelled any time unless the timer reaches zero meanwhile. SMFE requests can be cancelled as long the timer has not yet reached zero.

The MVBC provides no means to reinstate cancelled requests. However, MF dispatching can be suspended by setting MAS to '0' (inside SCR) temporarily.

4.9.7 External Synchronization

Timed MF Transmission (with SMFT, SMFE) can also be initiated by the external signal II3\ so multiple MVBCs can orchestrate their MVBs synchronously. See section 3.8.2.

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5 CLASS 1 LOGIC AND BEHAVIOR

The Class 1 Logic supports Class 1 Mode operation without assistance of a CPU or microcontroller. In this mode, the MVBC supports following transfers:

Ports	F-Code	Description
16 x 16-bit Process Data Ports (8 x source, 8 x sink ports; 16 x source ports if F-Code = 4)	0-4	Each port can be used to transfer 1-16 words of Process Data. Not supported: Forcing and automatic data comparison mechanism.
1 source port for Device Status Wd.	15	Device Status Report, generated by MVBC

Table 5.1: Data Transfers in Class 1 Mode

Class 1 operation is configured with pin class_mode = 0 (tied to VSS). Several other pins serve to configure class 1 behavior.

Device Address:

The unique Device Addresses, which are assigned to MVBCs operating in Class 1 Mode, must be divisible by 16 (Lower 4 bits are zero). In fact, the lower 4 bits are internally set to '0' since the corresponding input pins DA3..0 are used for different Class 1 Mode parameters.

Erroneous Data Transfers:

Class 1 Mode supports no external signaling for erroneous and missing frames. In case the MVBC receives erroneous data, no access is made to the peripheral devices in order to preserve the correct values from the previous transfers.

5.1 Process Data

The 16 Process Data ports are divided into 8 source and 8 sink ports. The MVBC is addressed if bits 11..4 of the Logical Address in the Master Frame equals to bits 11..4 of the configured Device Address. The sixteen ports are addressed with bits 3..0 of the Logical Address. Port 15 serves as a Synchro Port where the STROBE\-pin is activated at completion of every data reception.

Because no traffic memory is supported, the following accesses are not made when the MVBC operates in Class 1 Mode:

- Port Index Table (Port Index is derived from Logical Address)
- Port Control and Status Register (PCS)
  - Word 0 is substituted by internal parameters, see tables below
  - No TERR, STO, BNI, and TACK bits are written, No Valid Page (VP) bit
- Force Table, Service Area, etc.

F-Code 0 can be used to address each port individually. Using F-Code 1 (or 2, 3, 4) groups 2 (or 4, 8 or all 16) ports into one bigger port in order to access multiple ports with one telegram. This mechanism allows more efficient data transfers. The user must not use odd (or unaligned) port addresses when using nonzero F-Codes. Example: F-Code 2 with LA=004 is allowed, but not LA=005.

Table 5.2 - Process Data in Class 1 Mode, see next page.

Substitution for Port Control Register:

Since No PCS can be obtained from the outside, the MVBC assumes following PCS image when handling transferring Process Data:

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol:	$F\text{-}Code_{3..0}$				SRC	SINK	TWCS	WA	$IE_{2..0}$			$CPE_{1..0}$		QA	NUM	FE
Value:	0000 - 0100				see [2]	see [2]	0	0	0 0 0			0 0		0	1	0

MVBC Access: Internal substitution for PCS

[1] Depending on F-Code in Master Frame
[2] The lower eight ports (Port DA...DA+7), are source ports.
The upper eight ports (Port DA+8...DA+15), are sink ports.
Exception: F-Code 4 is used.

The MVBC02C supports now an enhanced class 1 mode with not decoded port numbers to increase number of accessible ports (multi – I/O devices), see description in next section. Please note that following table applies to traditional MVBC01 behavior, where

tm_req_cpu must be held passive: TM_REQ_CPU\ = ENH_CL1_MODE\ = '1' (disabled)!

xxYH: Address specified in Master Frame (xx = Bits 11..4 of Device Address Y = Port number (0 … F))

Port Address	F-Code 0	F-Code 1	F-Code 2	F-Code 3	F-Code 4
xxFH	Sink Port F [1]	(2 words)			
xxEH	Sink Port E	Sink Port E			
xxDH	Sink Port D	(2 words)	(4 words)		
xxCH	Sink Port C	Sink Port C	Sink Port C		
xxBH	Sink Port B	(2 words)			
xxAH	Sink Port A	Sink Port A			
xx9H	Sink Port 9	(2 words)	(4 words)	(8 words)	
xx8H	Sink Port 8	Sink Port 8	Sink Port 8	Sink Port 8	
xx7H	Source Port 7	(2 words)			
xx6H	Source Port 6	Source Port 6			
xx5H	Source Port 5	(2 words)	(4 words)		
xx4H	Source Port 4	Source Port 4	Source Port 4		
xx3H	Source Port 3	(2 words)			
xx2H	Source Port 2	Source Port 2			
xx1H	Source Port 1	(2 words)	(4 words)	(8 words)	(16 words)
xx0H	Source Port 0	Source Port 0	Source Port 0	Source Port 0	Source Port 0 [2]

[1] Accessing Port 15 with F-Code activates STROBE\ for 125 ns (Synchro Port)
[2] Since F-Code 4 relates to 16 words, all 16 ports are accessed as source ports. This F-Code is suitable for multichannel data acquisition. No sink port is available here

Table 5.2: Process Data Ports in Class 1 Mode (as with MVBC01)

5.1.1 Process Data in Enhanced Class 1 Mode

If increased amount of I/O ports is needed for certain class 1 devices, the MVBC02C supports now an Enhanced Class 1 Mode.

In this mode, all 16 ports have a total size of 16 words. The F-code specifies the number of words to be transferred from or to the port. The logical port address stays constant during the period a port is read or written. In addition, a

counter starts at zero and counts upward for every further word accessed during one telegram turn. The combination of the port address (16) and the counter (16) provides an address width of 2^8 = 256 words. This means:

Source ports: 8 x 16 words = 128 words (ports 0..7)
Sink ports: 8 x 16 words = 128 words (ports 8..F)

Example: Master Frame 0x2123 reaches MVBC02 in enhanced class 1 mode.
Device address = 0x120 (match!)
Function code = 2. This means: Telegram size = 4 words. 4 accesses will be made.
The counter Ctr[3..0] will count from 0...3
Port address PA[3..0] = 3.

The MVBC issues following addresses: 0x303 0x313 0x323 0x333.
Ignore the lower four CA bits to get following addresses: 0x30, 0x31, 0x32 and 0x33.

Using CA[3..0] allows interesting intermediate solutions with smaller memory areas in order to allow port overlapping with higher function codes.

Enabling this mode, tm_req_cpu must be activated: TM_REQ_CPU\ = ENH_CL1_MODE\ = '0' (enabled)

aaYH: Address specified in Master Frame (aa = Bits 11..4 of Device Address Y = Port number).
In this table, Port[k] is composed BY concatenating of { PA[3..0], Ctr[3..0] }.

	Port Address	F-Code 0	F-Code 1	F-Code 2	F-Code 3	F-Code 4
Sink	aaFH	Port 0xF0	Port 0xF0 ... 0xF1	Port 0xF0 ... 0xF3	Port 0xF0 ... 0xF7	Port 0xF0 ... 0xFF
	aaEH	Port 0xE0	Port 0xE0 ... 0xE1	Port 0xE0 ... 0xE3	Port 0xE0 ... 0xE7	Port 0xE0 ... 0xEF
	aaDH	Port 0xD0	Port 0xD0 ... 0xD1	Port 0xD0 ... 0xD3	Port 0xD0 ... 0xD7	Port 0xD0 ... 0xDF
	aaCH	Port 0xC0	Port 0xC0 ... 0xC1	Port 0xC0 ... 0xC3	Port 0xC0 ... 0xC7	Port 0xC0 ... 0xCF
	aaBH	Port 0xB0	Port 0xB0 ... 0xB1	Port 0xB0 ... 0xB3	Port 0xB0 ... 0xB7	Port 0xB0 ... 0xBF
	aaAH	Port 0xA0	Port 0xA0 ... 0xA1	Port 0xA0 ... 0xA3	Port 0xA0 ... 0xA7	Port 0xA0 ... 0xAF
	aa9H	Port 0x90	Port 0x90 ... 0x91	Port 0x90 ... 0x93	Port 0x90 ... 0x97	Port 0x90 ... 0x9F
	aa8H	Port 0x80	Port 0x80 ... 0x81	Port 0x80 ... 0x83	Port 0x80 ... 0x87	Port 0x80 ... 0x8F
Source	aa7H	Port 0x70	Port 0x70 ... 0x71	Port 0x70 ... 0x73	Port 0x70 ... 0x77	Port 0x70 ... 0x7F
	aa6H	Port 0x60	Port 0x60 ... 0x61	Port 0x60 ... 0x63	Port 0x60 ... 0x67	Port 0x60 ... 0x6F
	aa5H	Port 0x50	Port 0x50 ... 0x51	Port 0x50 ... 0x53	Port 0x50 ... 0x57	Port 0x50 ... 0x5F
	aa4H	Port 0x40	Port 0x40 ... 0x41	Port 0x40 ... 0x43	Port 0x40 ... 0x47	Port 0x40 ... 0x4F
	aa3H	Port 0x30	Port 0x30 ... 0x31	Port 0x30 ... 0x33	Port 0x30 ... 0x37	Port 0x30 ... 0x3F
	aa2H	Port 0x20	Port 0x20 ... 0x21	Port 0x20 ... 0x23	Port 0x20 ... 0x27	Port 0x20 ... 0x2F
	aa1H	Port 0x10	Port 0x10 ... 0x11	Port 0x10 ... 0x13	Port 0x10 ... 0x17	Port 0x10 ... 0x1F
	aa0H	Port 0x00	Port 0x00 ... 0x01	Port 0x00 ... 0x03	Port 0x00 ... 0x07	Port 0x00 ... 0x0F

Table 5.3: Process Data Ports in Class 1 Mode, enhanced mode (TM_REQ_CPU\ = '0')

5.2 Class 1 Peripheral Interface

In Class 1 Mode, the access mechanism from MVBC to the peripheral devices is similar to the access mechanism to the Traffic Memory in Class 2/3/4 Mode. The only difference is the decoded address bus. Very simple devices can use the CSi \-signals only to read or write ports (no class 1 Enhanced Mode).

The Interrupt Logic remains inactive since no method exists to configure the interrupt registers.

5.2.1 Class 1 Mode Address Bus Definition

Any MVBC: Class 2/3/4 Mode	**MVBC 01: Class 1 Mode**	**MVBC 02: Class 1 Mode ENH_CL1_MODE\='1'**	**MVBC 02: Class 1 Mode ENH_CL1_MODE\='0'**
A[19]	'1'	same as in MVBC 01	
A[18]	'1'	"	
A[17]	'1'	"	
A[16]	CS[0]\	"	
A[15]	CS[15]\	"	
A[14]	CS[14]\	"	
A[13]	CS[13]\	"	
A[12]	CS[12]\	"	PA[3]
A[11]	CS[11]\	"	PA[2]
A[10]	CS[10]\	"	PA[1]
A[9]	CS[9]\	"	PA[0]
A[8]	CS[8]\	"	Ctr[3]
A[7]	CS[7]\	"	Ctr[2]
A[6]	CS[6]\	"	Ctr[1]
A[5]	CS[5]\	"	Ctr[0]
A[4]	CS[4]\	"	CA[3]
A[3]	CS[3]\	"	CA[2]
A[2]	CS[2]\	"	CA[1]
A[1]	CS[1]\	"	CA[0]

A[19..1] MVBC address bus

CS[15]\..CS[0]\ Active-low chip-select lines: CS[k] = inv (decoder_4_to_16(PA))

PA[3..0] Port Address, as specified in bits 3..0 in the Master Frame. It will stay constant during the period all words are read from or written to the memory.

Ctr[3..0] Counter. Starts with 0 at first access, then counts upward.
For F-code 4, Ctr counts from 0 to 15.

CA[3..0] Combined Address. CA[3..0] = PA[3..0] or Ctr[3..0]

It is the encoded address equivalent to the decoded CS[15..0] signals.

5.3 Device Status Report

In Class 1 Mode, the Device Status Report is generated by the MVBC. It consists of fixed parameters (10 bits), internal flags (2 bits) and user-adjustable flags (4 bits). Since No PCS can be obtained from the outside, the MVBC assumes following PCS settings of the Device Address Port when sending the Device Status Report:

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol:	F-Code$_{3..0}$				SRC	SINK	TWCS	WA	IE$_{2..0}$			CPE$_{1..0}$		QA	NUM	FE
Value:	1 1 1 1				1	0	0	0	0 0 0			0 0		0	1	0

MVBC Access: Internal substitution for PCS

Internal Contents of the Device Status Report (DSR):

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol:	Device Type				Reserved				LAA	RLD	SSD	SDD	ERD	FRC	DNR	SER
Value:	1 1 1 1				0 0 0 0				Int.	Int.	Pin [1]	Pin [1]	0	0	Pin [1]	0

[1] Input pins: See Table 5.5

The pins DNR, SDD and SSD supply information to the Device Status Report. For DNR, the current level is used. The signals SDD and SSD are latched and will be kept until the next Device Status Report has been transmitted. After that, these internal bits will be cleared.

LAA is obtained from bit 3 of the Decoder Register (DR). If a line switch took place before a Device Status Poll, then the active line after the line switch is returned. See section 3.3 for details.

RLD (Redundant line Disturbed, see section 3.3.5) is obviously read before it is cleared.

5.4 Substitutions for Internal Signal Definition

Several assumptions are made for class 1 operation, some behavior selections are made on physical pins of the MVBC, substituting their class234 – meaning not supported in class1 – mode.

5.4.1 Internal Contents for Status Control Register (SCR):

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	IM	QUIET	MBC	-	TMO$_{1..0}$		WS$_{1..0}$		ARB$_{1..0}$		UTS	UTQ	MAS	RCEV	IL$_{1..0}$	
Init. Value:	0	0	0	0	Pins [1]		Pins [1]		0 1		0	0	0	0	11	

[1] Input pins: See Table 5.5

The MVBC starts up in full operational mode (IL = 3).

5.4.2 Substitution for Port Control and Status Register:

The MVBC assumes following PCS value when accessing any Process Data ports (refer to section 2.3.1for PCS description):

Since No PCS can be obtained from the outside, the MVBC assumes following PCS image when handling transferring Process Data:

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol:	F-Code$_{3..0}$				SRC	SINK	TWCS	WA	IE$_{2..0}$			CPE$_{1..0}$		QA	NUM	FE
Value:	0000 - 0100				see [2]	see [2]	0	0	0 0 0			0 0		0	1	0

MVBC Access: Internal substitution for PCS

[1] Depending on F-Code in Master Frame
[2] The lower eight ports (Port DA...DA+7), are source ports.
The upper eight ports (Port DA+8...DA+15), are sink ports.

Exception: F-Code 4 is used.

5.4.3 Interframe Spacing

The Interframe Spacing between frames (see section 3.2.2) is selected using timer output pins TMR2, TMR1 which are directed as inputs when CLASS_MODE = '0' (VSS).

Interframe Spacing	**Class 1 Mode: Inputs**		
	TMR2	**TMR1**	**Remarks**
6 µs	Open (1)	Open (1)	Default setting for Class1 Devices!
4 µs	Open (1)	Vss (0)	
8 µs	Vss (0)	Open (1)	
12 µs	Vss (0)	Vss (0)	

Table 5.4: Interframe Spacing Configuration

5.4.4 Class 1 Multiplexed Lines

When the MVBC operates in Class 1 Mode, different functions are assigned to some input pins and address outputs. Please note that 16 bits in the address bus are decoded as active-low chip-select (CS*i*\) signals. The remaining address bits are held at '1'. Please note also that some enhancements are supported by MVBC02C, not by MVBC01.

The following table summarizes these signals:

			Description	
Class 2/3/4 Mode	**Class 1 Mode MVBC01**	**Class 1 Mode MVBC 02**	**Class 1 Mode MVBC01**	**Class 1 Mode MVBC02**
$II_{3..2}$	$TMO_{1..0}$	$TMO_{1..0}$	Timeout Coefficient 1..0	Interrupt Inputs 3..2
$II_{1..0}$	$WS_{1..0}$	$WS_{1..0}$	Wait State Select bits 1..0	Interrupt Inputs 1..0
DA_0	DNR	DNR	Device Not Ready	Device Not Ready
DA_1	ERD (SPD)	--	Extended Reply Delay (Some Process Disturbance)	--
DA_2	SDD	SDD	Some Device Disturbance	Some Device Disturbance
DA_3	SSD	SSD	Some System Disturbance	Some System Disturbance
A_{16}	CS0\	CS0\	Chip Select bit 0	Chip Select bit 0
$A_{15}..A_1$	CS15\ ... CS1\	CS15\ ... CS1\	Chip Select bits 15..1	Freely configurable: Either address bus (if enhanced class 1 mode is active) or decoded chip select lines (usual mode).
TM_REQ_CPU	TM_REQ_CPU\	ENH_CL1-_MODE\	TM_REQ_CPU\	Enhanced Class 1 Mode enabled if class 1 mode is active.
RD	RD\	TURBO\	RD\	In class 1 mode, a '0' activates turbo mode (3.0 Mbit/s)
WR	WR\	TRAFO\	WR\	In class 1 mode, a '0' activates trafo mode.
INT1	INT1\	TRP\	Not used	Selecting Clocked Transmitter Mode
TMR2\, TMR1	TMR2\, TMR1\	$IFS_{1...0}$	Not used	Interframe space selector (input)

Table 5.5: Pin Reassignments for Class 1 Mode

6 HARDWARE APPLICATION SUGGESTIONS

6.1 MVBC with 16-Bit Traffic Memory

The following figure shows a typical schematic where the MVBC is running in Class 2/3/4 Mode. The Class_Mode-Pin must be connected to +5 V.

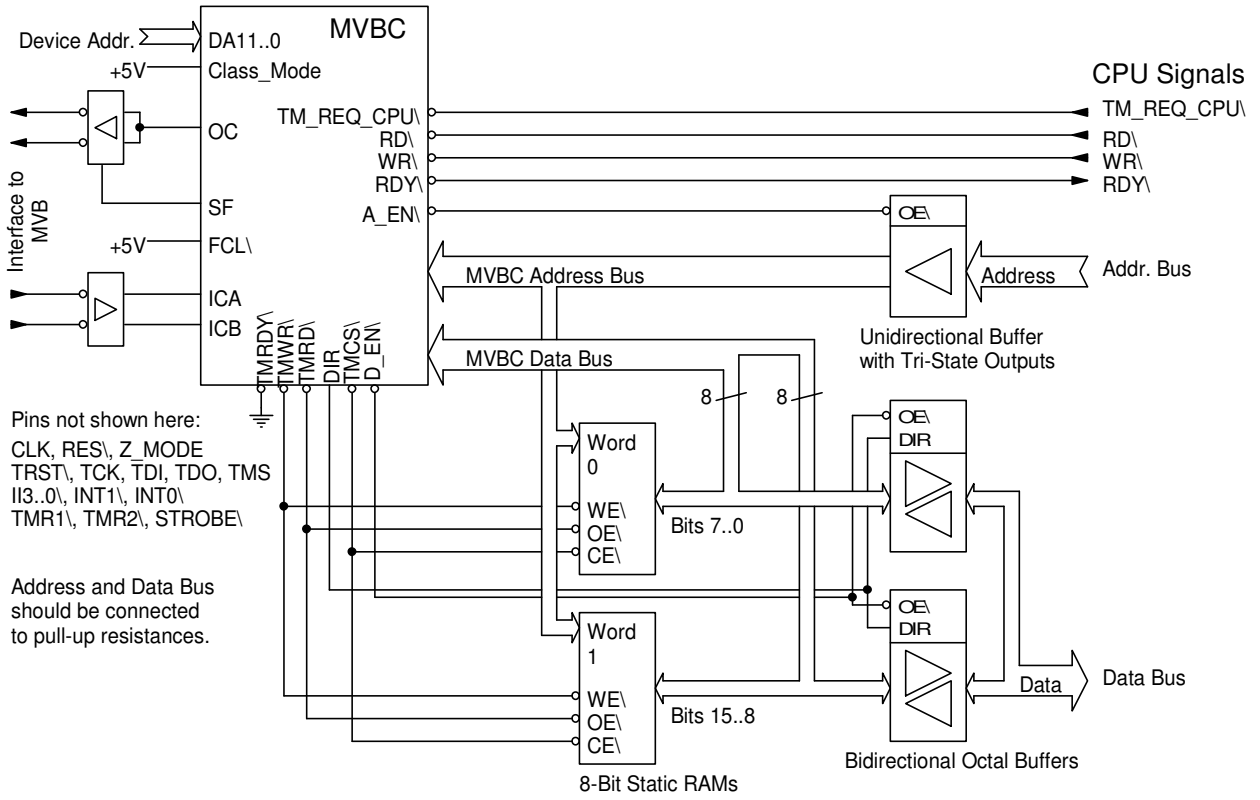


Figure 6.1: MVBC with 16-bit Traffic Memory

6.2 MVBC operating in Class 1 Mode

A diagram showing the MVBC operating in Class 1 Mode is shown on the next page. Class 1 Mode operation is enabled when the pin CLASS_MODE is connected to ground. In simple applications, the MVBC operates without assistance of a host CPU or microcontroller. The following default connections must be considered:

- RD\, WR\, TM_REQ_CPU\ are multiplexed to other signals of MVBC according Table 5.5
- $II_{3..0}$\ are tied individually to +5V or ground in order to configure reply timeout and TM access wait states.
- INT1\, INT0\, RDY\ are open
- Only $DA_{11..4}$ are used to define the Device Address. $DA_{3..0}$ are used to supply information for the Device Status Report and line switch control according to reassignment, see Table 5.5.

A microcontroller may be desirable when following features of the MVBC are to be utilized:

- Visibility of internal interrupts, i.e. due to telegram errors, timeouts, etc.
- Using the Universal Timers
- Overriding Device Address
- Accessing the ports directly over the same data bus

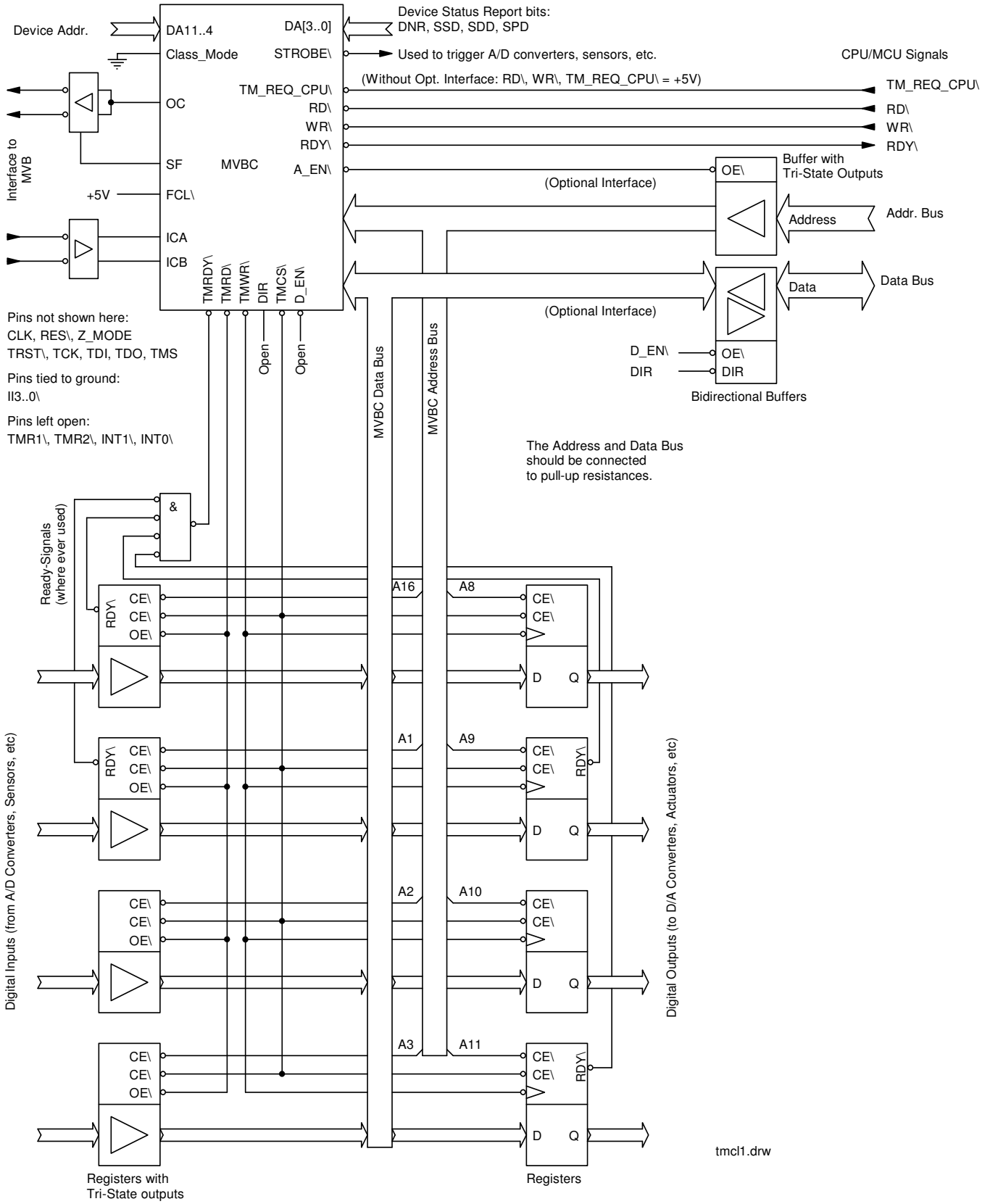


Figure 6.2: MVBC Operating in Class 1 Mode

MCM=0 is assumed when accesses to Internal Registers in Class 1 mode are made. In order to avoid access confusions, every port should check the address bit in combination with TMCS\. When the ports are accessed by the host over the same data bus, then the user must be aware not to choose addresses which collide with the Service Area where the Internal Registers are located. The danger is eliminated when at least one of the upper three address bits A19..17 are nonzero.

6.2.1 Class 1 Mode Operation with "Traffic Memory"

The following figure shows a simple application of the MVBC using a 2 KB Dual-Port RAM and a primitive interrupt mechanism. This example requires two sink ports and one source port for the data transfer, and port 15 to supply the STROBE\-signal. Two data transfers are required to perform a read or write access. The first transfer is used to supply the 8-bit address and, if a write access is intended, valid 8-bit data. The second transfer is used to read the data along with the previously supplied address. Using multiple ports allow applications with larger DPRAMs.

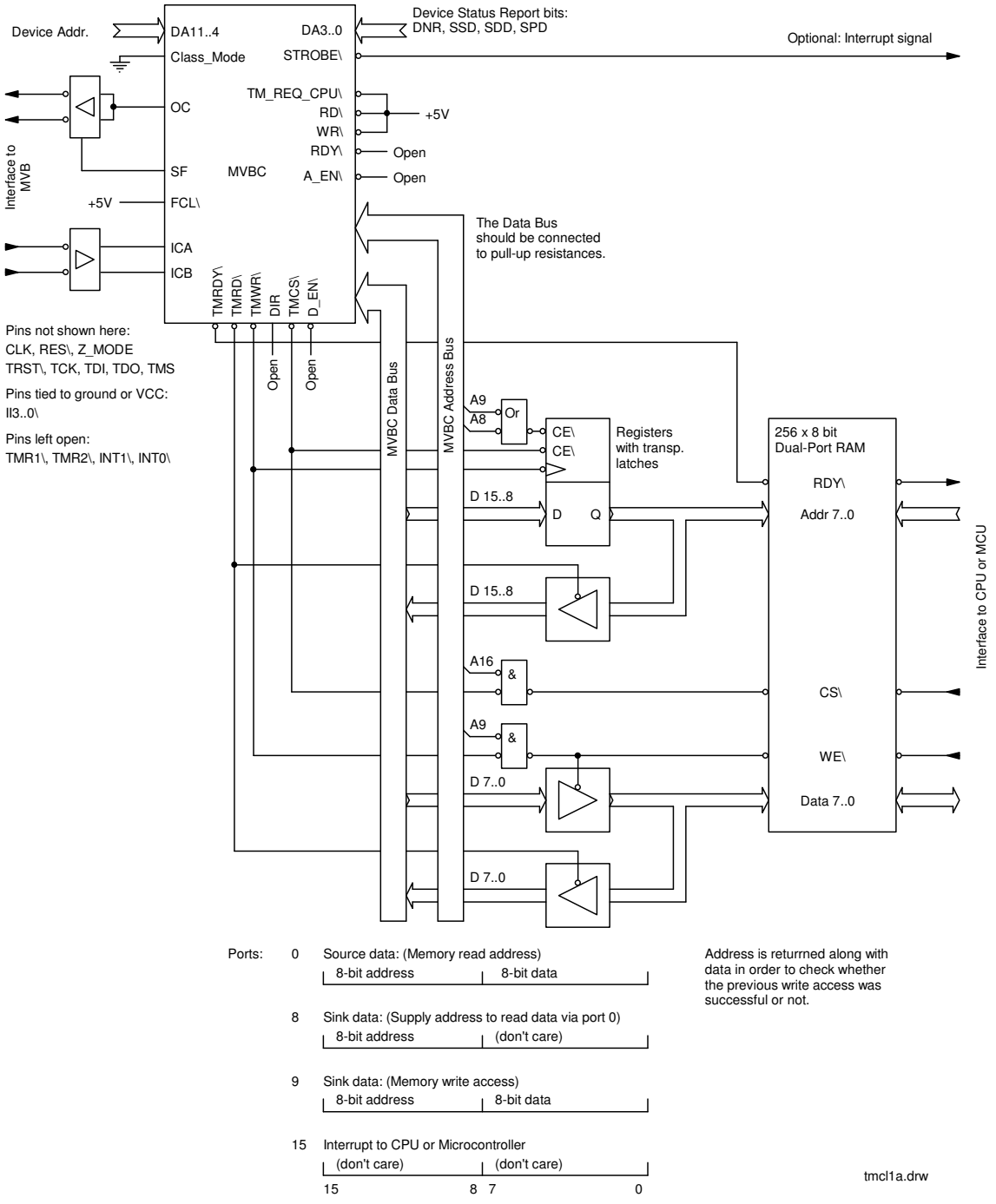


Figure 6.3: MVBC in Class 1 Mode and Dual-Port RAM

6.3 Interrupt, Timer and Strobe Signals

The MVBC provides two outgoing interrupt lines which should be connected to separate interrupt inputs at the host CPU. If only one input is available, then the two lines can be combined with an AND-gate. In this case, the interrupt handler software must check both ISR0/IVR0 and ISR1/IVR1 when an interrupt has occurred. On the other hand, the external interrupt inputs (II3..0) are available for any application.

If the host CPU provides more than two interrupt inputs, and must run a real-time system which is triggered by one Universal Timer, then the timer signal (TMR1\ or TMR2\) should be connected directly to an interrupt input in order to achieve minimum latency.

The STROBE\-Pin is a general-purpose active-low signal which may be used to interrupt the host CPU, synchronize an Universal Timer or trigger peripheral devices such as A/D converters. An easy way to let the STROBE\-signal cause an interrupt is to connect STROBE\ to one of $II_{3..0}$\.

6.4 Other Pins

Device Address $DA_{11..0}$:

The MVBC does not latch the DA at power-up. Therefore, a valid DA must be supplied while the MVBC is in service. DIP-Switches or hexadecimal rotary switches are strongly recommended. In Class 1 Mode, $DA_{3..0}$ supply information about Device Status and Line Switch Mode (DNR, SDD, SSD, LSM) which are not sampled. Valid values must be supplied at all time.

Z-Mode\: During normal operation, this pin is connected to VDD.

JTAG pins: If the Boundary Scan is not used, then all JTAG inputs except TRST should be connected to VDD. TRST is connected along with RESET\ to the asynchronous reset signal.

(Space below has been left blank intentionally)

7 PROGRAMMING GUIDELINES

This chapter gives a brief summary to initialize and operate the MVBC.

7.1 MVBC Initialization

The MVBC including JTAG Boundary Scan hardware must be reset with the asynchronous reset (RES\, TRST\). After that, the MVBC will be operating with Initialization Level IL=0 (Reset Mode) and MCM=0.

In this mode, the Traffic Memory is accessible, but all registers except the IL-bits (Initiation Level) of the Status Control Registers will be held at their initial values.

Step 1: Set IL to 1 to allow MVBC configuration

If a different Memory Configuration Mode should be used, then the configuration should be done now. If possible, the offset for Message Queues and MF-Tables should be defined.

Step 2: Write MCR to define MCM, QO and MO

If MCM is nonzero, then the Service Area has moved to its final position and shall no longer be moved around! If the TM works faster, then the number of waitstates should be reduced. Additional SCR parameters, such as Timeout Coefficient, Arbitration Strategy, should be defined. The MAS bit must be active for Bus Administrators. If Event Polling is supported, then RCEV must be active.

Step 3: Initial definition of SCR (but keep IL at 1)

Step 4: Configure and activate Universal Timers

Step 4 may be necessary if the host system requires timer pulses or interrupts. Example:

Timer 1: Basic Time Slot (i.e. 1 ms)

Timer 2: Timer Pulse for Real-Time Operating System

Step 5: RAM test on Traffic Memory (if required by user)

Before Process Data ports should be defined in the logical address space, the Port Index Table should be formatted in order to keep all unused ports inactive. The easiest solution is to clear the entire LA-PIT to zero so dock zero will be addressed by default. The PCS Word 0 and Word 1 of dock 0 shall also be zero in order to keep the port inactive.

Step 6: Format LA-PIT

Step 7: Format DA-PIT (same manner as with LA-PIT, if MCM>0)

Step 8: Clear PCS Word 0 and 1 of all Physical Ports

The last step assures that all Physical Ports are cleared. This is a safety measure in order to avoid unexpected MVBC behavior if not all Physical Ports are configured properly.

Step 9: Read original Device Address, or modify it

If the MVBC is connected to one MVB line only, the Decoder must be informed so.

Step 10: Switch lines if necessary, then set SLM to '1'

A read access to the Decoder Register shall be made afterward to assure SLM is set and the correct line is selected.

Step 11: Self-Test, if required

A few ports can be configured in order to transfer one or more telegrams over the internal loopback lines. At the end of the test, the initial PCS settings should be restored. Most MVBC functions, i.e. transfers with

all supported F-Codes, can be tested, but this may most likely limited by the time available to run the test before the system can go into full operation.

Step 12: Interrupt Controller

The interrupt controller should be activated for all interrupts which are used by the software. This step can take place while application-specific interrupt service routines are attached to the interrupt handler software. For all interrupts, which are not serviced, the corresponding bits in the Interrupt Mask Register shall be kept at zero.

7.2 TM and Port Initialization

Step 13: Initialization of all Process Data ports

All affected ports are located in the LA space. For every port, a Port Index must be defined and stored in the Port Index Table. Using the Port Index, the PCS must be configured and a defined value be written into the Data Area. If Forcing is active, then the Force Table must be configured accordingly.

Step 14: Initialization of Message Data Support

The affected ports are MSRC and MSNK. The PCS must be configured accordingly. Section 7.3 gives details on installing correct data structures for message queues.

Step 15: Initialization of ports for supervisory transfers

The Slave devices require proper configuration of EF0, EF1 and FC15. EF0 and EF1 are necessary to permit participation on Event Polling. FC15 must contain a correct initial Device Status Report.

Bus Administrators also require EFS, FC8 and MOS to be configured. Systems, which are in charge of collecting Device Status Reports, must initialize the DA space. This is done similarly as with the LA space.

Step 16: Bus Administrator: Master Frame Tables

This applies to Bus Administrators. If the MVBC shall transmit Master Frames automatically, then Master Frame Tables should be prepared. See section 7.4 for details.

Step 17: Sink-Time Supervision

Here, the maximum range of used LA ports must be known. The Sink-Time Supervision stays inactive until loopback test (IL=2) or full operation (IL=3) is enabled. The user must be careful not to choose a small time interval when the number of ports to be supervised is high. See Figure 3.15 in section 3.9.2. The TM traffic should not exceed 10%.

Step 18: Full Operation: Set IL to 3. Good Luck!

Step 19: Bus Administrator: Check for foreign active BA

The Bus Administrator must check if bus traffic is already present. If not, then a MF shall be sent. If a collision occurs, then it shall wait for a unique time period in order to watch the MVB and check if other masters are already active. If the time has elapsed and no Master Frame has been received meanwhile, then the Bus Administrator can start sending Master Frames. Otherwise, it must wait until it has been polled for Mastership Offer.

7.3 Message Queue Data Structures

If Message Queues are used, then the user must supply an adequate data structure the MVBC can work with. The MVBC considers following rules:

The MVBC treats nonexistent queues similarly as empty queues. The user may signify a non existing or empty Transmit Queue with one following parameter settings:

- Both QDT[XQ0] and QDT[XQ1] are zero
- First Data Pointers (DP) of both queues are zero
- Combinations of above

The empty Receive Queue can be specified in a similar manner:

- QDT[RQ] is zero
- First data Pointer (DP) is zero

The last record in a Transmit Queue can be specified with one of following parameter settings:

- Next Pointer (NP) in last LLR pointing to last valid data block is zero, in both Transmit Queues
- Data Pointer (DP) in subsequent LLR is zero, in both queues
- Combinations of above

The end of a Receive Queue can be specified in a similar manner:

- Next Pointer (NP) in last LLR is zero
- Data Pointer (DP) in subsequent LLR is zero

The user is free to choose linear linked lists or ring buffer structures. At least, the chosen data structure must be established before Message Data transfers start.

If the linear list solution is preferred, then the user should establish two linked lists for each queue where one list is attached to the MVBC while the other is attached to the software interface. 2*n* blocks are necessary to realize an effective buffer with capacity of *n* blocks. On the other hand, the ring buffer solution uses the memory more efficiently and requires only *n*+1 blocks.

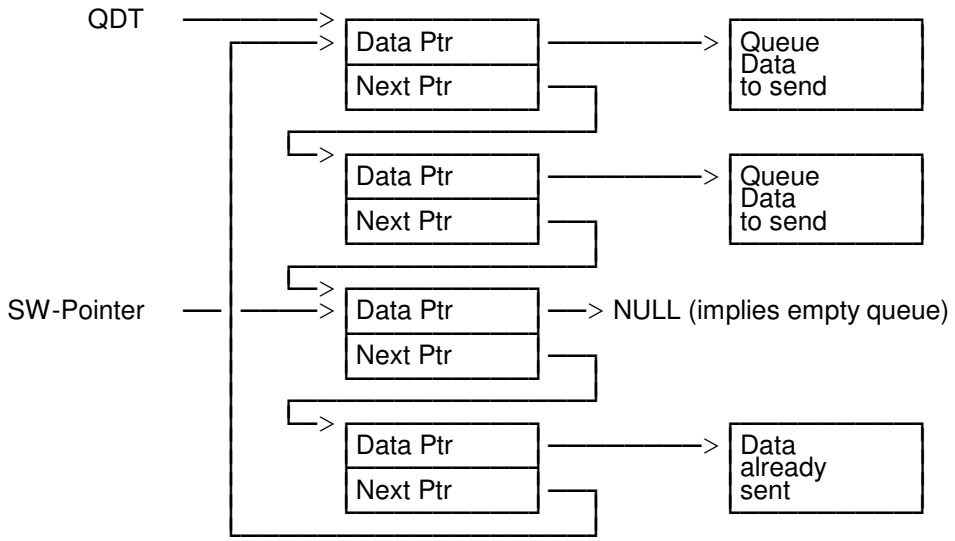


Figure 7.1: Ring-Buffer Solution for Message Queues

7.4 Master Frame Tables

Master Frame Tables allow the MVBC to send small series of up to 32 Master Frames automatically. These tables are primarily intended to handle cyclic Process Data. If the slot time is 1 ms, then up to 15-20 telegrams transferred within each time slot. One cycle contains a defined number of time slots. This depends on the biggest time interval for Process Data. If the interval is 1024 ms (210), the cycle contains 1024 time slots. Each time slot is associated with one MF-Table. However, one MF-Table can be shared among multiple time slots if the same Process Data variables must be transferred.

1. Assume ca 16 Master Frames per interval are exchanged. The size of each table ends up to be 16 words (some may require 8, 24 or 32 word blocks) -> 32 byte average.

2. 1024 x 32 bytes = 32 KB

3. A table containing frame sizes is required. This table may either be located in the Traffic Memory or in CPU local RAM workspace. The size is 1024 x 8 = 8 KB.

4. A MF Pointer Table is necessary to store the start addresses to every MF Table. The MF Pointer Table may be located in the TM or in the CPU local RAM workspace. The size is 1024 x 16 = 16 KB.

Result: Storing all Master Frame Tables requires roughly 56 KB. If several tables are identical (say 50% of them), then the duplicate MF-Tables can be discarded so the MF Table size reduces from 32 KB down to 16 KB. The overall memory requirement reduces from 56 KB down to 40 KB. MF-Tables to be distributed over all unused TM fragments. For the 1 MByte TM, all MF-Tables must be located within one aligned 256 KB block. The following figure summarizes the data recommended data structure:

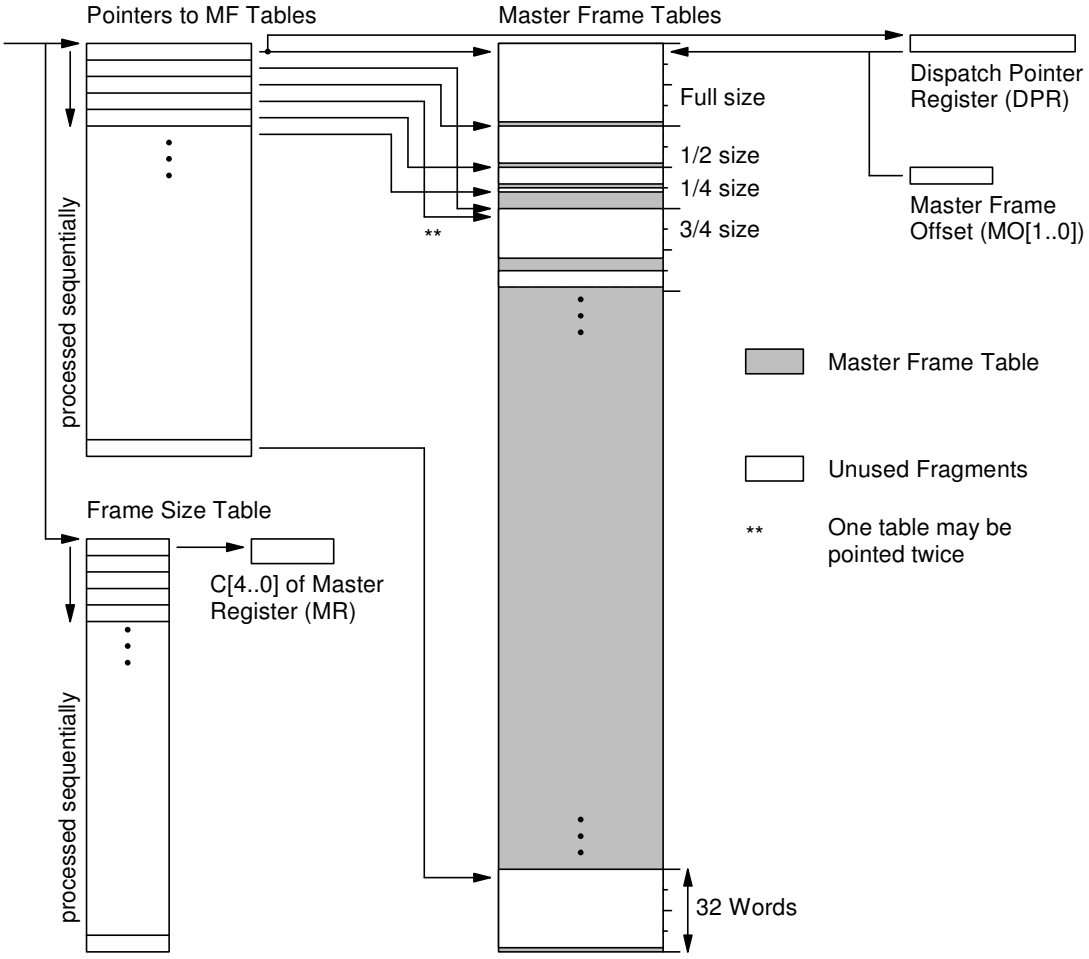


Figure 7.2: Recommended Data Structure for Managing MF-Tables

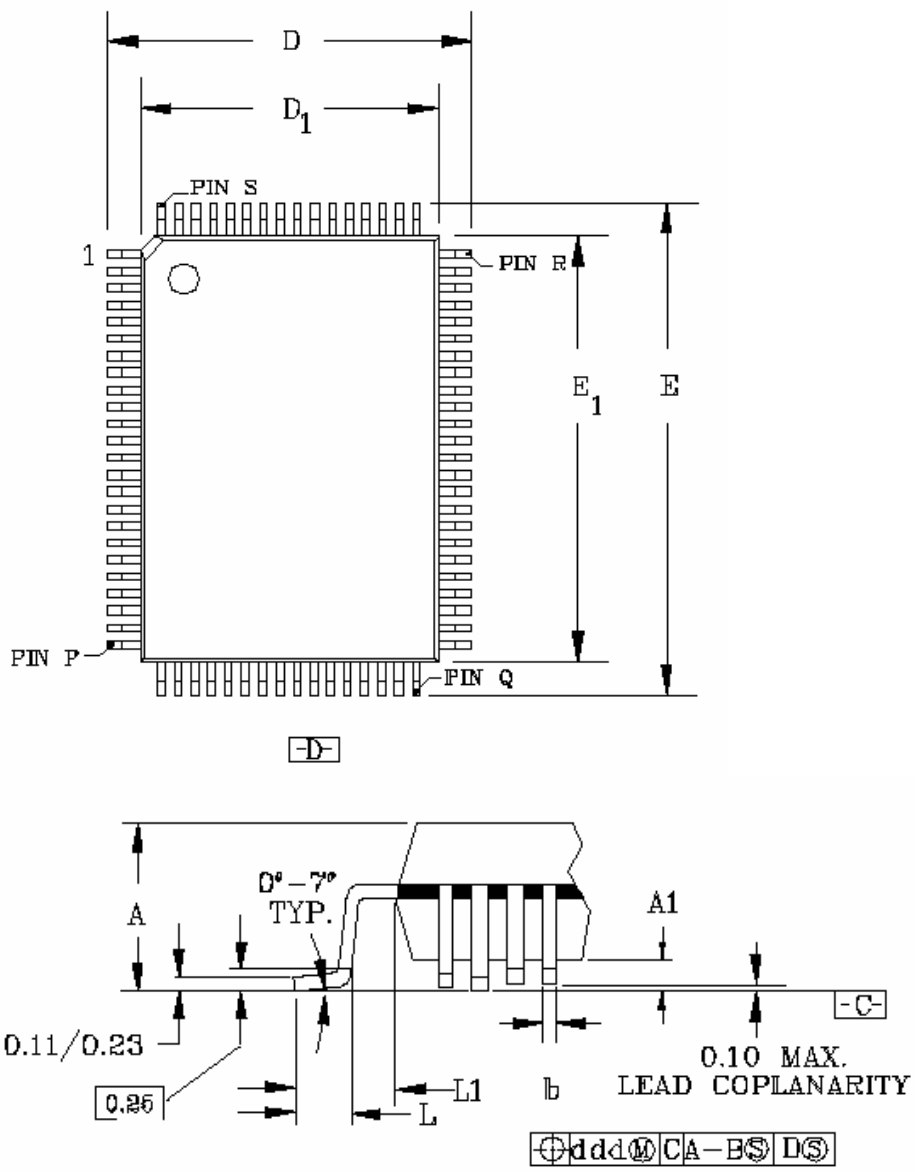
Insufficient TM Space for MF-Tables:

If the MF-Tables do not fit into the TM, then one would suggest to implement some sort of intelligent *caching mechanism* in order to keep additional TM traffic at a minimum. First, the programmer should identify the MF-Tables which are used frequently. These tables should reside in the TM permanently. Less frequently used MF-Tables should be copied from CPU local RAM workspace to the TM upon request.

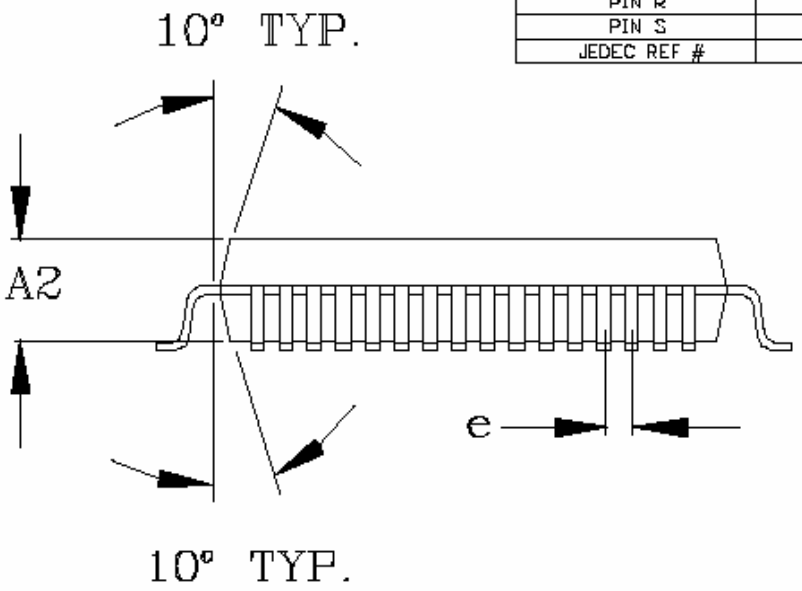
8 TECHNICAL DATA

8.1 Mechanical Data

100 pin QFPP quad flat pack plastic, dimensions see following page:



DIMS.	LEADS / TOL.	100
A	MAX.	3.40
A1	MIN / MAX	0.25 / 0.50
A2	MIN / NOM / MAX	2.50 / 2.70 / 2.90
D	BASIC	17.20
D1	BASIC	14.00
E	BASIC	23.20
E1	BASIC	20.00
L	±0.15	0.88
L1	REF	1.60
e	BASIC	0.65
b	MIN / MAX	0.22 / 0.40
ddd	NOM	0.13
PIN P		30
PIN Q		50
PIN R		80
PIN S		100
JEDEC REF #		MS-022



Notes:

- Chips are delivered in plastic packages.
- All dimensions are given in mm, which is controlling dimension
- The value of theta is measured in degrees

Figure 8.1: 100-Pin QFPP

8.2 Operating and Absolute Maximum Ratings

Warning: Exceeding absolute ratings may lead to permanent damage of the MVBC.

Power Supply Voltage: -0.5 V ... +7 V

Supply Voltage relative to Vss to any pin except Vcc:
-0.5 V to Vcc+0.5V

Maximum output current: 16 mA (short circuit load)

Soldering temperature: 235 °C
Operating temperature range: -40 ... 85 °C
Storage temperature: -55 ... 150 °C

Supply current: I_{cc} = 60 mA (@ 5 volts)
I_{cc} = 40 mA (@ 3.3 volts)

8.3 Recommended Operating Conditions

Description		Test Condition	Min	Typ	Max	Unit
Supply Voltage Vcc	V_{CC}	5 volts operation	4.50	5.00	5.50	V
Supply Voltage Vcc	V_{CC}	3.3 volts operation	3.00	3.30	3.60	V
Input Voltage, High	V_{IH}	5 volts operation	2.00	-	5.50	V
Input Voltage, High	V_{IH}	3.3 volts operation	2.00	-	3.60	V
Input Voltage, Low	V_{IL}	-	-0.50	-	0.80	V

Table 8.1: Recommended Operating Conditions

8.4 DC Electrical Characteristics

Default conditions: V_{DD} = +5 V, T = 25 °C, V_{SS} = 0 V (Ground)

Description		Test Condition	Min	Typ	Max	Unit
Output Voltage, High	V_{OH}	I_{OH} ·= -4 mA	2.40	-	-	V
Output Voltage, Low	V_{OL}	I_{OL} = +4 mA	-	-	0.40	V
Input Current, High	I_{IH}	$V_{in} = V_{SS}$	-	-	-10.0	µA
Input Current, Low	I_{IL}	$V_{in} = V_{DD}$	-	-	10.0	µA
Output Current, High	I_{OH}	$V_{out} = V_{OH}$	4.00	-	-	mA
Output Current, Low	I_{OL}	$V_{out} = V_{OL}$	4.00	-	-	mA
Tristate output leakage current	I_{OZ}	$V_{out} = V_{DD}$	-	-	10	µA
Fan-Out (74LS inputs)			10	-	-	inputs
Input Capacitance	C_{in}	including package	-	-	10	pF
Output Capacitance	C_{out}	including package	-	-	10	pF

Table 8.2: DC Electrical Characteristics

8.5 AC Electrical Characteristics

Description		Test Condition	Min	Typ	Max	Unit
Input rise time	t_R	0.8 - 2.0 V levels	-	-	100	ns
Input fall time	t_F	0.8 - 2.0 V levels	-	-	100	ns

Table 8.3: AC Electrical Characteristics

Further AC characteristics: see chapter 9: Timings.

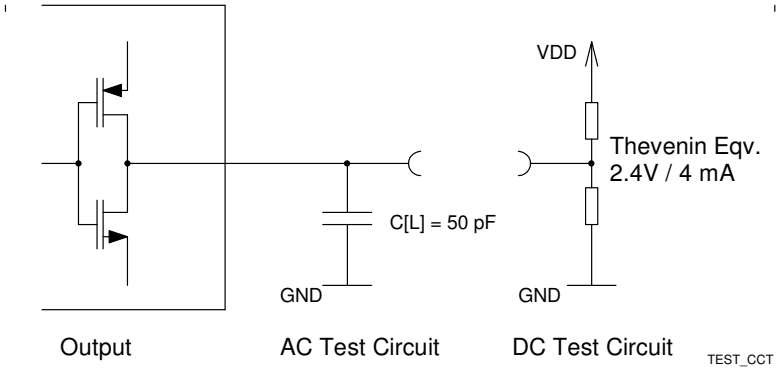


Figure 8.2: AC and DC Test Circuits

9 TIMINGS

All timings have been derived from timing analysis and simulation tools at worst-case conditions (50 pF load, +85 °C, minimum allowed supply voltage, expected worst-case fabrication lot, process corners etc.).

9.1 General Timings

Clock Signal:

The MVBC can operate both synchronously and asynchronously with the host CPU. Asynchronous operation is understood where the MVBC and host CPU are attached to separate clock signal oscillators. For asynchronous operation, greater care must be given on the timing of the TM and register access control signals (TM_REQ_CPU\, RD\, WR\, etc.), address and data bus. Mechanism have been implemented to avoid internal metastability situations when control signals change at inconvenient periods with respect to the rising clock edge.

Synchronous operation allows a more time-efficient communication between the MVBC, TM and host CPU. In this case, the clock frequency of the host CPU is not limited to 24 MHz only. A fraction or a multiple of this frequency can be used instead (i.e. 8, 12, 16, 24, 36, 48 MHz).

Symbol	Parameter	min	typ	max	Unit
tCLCK	Clock Signal Low Time	16.7	20.8	25	ns
tCHCK	Clock Signal High Time	16.7	20.8	25	ns
tCKHL	Clock Signal Fall Time (level V_{IH}, V_{IL})	-	-	5	ns
tCKLH	Clock Signal Rise Time	-	-	5	ns
tCKIN	Clock Input Period [1] (at level V_{IT}) [2]	-	41.7	-	ns
Duty Cycle	Clock signal level ratio	40	50	60	%

[1] The clock period will affect data transfer rate and all other timing parameters such as Reply Timeout, Bus Timeout, etc.

[2] V_{IT} applies to middle voltage level, $V_{IL} < V_{IT} < V_{IH}$. See also Figure 9.1.

Table 9.1: Timing Symbols for Clock Signal

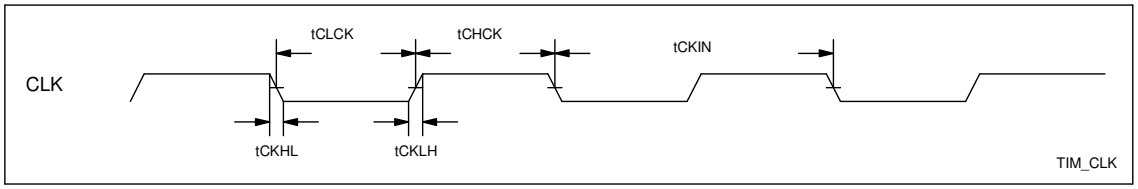


Figure 9.1: Clock Signal

V_{IT} applies to middle voltage level, $V_{IL} < V_{IT} < V_{IH}$ and is used as middle voltage reference points for all further timing diagrams.

(Space below has been left blank intentionally)

General Input and Output Signal Delays:

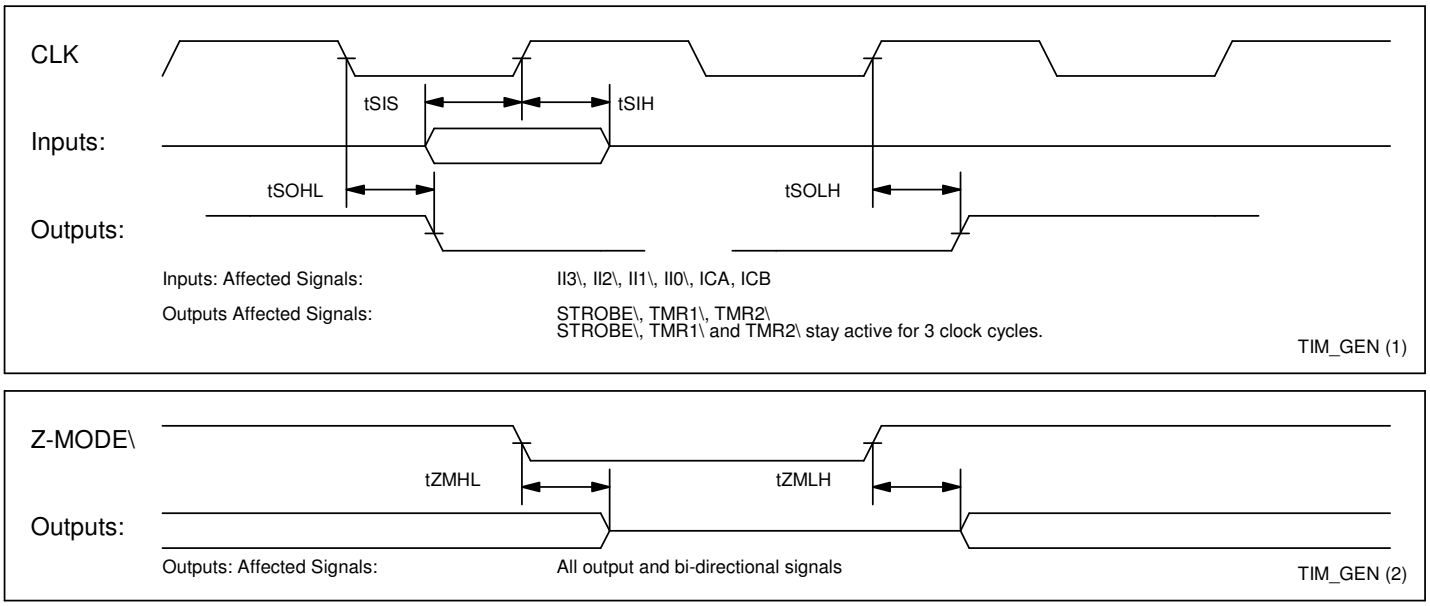


Figure 9.2: Synchronous Inputs, Synchronous Outputs, High-Impedance Mode

Symbol	Parameter	min	typ	max	Unit
tSIS	Setup Time for synchronous input signals	3	-	-	ns
tSIH	Hold Time for synchronous input signals [1]	1	-	-	ns
tSOHL	High-to-Low propagation delay for synchronous output signals	-	-	23	ns
tSOLH	Low-to-High propagation delay for synchronous output signals	-	-	25	ns
tZMHL	Z-Mode becoming active until all outputs changed to high impedance	-	-	12	ns
tZMLH	Z-Mode becoming inactive until all outputs have been re-enabled	-	-	22	ns

1 The hold time applies only if JTAG boundary scan test is made. Otherwise, it is zero.

Table 9.2: Timing Symbols for Synchronous Signals, High-Z Pin

Asynchronous Reset:

Proper operation is guaranteed, if both MVBC logic and the JTAG test facility are reset (TRST\). If application environment supports no JTAG signals, then TRST\ must also be connected to RESET\.

Symbol	Parameter	min	typ	max	Unit
tRESL	Reset signal duration	125	-	-	ns
tRESS	Reset signal setup time [1]	12	-	-	ns
tRESH	Reset signal hold time [1]	0	-	-	ns
tRESP	Reset signal to output signals settling to initial values	-	-	34	ns
tTAED	A_EN\ synchronously settling to initial value after reset	-	-	14	ns
tCASA	Addr. A19 ... 1 synchronously settling to initial values after reset	-	-	20	ns

1 Even though RESET\ is an asynchronous reset, it must not be deactivated inside the forbidden zone where the clock signal changes from '0' to '1'. Violations may cause metastability and inadequate operation.

Table 9.3: Timing Symbols for Asynchronous Reset

(Space below has been left blank intentionally)

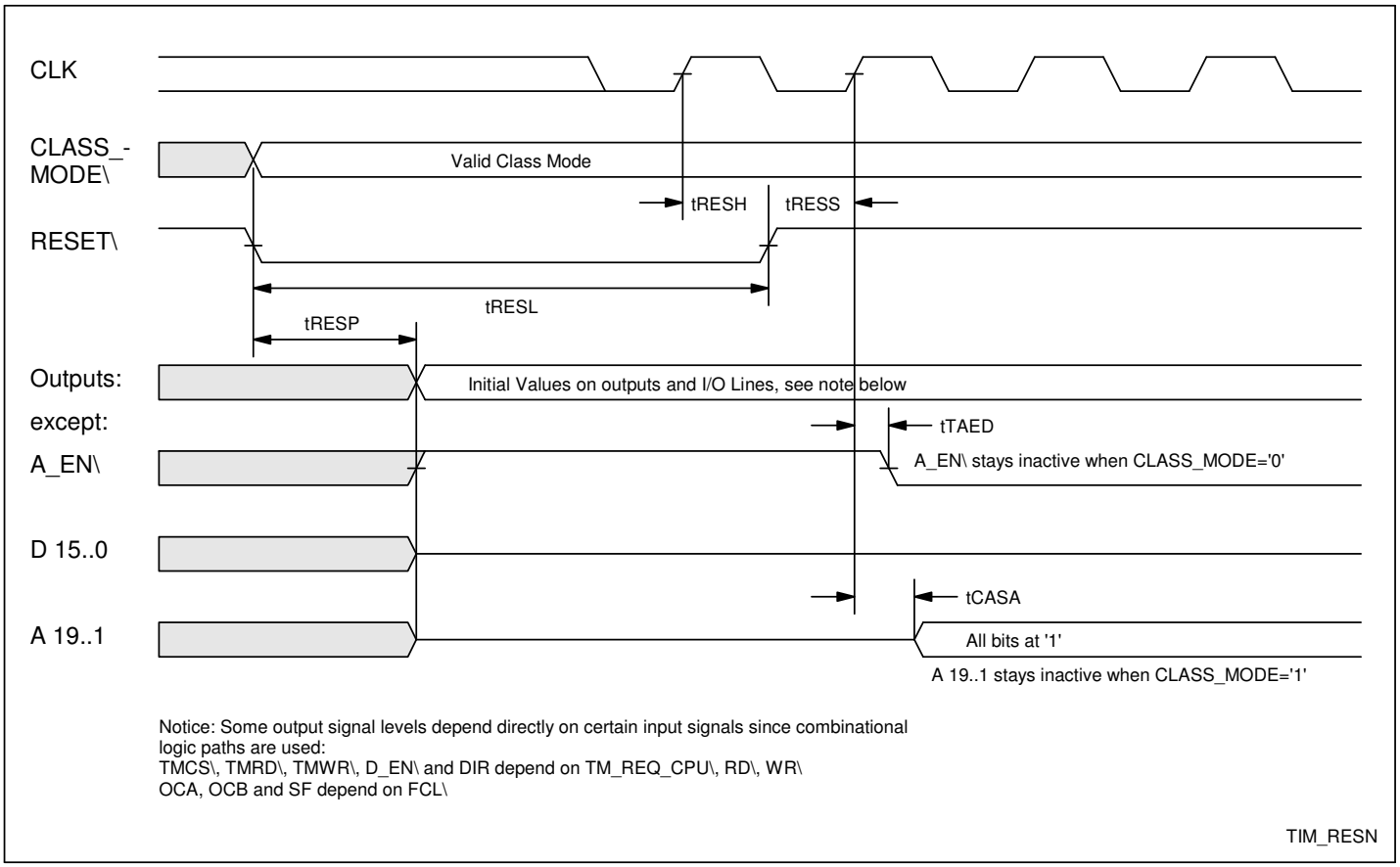


Figure 9.3: Asynchronous Reset

Miscellaneous Signals:

Symbol	Parameter	min	typ	max (5V)	max (3.3V)	Unit
tINHL,tINLH	Clock to falling / rising INT0\, INT1\	-	-	14	15	ns
tSIQS	Setup time for ext. interrupt	25	-	-	-	ns
tSIQH	Hold time for ext. interrupt	0	-	-	-	ns
tXIP	Penetration time for external interrupts to INT1\ [1]	-	-	160	160	ns
tOCHL. -H	Clock to falling / rising OC	-	-	13	15	ns
tSFHL, -H	Clock to falling / rising SF	-	-	13	15	ns
tFCHL, -H	falling / rising FCL\ to OC rising / falling	-	-	10	11	ns

[1] Sum of tSIQS, 3 clock cycles, tINLH

Table 9.4: Timing Symbols for Miscellaneous Signals

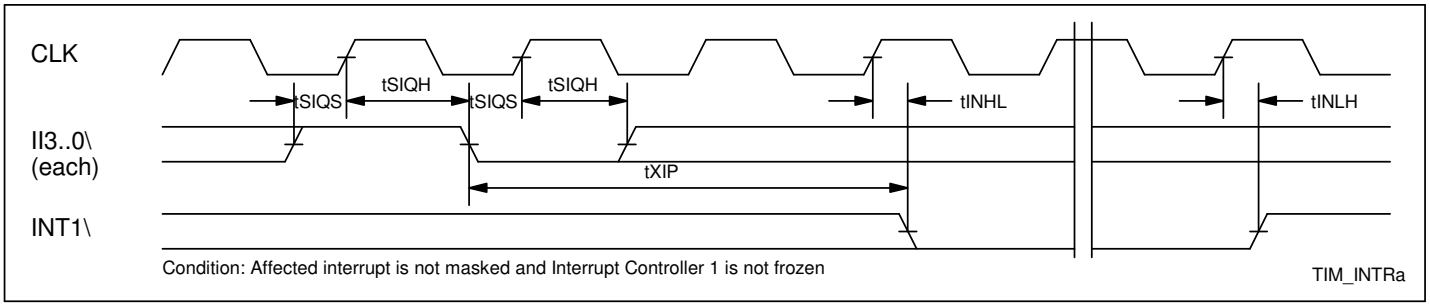


Figure 9.4: Propagation of External Interrupts

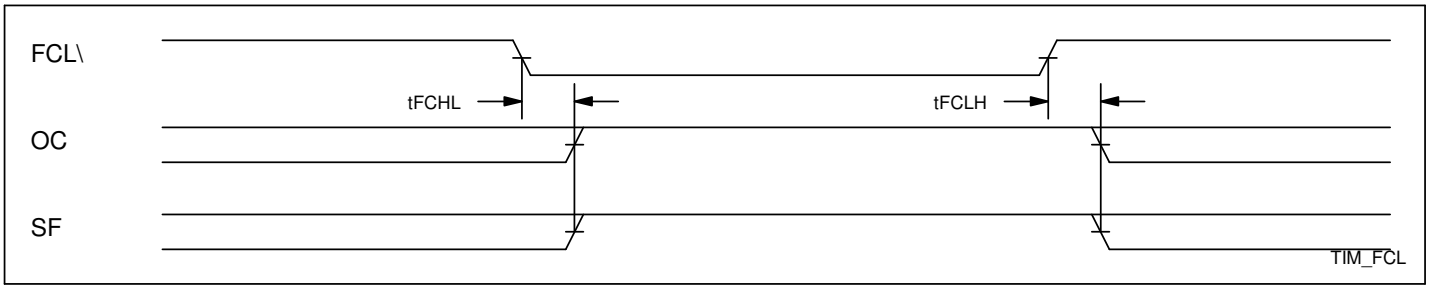


Figure 9.5: Combinational logic path for FCL

9.2 Timings for MVBC and CPU Accesses

Symbol	Parameter	min	typ	max (5V)	max (3.3V)	Unit
tCSL	TM_REQ_CPU\ active time	$4*t_{CKIN}$	-	-	-	ns
tCSS	TM_REQ_CPU\ setup time (for recognition at next clock cycle)	4	-	-	-	ns
tAP	access (TM_REQ_CPU\, RD\ or WR\) passive time	$1*t_{CKIN}$	-	-	-	ns
tRDL	RD\ active time	$3*t_{CKIN}$	-	-	-	ns
tRDS	RD\ setup time (for recognition at next clock cycle)	4 (6 @ 3.3V)	-	-	-	ns
tRRDH	RD\ active hold time after RDY\ falling	0	-	-	-	ns
tWRL	WR\ active time	$2.5*t_{CKIN}$	-	-	-	ns
tWRS	WR\ setup time (for recognition at next clock cycle)	4 (6 @ 3.3V)	-	-	-	ns
tRWRH	WR\ active hold time after RDY\ falling	0				ns
tRDYR	Access[1] beginning to RDY\ rising delay	-	-	12	14	ns
tRDYF	Rising clock edge to RDY\ falling delay	-	-	20	23	ns
tDACKS	Rising clock edge to DACK\ falling delay	-	-	20	23	ns
tDACKH	Access[1] end to DACK\ rising delay	-	-	12	14	ns
tRDYH	RDY\ passive time	-	-	$65*t_{CKIN}$	$65*t_{CKIN}$	ns
tTMCSF, -R	Rising clock edge to falling / rising TMCS\	-	-	17	20	ns
tTMCS	TMCS\ active duration	-	$4*t_{CKIN}$	-	-	ns
tTMCSH	TMCS\ rising hold after TM_REQ_CPU\ rising	0	-			ns
tTMRDF, -R	Rising clock edge to falling / rising TMRD\	-	-	17	20	ns
tTMRDL	TMRD\ active duration (MVBC access)	-	$2*t_{CKIN}$	-	-	ns
tTMRDH	TMRD\ rising hold after RD\ rising	4	-	-	-	ns
tTMRD	TMRD access time (CPU access)	-	$2*t_{CKIN}$			ns
tTMWRF,-R	Rising/Falling clock edge to falling / rising TMWR\	-	-	17	19	ns
tTMWRL	TMWR\ active duration (MVBC access)	-	$1.5* t_{CKIN}$	-	-	ns
tTMWR	TMWR access time (CPU access)	-	$2*t_{CKIN}$	-	-	ns
tAENF, -R	Rising clock edge to falling / rising A_EN\	-	-	13	14	ns
tDENF, -R	Rising clock edge to falling / rising D_EN\	-	-	14	16	ns
tDIRF, -R	Rising clock edge to falling / rising DIR	-	-	14	16	ns
tDIRH	DIR hold after WR\ rising	0				ns
tDENH	D_EN\ hold after WR\, RD\ rising	0	-			ns
tTMRDYS	TMRDY\ setup time (for recognition at next clock cycle)	7	-	-	-	ns
tTMRDYH	TMRDY hold after clock-edge ↑	0	-	-	-	ns
tADDS	Address bus setup prior to RD\, WR\ falling, if A_EN\ = 0	0	-	-	-	ns
tADDH	Address bus hold after RD\, WR\ rising	0				ns
tADDAES	Address bus setup to latching clock-edge ↑ (after A_EN\ -> 0)	6				ns
tADDWS	Rising clock edge to address bus valid / changing	-	-	19	22	ns
tADDWH	Address bus hold after clock-edge ↑	0	-	-	-	
tADDRS	Address setup to TMRD\	-	$1*t_{CKIN}$	-	-	ns
tADDRH	Address hold after TMRD\	-	$1*t_{CKIN}$	-	-	ns
tDATWS	Rising clock edge to data bus valid for write	-	-	19	23	ns
tDATWH	Data hold after TMWR\ ↑ inactive	-	$0.5*t_{CKIN}$	-	-	ns
tDATRS	Data bus valid (setup) to latching clock-edge ↑ [2]	16 (21 @3.3V)	-	-	-	ns
tDATRH	Data hold after latching clock-edge ↑ TMRD\ ↑	0	-	-	-	ns
tDATRDS	Data setup after clock edge recognizing RD\ falling, if A_EN\ = 0	-	-	$2*t_{CKIN}$ +19	$2*t_{CKIN}$ + 23	ns
tDATRDH	Data hold after RD\ rising,	0	-	-	-	ns

Signals RD\, WR\ are synchronized to clk, asserting TMRD\, TMWR\

[1] Access is understood as TM_REQ_CPU\ combined with RD\ or WR\. Read Access and Write Access correlate to RD\ and WR\ only

[2] This requirement request memory access time of < (tCKIN – tDATRS) or additional wait/ready cycles

Table 9.5: Timing Symbols for MVBC Accesses to TM

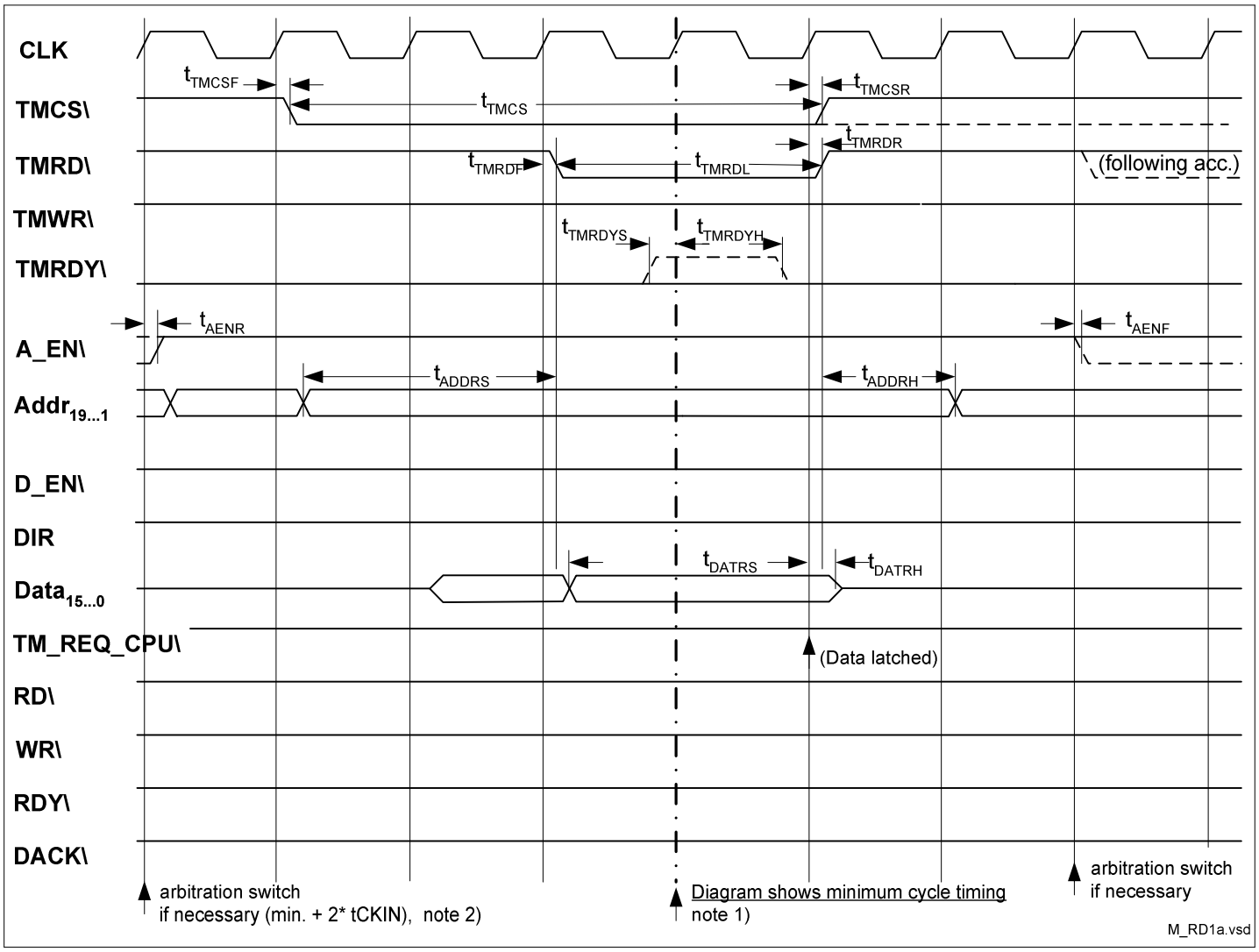


Figure 9.6: Read Access by MVBC to TM

Note:

1) Additional wait cycles are introduced here: 0 ... 3 * tCKIN depending on configured wait states (see SCR) and (n * tCKIN) if TM_RDY\ is still inactive (TM_RDY\ = 1).
Maximum count of additional wait cycles is restricted to (63 * tCKIN), otherwise a forced termination of read access occurs (tTMRDL max. 65 * tCKIN, TM_RDY\ = 1 for < 64 * tCKIN).

2) If an arbitration switch is necessary prior or after access, it takes in minimum two cycles tCKIN (obviously more for some wait cycles, if CPU access is in progress simultaneously (not shown in this diagram)).

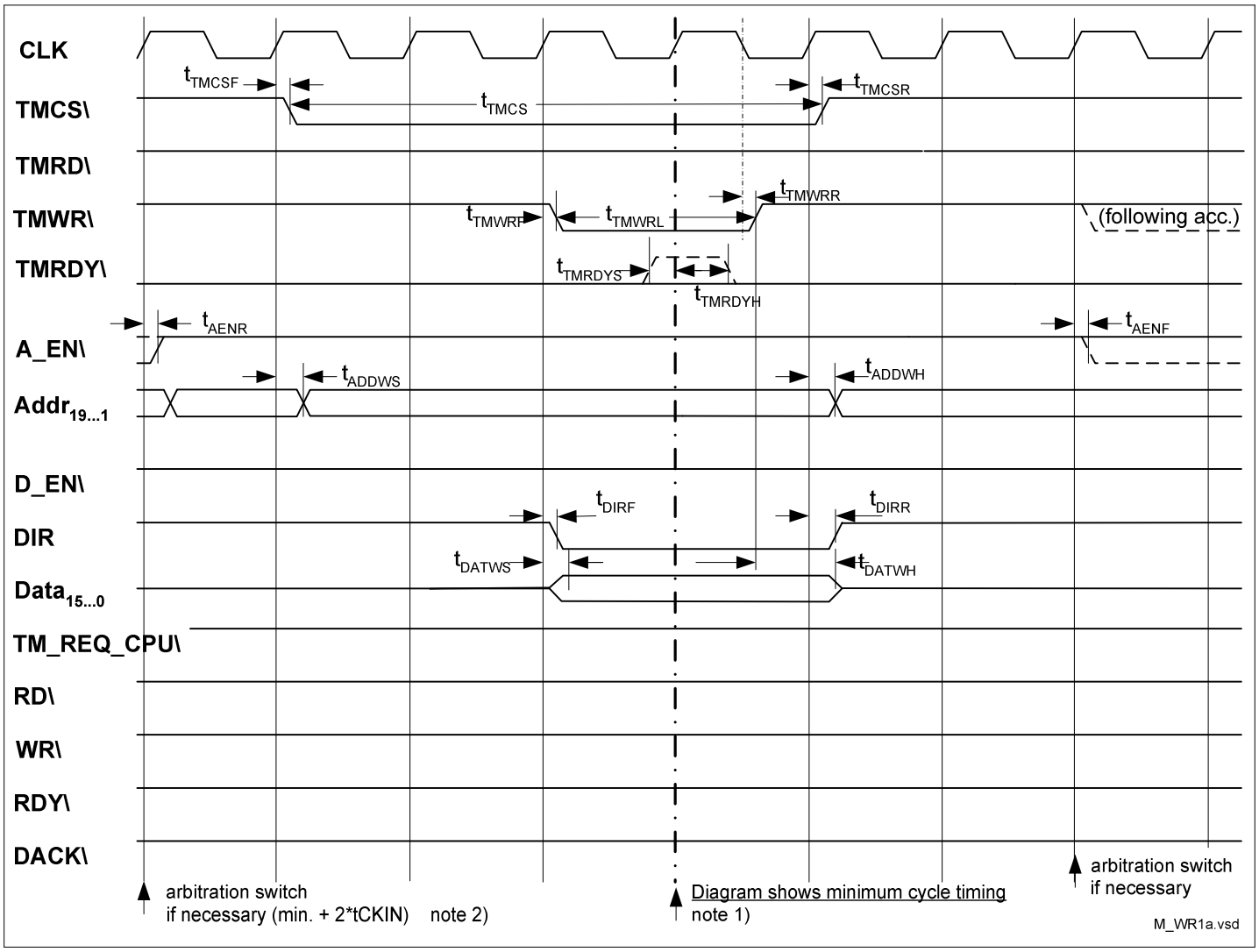


Figure 9.7: Write Access by MVBC to TM

1) Additional wait cycles are introduced here: 0 ... 3 * tCKIN depending on configured wait states (see SCR) and additional (n * tCKIN) if TM_RDY\ is still inactive (TM_RDY\ = 1).
Maximum count of additional wait cycles is restricted to (63 * tCKIN), otherwise a forced termination of write access occurs (tTMWRL max. 64.5 * tCKIN, TM_RDY\ = 1 for < 64 * tCKIN).

2) If an arbitration switch is necessary prior or after access, it takes in minimum two cycles tCKIN (obviously more for some wait cycles, if CPU access is in progress simultaneously (not shown in this diagram)).

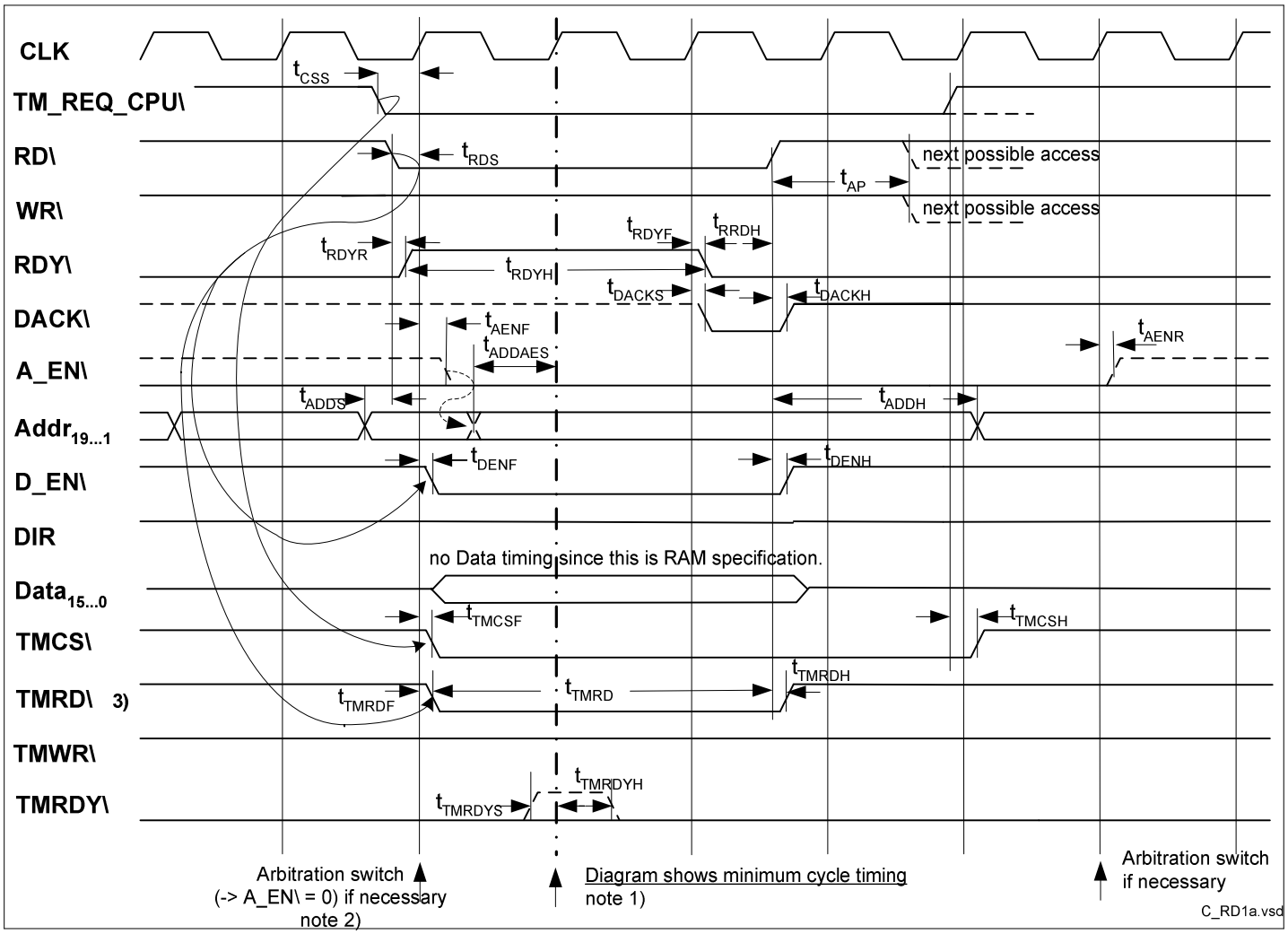


Figure 9.8: Read Access by CPU to TM

Note:

1) Additional wait cycles are introduced here: 0 ... 3 * tCKIN depending on configured wait states (see SCR) and (n * tCKIN) if TM_RDY\ is still inactive (TM_RDY\ = 1).
Maximum count of additional wait cycles is restricted to (63 * tCKIN), otherwise a forced termination of read access is performed by asserting RDY\ = 0 (tTMRD max. 65 * tCKIN, TM_RDY\ = 1 for < 64 * tCKIN).

2) If an arbitration switch is necessary prior or after access, it takes in minimum two cycles tCKIN (obviously more for some wait cycles, if CPU access is in progress simultaneously (not shown in this diagram)).

3) In case of active MVBC-access (A_EN\ = 1), an arbitration switch takes place after MVBC access is finished. In this case A_EN\ = 0 (dashed line) and TMCS\ = 0 will be activated simultaneously where activation of TMRD\ = 0 will be delayed one tCKIN.

TMRD\ , A_EN\, D_EN\ are synchronously activated after RD\ recognized.

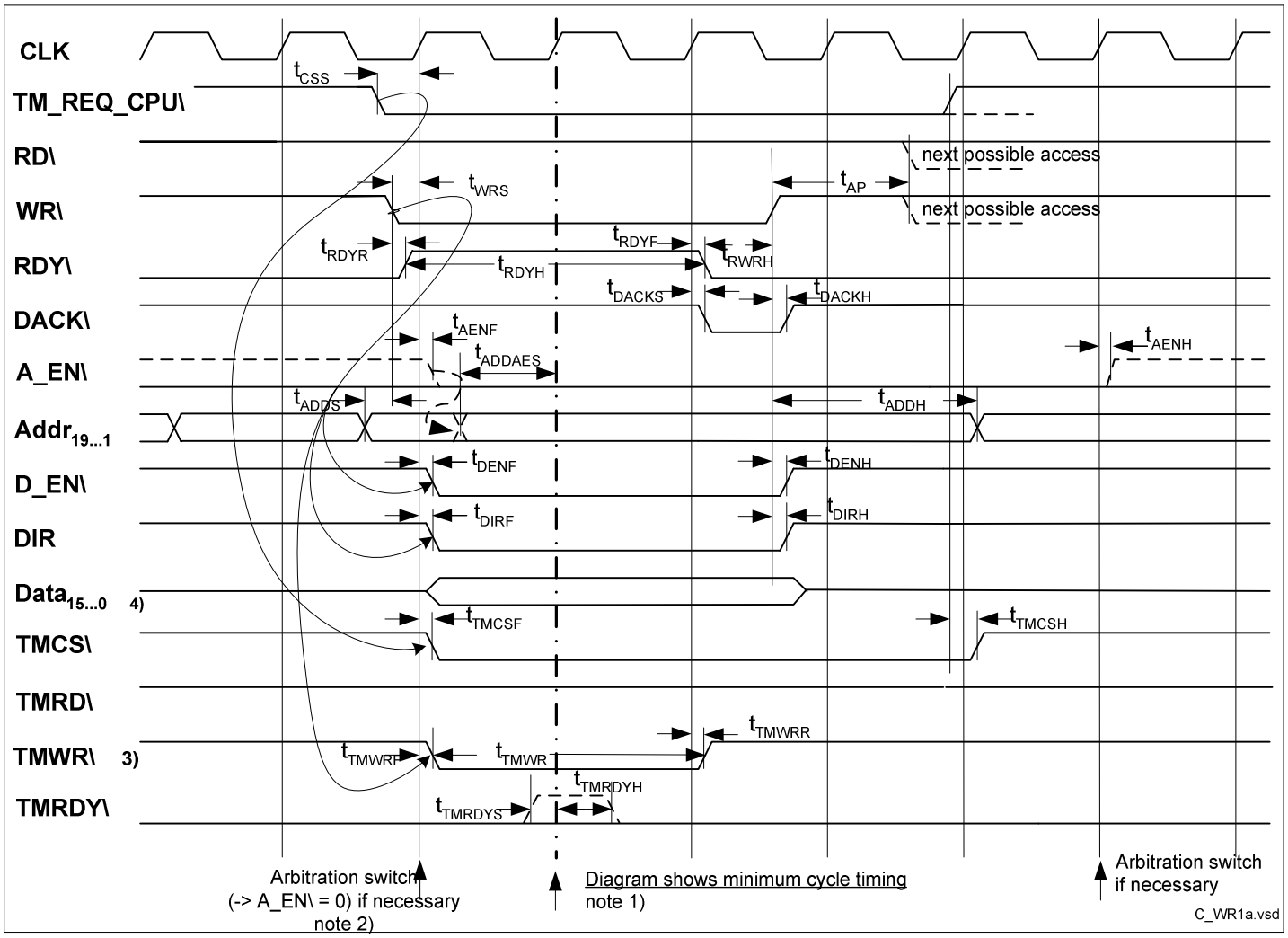


Figure 9.9: Write Access by CPU to TM

Note:

1) Additional wait cycles are introduced here: 0 ... 3 * tCKIN depending on configured wait states (see SCR) and (n * tCKIN) if TM_RDY\ is still inactive (TM_RDY\ = 1).
Maximum count of additional wait cycles is restricted to (63 * tCKIN), otherwise a forced termination of write access is performed by asserting RDY\ = 0 (tTMWR max. 65 * tCKIN, TM_RDY\ = 1 for < 64 * tCKIN).

2) If an arbitration switch is necessary prior or after access, it takes in minimum two cycles tCKIN (obviously more for some wait cycles, if CPU access is in progress simultaneously (not shown in this diagram)).

3) In case of active MVBC-access (A_EN\ = 1), an arbitration switch takes place after MVBC access is finished. In this case A_EN\ = 0 (dashed line) and TMCS\ = 0 will be activated simultaneously where activation of TMWR\ = 0 will be delayed one tCKIN.

4) No data timing specified, since this is CPU responsibility. MVBC address and data pins are in High-Impedance state.

TMRD\ , A_EN\, D_EN\, DIR are synchronously activated after WR\ recognized.

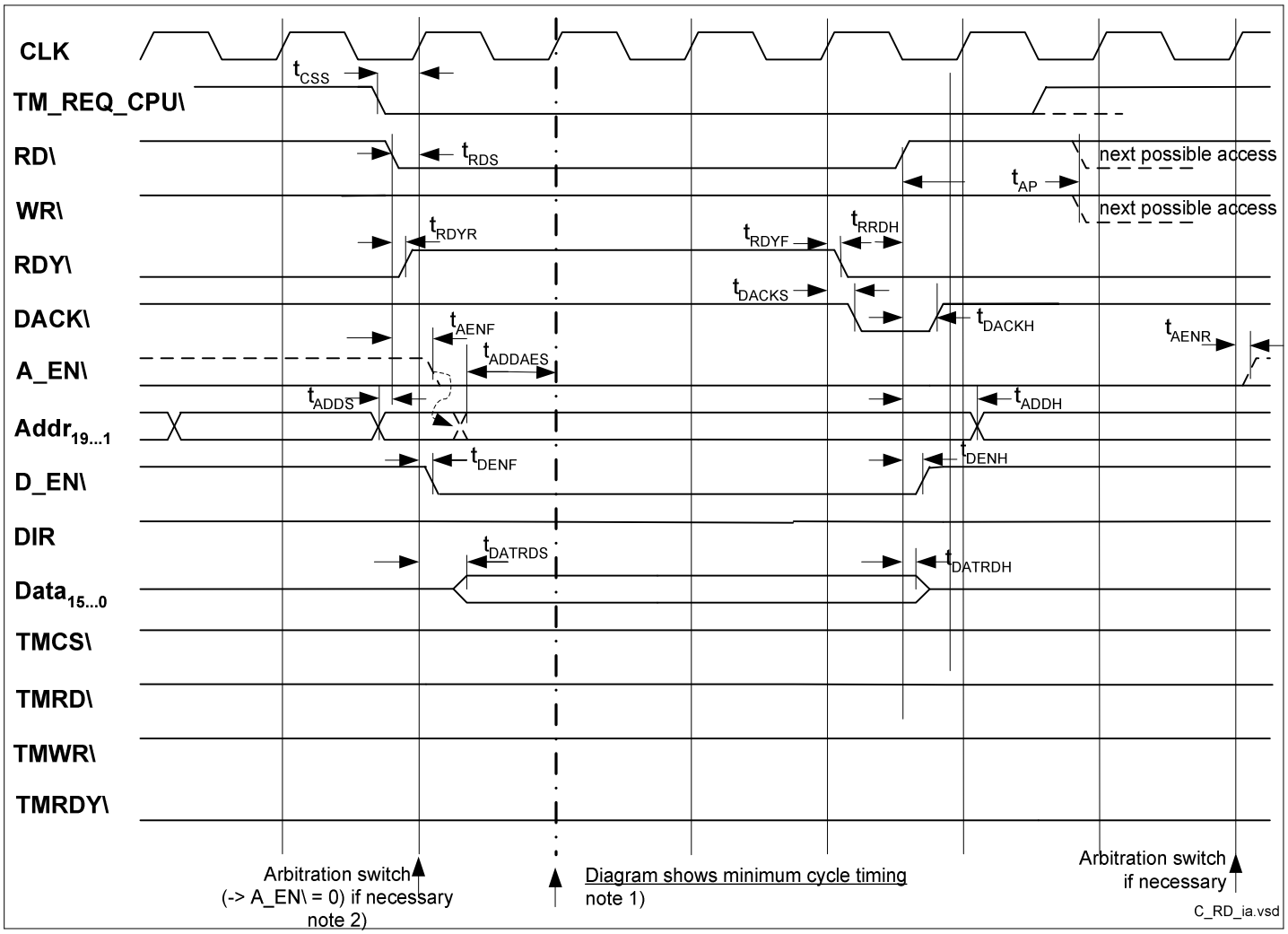


Figure 9.10: Read Access by CPU to Internal Registers

Note:

1) Additional wait cycles are introduced here: 0 ... 3 * tCKIN depending on configured wait states (see SCR) and (n * tCKIN) if TM_RDY\ is still inactive (TM_RDY\ = 1).
Maximum count of additional wait cycles is restricted to (63 * tCKIN), otherwise a forced termination of read access is performed by asserting RDY\ = 0 (tTMRD max. 65 * tCKIN, TM_RDY\ = 1 for < 64 * tCKIN).

2) If an arbitration switch is necessary prior or after access, it takes in minimum two cycles tCKIN (obviously more for some wait cycles, if CPU access is in progress simultaneously (not shown in this diagram)).

For accesses to Internal Registers, the MVBC assumes at least one wait state in order to synchronize the incoming read instructions and retrieve the data from the requested register. Due to this, minimum access is one cycle longer than to TM.

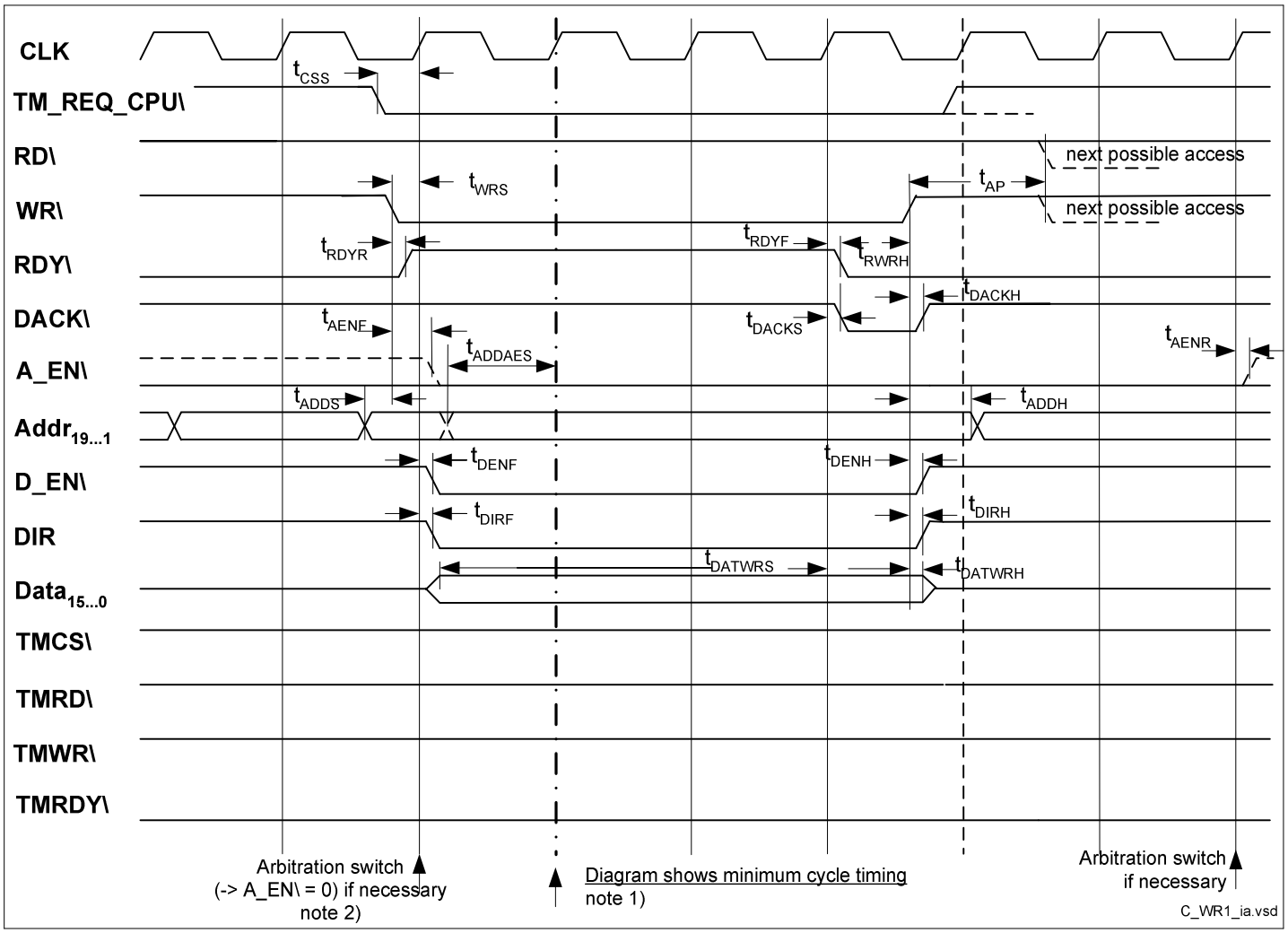


Figure 9.11: Write Access by CPU to Internal Registers

Note:

1) Additional wait cycles are introduced here: 0 ... 3 * tCKIN depending on configured wait states (see SCR) and (n * tCKIN) if TM_RDY\ is still inactive (TM_RDY\ = 1).
Maximum count of additional wait cycles is restricted to (63 * tCKIN), otherwise a forced termination of write access is performed by asserting RDY\ = 0 (tTMWR max. 65 * tCKIN, TM_RDY\ = 1 for < 64 * tCKIN).

2) If an arbitration switch is necessary prior or after access, it takes in minimum two cycles tCKIN (obviously more for some wait cycles, if CPU access is in progress simultaneously (not shown in this diagram)).

For accesses to Internal Registers, the MVBC assumes at least one wait state in order to synchronize the incoming read instructions and retrieve the data from the requested register. Due to this, minimum access is one cycle longer than to TM.

MF Dispatcher Latency Data:

Symbol	Parameter	min	typ	max	Unit
tSMFM	SMFM/SMFA: Latency btw completed access to MR and SF rising	-	6*tCKIN	-	ns
tSMFT	SMFT: Latency between II3\ and SF rising to transmit MF	-	8*tCKIN	-	ns
tSMFE	SMFE Latency between II3\ and INT0\ (AMFX Interrupt)	-	10*tCKIN	-	ns
tSF	see section 3.2.1				

Table 9.6: Timing Symbols for MF Dispatcher

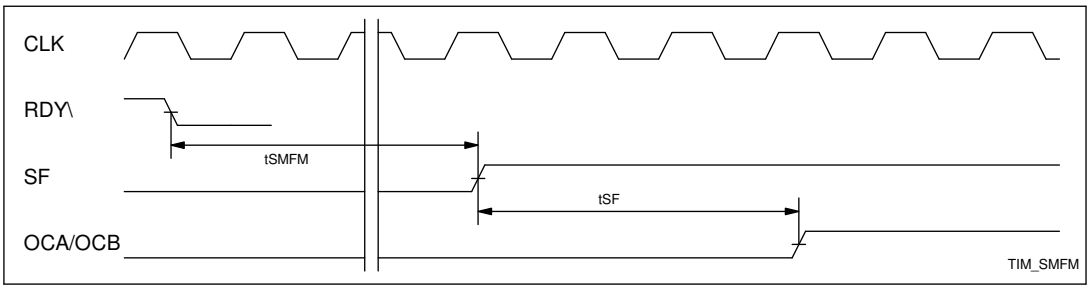


Figure 9.12: SMFM/SMFA MF-Dispatching: Latency between Request and SF

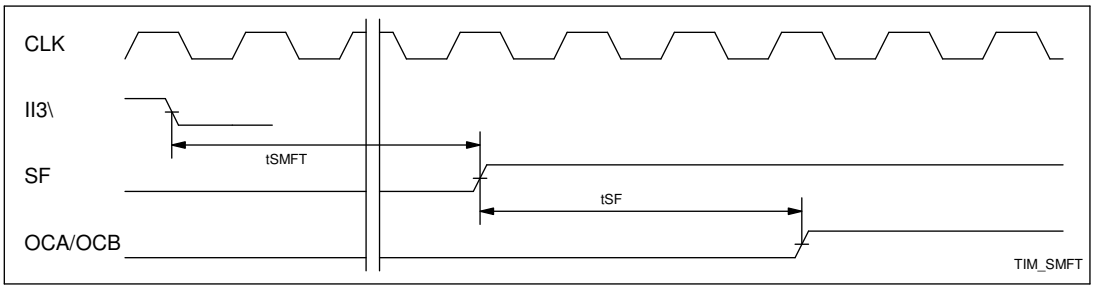


Figure 9.13: SMFT MF-Dispatching: Latency between Ext. Timer Signal and SF

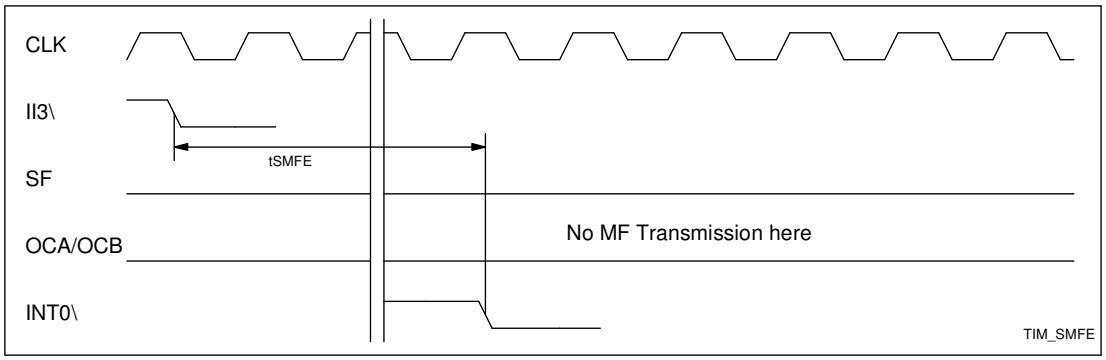


Figure 9.14: SMFE MF-Dispatching: Latency between Ext. Timer Signal and AMFX Interrupt

Notes to the timing diagrams shown above:

- The MVBC starts transmitting the delimiter while the access to Master Frame Slot or MF Table is made. Therefore, the SF signal will not be delayed if the MVBC must wait until clearance is given by the Arbitration Controller.
- RDY\ signal refers to finished write access to the Master Register (MR) which initiates MF dispatching.
- Assumption for II3\-signal: The Interrupt Logic does not process II3\ as a regular external interrupt. The corresponding mask bit masks "External Interrupt 3" out.

10 OPERATION IN SYSTEM

10.1 Reliability

10.1.1 Failure Rate

Estimated FIT value for the MVBC02C is 125 FIT (failures in 10^9hrs, derived from Flextronics Semiconductor Gate Array qualification @ 25°C and recalculated @ 125°C T_j acc. to MIL HB 217).

10.2 Testing Facilities

The MVBC exhibits a high degree of testability and observability. The different test mechanisms are described in the following sections.

10.2.1 Ad-Hoc Test Facilities

The internal MVB loopback mechanism allows elaborate functional tests such as

- Transfers using all F-Codes
- Full scale event arbitration
- Device Status Polls
- Simulated telegram errors (i.e. CRC), timeouts and jammed lines

In addition, the high degree of obsersvability (read-access to all Internal Registers) permits tests such as

- Interrupt Logic with simulated interrupts
- Universal Timers
- Device Address Override Mechanism
- Register Test

10.2.2 JTAG: Boundary Scan

The MVBC supports following Boundary Scan commands according to IEEE 1149.1 JTAG:

Command	Description
IDCODE	Returns ID Code for MVBC02C: **107E C185** (Hexadecimal)
SAMPLE	Boundary Scan: Captures values of input, I/O pads
EXTEST	Boundary Scan: Sets values on output, I/O pads
BYPASS	Bypass Mode

Table 10.1: Supported JTAG Functions

Besides the four mandatory JTAG signals (TCK, TMS\, TDI, TDO), the MVBC provides a Test-Reset-Signal (TRST\). At power-up, this signal must be active while RESET\ is active. After that, TRST\ will reset the JTAG logic only.

For implementing a JTAG test please request a BSDL – file for MVBC02C, Ident.-No. 3EGM 080 920 E0010.

10.2.3 Internal Scan

Scan test is only foreseen for production test.

10.2.4 High-Impedance Mode

All I/O and output pads enter High-Impedance Mode immediately when the input signal Z_MODE\ is active. As long the MVBC is not operating in initialization level 2 or 3, and the input signals remain unchanged, the internal state will be preserved. In the application environment, Z_MODE\ must be connected to '1'.

10.2.5 RAM Tests on Traffic Memory

As long the MVBC operates with Initialization Level 1, any regular RAM-test algorithm can be applied to test the Traffic Memory. If the MVBC operates with the level 2 or 3, then testing capabilities are restricted in order to maintain data consistency.

If an on-line RAM test is compulsory, then Arbitration Mode 2 (ARB=2, see SCR) can be applied. This mode holds back any accesses made by the MVBC in order to assure data consistency. However, this mode must not be active for a too long time in order to avoid overruns. Therefore, the on-line RAM test should be divided into a series of small indivisible access sequences. Each locked interval should not exceed 2-4 µs, and the time fraction the TM is locked should not exceed 1/5. Two examples are shown below:

Example 1: RAM Test without checking for coupling faults:

Set Arbitration Mode to 2	$ARB_{1..0}$ <= "10"
Read primary cell	X1 <= TM[A1]
Write pattern to primary cell	TM[A1] <= P1
Read + Check primary cell	P1 =?= TM[A1]
Restore primary cell	TM[A1] <= X1
Restore old arbitration Mode	$ARB_{1..0}$ <= *Old Value*

Pause! Do not continue immediately!

Example 2: RAM Test with checking for coupling faults:

Set Arbitration Mode to 2	$ARB_{1..0}$ <= "10"
Read primary cell	X1 <= TM[A1]
Read secondary cell	X2 <= TM[A2]
Write pattern to primary cell	TM[A1] <= P1
Read + Check primary cell	P1 =?= TM[A1]
Read + Check secondary cell	X2 =?= TM[A2]
Restore primary cell	TM[A1] <= X1
Restore old arbitration Mode	$ARB_{1..0}$ <= *Old Value*

Pause! Do not continue immediately!

11 MISCELLANEOUS

11.1 Normal Handling, Packing and Unpacking

Device handling shall be performed according to IPC/JEDEC standard J-STD-033A.

The MVBC is shipped in trays in a vapor-barrier bag which contains desiccants and a humidity indicator card. The bag is vacuum-sealed.

11.2 Reflow Soldering Conditions:

Soldering shall be performed according to IPC/JEDEC standard J-STD-020B.

11.3 Ordering Information

Product identification: 3BHC140027R0003

11.4 Contacts

If you need more information or any problem occurs concerning this document or the product described by this document, please contact Bombardier Transportation Propulsion and Control (info@mitrac.bombardier.com).
Our Internet home page www.transportation.bombardier.com provides you up to date information on contacts and products.

12 APPENDIX A: FUNCTION CODE SUMMARY

F-Code	MF Parameters	Description
0	Logical Address	Process Data, 1 Word
1	Logical Address	Process Data, 2 Words
2	Logical Address	Process Data, 4 Words
3	Logical Address	Process Data, 8 Words
4	Logical Address	Process Data, 16 Words
5	n/a	(reserved) [1]
6	n/a	(reserved) [1]
7	n/a	(reserved) [1]
8	Device Address	Mastership Offer Poll
9	Parameters [2]	Start/Continue Event Polling Round
10	n/a	(reserved) [1]
11	n/a	(reserved) [1]
12	Device Address [3]	Message Transfer
13	Device Group Address	Group Event Polling
14	Device Address	Individual Event Polling
15	Device Address	Device Status Poll

1 The MVBC does not reply to these F-Codes.

2 Event Mode (EM) and Event Type (ET), see 3.5.

3 First word in Slave Frame is checked for Communication Mode (CM) and Destination Device Address

Table 12.1: Function Codes

(Space below has been left blank intentionally)

13 APPENDIX B: PORT PROCESSING OVERVIEW

F-Code	UTQ	UTS	DA-FIT	Event Round	Other	Port A	Port B
0-4	0	0	-	-	-	LA Port	-
0-4	0	1	-	-	-	LA Port	TSNK [1]
0-4	1	0	-	-	-	TSRC [1]	LA Port
0-4	1	1	-	-	-	TSRC	TSNK
5-7	-	-	-	-	-	-	-
8	0	0	0	-	-	MOS	-
8	0	0	1	-	-	FC8	MOS
8	0	1	0	-	-	TSNK	-
8	0	1	1	-	-	FC8	TSNK
8	1	0	0	-	-	MOS	-
8	1	0	1	-	-	TSRC	MOS
8	1	1	0	-	-	TSNK	-
8	1	1	1	-	-	TSRC	TSNK
9	0	0	-	not partic.	-	EFS	-
9	0	0	-	participating	ET=0	EF0	EFS
9	0	0	-	participating	ET=1	EF1	EFS
9	0	1	-	not partic.	-	TSNK	-
9	0	1	-	participating	ET=0	EF0	TSNK
9	0	1	-	participating	ET=1	EF1	TSNK
9	1	0	-	-	-	TSRC	EFS
9	1	1	-	-	-	TSRC	TSNK
10-11	-	-	-	-	-	-	-
12	0	0	0	-	see [2]	MSNK	-
12	0	0	1	-	"	MSRC	MSNK
12	0	1	0	-	"	TSNK	-
12	0	1	1	-	"	MSRC	TSNK
12	1	0	-	-	"	TSRC	MSNK
12	1	1	-	-	"	TSRC	TSNK
13,14	0	0	0	-	-	EFS	-
13,14	0	0	-	0	-	EFS	-
13,14	0	0	1	1	ET=0	EF0	EFS
13,14	0	0	1	1	ET=1	EF1	EFS
13,14	0	1	0	-	-	TSNK	-
13,14	0	1	-	0	-	TSNK	-
13,14	0	1	1	1	ET=0	EF0	TSNK
13,14	0	1	1	1	ET=1	EF1	TSNK
13,14	1	0	-	-	-	TSRC	EFS
13,14	1	1	-	-	-	TSRC	TSNK
15	0	0	0	-	MCM=0	-	-
15	0	0	1	-	MCM=0	FC15	-
15	0	1	0	-	MCM=0	TSNK	-
15	0	1	1	-	MCM=0	FC15	TSNK
15	1	-	-	-	MCM=0	TSRC	TSNK
15	0	0	0	-	MCM>0	DA Port	-
15	0	0	1	-	MCM>0	FC15	DA Port
15	0	1	0	-	MCM>0	TSNK	-
15	0	1	1	-	MCM>0	TSRC	DA Port
15	1	0	-	-	MCM>0	TSRC	DA Port
15	1	1	-	-	MCM>0	TSRC	TSNK

1 Test and Message Ports are equivalent

2 Sink port is processed only if a valid Communication Mode (CM) is specified and at least one of the following conditions are met: 1) DA of MVBC matches with destination DA inside the message; 2) CM equals 15 (Broadcasting); 3) Message Broadcalling (MBC-Bit in SCR) is enabled.

Table 13.1: Port Processing Overview

14 APPENDIX C: REQUIRED PCS SETTINGS FOR ALL PORTS

Port ID or Type		F-Code	SRC/SINK	TWCS	$IE_{2..0}$	$CPE_{1,0}$	QA	NUM	FE	VP	WA
Non-Event-Driven Data Transfers:											
	LA Ports	0..4	Both	Valid	Valid [7]	00	0	Valid [2]	Valid	Valid	Valid
	DA Ports	15	Sink	Valid	Valid [7]	00	0	1	0	Valid	Valid
Event-Driven Data Transfers:											
	LA Ports	0..4	Both	Valid	Valid [7]	01/10	0	Valid [2]	Valid	Valid	Valid
	DA Ports	15	Sink	Valid	Valid [7]	01/10	0	1	0	Valid	Valid
MSRC	Queued Message	12	Source	Valid [1]	Valid [7]	See [3]	1	0	0	Valid [1]	Valid
MSRC	Nonqueued Message	12	Source	Valid	Valid [7]	See [3]	0	0	0	Valid	Valid
MSNK	Queued Message	12	Sink	Valid [1]	Valid [7]	0	1	0	0	Valid [1]	Valid
MSNK	Nonqueued Message	12	Sink	Valid	Valid [7]	0	0	0	0	Valid	Valid
FC15	Device Status Source	15	Source	0 [6]	Valid [7]	0 [6]	0	1	0	Valid	0 [6]
	Device Status Sink	See DA Ports									
FC8	Mastership O. Source	8	Source	0 [6]	Valid [7]	0	0	1	0	Valid	0 [6]
MOS	Mastership O. Sink	8	Sink	0 [6]	Valid [7]	0	0	1	0	Valid	0 [6]
EF0, EF1	Event Source	9 [4]	Source	0 [6]	0 [6]	0 [6]	0	1	0	Valid	0 [6]
EFS	Event Sink	9 [4]	Sink	0 [6]	Valid [7]	0 [6]	0	1	0	Valid	0 [6]
TSRC	Test Source	Valid [5]	Source	Valid	Valid [7]	See [3]	Valid	Valid	Valid [8]	Valid	Valid
TSNK	Test Sink	Valid [5]	Sink	Valid	Valid [7]	See [3]	Valid	Valid	Valid [8]	Valid	Valid

1 TWCS and VP: VP shall be valid if TWCS=1. CS will be transferred from/to the selected halfword of word 3 of PCS. If TWCS=0, then VP will not be checked.

2 Numeric Process Data: Use '1', Non-numeric Process Data: Use '0'.

3 Depends if data transfer follows Event Arbitration or not.

4 For EF0, EF1 and EFS, the MVBC does not check for matching F-Codes. However, configuring this port with F-Code 9 is strongly recommended.

5 Test Ports are enabled only if corresponding UTQ/UTS bits are enabled in the SCR.

6 Recommended, but not required

7 $IE_{2..0}$='111' invokes automatic comparison mechanism. Not suitable for supervisory frames.

8 Applies to Process Data only (F-Codes 0-4). Must be zero for all other F-Codes.

Table 14.1: Required PCS Settings

15 APPENDIX D: SUMMARY OF INTERNAL REGISTERS

Addresses: "y" stands for "3" if MCM=0; "7" if MCM=1; or "F" if MCM = 2, 3 or 4.

Status Control Register (SCR, see section 3.5.1, page 61): Address 0yF80H, init. value = 0x0700

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	IM	QUIET	MBC	LD	$TMO_{1..0}$		$WS_{1..0}$		$ARB_{1..0}$		UTS	UTQ	MAS	RCEV	$IL_{1..0}$	

Memory Configuration Register (MCR, see section 3.6.1, page 70): Address 0yF84H, init. value = 0x2080

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	$VERSION_{4..0}$					DMAD	$PO_{1..0}$		ICD	$MO_{1..0}$		$QO_{1..0}$		$MCM_{2..0}$		

Decoder Register (DR, see section 3.3.7, page 53): Address 0yF88H, init. value = 0x0008

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	LTE	NDH	ATO	RLDS	BLVL	BCHG	ALVL	ACHG	Turbo	Opto	Trafo	WTR	LAA	RLD	LS	SLM

Sink-Time Supervision Register (STSR, see section 3.9.1, page 86): Address 0yF8CH, init. value = 0x0000

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	$SI_{3..0}$				$R_{11..0}$											

Frame Counter (FC, see section 3.4.5, page 57): Address 0yF90H, init. value = 0x0000

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	$FC_{15..0}$															

Error Counter (EC, see section 3.4.5, page 57): Address 0yF94H, init. value = 0x0000

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	$EC_{15..0}$															

Master Frame Registers (MFR, see section 56, page 56): Address 0yF98H, init. value = 0x0000
Master Frame Register Duplicate Exception (MFRE): Address 0yF9CH, init. value = 0x0000

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	$F\text{-}Code_{3..0}$				$Addr_{11..0}$											

Master Register (MR, see section 3.5.2, page 64): Address 0yFA0H, init. value = 0x0000

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	$PAR_{1..0}$		$EA_{1..0}$		$EC_{1..0}$		BUSY	CSMF	$SMF_{1..0}$		SMSM	$C_{4..0}$				

Secondary Master Register (MR2, see section 3.5.2, page 64): Address 0yFA4H, init. value = 0x0000

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	-								$SMF_{1..0}$		SMSM	$C_{4..0}$				

Dispatch Pointer Register (DPR, see section 3.5.3, page 67): Address 0yFA8H, init. value = 0x0000
Secondary Dispatch Pointer Register (DPR2): Address 0yFACH, init. value = 0x0000

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	$DPR_{15..2}$														-	

Interrupt Pending Register (IPR0, see section 3.7.3, page 80): Address 0yFB0H, init. value = 0x0000
Interrupt Mask Register (IMR0, see section 3.7.4, page 80): Address 0yFB8H, init. value = 0x0000
Interrupt Status Register (ISR0, see section 3.7.5, page 81): Address 0yFC0H, init. value = 0x0000

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	EMF	ESF	DMF	DSF	AMFX	MFC	SFC	RTI	BTI	DTI7	DTI7	DTI5	DTI4	DTI3	DTI2	DTI1

Interrupt Pending Register 1 (IPR1): Address 0yFB4H, init. value = 0x0000
Interrupt Mask Register 1 (IMR1): Address 0yFBCH, init. value = 0x0000
Interrupt Status Register 1 (ISR1): Address 0yFC4H, init. value = 0x0000

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	TI2	XI3	XI2	XQE	RQE	XQ1C	XQ0C	RQC	FEV	Not used				TI1	XI1	XI0

Interrupt Vector Register (IVR0, see section 3.7.6, page 82): Address 0yFC8H, init. value = 0x0000
Interrupt Vector Register 1 (IVR1): Address 0yFCCH, init. value = 0x0000

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	Not used							IAV	Not used				$VEC_{3..0}$			

Line Error Counter A (ECA, see section 3.4.8, page 60): Address 0yFD0H, init. value = 0x0000
Line Error Counter B (ECB, see section 3.4.8, page 60): Address 0yFD4H, init. value = 0x0000

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	$ECA_{15..0}$, $ECB_{15..0}$															

Device Address Override Register (DAOR, see section 3.5.5.1, page 69): Address 0yFD8H, init. value = $DA_{11..0}$ pins

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	-				$DA_{11..0}$											

Device Address Override Key (DAOK, see section 3.5.5.1, page 69): Address 0yFDCH, init. value = 0x0000

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	-								$K_{7..0}$							

Special Function Register (SFR, see section 3.2.5, page 48): Address 0yFE4H, init. value = 0x0000

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol																TRP

Timer Control Register (TCR, see section 3.8.1, page 83): Address 0yFE0H, init. value = 0x0022

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	Not used						$IFS_{1..0}$		Not used		RS2	TA2	n. used	XSYN	RS1	TA1

Timer Reload Register 1 (TR1, see section 3.8.1, page 83): Address 0yFF0H, init. value = 0x0000
Timer Reload Register 2 (TR2): Address 0yFF4H, init. value = 0x0000

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	TR1, TR2															

Timer Counter Register 1 (TC1, see section 3.8.1, page 83): Address 0yFF8H, init. value = 0x0000
Timer Counter Register 2 (TC2): Address 0yFFCH, init. value = 0x0000

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	TR1, TR2															

16 APPENDIX E: RESET BEHAVIOR

Asynchronous Reset

The asynchronous reset is activated with RESET\. All flags, registers and internal control states are initialized. The internal Transmit and Receive Buffers will not be reset, but this does not affect the operation.

The RESET – signal is latched internally, internal clearing of reset is synchronized with positive edge of clock CLK.

Test Reset

The reset is activated with TRST\. The JTAG boundary scan system (TAP controller, etc) is initialized. Normally, TRST\ is activated along with RESET\ to start up the MVBC.

Synchronous Reset

The synchronous reset is activated by selecting Initialization Level (IL) to 0, deactivated by setting IL to a different value. This reset shall be active for at least 5 clock cycles.

- Decoder Register (DR) is reset (Line A selected). Incoming data is not affected except when the reset caused a line switch (Line B -> Line A).
- Telegram Analysis Unit: All Timeout counters, Frame Counter (FC), Error Counter (EC), FEV-interrupt reset
- Device Address: Override state. The Device Address from the DA input pins becomes effective.
- Memory Configuration Register (MCR)
- MCU enters idle state within 5 clock cycles. This applies for both synchronous reset and configuration mode (IL = 0 and 1).
- Status Control Register (SCR), except Initialization Level bits
- Master Register (MR, MR2)
- Universal Timers disabled, Timer Counter Registers (TC1/2) set to 0, Timer Control Register (TCR) reset. TR1 and TR2 will not be reset since counters are already inactive.
- All registers in the Interrupt Logics (IPR0/1, IMR0/1, ISR0/1, IVR0/1) are set to zero. The frozen states are released.

<u>Following parts remain unaffected by the synchronous reset:</u>

- MFR and MFRE are not reset.
- STSR Sink-Time Supervision Register stays unchanged. Sink-Time supervision activity is already ceased since IL is forced to 0. Sink-Time Supervision is running only if IL = 2 or 3.

<u>Encoder: Transmission of frames already underway will be completed properly</u>

- Dispatch Pointer Registers (DPR, DPR2)
- Traffic Memory access mechanisms such as Arbitration Controller and TM Controller in order to maintain access to TM and registers
- Device Address Override Register (DAOR) and Key (DAOK)

17 APPENDIX F: BIBLIOGRAPHY

[1] International Electrotechnical Commission
Train Communication Network TCN IEC 61375-1, Part 3: Multifunction Vehicle Bus, 1999

[2] Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices, IPC/JEDEC J-STD-020B, July 2002

[3] Handling, Packing and Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices, IPC/JEDEC J-STD-033A, July 2002

18 APPENDIX G: KNOWN ERRATA AND BUGFIXES

18.1 MVB Physical Layer Signals

18.1.1 Decoder hang in redundant “opto” - mode

Severity: Severe in MVBC – “opto” – mode (decoder register bit TRAFO = ‘0’, ref. chptr. 3.3.7).
Summary: In decoder “opto” – mode the MVBC considers a hanging serial line input (ICA, ICB) to permanent ‘1’ as active, waiting for a delimiter. This stuck-at-one could be caused by a short circuit to the line or failing negative line precharge.
Workaround: Set bit ATO in the decoder register (ref. chptr. 3.3.7).

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