AN3025

Transimpedance Amplifier Design

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Introduction

The PS8501 is a unique high speed optocoupler that has a maximum isolation voltage of 5000 Vrms and provides an 8 mm creepage distance. This particular model of optocoupler not only has a photodiode connected to an amplifying transistor for an output (speeds up to 1 Mbps), it also provides direct access to the photodiode itself. This feature allows users to not only use the 1 Mbps transistor output but also offers an alternative output for higher speed applications over 1 Mbps with the implementation of a TIA. Transimpedance amplifiers (TIA's) are used to amplify low-level output current of a photodiode to a voltage level used for high speed data transmission or sensing applications. This application note examines a single-power supply TIA which is driven by CEL's PS8501 optocoupler.

Overview of Photoconductive Transimpedance Amplifiers

The TIA discussed in this application note is being operated in photoconductive mode. This means that a photodiode being driven by an IRLED has a positive voltage applied to the cathode for the purpose of reverse biasing the photodiode. This improves the circuit's performance at high frequency by increasing the space charge region and also by lowering the junction capacitance. The current generated from the photodiode is then routed into an inverting operational amplifier (op-amp) which has a feedback resistor (Rf) that determines the gain. The feedback capacitor (Cf) is added to help reduce gain peaking in order to achieve a flatter response. The output voltage here is Vout=-IP*Rf. An example of a photoconductive TIA can be seen below in Figure 1:

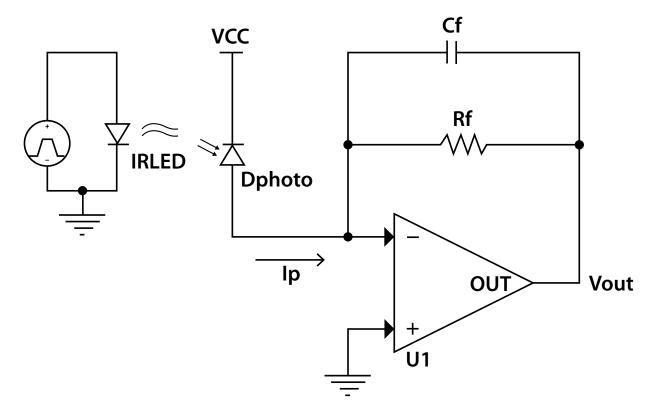


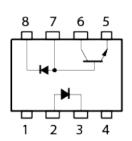
Figure 1: A Photoconductive Transimpedance Amplifier

Overview of Components

The TIA designed here consists of 1 optocoupler, 2 op-amps, 1 comparator, 8 resistors, and 3 capacitors:

As noted earlier, the optocoupler is CEL's PS8501 which is an 8-pin DIP analog output type optocoupler. It contains a GaAlAs LED on the input side, and a PN photodiode and a high speed amplifier transistor on the output side. This optocoupler also allows direct access to the PN photodiode (Pin 7) which is the optocoupler output used in this TIA. The equivalent circuit of the PS8501 can be seen below in Figure 2:

PIN CONNECTION (Top) View



- 1. NC
- 2. Anode
- 3. Cathode
- 4. NC
- 5. Emitter
- 6. Vo
- 7. Base
- 8. Vcc

Figure 2: PS8501 schematic

The op-amps are Texas Instruments OPA380AID which are precision 8-pin SOIC amplifiers. They have a GBW (Gain Bandwidth) of 90 MHz, a supply voltage range from 2.7 V to 5.5 V, very low bias current (50 pA max), very low offset voltage (25 μV max), and are well suited for high speed photodiode applications. The equivalent circuit can be seen below in Figure 3:

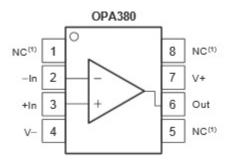


Figure 3: OPA380AID schematic

The comparator is a Texas Instruments TLV3501 which is a push-pull CMOS output stage comparator that features a fast 4.5 ns propagation delay and operation from +2.7 V to +5.5 V. This comparator was chosen because of its high speed performance (maximum toggle frequency is 80 MHz) and its beyond-the-rails input common-mode range which makes it fitting for low-voltage applications. The equivalent circuit can be seen below in Figure 4:

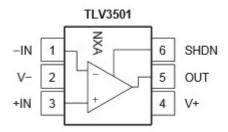


Figure 4: TLV3501 schematic

The resistors used are 1/4-watt, 5% tolerance carbon-film resistors. The capacitors used are Hi-Q ceramic disc capacitors.

Design of Transimpedance Amplifier

4.1. Design Goals

The main goal of this circuit design is to showcase the PS8501's capability to drive a TIA at speeds >1 Mbps by using the direct photodiode output of the PS8501. Another goal for this design is to have an isolated output signal that is both non-inverted and equal to Vcc. The TIA is also designed to operate with a single-power supply. In order to satisfy these goals the design requires a three stage output.

4.2. Design Schematic

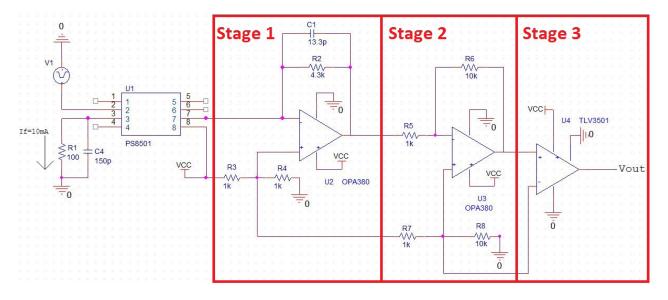


Figure 5: TIA implementation with PS8501 schematic

As shown in Figure 5, square waves (50% Duty Cycle) are being generated at the input of the PS8501 (Pins 2 & 3) maintaining a forward current (IF) equal to 10 mA when active. Then the output signals from the PS8501's output (Pin 7) are fed to 3 output stages. The purposes of these stages are as follows:

Stage 1 has an op-amp that amplifies the signal coming directly from the PS8501 (Pin 7). This is the transimpedance stage. Since the op-amp at this stage is configured as an inverting amplifier, the output voltage at this stage is VOUT1 = -IPin7*R2. Due to the fact the op-amp has a positive single-supply voltage and cannot output a negative voltage, apply a positive voltage bias to the non-inverting input (Vcc/2 is used here) so the amplified signal will be positively offset and passed to the op-amp output in its entirety.

Stage 2 has an op-amp configured as a difference amplifier that inverts the output of the previous stage and also removes the bias that was set in the previous stage in order to emulate to original PS8501 input waveform. This stage also further amplifies the signal by a factor of x10.

Stage 3 has a comparator which compares its input voltage (Stage 2 output) to a reference voltage (Vcc/2) to indicate if the input signal is either High or Low. Once the Stage 3 input voltage exceeds the reference voltage the comparator pulls up its output High otherwise the output stays Low.

4.4. On-board Prototyping

It should be noted that testing done for this application note was done on a solderless breadboard along with a HP 8116A Pulse/Function Generator, and a HP E3611A DC Power Supply. All of the components, except for the op-amps (OPA380AID) and the comparator (LTV3501), are through-hole components. The op-amps and comparator used here are surface mount components so SOIC-to-DIP adapters had to be used for each one in order to carry out testing on a breadboard.

The key elements for this design are the feedback resistors and capacitors. Resistors are important because they determine the gain of the amplifier. Capacitors are important because they factor into reducing noise and noise gain, especially in Stage 1 where noise would have the most drastic effect on the output of the TIA. Depending on numerous factors such as chosen components, prototyping equipment, desired applications, desired gain, and desired operation speed, achieving a maximally flat frequency response will require varying combinations of feedback resistor/capacitor values.

The initial feedback resistor (R2) at Stage 1 determines the transimpedance gain of the circuit. Here R2 = 4.3 K Ω is selected as a reasonable tradeoff between gain and bandwidth. Stage 1 is very important because it has to produce an acceptable output signal that can be amplified at later stages

without compromising the bandwidth aspect due to the constraint of a constant gain bandwidth product of the opamp, which is 90 MHz here.

The TIA should be assembled stage by stage; making sure each stage's component configuration delivers a desirable output before moving on to the subsequent stage. An additional 0.1 μ F capacitor should be used to bypass the Vcc and GND pins to filter out high frequency supply noise and prevent unwanted communication between the devices sharing the same power source. A picture of the assembled test circuit can be seen below in Figure 6:

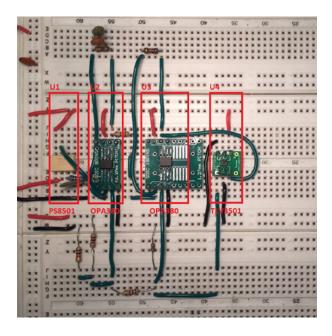


Figure 6: The TIA test circuit

Tests/Results

Once the TIA design and component values were solidified, the TIA circuit was tested. The tests consisted of inputting square waves (100 KHz to 4 MHz, 50% Duty Cycle) to the PS8501 with IF = 10 mA and Vcc = 4 V (Pin 8 of PS8501) then monitoring the rise/fall times of the Stage 3 output signal on the oscilloscope. The purpose of the tests was to find the maximum speed the circuit could operate while maintaining an acceptable output, meaning an output whose combined rise and fall time is less than 1/3 of input signal duration. Ideally once the combined rise and fall times exceed 1/3 of input signal duration, the signal is no longer acceptable. Each of the three output stages where monitored to show the behavior of the signal at each stage. Each of the outputs of the 3 stages will be shown along with the optocoupler's input signal (Pins 2 & 3 of the PS8501) which is monitored across R1.

5.1. TIA @ 100 KHz

At 100 KHz, the input/output voltage signals for the 3 stages can be seen below in Figures 7, 8, and 9:

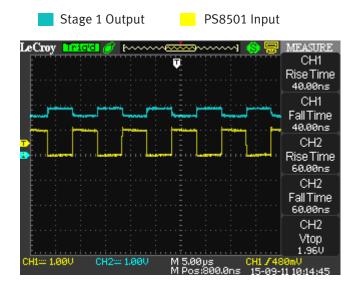


Figure 7: Stage 1 Output @ 100KHz

Looking at Figure 7, notice that the Stage 1 output (blue) is inverted when compared to the optocoupler input signal (yellow). Also note that the inverted signal is offset 2 V with the purpose of keeping the signal's integrity.

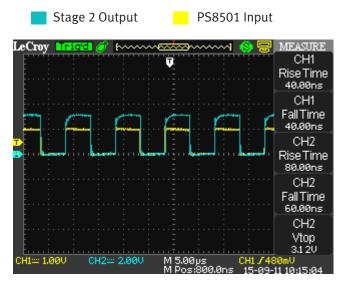


Figure 8: Stage 2 Output @ 100KHz

Due to Stage 2's inverting amplifier configuration, looking at Figure 8, we see the Stage 2 output (blue) returns the signal to a non-inverted state and amplifies the signal by a factor of x10. Also the voltage bias at this stage removes the bias set from the previous stage pulling the signal towards ground level and further replicating the optocoupler's input waveform (yellow).

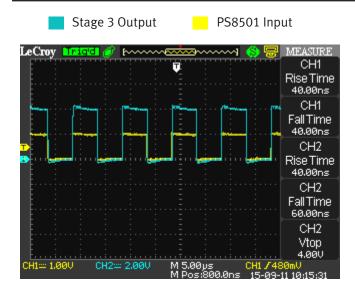


Figure 9: Stage 3 Output @ 100KHz

Looking at Figure 9, we see the Stage 3 output (blue) not only removes the rising slope from the Stage 2 squaring up the output signal, it also amplifies the output signal to 4 V (Vcc). Notice the rise times for both input/output signals are 40 ns and the fall times differ by 20 ns. For the optocoupler's square wave input (yellow) at frequency of 100 KHz, the time period is T = 1/100 KHz = 10 μ s. The duty cycle is 50% so the pulse width is 10μ s/2 = 5μ s and 1/3 of that is 1.67μ s which is much greater than the combined rise/fall time of output signal which is 100 ns, so the output is acceptable.

5.2. TIA @ 4 MHz

At 4 MHz, the output for the 3 stages can be seen below in Figures 10, 11, and 12:

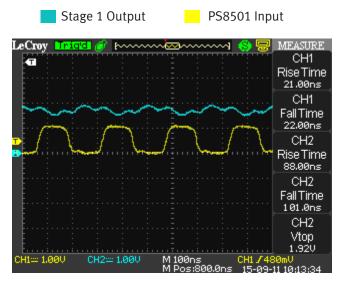


Figure 10: Stage 1 Output @ 4 MHz

Looking at Figure 10, again we see that the inverted Stage 1 output (blue) but this time with noticeable noise when compared to the optocoupler's square wave input (yellow). This is a sign that the maximum operating frequency is being approached and the signal-to-noise ratio is decreasing.

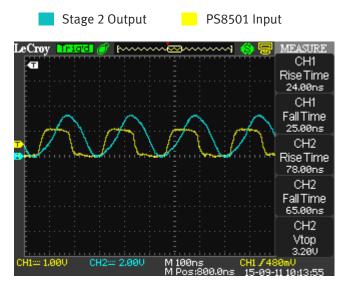


Figure 11: Stage 2 Output @ 4 MHz

Looking at Figure 11, we see the non-inverted Stage 2 output (blue) which is starting to show signs of signal degradation at this frequency looking more like a sine wave. The large difference in rise/fall times between the input (yellow) and output waveforms is a further indication that the maximum operating frequency is being approached.

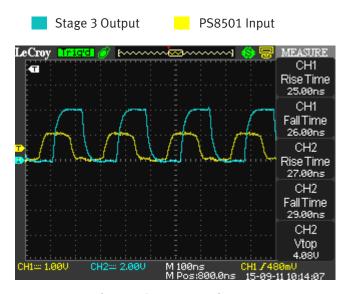


Figure 12: Stage 3 Output @ 4 MHz

Looking at Figure 12, we see the final Stage 3 comparator output (blue) which improves upon the previous stage's

rise/fall times and pulls up the output voltage to 4 V (Vcc). Notice this Stage 3 output's rise time is 27 ns and the fall time is 29 ns for a combined time of 56 ns. At a frequency of 4 MHz, the time period is T = 1/4 MHz = 0.25 μ s. The duty cycle is 50% so the square wave is active for 0.25 μ s/2 = 0.125 μ s and 1/3 of that is 41.67 ns which is slightly less than the combined rise/fall time of output signal. However, notice the original input signal (yellow) has rounded edges and a combined rise/fall time of 25 ns + 26 ns = 51 ns which is marginal. This is most likely due to factors such as breadboard prototyping and the function generator's inadequate performance at higher frequencies.

Design Considerations/Tips to Improve Performance of TIA

Keep in mind this TIA was prototyped on a solderless breadboard which automatically hinders the TIA from operating at optimum performance because breadboards tend to have high parasitic capacitance and inductance. Through-hole components were used here in order to make adjusting component values and troubleshooting easier. However, using surface mount components would be more efficient and less noisy since there would be no need for numerous jumper wires and DIP adapters.

If an even higher transimpedance bandwidth is desired, lower the gain set by the feedback resistor in Stage 1, this will allow operations at higher speeds. Or look into using op-amps with a higher gain bandwidth product.

If other operational amplifiers or components are used instead of those discussed in this application note, it is important to make sure the op-amps have high precision and low-noise characteristics to allow the low-level current from the photodiode to be accurately measured. Also, all of the components used should have low input impedance and low input capacitances to help prevent signal degradation/noise.

Conclusion

A transimpedance amplifier is an effective tool for optical communication and can be easily implemented with the PS8501. The PS8501 is a versatile optocoupler that can be used for operations which desire both high gain (transistor

output) and high speed (photodiode output) while maintaining the same electrical characteristics for both. The PS8501 is rated at 1 Mbps but as shown in this application note its photodiode output can be used for operations up to 4 MHz (8 Mbps) while maintaining the same isolation voltage of 5000 Vrms and 8 mm creepage distance. TIA operations at higher speeds may be possible if steps are taken to improve performance as discussed in the Design Considerations part of this application note.

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