ECE 310-001

Project #1 Report

Charles Zhu

1. Snapshot of the RTL synthesized in Quartus.

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*Part 1: Fill in the synthesis results*

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| **Synthesis Results** |
| Number of logic elements  7,302 / 15,408 ( 47 % ) |
| Number of registers:  68 |
| Number of tri-state buffers:  27 / 79 ( 34 % ) |
| Number of memory bits:  0 / 516,096 ( 0 % ) |
| Please attach to the end of this report all text from the *Analysis and Synthesis Messages* section of your **.map.rpt** file. If you have warnings and/or errors, please provide your best one- or two- sentence explanation for why each warning or error is occurring. |

Info: \*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Info: Running Quartus Prime Analysis & Synthesis

Info: Version 20.1.0 Build 711 06/05/2020 SJ Lite Edition

Info: Processing started: Mon Oct 26 17:25:12 2020

Info: Command: quartus\_map --read\_settings\_files=on --write\_settings\_files=off proj1 -c proj1

Warning (18236): Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM\_PARALLEL\_PROCESSORS in your QSF to an appropriate value for best performance.

Info (20030): Parallel compilation is enabled and will use 2 of the 2 processors detected

Info (12021): Found 10 design units, including 10 entities, in source file proj1.v

Info (12023): Found entity 1: ram

Info (12023): Found entity 2: half\_adder

Info (12023): Found entity 3: full\_adder

Info (12023): Found entity 4: my16bitadder

Info (12023): Found entity 5: my8bitmultiplier

Info (12023): Found entity 6: alu

Info (12023): Found entity 7: ctr

Info (12023): Found entity 8: registers

Info (12023): Found entity 9: datapath

Info (12023): Found entity 10: proj1

Warning (10236): Verilog HDL Implicit Net warning at proj1.v(690): created implicit net for "Zflag\_reg"

Fixed by assigning zflag\_reg to be not an implicit net

Info (12127): Elaborating entity "proj1" for the top level hierarchy

Info (12128): Elaborating entity "ram" for hierarchy "ram:tomato"

Warning (10240): Verilog HDL Always Construct warning at proj1.v(20): inferring latch(es) for variable "q", which holds its previous value in one or more paths through the always construct

Fixed by assigning adding else statement to fix the latch.

Info (10041): Inferred latch for "q[0]" at proj1.v(20)

Info (10041): Inferred latch for "q[1]" at proj1.v(20)

Info (10041): Inferred latch for "q[2]" at proj1.v(20)

Info (10041): Inferred latch for "q[3]" at proj1.v(20)

Info (10041): Inferred latch for "q[4]" at proj1.v(20)

Info (10041): Inferred latch for "q[5]" at proj1.v(20)

Info (10041): Inferred latch for "q[6]" at proj1.v(20)

Info (10041): Inferred latch for "q[7]" at proj1.v(20)

Info (10041): Inferred latch for "q[8]" at proj1.v(20)

Info (10041): Inferred latch for "q[9]" at proj1.v(20)

Info (10041): Inferred latch for "q[10]" at proj1.v(20)

Info (10041): Inferred latch for "q[11]" at proj1.v(20)

Info (10041): Inferred latch for "q[12]" at proj1.v(20)

Info (10041): Inferred latch for "q[13]" at proj1.v(20)

Info (10041): Inferred latch for "q[14]" at proj1.v(20)

Info (10041): Inferred latch for "q[15]" at proj1.v(20)

Info (12128): Elaborating entity "ctr" for hierarchy "ctr:potato"

Warning (10230): Verilog HDL assignment warning at proj1.v(280): truncated value with size 8 to match size of target (4)

Tried to fix Using a comparison logic when value does not match

Warning (10230): Verilog HDL assignment warning at proj1.v(296): truncated value with size 8 to match size of target (4)

Tried to fix Using a comparison logic when value does not match

Warning (10230): Verilog HDL assignment warning at proj1.v(312): truncated value with size 8 to match size of target (4)

Tried to fix using a comparison logic when value does not match

Warning (10230): Verilog HDL assignment warning at proj1.v(330): truncated value with size 8 to match size of target (4)

Tried to fix Using a comparison logic when value does not match

Warning (10230): Verilog HDL assignment warning at proj1.v(331): truncated value with size 8 to match size of target (4)

Tried to fix Using a comparison logic when value does not match

Warning (10230): Verilog HDL assignment warning at proj1.v(332): truncated value with size 8 to match size of target (4)

Tried to fix Using a comparison logic when value does not match

Warning (10230): Verilog HDL assignment warning at proj1.v(333): truncated value with size 8 to match size of target (4)

Tried to fix Using a comparison logic when value does not match

Warning (10230): Verilog HDL assignment warning at proj1.v(334): truncated value with size 8 to match size of target (4)

Tried to fix Using a comparison logic when value does not match

Warning (10230): Verilog HDL assignment warning at proj1.v(335): truncated value with size 8 to match size of target (4)

Tried to fix Using a comparison logic when value does not match

Warning (10230): Verilog HDL assignment warning at proj1.v(336): truncated value with size 8 to match size of target (4)

Tried to fix Using a comparison logic when value does not match

Warning (10230): Verilog HDL assignment warning at proj1.v(337): truncated value with size 8 to match size of target (4)

Tried to fix Using a comparison logic when value does not match

Warning (10230): Verilog HDL assignment warning at proj1.v(353): truncated value with size 8 to match size of target (4)

Tried to fix Using a comparison logic when value does not match

Warning (10230): Verilog HDL assignment warning at proj1.v(369): truncated value with size 8 to match size of target (4)

Tried to fix Using a comparison logic when value does not match

Warning (10230): Verilog HDL assignment warning at proj1.v(387): truncated value with size 8 to match size of target (4)

Tried to fix Using a comparison logic when value does not match

Warning (10230): Verilog HDL assignment warning at proj1.v(404): truncated value with size 8 to match size of target (4)

Tried to fix Using a comparison logic when value does not match

Warning (10230): Verilog HDL assignment warning at proj1.v(423): truncated value with size 8 to match size of target (4)

Tried to fix Using a comparison logic when value does not match

Warning (10230): Verilog HDL assignment warning at proj1.v(438): truncated value with size 8 to match size of target (4)

Tried to fix Using a comparison logic when value does not match

Warning (10230): Verilog HDL assignment warning at proj1.v(454): truncated value with size 8 to match size of target (4)

Tried to fix Using a comparison logic when value does not match

Warning (10230): Verilog HDL assignment warning at proj1.v(471): truncated value with size 8 to match size of target (4)

Tried to fix Using a comparison logic when value does not match

Warning (10230): Verilog HDL assignment warning at proj1.v(488): truncated value with size 8 to match size of target (4)

Tried to fix Using a comparison logic when value does not match

Warning (10230): Verilog HDL assignment warning at proj1.v(504): truncated value with size 8 to match size of target (4)

Tried to fix Using a comparison logic when value does not match

Warning (10230): Verilog HDL assignment warning at proj1.v(522): truncated value with size 8 to match size of target (4)

Tried to fix Using a comparison logic when value does not match

Warning (10230): Verilog HDL assignment warning at proj1.v(538): truncated value with size 8 to match size of target (4)

Tried to fix Using a comparison logic when value does not match

Warning (10199): Verilog HDL Case Statement warning at proj1.v(541): case item expression never matches the case expression

This is a special case where for when it needs to branch out to the jump when value is zero

Warning (10240): Verilog HDL Always Construct warning at proj1.v(267): inferring latch(es) for variable "opALU", which holds its previous value in one or more paths through the always construct

This is a special case where for when it needs to branch out to the jump when value is zero

Info (10041): Inferred latch for "opALU[0]" at proj1.v(267)

Info (10041): Inferred latch for "opALU[1]" at proj1.v(267)

Info (12128): Elaborating entity "datapath" for hierarchy "datapath:datapath\_name"

Info (12128): Elaborating entity "alu" for hierarchy "datapath:datapath\_name|alu:start1"

Warning (10235): Verilog HDL Always Construct warning at proj1.v(167): variable "A" is read inside the Always Construct but isn't in the Always Construct's Event Control

Fixed by putting always(\*)

Warning (10235): Verilog HDL Always Construct warning at proj1.v(167): variable "B" is read inside the Always Construct but isn't in the Always Construct's Event Control

Fixed by putting always(\*)

Warning (10235): Verilog HDL Always Construct warning at proj1.v(168): variable "SumOutput" is read inside the Always Construct but isn't in the Always Construct's Event Control

Fixed by putting always(\*)

Warning (10235): Verilog HDL Always Construct warning at proj1.v(169): variable "product0utput" is read inside the Always Construct but isn't in the Always Construct's Event Control

Fixed by putting always(\*)

Warning (10235): Verilog HDL Always Construct warning at proj1.v(170): variable "A" is read inside the Always Construct but isn't in the Always Construct's Event Control

Fixed by putting always(\*)

Info (12128): Elaborating entity "my16bitadder" for hierarchy "datapath:datapath\_name|alu:start1|my16bitadder:addie"

Info (12128): Elaborating entity "full\_adder" for hierarchy "datapath:datapath\_name|alu:start1|my16bitadder:addie|full\_adder:Add0"

Info (12128): Elaborating entity "half\_adder" for hierarchy "datapath:datapath\_name|alu:start1|my16bitadder:addie|full\_adder:Add0|half\_adder:a1"

Info (12128): Elaborating entity "my8bitmultiplier" for hierarchy "datapath:datapath\_name|alu:start1|my8bitmultiplier:multiplie"

Warning (10230): Verilog HDL assignment warning at proj1.v(112): truncated value with size 32 to match size of target (16)

Tried to fix the size of target to match output since multiplier had size 32

Info (12128): Elaborating entity "registers" for hierarchy "datapath:datapath\_name|registers:another\_one"

Info (278001): Inferred 1 megafunctions from design logic

Info (278003): Inferred multiplier megafunction ("lpm\_mult") from the following logic: "datapath:datapath\_name|alu:start1|Mult0"

Info (12130): Elaborated megafunction instantiation "datapath:datapath\_name|alu:start1|lpm\_mult:Mult0"

Info (12133): Instantiated megafunction "datapath:datapath\_name|alu:start1|lpm\_mult:Mult0" with the following parameter:

Info (12134): Parameter "LPM\_WIDTHA" = "8"

Info (12134): Parameter "LPM\_WIDTHB" = "8"

Info (12134): Parameter "LPM\_WIDTHP" = "16"

Info (12134): Parameter "LPM\_WIDTHR" = "16"

Info (12134): Parameter "LPM\_WIDTHS" = "1"

Info (12134): Parameter "LPM\_REPRESENTATION" = "UNSIGNED"

Info (12134): Parameter "INPUT\_A\_IS\_CONSTANT" = "NO"

Info (12134): Parameter "INPUT\_B\_IS\_CONSTANT" = "NO"

Info (12134): Parameter "MAXIMIZE\_SPEED" = "5"

Info (12021): Found 1 design units, including 1 entities, in source file db/mult\_3at.tdf

Info (12023): Found entity 1: mult\_3at

Warning (13012): Latch ctr:potato|opALU[1] has unsafe behavior

Tried to fix the ctr potato to have safe behavior

Warning (13013): Ports D and ENA on the latch are fed by the same signal ctr:potato|present\_state[3]

Fixed by changing to different signals instead of duplicate signals.

Warning (13012): Latch ctr:potato|opALU[0] has unsafe behavior

Tried to fix the ctr potato to have safe behavior

Warning (13013): Ports D and ENA on the latch are fed by the same signal ctr:potato|present\_state[0]

Info (286030): Timing-Driven Synthesis is running

Info (17049): 22 registers lost all their fanouts during netlist optimizations.

Info (144001): Generated suppressed messages file C:/Users/charlie/Desktop/ece310/Verilog/something/output\_files/proj1.map.smsg

Info (16010): Generating hard\_block partition "hard\_block:auto\_generated\_inst"

Info (16011): Adding 0 node(s), including 0 DDIO, 0 PLL, 0 transceiver and 0 LCELL

Info (21057): Implemented 7328 device resources after synthesis - the final resource count might be different

Info (21058): Implemented 2 input pins

Info (21059): Implemented 25 output pins

Info (21061): Implemented 7300 logic cells

Info (21062): Implemented 1 DSP elements

Info: Quartus Prime Analysis & Synthesis was successful. 0 errors, 38 warnings

Info: Peak virtual memory: 4787 megabytes

Info: Processing ended: Mon Oct 26 17:25:53 2020

Info: Elapsed time: 00:00:41

Info: Total CPU time (on all processors): 00:00:46

**Name: Charles Zhu Student ID:200217093**

I certify that I did not copy the answers to this homework and did not let

anyone copy my answers (sign):

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