Post Processing C66x Benchmarking

Byte operations

Test Setup

- Use Appleton EVM board for C66x benchmarking
- Use 2M of MSMC for input and output
  - Configured as cachable with prefetch on
- L1D and L1P configured as 32K cache
- No L2 cache
- Code and small memory (filter etc) are in L2

Modules: 2D convolutions

- Assumption:
  - Inputs are real uint8 in Q8 fixed-point format, stored sequentially row by row
  - 2D filter coefficients are real uint8 in Q8 fixed-point format, unit gain, always 5x5 in size, stored sequentially row by row
  - Outputs are real uint8 in Q8 fixed-point format, no overflow protection. They are stored sequentially row by row.
- Implementation details:
  - Read 8-bytes per row for 5 rows, generate 4 outputs per row for 5 rows.
  - Edge conditions are unrolled and hard coded.
  - Main loop is .S bounded @ ii = 14 (.M unit usage is 13) for 4 outputs
- Size 1024x1024 convolution takes 3,875,705 cycles (dirty cache state)
  - Comparing to flat memory estimation of 1024*1024*14/4 = 3,670,016 cycles
  - Comparing to Conti requirement of 400us which is 400,000 cycles for 1GHz device.

Modules: 2D Thresholding

- Assumption:
  - Inputs are real uint8 in Q8 fixed-point format, stored sequentially row by row.
  - Threshold is a single uint8 in Q8 fixed-point format
  - Outputs are 1-bit per threshold decision, packed in byte format.
- Implementation details:
  - Read 64 bytes (one cache line), generate 8 bytes outputs.
  - Main loop is .D bounded @ ii = 5 (if we unroll by 2 we can get ii = 9, but cycles are more heavily impacted by cache miss penalty)
- Size 1024x1024 thresholding takes 248,421 cycles (dirty cache state)
  - Comparing to flat memory estimation of 1024*1024*5/64 = 81,920 cycles
  - Comparing to Conti requirement of 16us which is 16,000 cycles for 1GHz device.

Modules: 2D Morphological Erosion

- Assumption:
  - Inputs are real uint8 in Q8 fixed-point format, stored sequentially row by row.
  - Neighborhood is all 1s 5x5 square (since assuming inputs being uint8, it does not make sense to have none-all 1s neighborhood)
  - are real uint8 in Q8 fixed-point format, stored sequentially row by row
  - Other morphological operations are similar so did not code up
- Implementation details:
  - Read 8-bytes per row for 5 rows, generate 4 outputs per row for 5 rows.
  - Edge conditions are unrolled and hard coded.
  - Main loop is .L bounded @ ii = 9 for 4 outputs
- Size 1024x1024 convolution takes 2,632,477 cycles (dirty cache state)
  - Comparing to flat memory estimation of 1024*1024*9/4 = 2,359,296 cycles
  - Comparing to Conti requirement of 80us which is 80,000 cycles for 1GHz device.
  - This module is especially bad for C66x because there is no fast comparison engine to compare 4 bytes within a register, or 8 bytes within a pair-register.