A. 演算法架構

QR factorization 的實際計算有很多方法，本篇使用 Givens rotation 演算法來實現。其中 Givens rotation 演算法使用 CORDIC 迭代來求出近似值。輸入資料為 8x4 矩陣(A_{8x4})，透過 Givens rotation 演算法將其轉換成 4x4 的上三角矩陣(R_{4x4})。如圖一的左圖，紅色為計算後的有效數值，黑色為需要消除的數值。

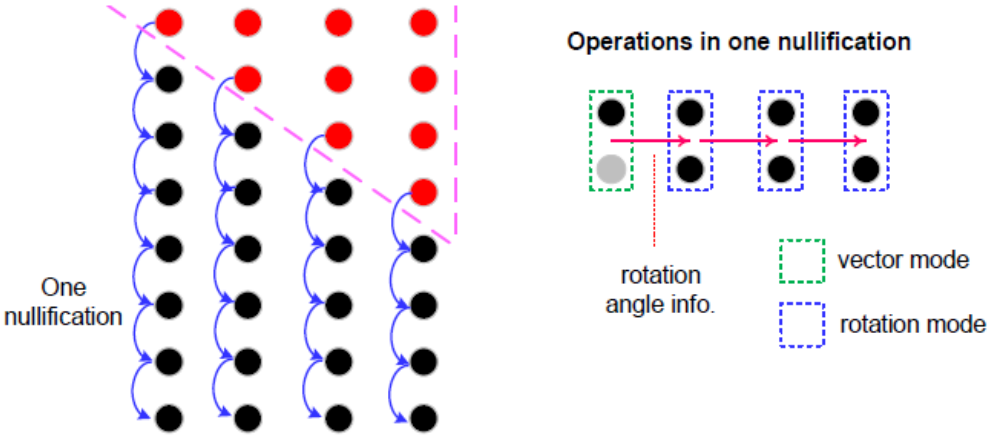

圖 1、QR factorization scheme achieved of Givens rotations

CORDIC 計算分為 vectoring mode 與 rotation mode 兩種模式，每次計算由鄰近的兩筆資料進行計算。綠色框線為 vectoring mode，此步驟會計算旋轉角度($\boldsymbol{d_i}$)並將$\boldsymbol{y_i}$消除掉。藍色框線為 rotation mode 模式，此步驟會向計算的旋轉角度($\boldsymbol{d_i}$)更新$\boldsymbol{x_i}$與$\boldsymbol{y_i}$的值。此外迭代的輸出必須乘上 K = 0.607252935…。($\boldsymbol{i}$ 為迭代次數 0)

最後可總結出下式:

$$\boldsymbol{x_{i+1} = x_i - y_i * d_i * 2^{-i}} \quad \textbf{(1)}$$

$$\boldsymbol{y_{i+1} = y_i + x_i * d_i * 2^{-i}} \quad \textbf{(2)}$$

B. 系統架構 & IO Ports

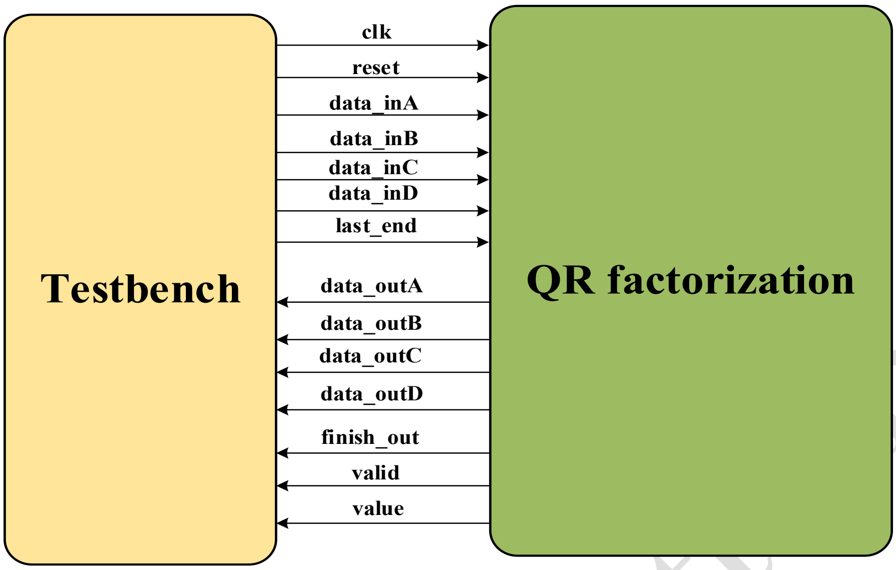

圖 2、QR factorization 與 Testbench 之系統方塊圖

表 1、輸入/輸出訊號

Signal Name	I/O	Width	Simple Description
clk	I	1	Positive edge triggered clock
reset	I	1	Active low asynchronous reset
data_inA	I	13	1st column signed number input of 8*4 matrix
data_inB	I	13	2nd column signed number input of 8*4 matrix
data_inC	I	13	3rd column signed number input of 8*4 matrix
data_inD	I	13	4th column signed number input of 8*4 matrix
last_end	I	1	High bit when last input data
data_outA	O	13	1st column signed number output of 8*4 matrix
data_outB	O	13	2nd column signed number output of 8*4 matrix
data_outC	O	13	3rd column signed number output of 8*4 matrix
data_outD	O	13	4th column signed number output of 8*4 matrix
finish_out	O	1	High bit when encoder ended
valid	O	1	When the high bit the output is valid
value	O	1	Set to high when data input is required

C. 硬體架構

將演算法 mapping 成各個 PE 如圖 3 所示，GG 為 vectoring mode，GR 為 rotation mode。本篇輸入訊號與輸出訊號是 13bit 的有號數，包含 4bit 整數、8bit 小數。資料陣列由最後一筆開始依序輸入，已鄰近的兩筆資料做運算，每次的運算結果$\boldsymbol{x_{i+1}}$保留至下次運算，$\boldsymbol{y_{i+1}}$則是會輸出 GR 會將計算結果$\boldsymbol{y_{i+1}}$傳遞給下一級，GG 會將計算的旋轉角度$(\boldsymbol{d_i})$向右邊傳遞給 GR。因輸出資料會因為每一列的運算 PE 數量不同導致偏移，所以增加 shift register 來對齊偏移的輸出。

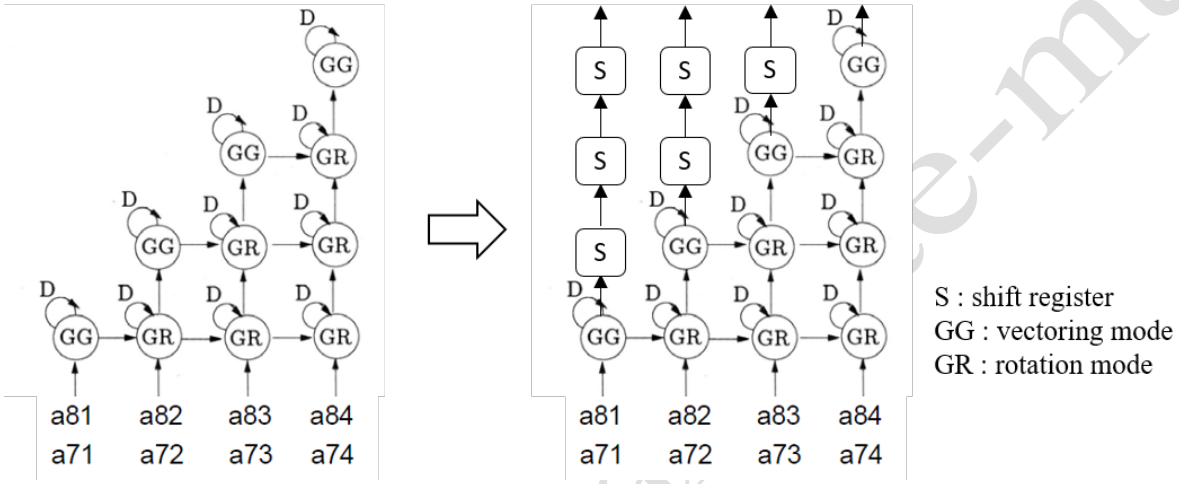

圖 3、Triangular systolic array design for QR factorization

本篇運算進行 12 次的迭代，每個 Cycle 進行 3 次的迭代，所以代表每個 PE 會有 3 次迭代的硬體。其 GG 與 GR 的硬體架構圖分別如圖 4 與圖 5。此外在 GG 與 GR 的內部運算是 26bit 的有號數，包含 13bit 整數、12bit 小數。

GG(vectoring mode):

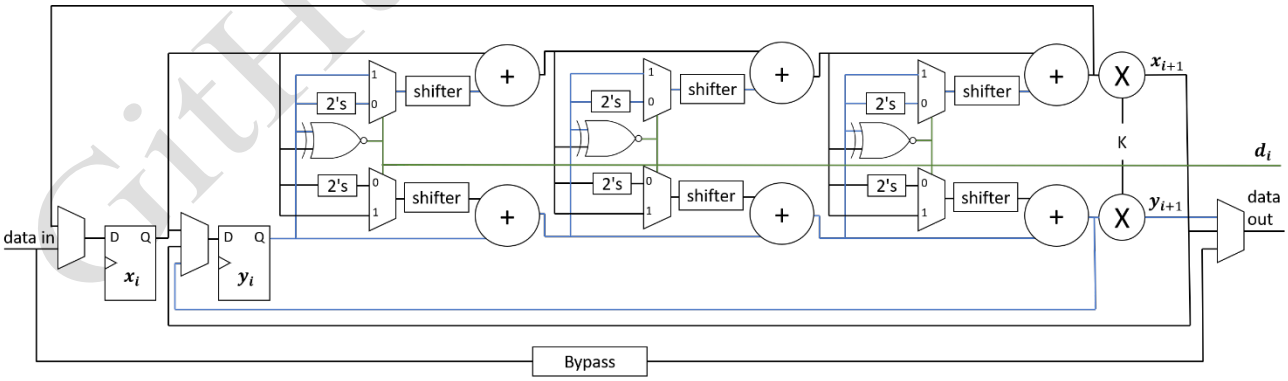

圖 4、GG 硬體架構圖

GR(rotation mode):

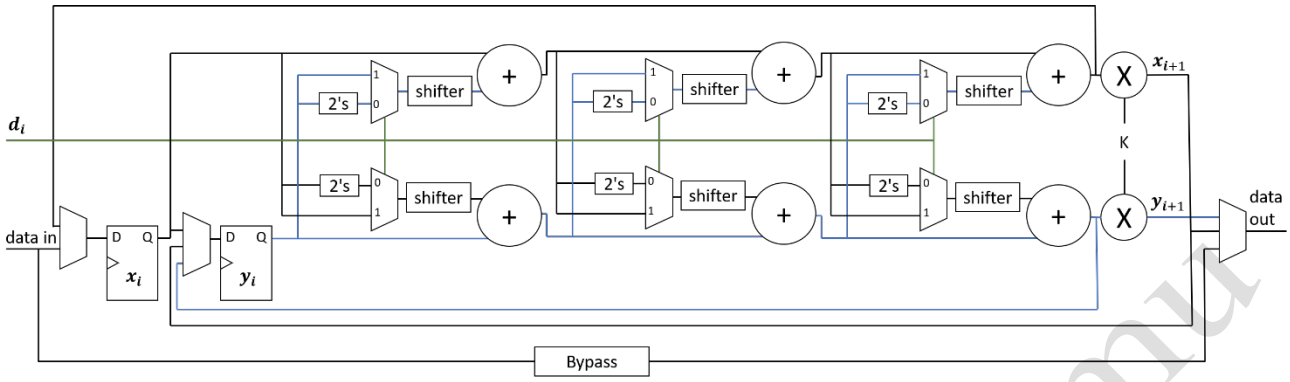

圖 5、GR 硬體架構圖

D. 時序

Testbench 傳送給硬體的資料時序如圖 6 所示，value 訊號在 Clock 上升緣時為 High，Testbench 會在 Clock 下降緣時依序給出資料，當輸出最後一筆資料的同時 Testbench 會將 last_end 訊號更新為 High。

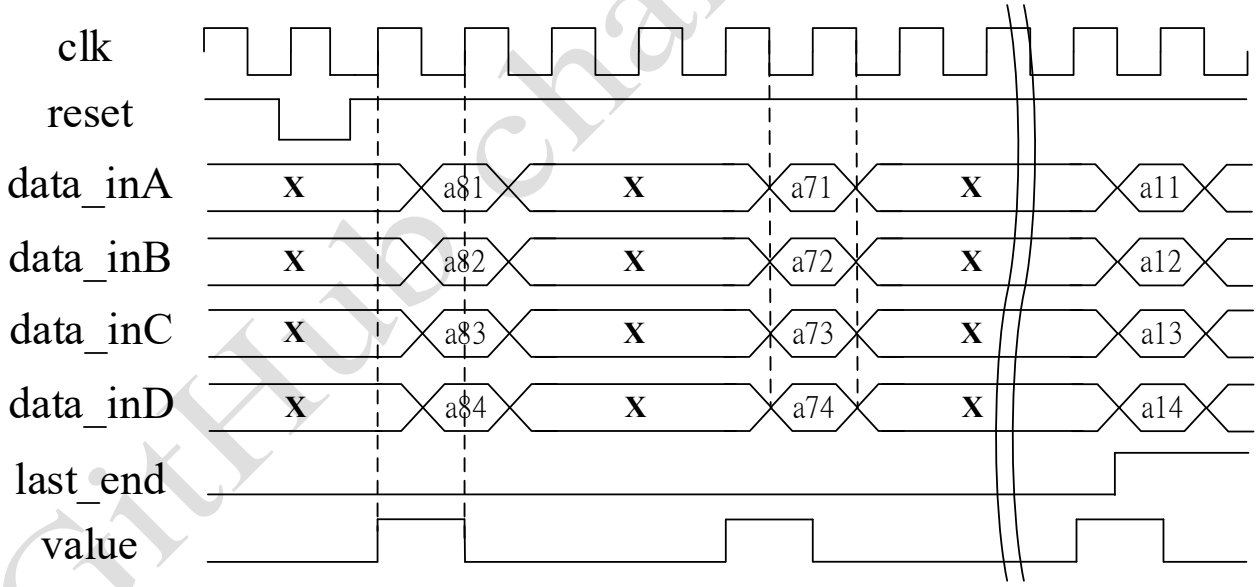

圖 6、資料輸入時序圖

本篇運算進行 12 次的迭代，代表每 4 個 Cycle 可產生一次結果。輸出訊號時序圖如圖 7 所示，當輸出訊號為有效值時須在 Clock 上升緣時將 valid 訊號設置為 High，並且將資料輸出。當所有資料輸出完畢後將 finish_out 訊號設置為 High，代表系統已完成運算，Testbench 會將輸出訊號與 Answer 做比對。

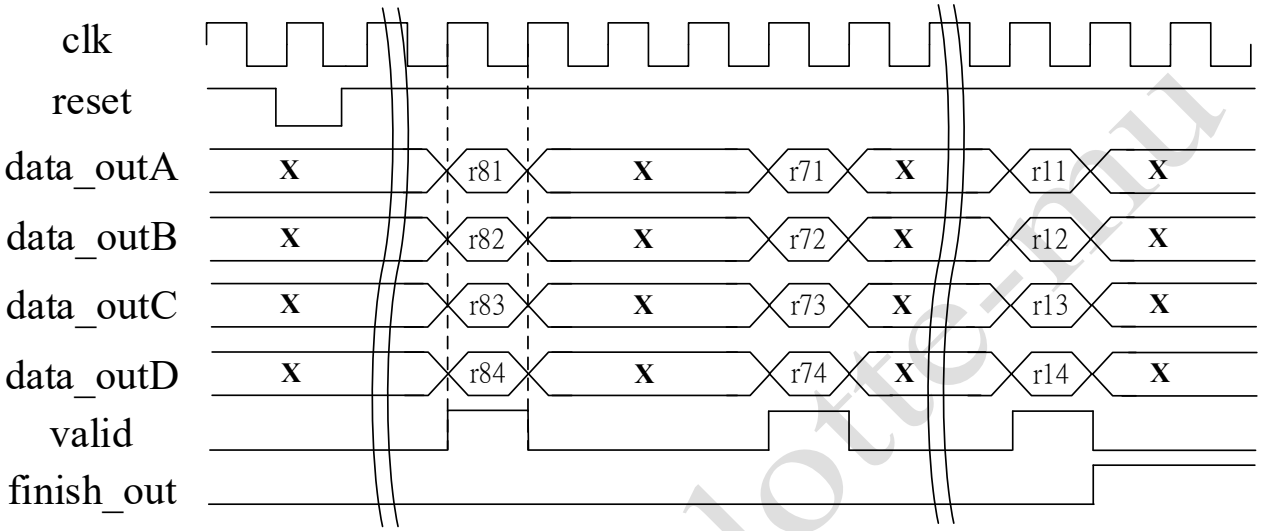

圖 7、資料輸出時序圖

E. Simulation & Synthesis

- **Matlab**

本篇所使用的 Test pattern 為下列矩陣:

Input matrix

$$\begin{bmatrix} 1 & 2 & 3 & 4 \\ 2 & 1 & 3 & 4 \\ 2 & 3 & 1 & 4 \\ 2 & 3 & 4 & 1 \\ 3 & 2 & 4 & 1 \\ 3 & 4 & 2 & 1 \\ 3 & 4 & 1 & 2 \\ 4 & 3 & 1 & 2 \end{bmatrix}$$

使用 Matlab 模擬硬體的整數運算，所以須將矩陣(左邊 Input matrix)向左位移 8bit 作為小數。Matlab 的運算結果為右邊 output matrix。

Input matrix **output matrix**

$$\begin{bmatrix} 256 & 512 & 768 & 1024 \\ 512 & 256 & 768 & 1024 \\ 512 & 768 & 256 & 1024 \\ 512 & 768 & 1024 & 256 \\ 768 & 512 & 1024 & 256 \\ 768 & 1024 & 512 & 256 \\ 768 & 1024 & 256 & 512 \\ 1024 & 768 & 256 & 512 \end{bmatrix} \begin{bmatrix} 1885 & 1953 & 1490 & 1424 \\ 1 & -709 & -127 & -316 \\ -1 & 0 & -1185 & -453 \\ 0 & 0 & 0 & 1201 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix}$$

- **functional Simulation**

使用 Modelsim 進行 functional Simulation，圖 8 為資料輸入的波形圖，圖 9 為資料輸出的波形圖，圖 10 為輸出訊號與 Answer 比對結果。因硬體運算有位元的限制，所以計算結果與 Matlab 所產生出的結果會有差異，但這是在合理範圍內的誤差。

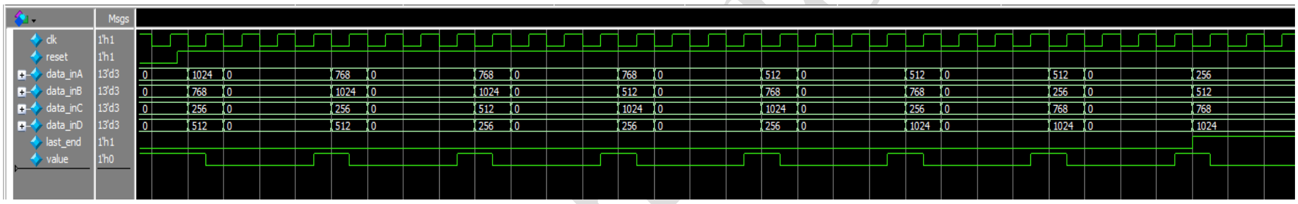

圖 8、資料輸入之模擬波形圖

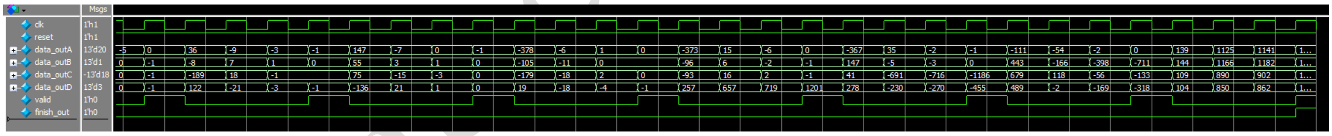

圖 9、資料輸出之模擬波形圖

```
# ---------------------
# -- Simulation Start --
# ---------------------
# index          0:  0,  1024,   768,   256,   512
# index          1:  0,   768,  1024,   256,   512
# index          2:  0,   768,  1024,   512,   256
# index          3:  0,   768,   512,  1024,   256
# index          4:  0,   512,   768,  1024,   256
# index          5:  0,   512,   768,   256,  1024
# index          6:  0,   512,   256,   768,  1024
# index          7:  1,   256,   512,   768,  1024
# index          8:  1,     3,     3,     3,     3
# pass 1 gold:     0,    -1,    -1,    -1; ans:     0,    -1,    -1,    -1
# pass 2 gold:    -1,     0,    -1,    -1; ans:    -1,     0,    -1,    -1
# pass 3 gold:    -1,     0,     0,     0; ans:    -1,     0,     0,     0
# pass 4 gold:     0,     0,     0,    -1; ans:     0,     0,     0,    -1
# pass 5 gold:     0,    -1,    -1,  1201; ans:     0,    -1,    -1,  1201
# pass 6 gold:    -1,     0, -1186,  -455; ans:    -1,     0, -1186,  -455
# pass 7 gold:     0,  -711,  -133,  -318; ans:     0,  -711,  -133,  -318
# pass 8 gold:  1886,  1954,  1491,  1424; ans:  1886,  1954,  1491,  1424
# --------------------------------------------------
# ------Simulation finish all pass-----------------
# --------------------------------------------------
#
# --------------------------------------------------
# cycle :        60
# --------------------------------------------------
```

圖 10、輸出訊號與 Answer 比對結果

- **Synthesis**

本篇使用 CBDK_IC_Contest_v2.1 虛擬製程進行 Synthesis，sdc 設定檔 Cycle 為 10ns(100MHz)，圖 11 所示。合成後 Clock 速度可達到 100MHz，Timing Report 如圖 12 所示。如圖 13 所示合成後 Cell Area 為 956,912，一個 adder (全加器) Cell Area 為 44.132(如圖 14 所示)，此 QR factorization 硬體等同為 21,682 個 adder (全加器)。合成後進行 pre-sim，Test pattern 皆比對正確，如圖 15 所示。

另外本篇有合成每個 Cycle 進行 12 次的迭代，合成後 Timing 及 Area 皆不理想，如圖 16 與圖 17 所示。

Open | QR_top.sdc ~/DV/DV_QR/design_data | Save

```
# operating conditions and boundary conditions #

set cycle 10.0
create_clock -name clk  -period $cycle   [get_ports  clk]

set_dont_touch_network      [all_clocks]
set_fix_hold                [all_clocks]
set_clock_uncertainty  0.1  [all_clocks]
set_clock_latency      0.5  [all_clocks]
set_ideal_network           [get_ports clk]


#Don't touch the basic env setting as below
set_input_delay  0   -clock clk [remove_from_collection [all_inputs] [get_ports
clk]] -clock_fall
set_output_delay 0    -clock clk [all_outputs]  -clock_fall

set_load         1   [all_outputs]
set_drive        0.1   [all_inputs]

set_operating_conditions -max_library slow -max slow
set_wire_load_model -name tsmc13_wl10 -library slow
set_max_fanout 20 [all_inputs]
```

圖 11、Synthesis sdc 設定檔

```
U99508/Y (NOR2X8)                        0.10       7.88 f
U79178/Y (OA21X4)                        0.26       8.15 f
U47050/Y (OR2X4)                         0.23       8.37 f
U47125/Y (NAND2X4)                       0.09       8.46 r
U73505/Y (XOR2X4)                        0.18       8.64 r
U53210/Y (INVX3)                         0.12       8.76 f
U82368/Y (XOR2X4)                        0.17       8.93 r
U82367/Y (XNOR2X4)                       0.21       9.14 r
U106677/Y (NAND2X6)                      0.15       9.29 f
U82375/Y (NAND2X4)                       0.15       9.44 r
U72381/Y (NOR2X6)                        0.08       9.52 f
U53006/Y (NAND2X6)                       0.08       9.59 r
U66241/Y (NAND3X6)                       0.08       9.67 f
U72051/Y (XNOR2X4)                       0.17       9.84 f
U72048/Y (NAND2X6)                       0.09       9.93 r
U86349/Y (AND2X8)                        0.15      10.08 r
U46819/Y (INVX20)                        0.08      10.16 f
U108479/Y (NAND2X2)                      0.08      10.24 r
u6/x_reg_reg[0][16]/D (DFFRX2)           0.00      10.24 r
data arrival time                                  10.24

clock clk (rise edge)                   10.00      10.00
clock network delay (ideal)              0.50      10.50
clock uncertainty                       -0.10      10.40
u6/x_reg_reg[0][16]/CK (DFFRX2)          0.00      10.40 r
library setup time                      -0.16      10.24
data required time                                 10.24
-----------------------------------------------------------
data required time                                 10.24
data arrival time                                 -10.24
-----------------------------------------------------------
slack (MET)                                        0.00
```

圖 12、Timing Report of Synthesis

```
****************************************
Report : area
Design : QR_top
Version: S-2021.06-SP2
Date   : Mon May 30 14:22:42 2022
****************************************

Library(s) Used:

    slow (File: /cad/CBDK/CBDK_IC_Contest_v2.1/SynopsysDC/
db/slow.db)

Number of ports:                          110
Number of nets:                         72610
Number of cells:                        71870
Number of combinational cells:          69516
Number of sequential cells:              2354
Number of macros/black boxes:               0
Number of buf/inv:                      11714
Number of references:                     211

Combinational area:             876438.909793
Buf/Inv area:                    75189.727320
Noncombinational area:           80473.732666
Macro/Black Box area:                0.000000
Net Interconnect area:         7122815.901062

Total cell area:                956912.642459
Total area:                    8079728.543521
```

圖 13、Area Report of Synthesis

```
module top (
        input A,B,
        output [1:0]C
);
assign C = A + B;

endmodule
```

top.sdc

```
# operating conditions and boundary conditions #

set_load         1   [all_outputs]
set_drive        0.1   [all_inputs]

set_operating_conditions -max_library slow -max slow
set_wire_load_model -name tsmc13_wl10 -library
slow
set_max_fanout 20 [all_inputs]
```

```
Operating Conditions: slow   Library: slow
Wire Load Model Mode: top

  Startpoint: A (input port)
  Endpoint: C[0] (output port)
  Path Group: (none)
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  top                tsmc13_wl10           slow

  Point                                    Incr       Path
  ------------------------------------------------------------
  input external delay                     0.00       0.00 f
  A (in)                                   0.00       0.00 f
  U3/Y (NAND2XL)                           0.56       0.56 r
  U4/Y (INVX12)                            0.68       1.24 f
  U6/Y (AOI2BB1X1)                         0.41       1.65 r
  U5/Y (BUFX12)                            0.73       2.37 r
  C[0] (out)                               0.00       2.37 r
  data arrival time                                   2.37

  (Path is unconstrained)
```

area.log

```
****************************************
Report : area
Design : top
Version: S-2021.06-SP2
Date   : Thu May 26 22:56:21 2022
****************************************

Library(s) Used:

    slow (File: /cad/CBDK/CBDK_IC_Contest_v2.1/
SynopsysDC/db/slow.db)

Number of ports:                          4
Number of nets:                           6
Number of cells:                          4
Number of combinational cells:            4
Number of sequential cells:               0
Number of macros/black boxes:             0
Number of buf/inv:                        2
Number of references:                     4

Combinational area:               44.132401
Buf/Inv area:                     30.553201
Noncombinational area:             0.000000
Macro/Black Box area:              0.000000
Net Interconnect area:           420.002106

Total cell area:                  44.132401
Total area:                      464.134507
```

圖 14、adder (全加器) Synthesis 結果

```
---------------------
-- Simulation Start --
---------------------
index           0:  0,  1024,   768,   256,   512
index           1:  0,   768,  1024,   256,   512
index           2:  0,   768,  1024,   512,   256
index           3:  0,   768,   512,  1024,   256
index           4:  0,   512,   768,  1024,   256
index           5:  0,   512,   768,   256,  1024
index           6:  0,   512,   256,   768,  1024
index           7:  1,   256,   512,   768,  1024
index           8:  1,     3,     3,     3,     3
pass 1 gold:     0,    -1,    -1,    -1; ans:     0,    -1,    -1,    -1
pass 2 gold:    -1,     0,    -1,    -1; ans:    -1,     0,    -1,    -1
pass 3 gold:    -1,     0,     0,     0; ans:    -1,     0,     0,     0
pass 4 gold:     0,     0,     0,    -1; ans:     0,     0,     0,    -1
pass 5 gold:     0,    -1,    -1,  1201; ans:     0,    -1,    -1,  1201
pass 6 gold:    -1,     0, -1186,  -455; ans:    -1,     0, -1186,  -455
pass 7 gold:     0,  -711,  -133,  -318; ans:     0,  -711,  -133,  -318
pass 8 gold:  1886,  1954,  1491,  1424; ans:  1886,  1954,  1491,  1424
------------------------------------------------
------Simulation finish all pass----------------
------------------------------------------------
------------------------------------------------
cycle :         60
------------------------------------------------
```

圖 15、pre-sim 結果

```
U62915/Y (NAND2X4)                                      0.10      27.60 r
U126633/Y (XNOR2X4)                                     0.12      27.72 r
U182376/S (ADDFHX4)                                     0.36      28.07 f
U126709/Y (OAI21X4)                                     0.09      28.17 r
U126708/Y (OAI2BB1X4)                                   0.09      28.26 f
U182523/CO (ADDFHX4)                                    0.24      28.50 f
U185950/CO (ADDFHX4)                                    0.32      28.82 f
U1597/Y (INVX6)                                         0.13      28.95 r
U188506/S (ADDFHX4)                                     0.35      29.30 r
U117055/Y (XOR2X4)                                      0.18      29.48 r
U131532/Y (XOR2X4)                                      0.16      29.64 r
U188507/S (ADDFHX4)                                     0.42      30.06 f
U121185/Y (NOR2X8)                                      0.14      30.20 r
U120973/Y (NOR2X8)                                      0.10      30.30 f
U747/Y (NAND2X4)                                        0.10      30.40 r
U117059/Y (NAND3X8)                                     0.15      30.55 f
U33308/Y (BUFX20)                                       0.15      30.70 f
U85675/Y (NAND2X6)                                      0.07      30.77 r
U118431/Y (NAND3X6)                                     0.08      30.85 f
U118430/Y (XOR2X4)                                      0.13      30.98 f
U121030/Y (OAI21X4)                                     0.13      31.11 r
u6/y_reg_reg[0][16]/D (DFFRX2)                          0.00      31.11 r
data arrival time                                                 31.11

clock clk (rise edge)                                  10.00      10.00
clock network delay (ideal)                             0.50      10.50
clock uncertainty                                      -0.10      10.40
u6/y_reg_reg[0][16]/CK (DFFRX2)                         0.00      10.40 r
library setup time                                     -0.17      10.23
data required time                                                10.23
-----------------------------------------------------------------------
data required time                                                10.23
data arrival time                                                -31.11
-----------------------------------------------------------------------
slack (VIOLATED)                                                 -20.88
```

圖 16、每個 Cycle 12 次迭代之 Timing

```
****************************************
Report : area
Design : QR_top
Version: S-2021.06-SP2
Date   : Wed May 25 23:58:35 2022
****************************************

Library(s) Used:

    slow (File: /cad/CBDK/CBDK_IC_Contest_v2.1/SynopsysDC/db/
slow.db)

Number of ports:                          109
Number of nets:                        232707
Number of cells:                       195604
Number of combinational cells:         194937
Number of sequential cells:               667
Number of macros/black boxes:               0
Number of buf/inv:                      34999
Number of references:                     193

Combinational area:            4088396.689525
Buf/Inv area:                   235619.487273
Noncombinational area:           25980.403927
Macro/Black Box area:                0.000000
Net Interconnect area:       20172794.292694

Total cell area:               4114377.093452
Total area:                  24287171.386146
1
```

圖 17、每個 Cycle 12 次迭代之 Area