Digital Systems Design and Laboratory
[13. Analysis of Clocked Sequential Circuits]

Chung-Wei Lin

cwlin@csie.ntu.edu.tw

CSIE Department

National Taiwan University

Outline

☐ **A Sequential Parity Checker**

☐ Analysis by Signal Tracing and Timing Charts

☐ State Tables and Graphs

☐ General Models for Sequential Circuits
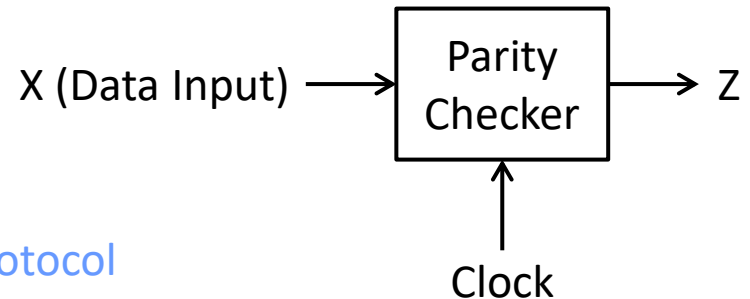
Parity Checker (1/3)

❑ Error detection

➢ Add an extra bit (parity bit) when transmitting or storing binary data

➢ When the total number of 1 bits in the block (data bits + parity bit) is odd (even), we say the parity is odd (even)

| Even Parity		Odd Parity	
0000000	0	0000000	1
0000001	1	0000001	0
0110110	0	0110110	1
1010101	0	1010101	1
0111000	1	0111000	0

Parity Checker (2/3)

❑ **Design an odd-parity checker**

➢ Z = 1 if total # of 1's is odd

➢ Z = 0 if total # of 1's is even

• Z = 0 → an error occurs in odd-parity protocol

• Initially, Z = 0

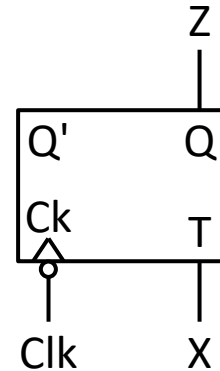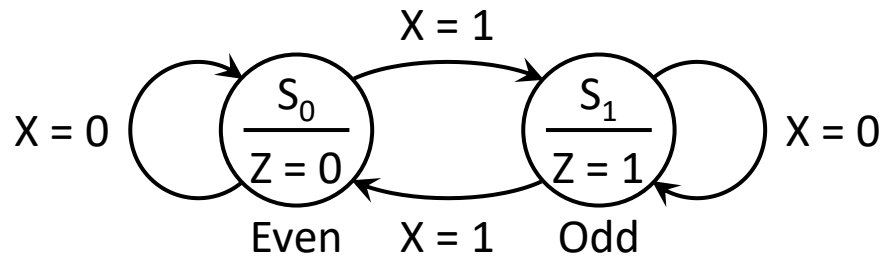X (Data Input) → Parity Checker → Z

Clock

❑ **Timing chart of the odd parity checker (falling-edge triggered)**

Clock

| X | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 |

Z = Q
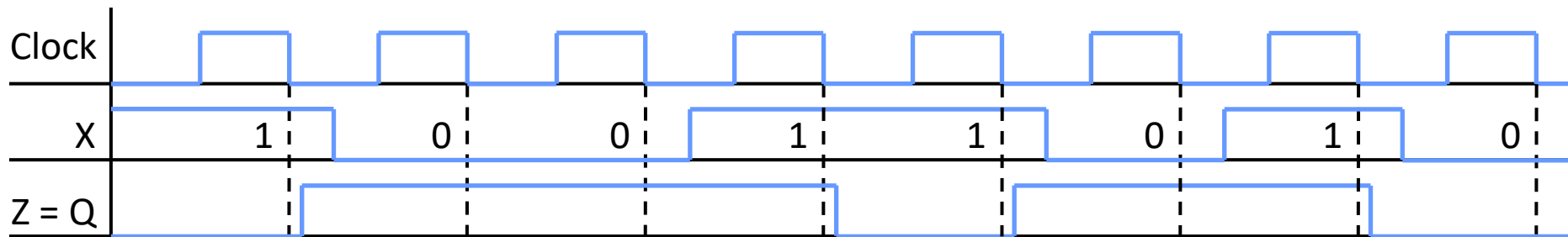
Parity Checker (3/3)

❑ State graph

❑ State table

Present State	Next State		Present Output (Z)
	X = 0	X = 1	
S_0	S_0	S_1	0
S_1	S_1	S_0	1

➡

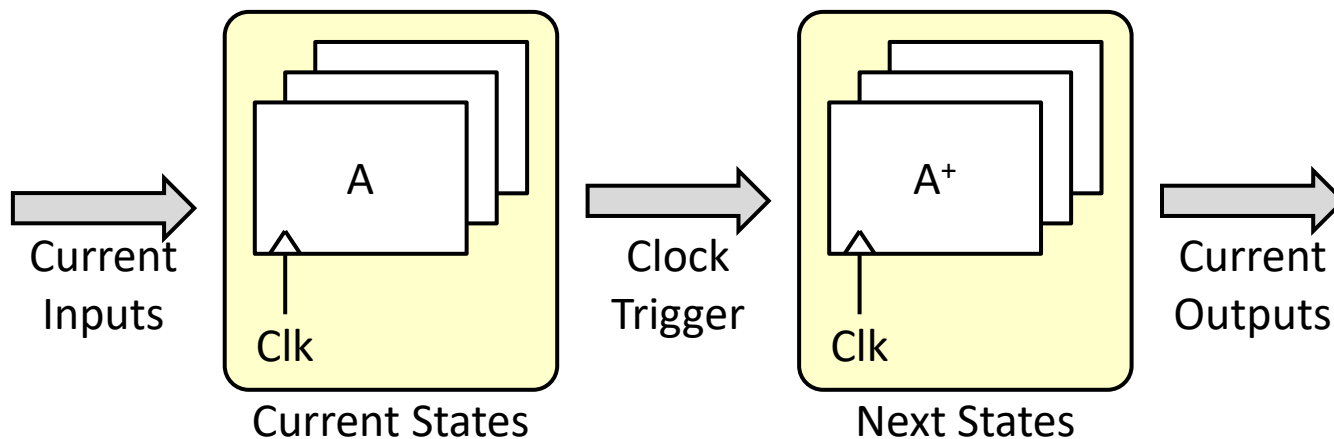| Q	Q^+		Present Output (Z)
	X = 0	X = 1	
0	0	1	0
1	1	0	1

Outline

❑ A Sequential Parity Checker

❑ **Analysis by Signal Tracing and Timing Charts**

❑ State Tables and Graphs

❑ General Models for Sequential Circuits

Analysis of Clocked Sequential Circuits

❑ Find the output sequence resulting from a given input one

➢ Draw a timing chart to show inputs, clock, flip-flop states, outputs

1. Assume an initial state of flip-flops (reset to 0)

2. For the first input, determine the circuit outputs and flip-flop inputs

3. Determine the new flip-flop states after the next active clock edge

4. Determine the outputs for the new states

5. Repeat 2--4 for each input pattern

Current Inputs → [A Clk] Current States → Clock Trigger → [A⁺ Clk] Next States → Current Outputs

Type I: Moore Machine

❑ Moore machine: the output depends only on the present state

➤ The output which corresponds to a given input appears until after the active clock edge

$Z = A \oplus B$
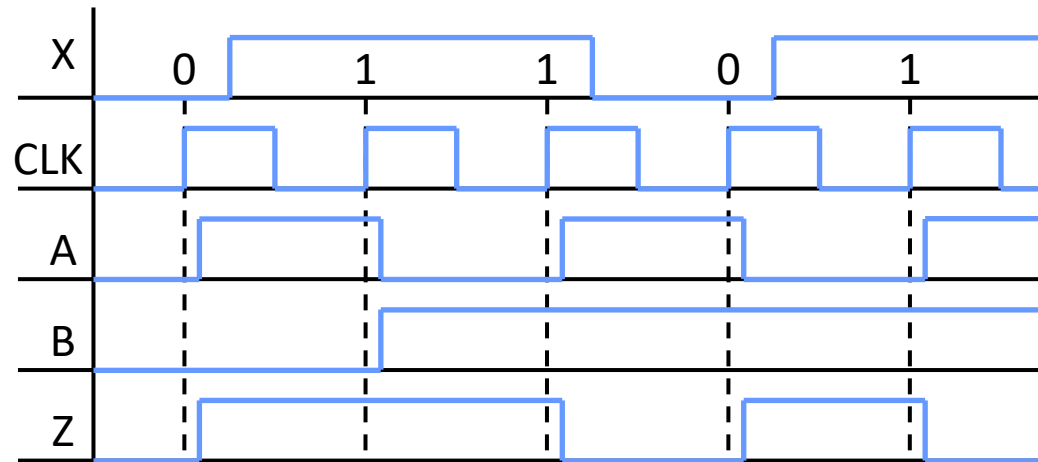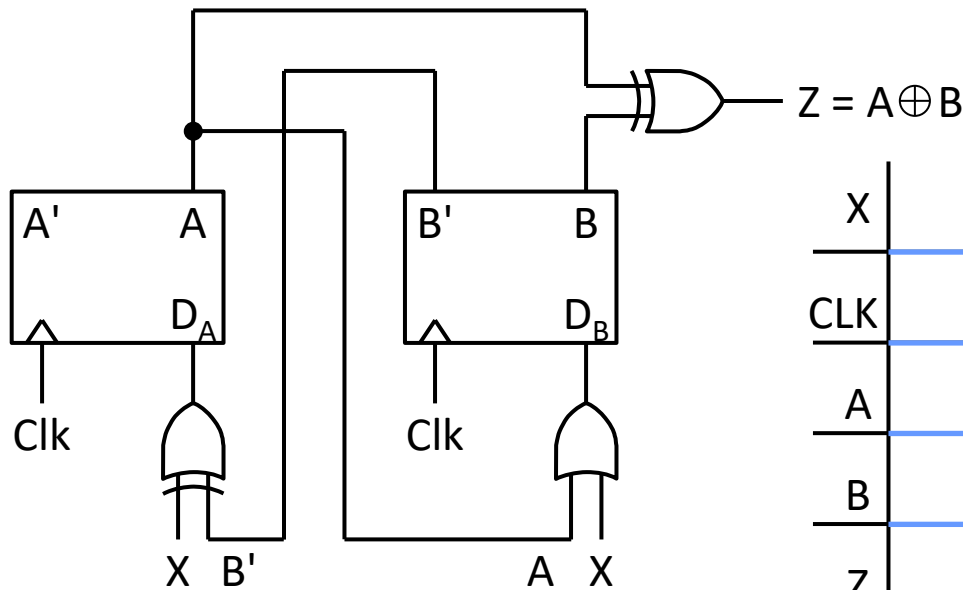
X = 0 1 1 0 1
A = 0 1 0 1 0 1
B = 0 0 1 1 1 1
Z = 0 1 1 0 1 0

Type II: Mealy Machine

❑ Mealy machine: the output depends on both the present state and on the inputs

➢ False outputs may occur

• Glitches and spikes
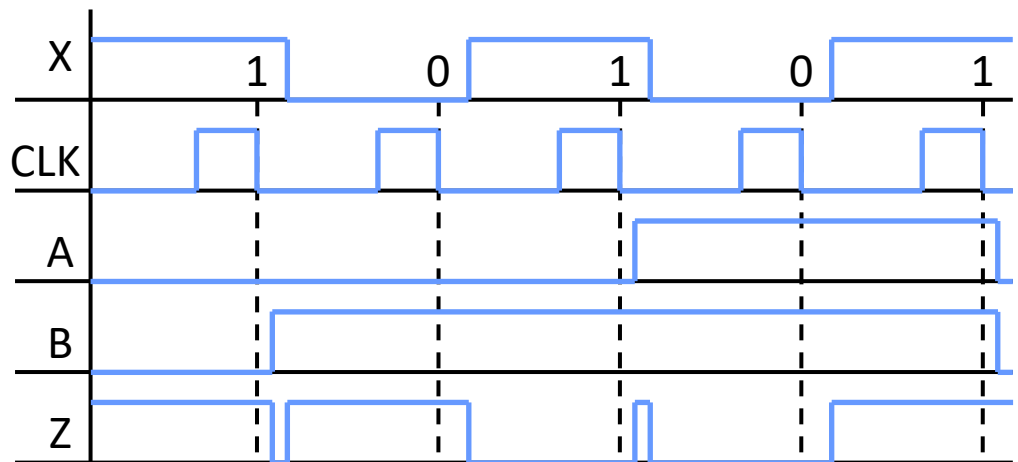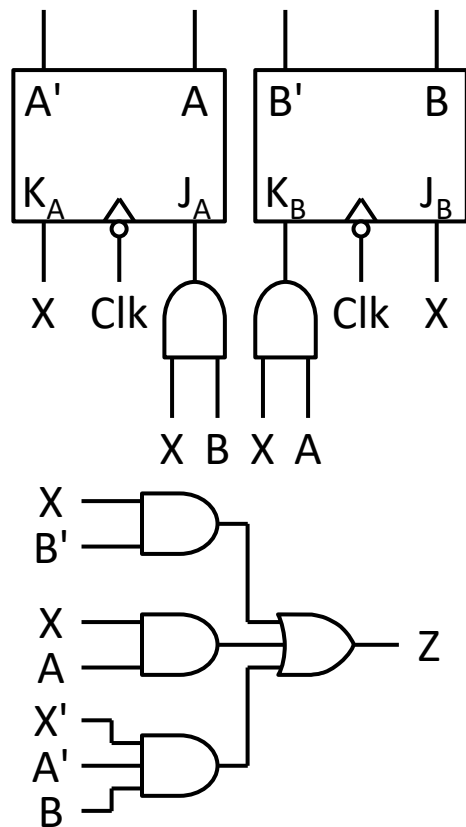
$X = 1\ 0\ 1\ 0\ 1$
$A = 0\ 0\ 0\ 1\ 1\ 0$
$B = 0\ 1\ 1\ 1\ 1\ 0$
$Z = 1\ 1\ 0\ 0\ 1$

Outline

❑ A Sequential Parity Checker

❑ Analysis by Signal Tracing and Timing Charts

❑ **State Tables and Graphs**

❑ General Models for Sequential Circuits

How to Construct the State Table?

❑ **Procedure to construct the state table for a given circuit**

1. Determine the flip-flop input equations and the output equations from the circuit

2. Derive the next-state equation for each flip-flop from its input equations

3. Plot a next-state map for each flip-flop

4. Combine these maps to form the state table

❑ **Recap: next-state equations**

Type	Q^+
D Flip-Flop	D
S-R Flip-Flop	S + R'Q
J-K Flip-Flop	JQ' + K'Q
T Flip-Flop	TQ' + T'Q
D-CE Flip-Flop	D(CE) + Q(CE)'

Example: Moore Machine (1/3)

❑ **Procedure to construct the state table for a given circuit**

1. Determine the flip-flop input equations and the output equations from the circuit

   - $D_A = X \oplus B'$, $D_B = A + X$, $Z = A \oplus B$

2. Derive the next-state equation for each flip-flop from its input equations

   - $A^+ = X \oplus B'$, $B^+ = A + X$
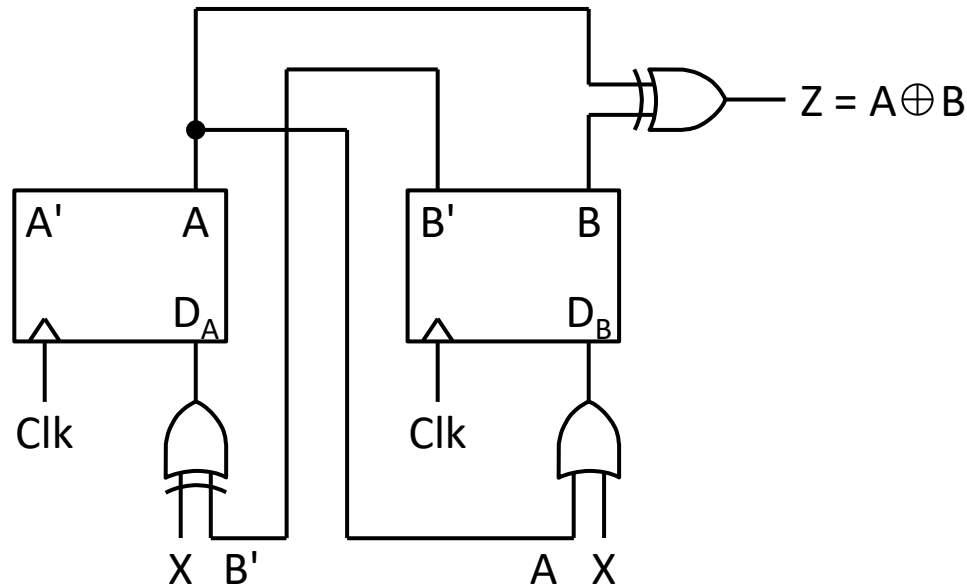
Example: Moore Machine (2/3)

❑ Procedure to construct the state table for a given circuit

- $A^+ = X \oplus B'$, $B^+ = A + X$

3. Plot a next-state map for each flip-flop

4. Combine these maps to form the state table

AB	A^+B^+		Z
	X = 0	X = 1	
00	10	01	0
01	00	11	1
11	01	11	0
10	11	01	1

AB \ X	0	1
00	1	0
01	0	1
11	0	1
10	1	0

A^+

AB \ X	0	1
00	0	1
01	0	1
11	1	1
10	1	1

B^+

Example: Moore Machine (3/3)

❑ Procedure to construct the state table for a given circuit

4. Combine these maps to form the state table

AB	A⁺B⁺		Z
	X = 0	X = 1	
00	10	01	0
01	00	11	1
11	01	11	0
10	11	01	1

Present State	Next State		Z
	X = 0	X = 1	
S_0	S_3	S_1	0
S_1	S_0	S_2	1
S_2	S_1	S_2	0
S_3	S_2	S_1	1
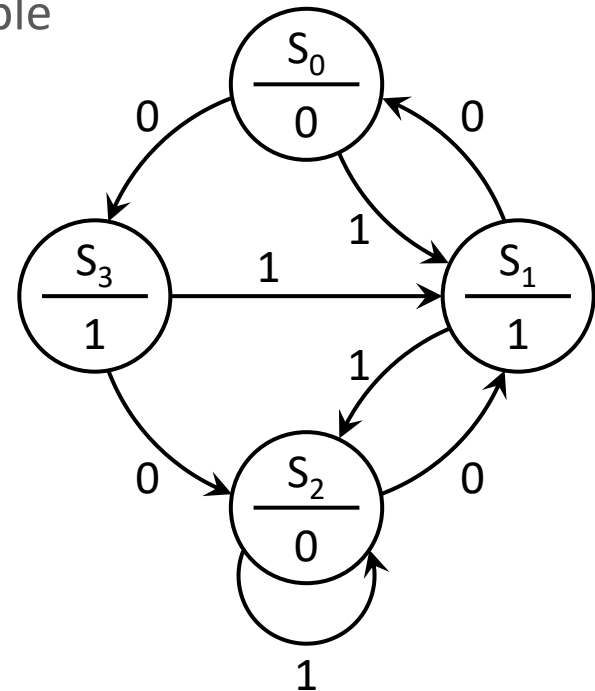
Example: Mealy Machine (1/3)

❑ **Procedure to construct the state table for a given circuit**

1. Determine the flip-flop input equations and the output equations from the circuit

   - $J_A = XB$, $K_A = X$, $J_B = X$, $K_B = XA$, $Z = XB' + XA + X'A'B$

2. Derive the next-state equation for each flip-flop from its input equations

   - $A^+ = J_A A' + K_A'A = XA'B + X'A$
   - $B^+ = J_B B' + K_B'B = XB' + (XA)'B = XB' + X'B + A'B$
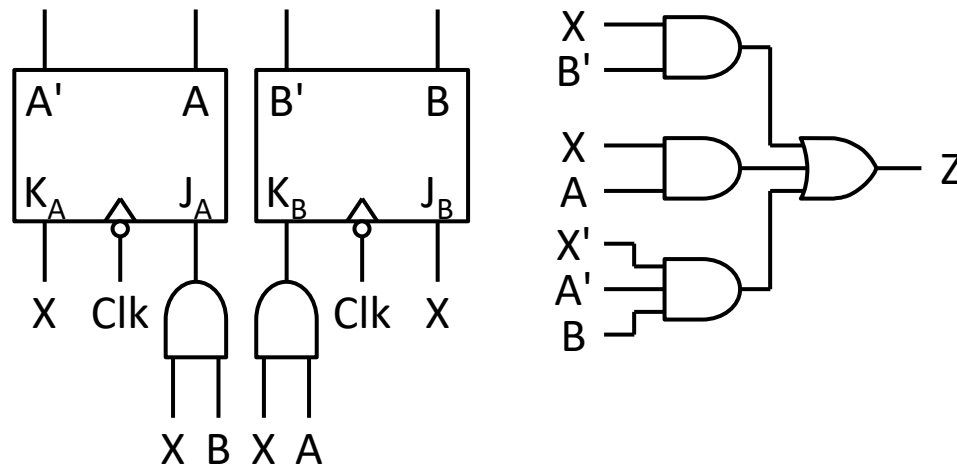
Example: Mealy Machine (2/3)

❑ Procedure to construct the state table for a given circuit

- $A^+ = XA'B + X'A$
- $B^+ = XB' + X'B + A'B$
- **$Z = XB' + XA + X'A'B$**

3. Plot a next-state map for each flip-flop

4. Combine these maps to form the state table

AB	A⁺B⁺		Z	
	X = 0	X = 1	X = 0	X = 1
00	00	01	0	1
01	01	11	1	0
11	11	00	0	1
10	10	01	0	1

X
AB \ 0 1

AB	0	1
00	0	0
01	0	1
11	1	0
10	1	0

A^+

X
AB \ 0 1

AB	0	1
00	0	1
01	1	1
11	1	0
10	0	1

B^+

X
AB \ 0 1

AB	0	1
00	0	1
01	1	0
11	0	1
10	0	1

Z

Example: Mealy Machine (3/3)

❑ Procedure to construct the state table for a given circuit

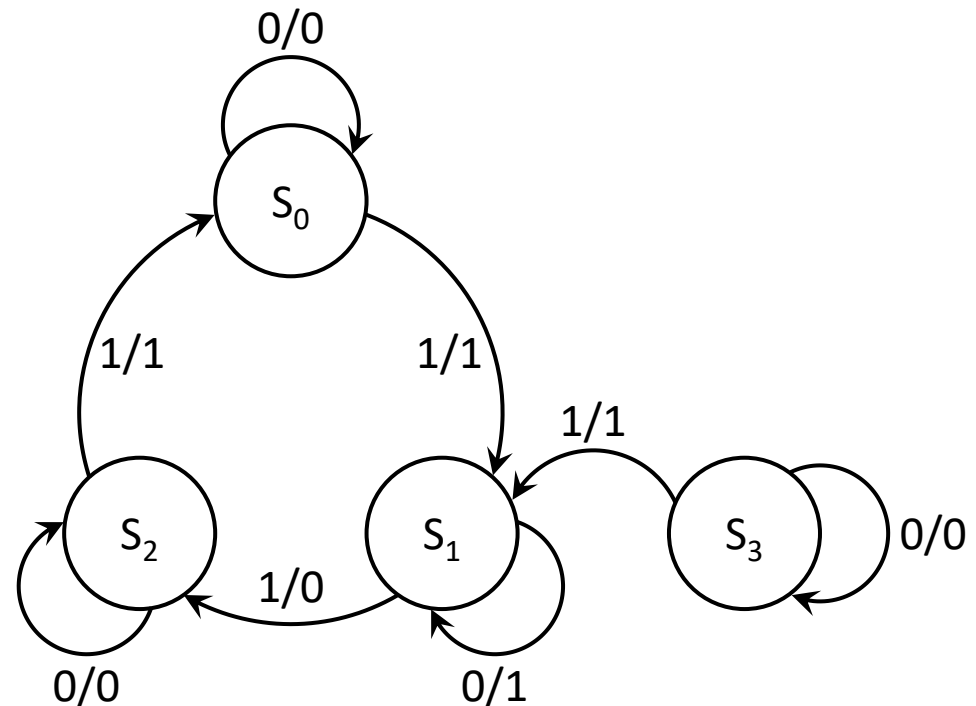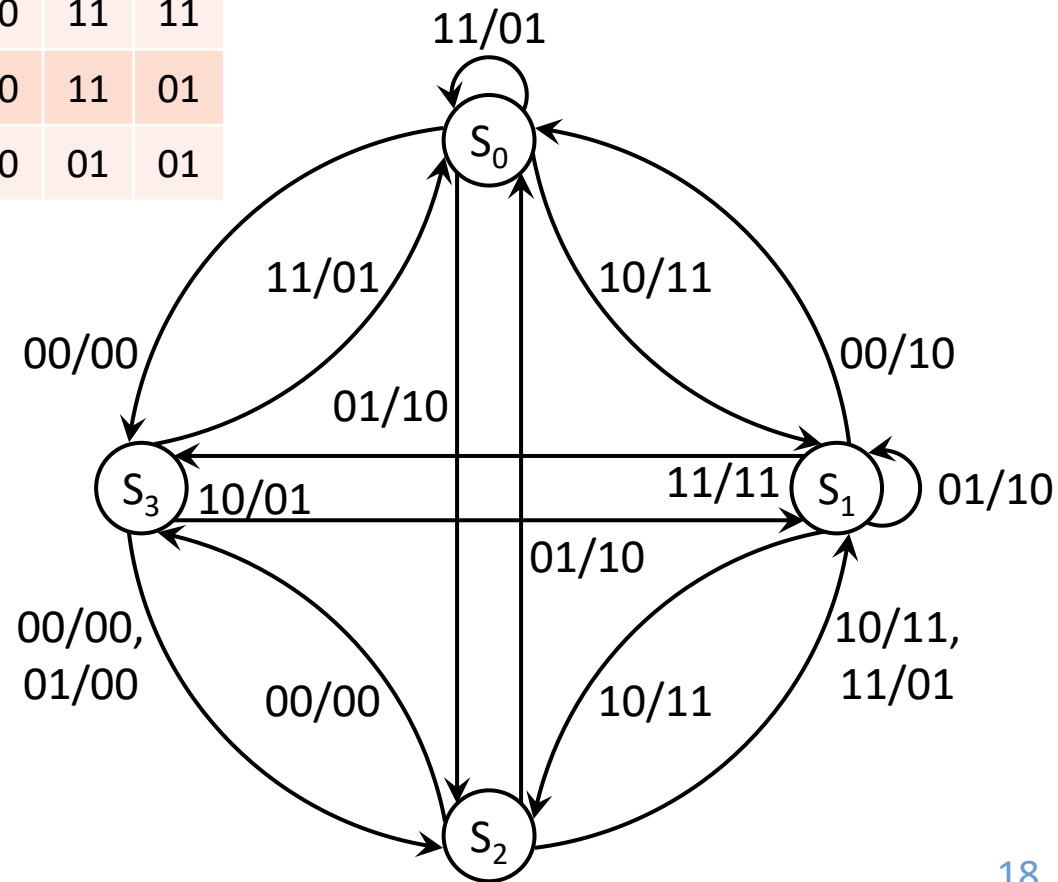4. Combine these maps to form the state table

AB	A^+B^+		Z	
	X = 0	X = 1	X = 0	X = 1
00	00	01	0	1
01	01	11	1	0
11	11	00	0	1
10	10	01	0	1

AB	A^+B^+		Z	
	X = 0	X = 1	X = 0	X = 1
S_0	S_0	S_1	0	1
S_1	S_1	S_2	1	0
S_2	S_2	S_0	0	1
S_3	S_3	S_1	0	1

Example: Multiple Inputs and Outputs

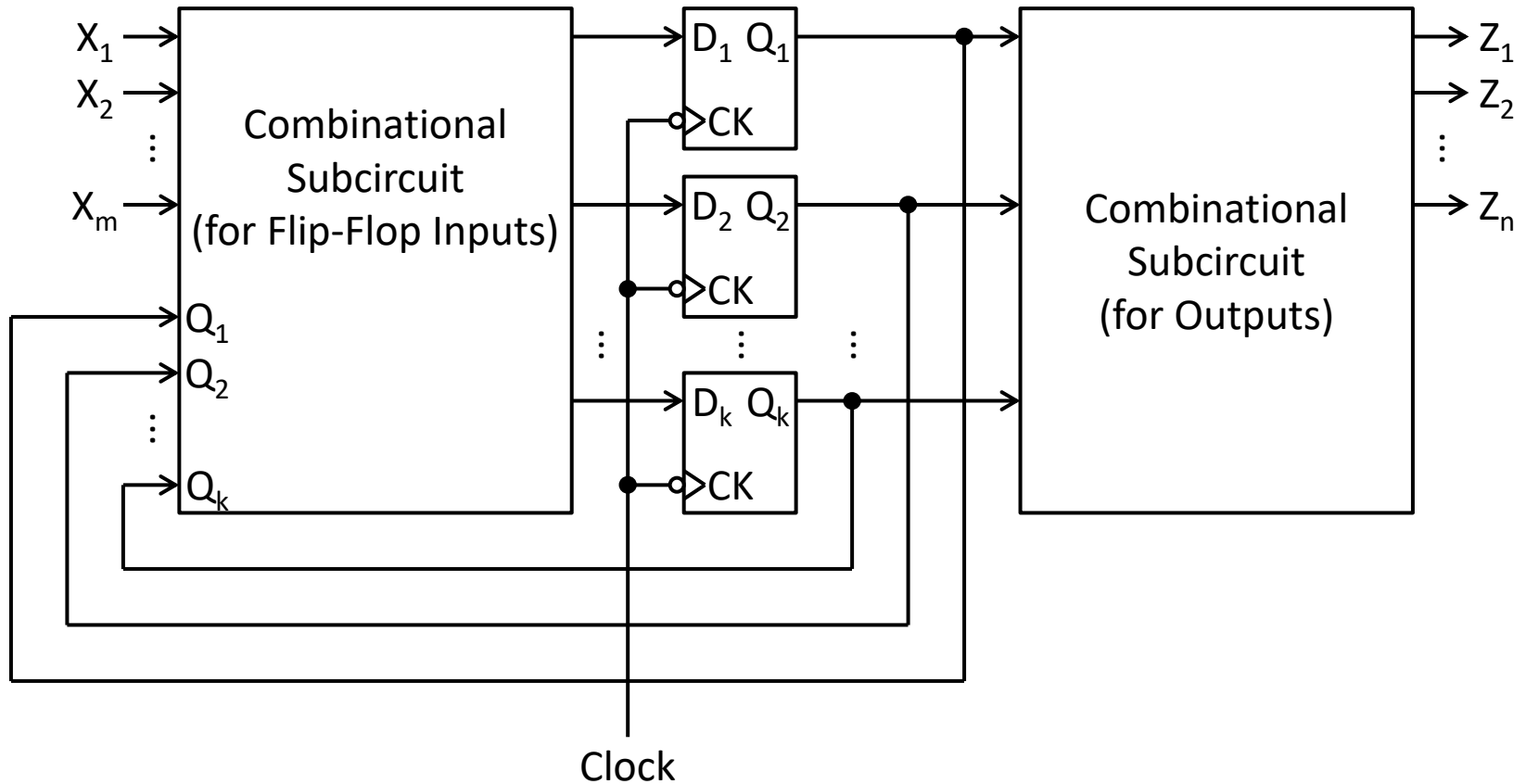| AB	A^+B^+				Z_1Z_2			
	$X_1X_2 = 00$	01	10	11	$X_1X_2 = 00$	01	10	11
S_0	S_3	S_2	S_1	S_0	00	10	11	01
S_1	S_0	S_1	S_2	S_3	10	10	11	11
S_2	S_3	S_0	S_1	S_1	00	10	11	01
S_3	S_2	S_2	S_1	S_0	00	00	01	01

Outline

❑ A Sequential Parity Checker

❑ Analysis by Signal Tracing and Timing Charts

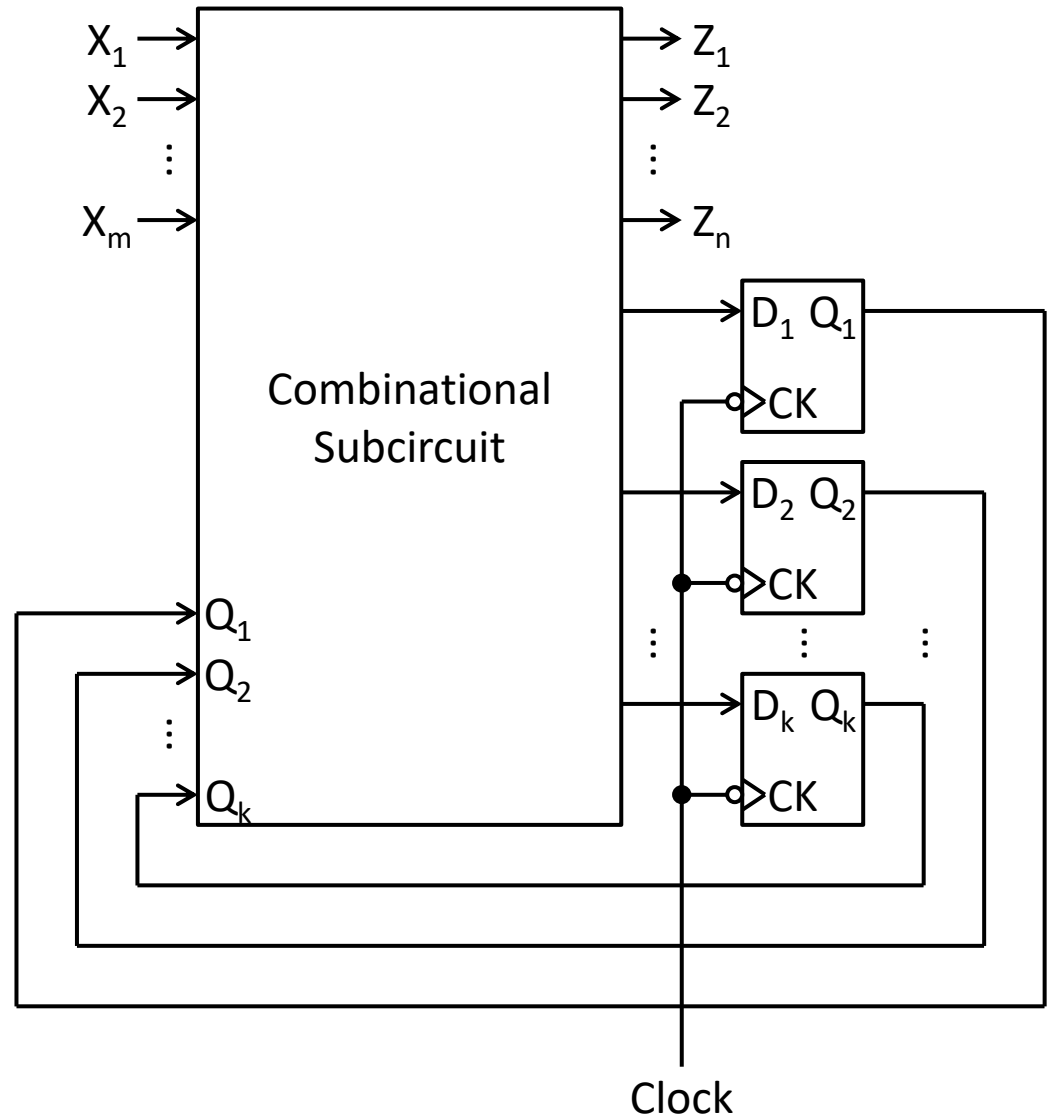❑ State Tables and Graphs

❑ **General Models for Sequential Circuits**

General Model for Moore Machines

❑ An output is a function of only states

General Model for Mealy Machines

❑ An output is a function of states and inputs

$X_1 \rightarrow$

$X_2 \rightarrow$

$\vdots$

$X_m \rightarrow$

Combinational Subcircuit

$\rightarrow Z_1$

$\rightarrow Z_2$

$\vdots$

$\rightarrow Z_n$

$D_1 \; Q_1$

$\triangleright CK$

$D_2 \; Q_2$

$\triangleright CK$

$\vdots$

$D_k \; Q_k$

$\triangleright CK$

Q_1

Q_2

$\vdots$

Q_k

$\vdots$

Clock

Q&A