CSIE 2344, Spring 2024: Midterm Solution Sketch

Name: _____ SID: _____

- Do NOT start when you get the exam sheets — Wait!
- There are 100 points in total.
- You have 120 minutes.
- You should write your answers in the specific areas. If the areas are not enough, you can mention Page 1 and use it.
- You should provide sufficient and clear explanation, except the questions with "no explanation is required" or "only something is required".
- When the exam starts, write down the last three digits of your student ID on the top-right corners of Pages 3 and 5.
- If you want to go to the restroom, turn in the exam sheets and your smart phone.
- Do NOT ask questions in the last 15 minutes
- Do NOT leave your seat in the last 10 minutes.

1 Boolean Algebra (8pts)

Statement: $A + (B \oplus C) = (A + B) \oplus (A + C)$, where $\oplus$ is XOR. Answer if the statement is True or False and then prove it (if True) or find all counterexamples (if False).

Answer: False. When $A = 1$, the statement is false.

2 Application of Boolean Algebra (8pts)

A and B respectively represent the first and second bits of a binary number N_1. For example. $(A, B) = (1, 0)$ represents $N_1 = 2$. C and D respectively represent the first and second bits of a binary number N_2. The Boolean function $F(A, B, C, D) = 1$ if and only if $N_1 \times N_2 \leq 2$. Complete the following truth table. No explanation is required.

Answer:

A	B	C	D	F
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0

A	B	C	D	F
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

3 Two-Level Circuit Conversion (8pts)

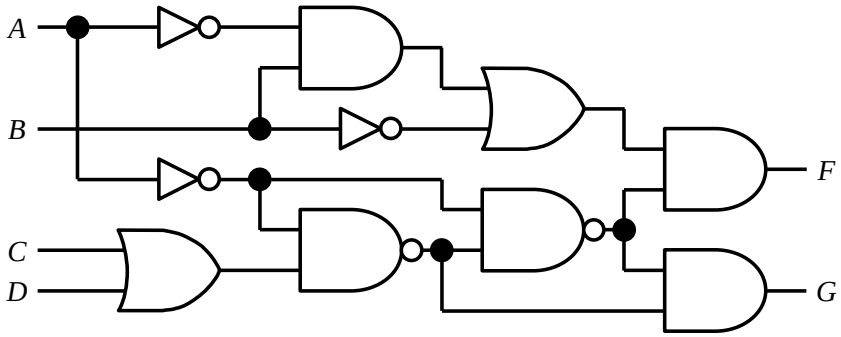
Draw the following two-level gate circuits to realize $F(A, B, C) = A' + BC$. No explanation is required.

1. (2pts) AND-OR	2. (2pts) NAND-NAND
3. (2pts) NOR-OR	4. (2pts) OR-NAND

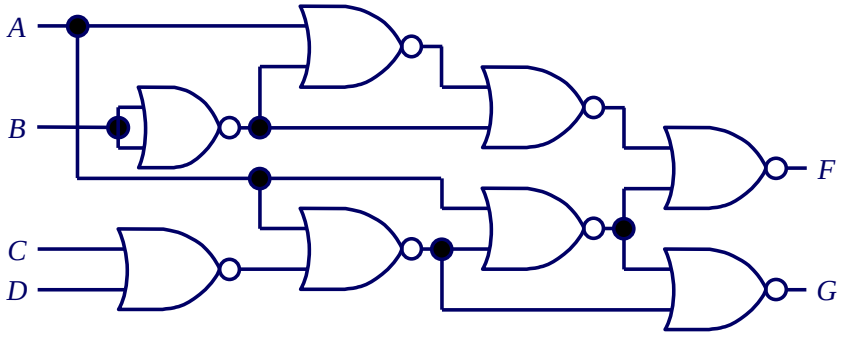
Answer: Omitted.

4 Multi-Level Circuit Conversion (8pts)

Convert the following circuit *directly* (not from a Karnaugh Map) to a four-level circuit containing only NOR gates (NOT gates are not allowed) and circuit inputs A, B, C, D (A', B', C', D' are not allowed as circuit inputs). The number of NOR gates should be 8. No explanation is required.



Answer:



5 Karnaugh Maps and Static Hazards (32pts)

Given Boolean functions $F(A,B,C,D) = \sum m(0,3,9,10,11,15) + \sum d(2,5,7,8)$, $G(A,B,C,D) = AD' + BD$, and $H(A,B,C,D) = \sum m(5,14) + \sum d(7,15)$.

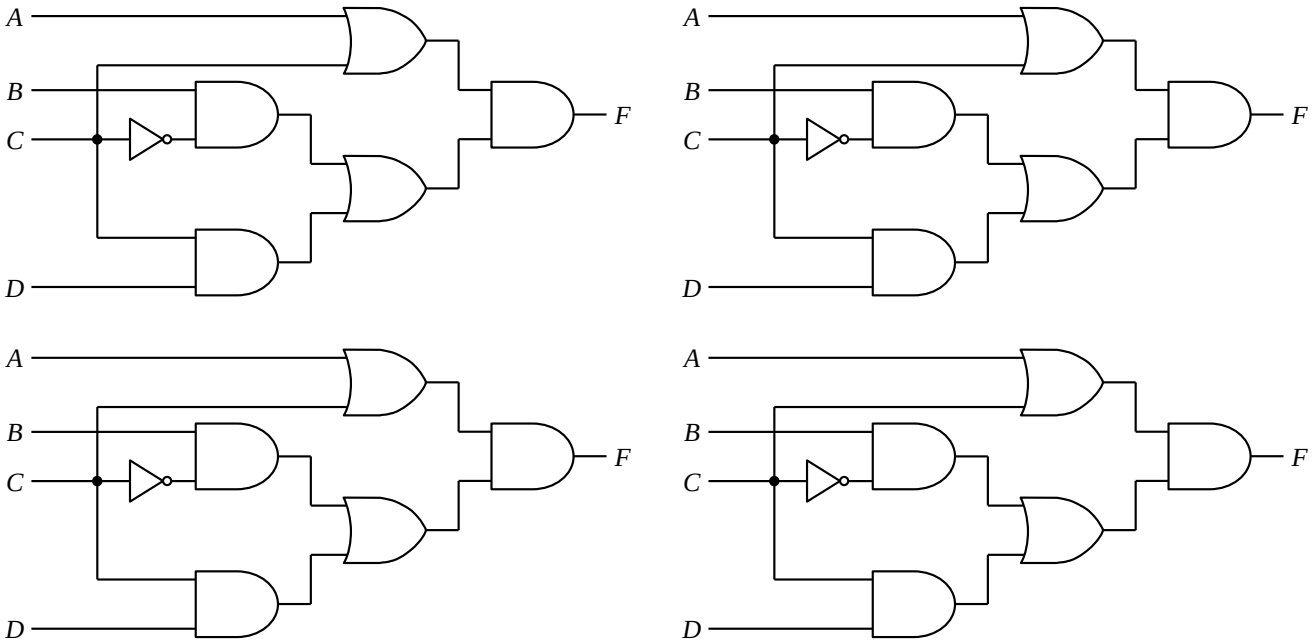
1. (8pts) Find a minimum sum-of-products expression for F. Hazards can be ignored. Only the Karnaugh Map (top left) and the final expression are required.
2. (8pts) Find a minimum product-of-sums expression for F. Hazards can be ignored. Only the Karnaugh Map (top right) and the final expression are required.
3. (8pts) Find a minimum sum-of-products expression for G, where the corresponding gate circuit has no static-1 hazard. Only the Karnaugh Map (bottom left) and the final expression are required.
4. (8pts) Find a minimum sum-of-products expression for H and explain how you consider potential static-1 hazards.

Answer:

1. Use a Karnaugh map to derive $F = AB' + B'D' + CD$.
2. Use a Karnaugh map to derive $F' = BC' + BD' + A'C'D$ and use DeMorgan's Law to derive $F = (B' + C)(B' + D)(A + C + D')$.
3. Use a Karnaugh map to derive $F = AD' + BD + AB$.
4. Use a Karnaugh map to derive $F = ABC + A'BD$, where BCD is not needed as the potential static-1 hazard is don't care.

6 Hazards (16pts)

Assume the propagation delays (including rising and falling delays) of all gates are the same. Find all hazards and the corresponding input changes (for example, (A, B, C, D) changes from 0000 to 0001) in the following circuit. Points will be deducted if (1) not listing a hazard which really happens or (2) listing a hazard which does not really happen. Intermediate progress and explanation are required.



Answer: $F = (BC' + CD)(A + C) = CD + ABC' + BCC'$. Use a Karnaugh map and perform analysis.

- Static-1 hazard: (A, B, C, D) changes from 1111 to 1101. Note that the change from 1101 to 1111 has no dynamic hazard based on the analysis.
- Static-0 hazard: (A, B, C, D) changes from 0100 to 0110. Note that the change from 0110 to 0100 has no dynamic hazard based on the analysis.
- Dynamic hazard: none. Note that (1100,1110) has only one propagation path, and (0101,0111) has no dynamic hazard based on the analysis.

7 True or False (20pts)

Answer "True" (T) or "False" (F) by circling the correct choices. No explanation is required.

T F 1. (2pts) {NOR} is a functional complete set.

T F 2. (2pts) With 3 Boolean variables, $F = \sum m(0, 2, 4, 6)$ if and only if $F' = \prod M(0, 2, 4, 6)$.

T F 3. (2pts) With 3 Boolean variables, $F_1 = \sum m(0, 2, 4, 6)$ and $F_2 = \sum m(4, 5, 6, 7)$ if and only if $F_1 \cdot F_2 = \sum m(4, 6)$.

T F 4. (2pts) The Quine-McCluskey method is a heuristic which cannot return a minimum (optimal) sum-of-products expression.

T F 5. (2pts) With 4 Boolean variables, it is possible to reorder indexes (00-01-11-10 of both sides) in a Karnaugh map so that m_4 is at the bottom-right corner and the Karnaugh map can still work.

T F 6. (2pts) A two-level AND-OR gate circuit (corresponding to a sum-of-products expression) must have no static-0 hazard.

T F 7. (2pts) A two-level AND-OR gate circuit (corresponding to a sum-of-products expression) must have no dynamic hazard.

T F 8. (2pts) With 4 Boolean variables, the number of possible product terms (implicants) is smaller than or equal to 80.

T F 9. (2pts) If the minimum sum-of-products expression for a Boolean function is unique, then all prime implicants in the minimum sum-of-products expression are essential prime implicants.

T F 10. (2pts) If the change from 0 to 1 of one circuit input results in a dynamic hazard, then the change from 1 to 0 of the same circuit input will not result in a dynamic hazard.

Answer: T, T, F, F, T, T, T, F, F, F.

8. It is 3^4.

9. Counterexample: $F(A, B, C, D) = \sum m(0, 4, 5, 11, 13, 15))$.

10. Counterexample: a NOT-XOR-XOR gate circuit, where the circuit input is the gate inputs of the three gates, and a gate output is the gate input of the next gate or the circuit output. An alternative counterexample can have well-designed propagation delays, where the rising and falling delays are different.