Digital Systems Design and Laboratory
[Lab 2. Pipelined Multiplier]

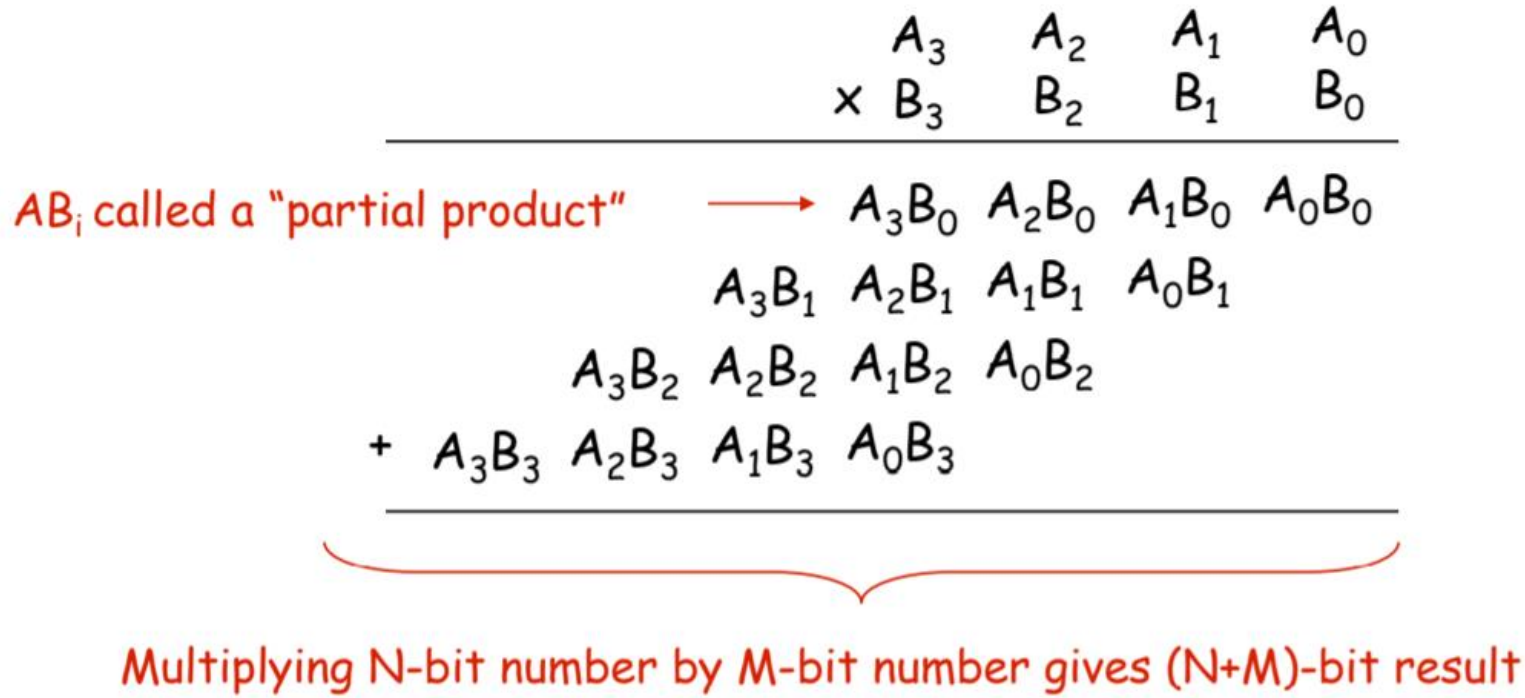
CSIE Department
National Taiwan University

Outline

- **Multiplier**
- Pipeline
- Fast Multiplier
- Assignment
- Appendix

Definition

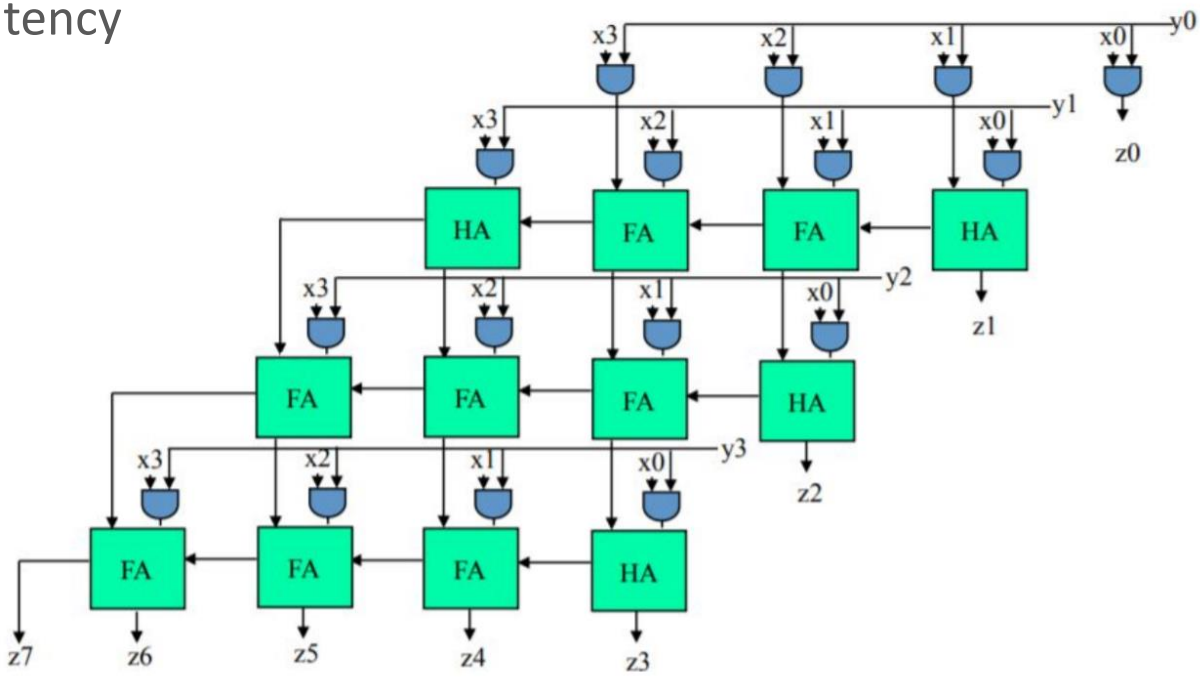
- Unsigned multiplier
  - Multiplicand × Multiplier = Product
  - Signed multipliers will not be covered in Lab 2



http://courses.csail.mit.edu/6.111/f2008/handouts/L09.pdf

Metrics

- For an n-bit × n-bit multiplier
- Latency (longest propagation delay)
  - ≈ 2n*delay(FA)
- Throughput (operations per second)
  - ≈ 1/Latency



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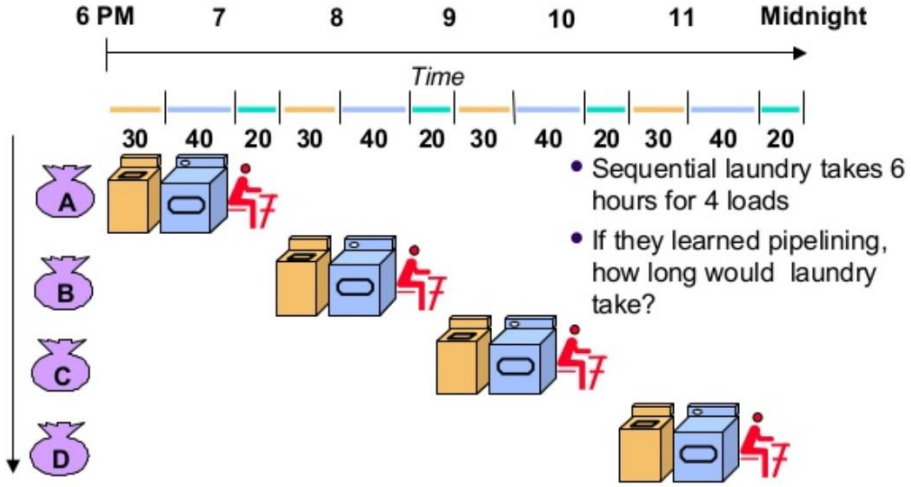
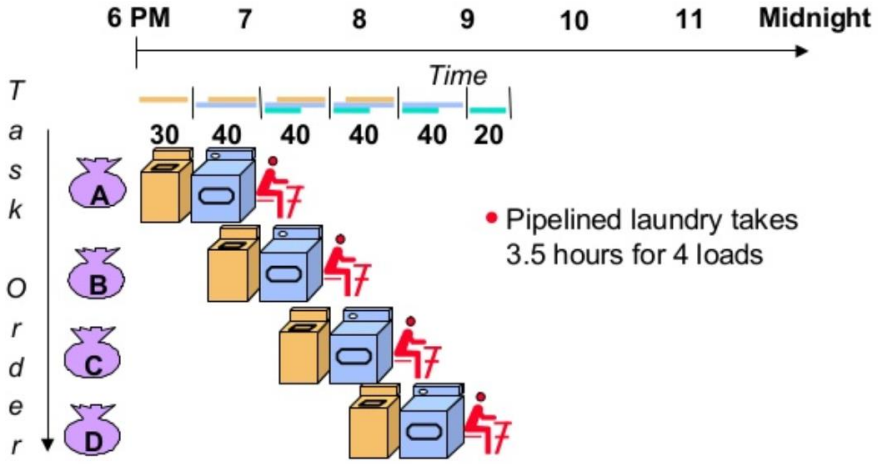
How to Increase Throughput?

- Cut the circuit into different stages
- Do different tasks in each stage at the same time
- Does the latency change? How about the throughput?

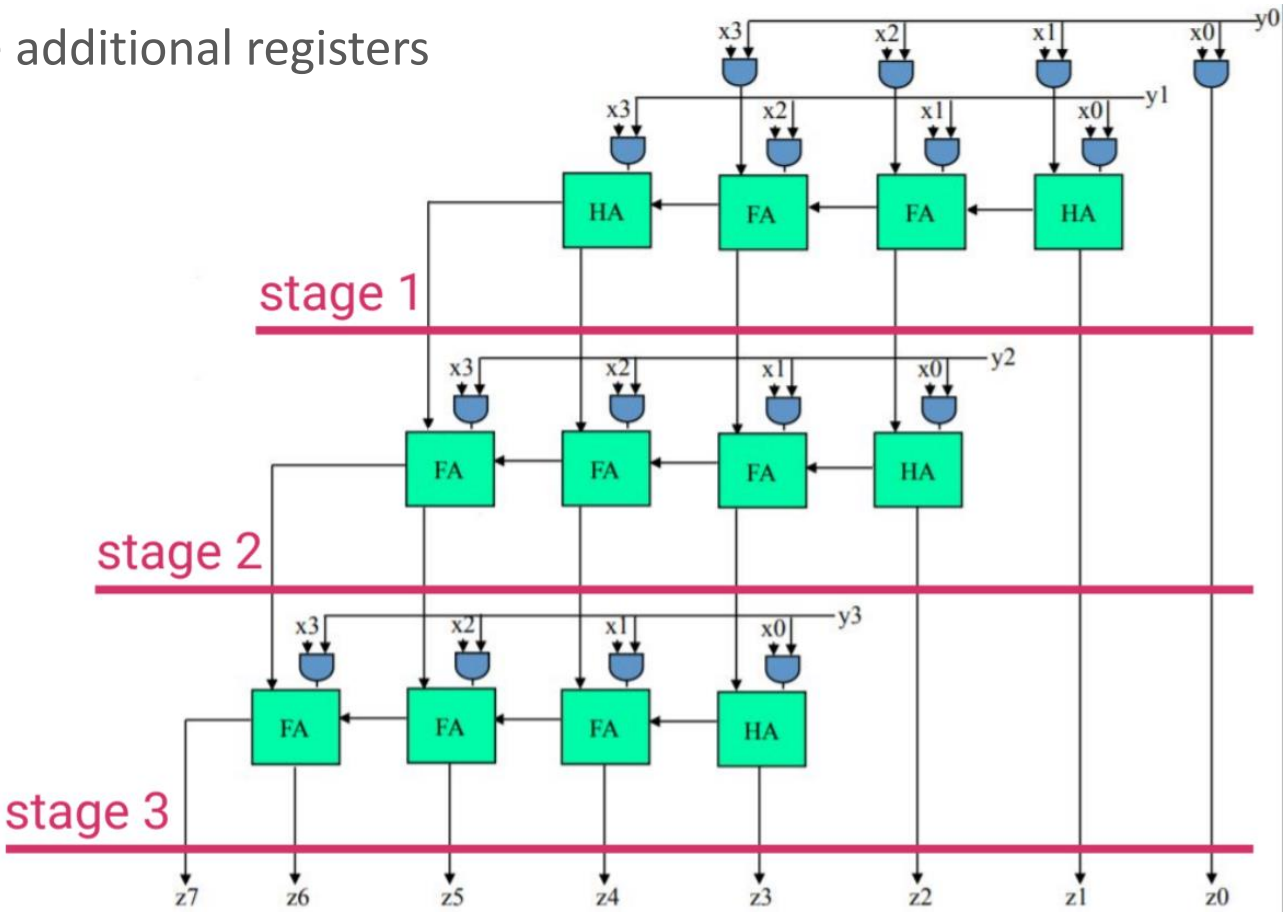




https://www.slideshare.net/siddiqueibrahim37/pipelining-41608675

Pipelined Multiplier

- Add registers at the end of each stage to keep states
- x[3:0] and y[3:0] should also be kept in each stage
  - Use additional registers



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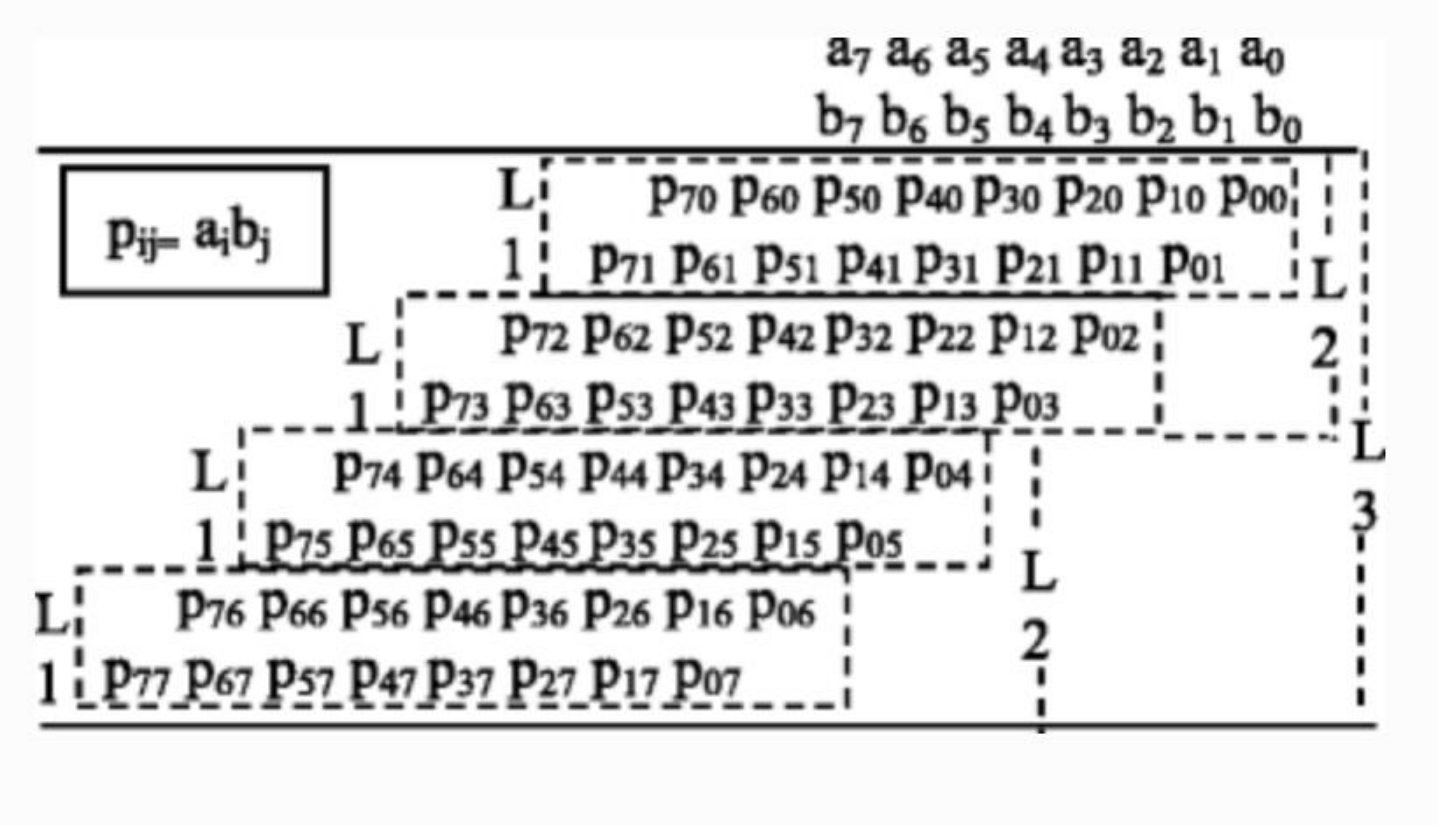
Popular Techniques

- Carry-save adder
- Wallace tree
- High-radix
- And more …

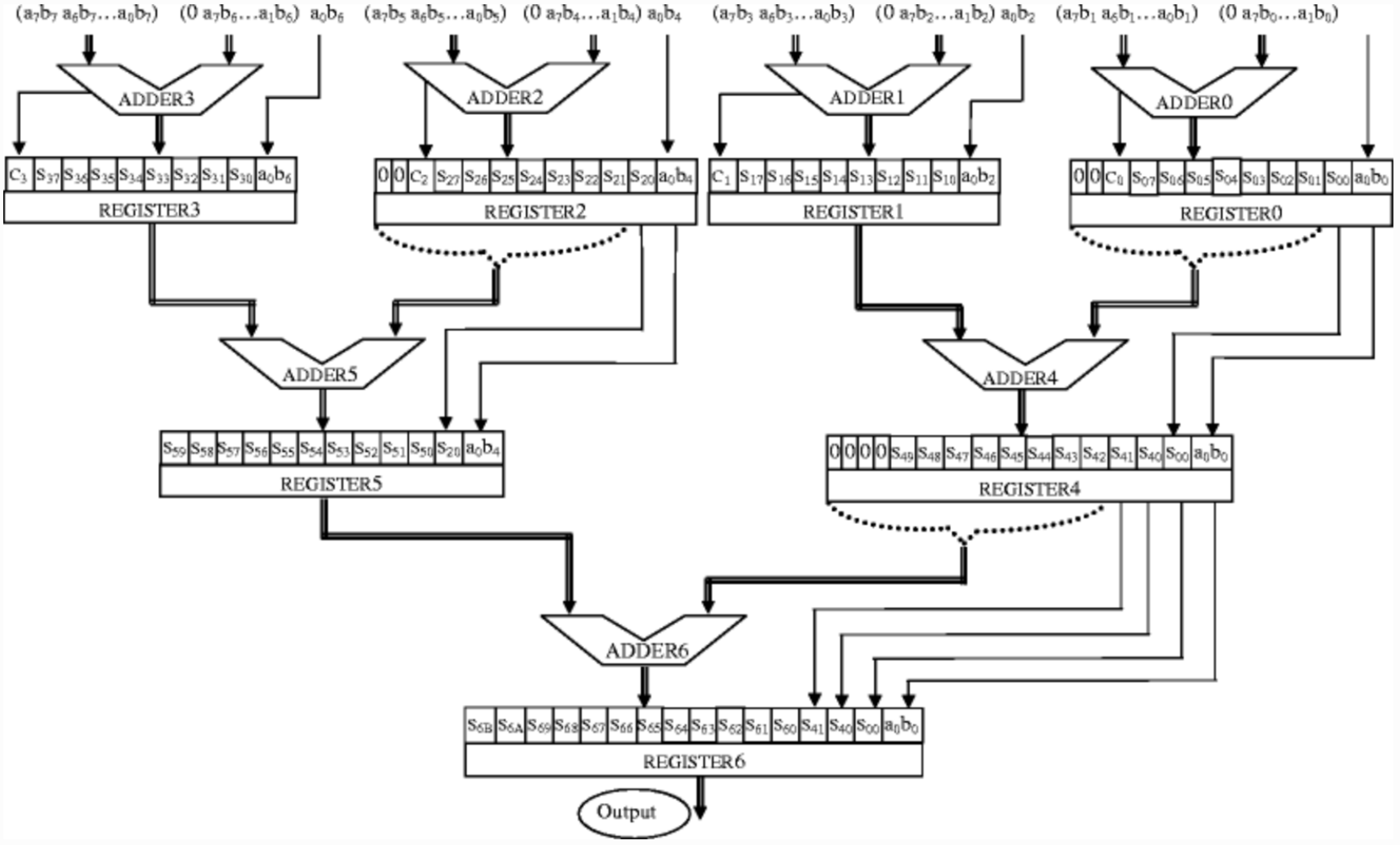
https://www.slideshare.net/siddiqueibrahim37/pipelining-41608675

A Hierarchical Design



https://link.springer.com/article/10.1007/s11265-012-0657-7

A Hierarchical Design



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Execution

- Download the sample code
- Compile
  - `> iverilog -o lab2.vvp lab2.v`
- Simulate
  - `> vvp lab2.vvp`
    - Generates **`lab2.vcd`**
- View waveform
  - `> gtkwave lab2.vcd lab2.sav`

Requirements (1/2)

- Replace **`<index>`** in **`lab2.v`** with proper indexes
  - Leave the rest of the code unchanged
- Show your source code
- Show the waveform with the settings in **`lab2.sav`**
- What is the latency?
  - Worst case waiting time from the input becomes steady to the register of the last stage refreshes
  - Use tick as time unit

Requirements (2/2)

- Minimize the clock cycle by **changing the delays** in the module **`mult_tb`**
  - What is the minimum clock cycle?
    - Use tick as time unit
  - Show the waveform with the settings in **`lab2.sav`**
    - Should include 1750 to 1800 sec

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Multiplier and Pipelining

- Signed multiplier
  - http://courses.csail.mit.edu/6.111/f2008/handouts/L09.pdf
- Details on pipelining
  - https://www.slideshare.net/siddiqueibrahim37/pipelining-41608675
- Details on fast multiplier
  - https://link.springer.com/article/10.1007/s11265-012-0657-7

Some Details on Verilog

- Expression bit width
  - http://yangchangwoo.com/podongii_X2/html/technote/TOOL/MANUAL/21i_doc/data/fndtn/ver/ver4_4.htm
- Event queue
  - Determine the order of different types of assignment
  - http://www.ece.lsu.edu/v/2015/lsli-event-q.pdf
- Transport delay and inertial delay
  - http://www-inst.eecs.berkeley.edu/~cs152/fa06/handouts/CummingsHDLCON1999_BehavioralDelays_Rev1_1.pdf

Q&A