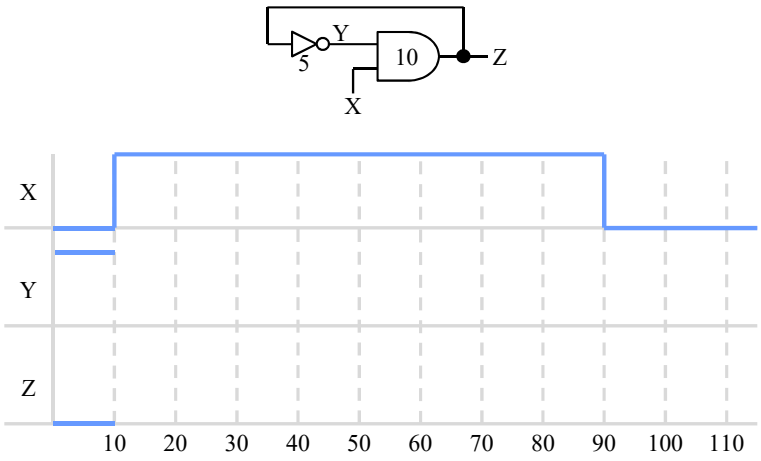
CSIE 2344: Discussion (Unit 11)

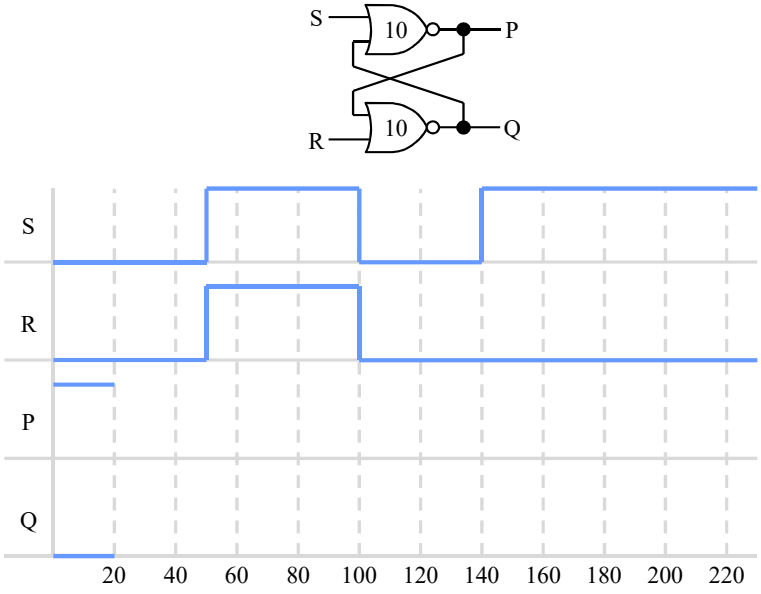
1 Timing Diagram

The numbers are the propagation delays of the gates. Complete the timing diagram below.



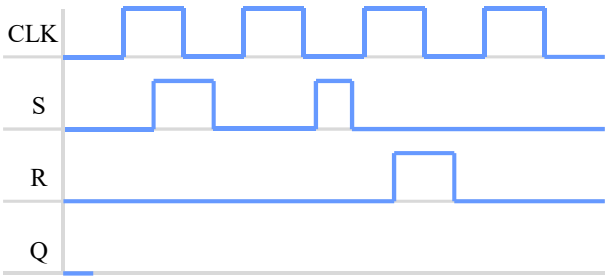
2 S-R Latch

This problem illustrates the improper operation that can occur if both inputs to an S-R latch are 1 and are then changed back to 0. The numbers are the propagation delays of the gates.

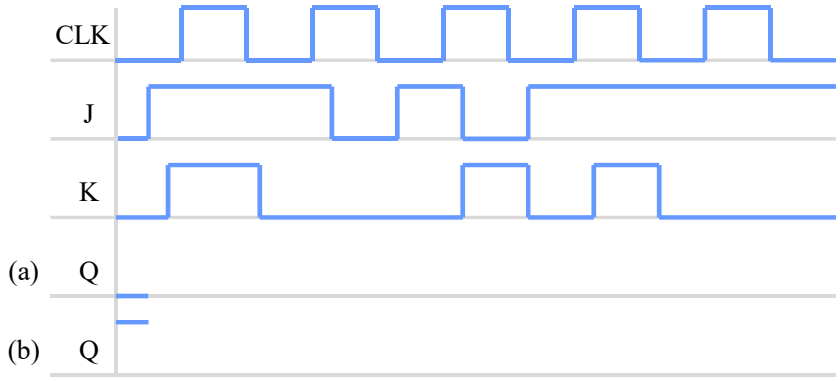


3 Flip-Flops

1. Fill in the timing diagram for a falling-edge-triggered S-R flip-flop.



2. Fill in the timing diagram for a falling-edge-triggered J-K flip-flop. (a) Assume Q begins at 0. (b) Assume Q begins at 1.



3. Find the input and fill in the timing diagram for a rising-edge-triggered (a) D flip-flop and (b) T flip-flop that would produce the output Q as shown.