CSIE 2344: Homework 3

Due April 29 (Monday) at Noon

There are 90 points in total. Points will be deducted if no appropriate intermediate step is provided.

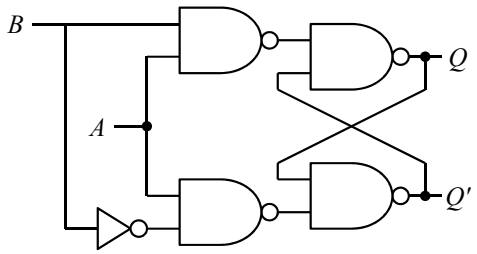
When you submit your homework on Gradescope, please select the corresponding page(s) of each question.

1 MUXes and Three-State Buffers (8pts)

Show how to make an 8-to-1 MUX using two 4-to-1 MUXes, two three-state buffers, and one inverter.

2 Latch I (8pts)

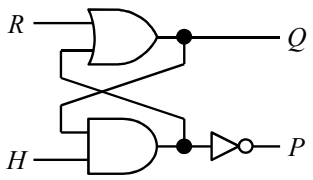
Given the latch as below, complete the following truth table.



A	B	Q	Q^+
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

3 Latch II (16pts)

A latch can be constructed from an OR gate, an AND gate, and an inverter connected as below.



1. What restriction must be placed on R and H so that P will always equal Q' (under steady-state conditions)?
2. Construct a next-state table and derive the minimum characteristic (next-state) equation for the latch.

4 Lab 1: Source Code (28pts)

1. (16pts) Print out your `cla_gl` source code and attach it with your Homework 3.
2. (12pts) Print out your `rca_gl` source code and attach it with your Homework 3.

We may ask you to demo in the future. Points will be deducted if your demo fails. **You can only demo with the source code same as that you submit**.

5 Lab 1: Waveform (12pts)

Show the waveform of `cla_gl` on input transition from $000 + 000 + 0$ to $000 + 111 + 1$. You should select all the input and output signals of `cla_gl` module.

6 Lab 1: Propagation Delays (8pts)

1. (4pts) Find the maximum propagation delay of `rca_gl` and one of the corresponding input transitions.
2. (4pts) Find the maximum propagation delay of `cla_gl` and one of the corresponding input transitions.

7 Lab 1: Some Derivation (10pts)

Assume that only 2-input gates are used. Derive the number of levels needed in an n-bit carry-lookahead adder as a function of n.