Digital Systems Design and Laboratory
[16. Sequential Circuit Design]

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Sequential Logic Design

- Unit 11: Latches and Flip-Flops
- Unit 12: Registers and Counters
- Units 13--15: Finite State Machines
- Unit 16: Summary

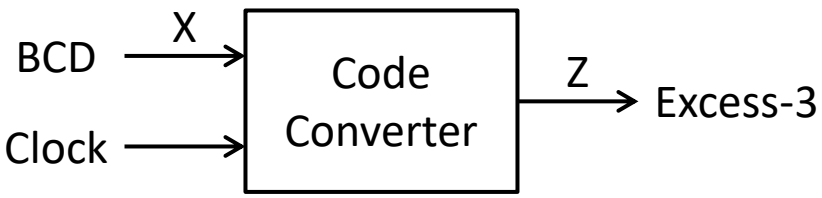
- Designing a sequential circuit
  - Construct a state graph or state table (Unit 14)
  - Simplify it (Unit 15)
  - Derive flip-flop input equations and output equations (Unit 12)

Outline

- **Design Example --- Code Converter**
- Design of Iterative Circuits
- Summary

BCD to Excess-3 Conversion

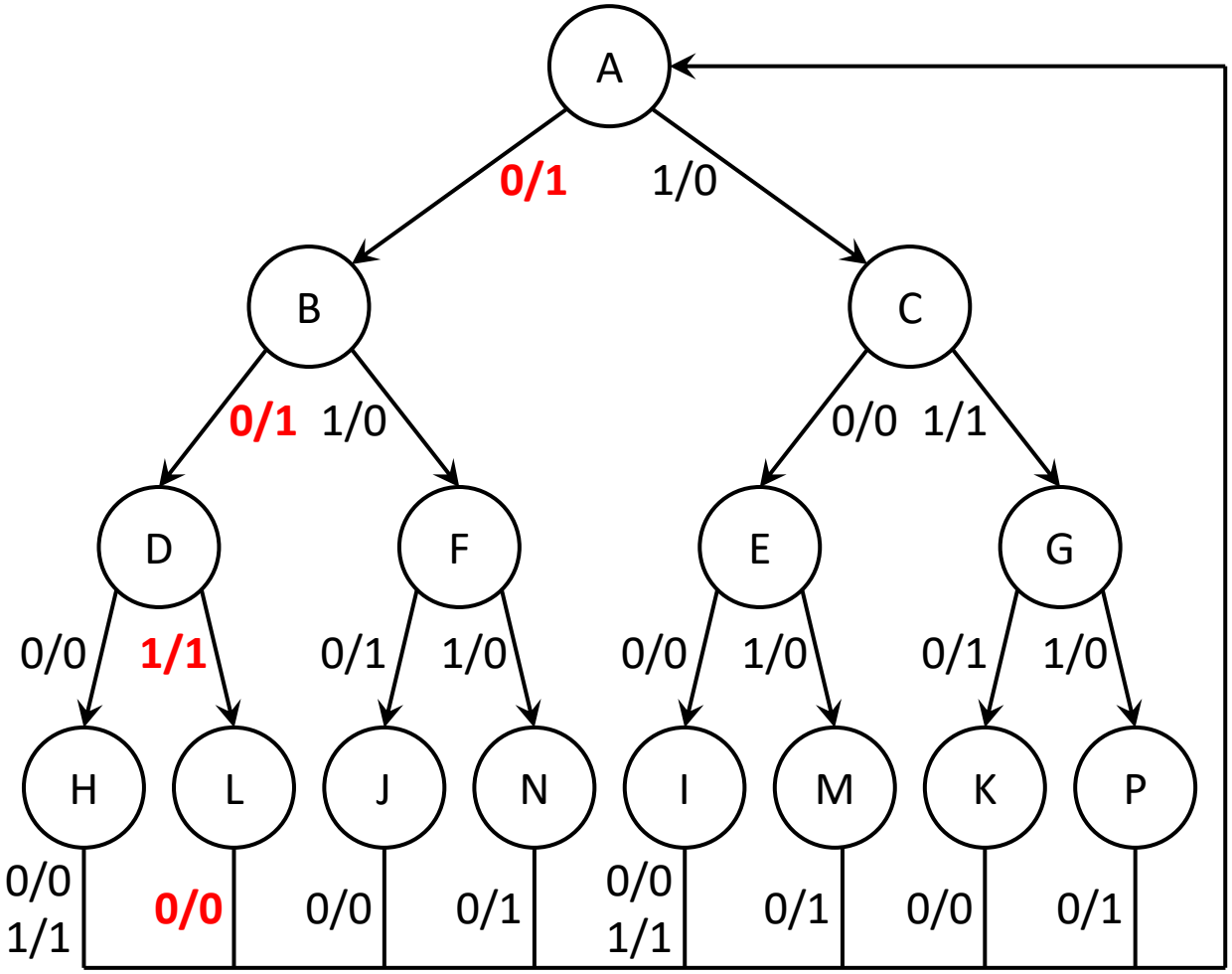
- Add 3 to BCD (0--9)
- Serial I/O with the LSB first
  - $X_0 \rightarrow X_1 \rightarrow X_2 \rightarrow X_3$
  - $Z_0 \rightarrow Z_1 \rightarrow Z_2 \rightarrow Z_3$
- Reset to initial state after receiving 4 inputs



X Input (BCD)	Z Output (Excess-3)
$t_3\,t_2\,t_1\,t_0$	$t_3\,t_2\,t_1\,t_0$
0 0 0 0	0 0 1 1
0 0 0 1	0 1 0 0
0 0 1 0	0 1 0 1
0 0 1 1	0 1 1 0
0 1 0 0	0 1 1 1
0 1 0 1	1 0 0 0
0 1 1 0	1 0 0 1
0 1 1 1	1 0 1 0
1 0 0 0	1 0 1 1
1 0 0 1	1 1 0 0
Others	X X X X

State Graph

X	Z
$t_3 t_2 t_1 t_0$	$t_3 t_2 t_1 t_0$
0 0 0 0	0 0 1 1
0 0 0 1	0 1 0 0
0 0 1 0	0 1 0 1
0 0 1 1	0 1 1 0
0 1 0 0	**0 1 1 1**
0 1 0 1	1 0 0 0
0 1 1 0	1 0 0 1
0 1 1 1	1 0 1 0
1 0 0 0	1 0 1 1
1 0 0 1	1 1 0 0
Others	X X X X



State Table

Time	Input Sequence	Present State	Next State		Present Output	
			X = 0	X = 1	X = 0	X = 1
t_0	Reset	A	B	C	1	0
t_1	0_{LSB}	B	D	F	1	0
	1_{LSB}	C	E	G	0	1
t_2	00_{LSB}	D	H	L	0	1
	01_{LSB}	E	I	M	1	0
	10_{LSB}	F	J	N	1	0
	11_{LSB}	G	K	P	1	0
t_3	000_{LSB}	H	A	A	0	1
	001_{LSB}	I	A	A	0	1
	010_{LSB}	J	A	-	0	-
	011_{LSB}	K	A	-	0	-
	100_{LSB}	L	A	-	0	-
	101_{LSB}	M	A	-	1	-
	110_{LSB}	N	A	-	1	-
	111_{LSB}	P	A	-	1	-

State Reduction (1/3)

- Row matching
  - $M \equiv N \equiv P$
  - $H \equiv I \equiv J \equiv K \equiv L$
    - Use don't cares

Time	Input Sequence	Present State	Next State		Present Output	
			X = 0	X = 1	X = 0	X = 1
t_0	Reset	A	B	C	1	0
t_1	0_{LSB}	B	D	F	1	0
	1_{LSB}	C	E	G	0	1
t_2	00_{LSB}	D	H	L → **H**	0	1
	01_{LSB}	E	I → **H**	M	1	0
	10_{LSB}	F	J → **H**	N → **M**	1	0
	11_{LSB}	G	K → **H**	P → **M**	1	0
t_3	000_{LSB}	H	A	A	0	1
	001_{LSB}	I	A	A	0	1
	010_{LSB}	J	A	-	0	-
	011_{LSB}	K	A	-	0	-
	100_{LSB}	L	A	-	0	-
	101_{LSB}	M	A	-	1	-
	110_{LSB}	N	A	-	1	-
	111_{LSB}	P	A	-	1	-

State Reduction (2/3)

- Row matching
  - E ≡ F ≡ G

Time	Input Sequence	Present State	Next State		Present Output	
			X = 0	X = 1	X = 0	X = 1
t_0	Reset	A	B	C	1	0
t_1	0_{LSB}	B	D	F → **E**	1	0
	1_{LSB}	C	E	G → **E**	0	1
t_2	00_{LSB}	D	H	H	0	1
	01_{LSB}	E	H	M	1	0
	10_{LSB}	F	H	M	1	0
	11_{LSB}	G	H	M	1	0
t_3	000_{LSB}	H	A	A	0	1
	001_{LSB}	I	A	A	0	1
	010_{LSB}	J	A	-	0	-
	011_{LSB}	K	A	-	0	-
	100_{LSB}	L	A	-	0	-
	101_{LSB}	M	A	-	1	-
	110_{LSB}	N	A	-	1	-
	111_{LSB}	P	A	-	1	-

State Reduction (3/3)

- 7 states

Time	Present State	Next State		Present Output	
		X = 0	X = 1	X = 0	X = 1
t_0	A	B	C	1	0
t_1	B	D	E	1	0
	C	E	E	0	1
t_2	D	H	H	0	1
	E	H	M	1	0
t_3	H	A	A	0	1
	M	A	-	1	-

State Assignment

- To simplify the next state functions
  - (B,C), (D,E), (H,M) should be adjacent
- To simplify the output functions
  - (A,B,E,M), (C,D,H) should be adjacent

Q_2Q_3 \ Q_1	0	1
00	A	B
01		C
11	H	D
10	M	E

Time	Present State	Next State		Present Output	
		X = 0	X = 1	X = 0	X = 1
t_0	A	B	C	1	0
t_1	B	D	E	1	0
	C	E	E	0	1
t_2	D	H	H	0	1
	E	H	M	1	0
t_3	H	A	A	0	1
	M	A	-	1	-

	$Q_1Q_2Q_3$	Next State		Present Output	
		X = 0	X = 1	X = 0	X = 1
A	0 0 0	1 0 0	1 0 1	1	0
B	1 0 0	1 1 1	1 1 0	1	0
C	1 0 1	1 1 0	1 1 0	0	1
D	1 1 1	0 1 1	0 1 1	0	1
E	1 1 0	0 1 1	0 1 0	1	0
H	0 1 1	0 0 0	0 0 0	0	1
M	0 1 0	0 0 0	X X X	1	X
-	0 0 1	X X X	X X X	X	X

Choose Flip-Flops and Derive Equations

- Choose D flip-flops
- Derive flip-flop input & output equations (by K-maps)
  - $D_1 = Q_1^+ = Q_2'$
  - $D_2 = Q_2^+ = Q_1$
  - $D_3 = Q_3^+ = Q_1Q_2Q_3 + X'Q_1Q_3' + XQ_1'Q_2'$
  - $Z = X'Q_3' + XQ_3$

	$Q_1Q_2Q_3$	Next State		Present Output	
		X = 0	X = 1	X = 0	X = 1
A	0 0 0	1 0 0	1 0 1	1	0
B	1 0 0	1 1 1	1 1 0	1	0
C	1 0 1	1 1 0	1 1 0	0	1
D	1 1 1	0 1 1	0 1 1	0	1
E	1 1 0	0 1 1	0 1 0	1	0
H	0 1 1	0 0 0	0 0 0	0	1
M	0 1 0	0 0 0	X X X	1	X
-	0 0 1	X X X	X X X	X	X

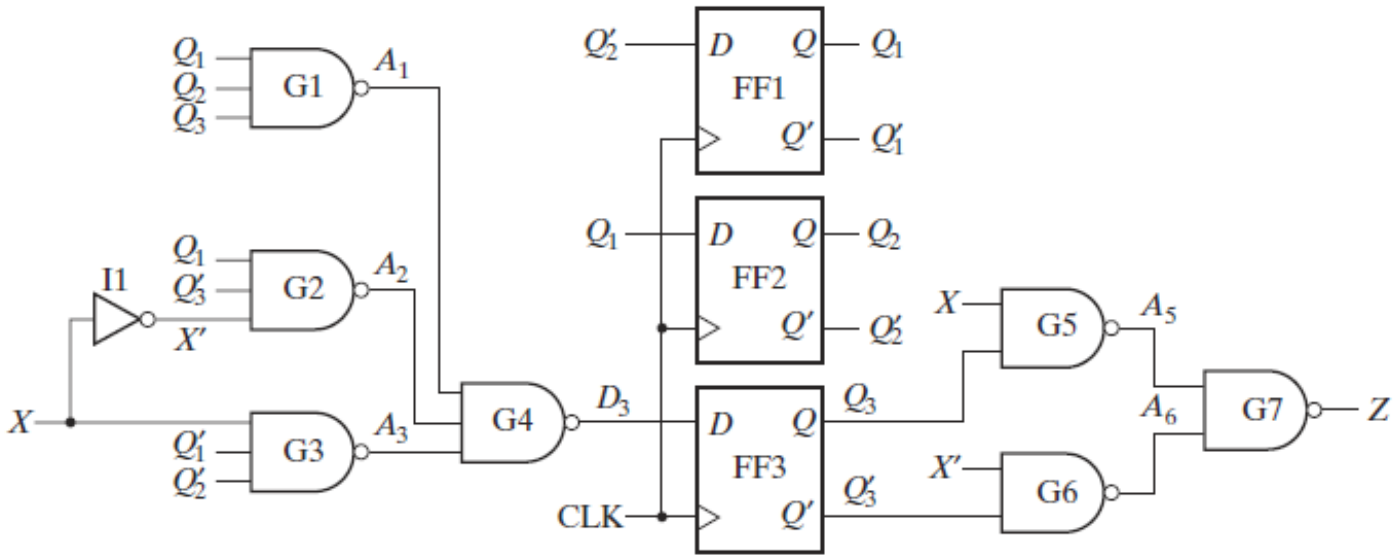
Q_2Q_3 \ Q_1	0	1
00	A	B
01		C
11	H	D
10	M	E

Q_2Q_3 \ XQ_1	00	01	11	10
00	1	1	0	0
01	X	0	1	X
11	0	0	1	1
10	1	1	0	X

Z

Circuit Realization

FIGURE 16-4
Code Converter Circuit

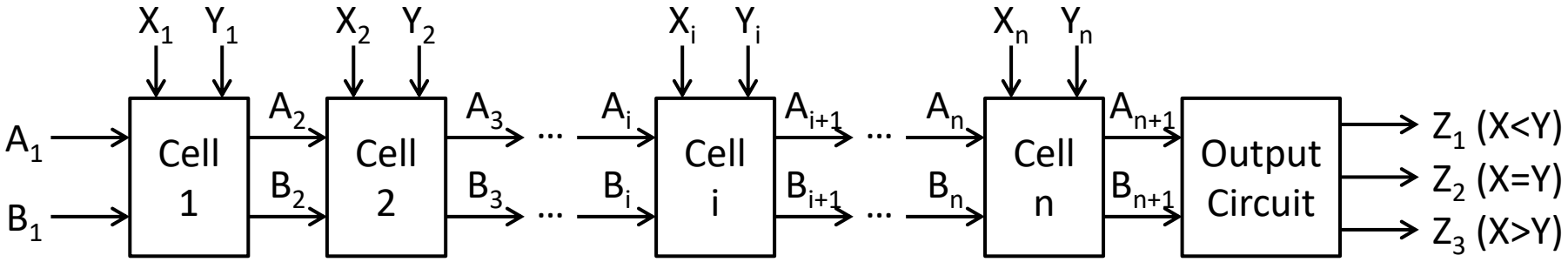


Outline

- Design Example --- Code Converter
- **Design of Iterative Circuits**
- Summary

Sequential Comparator

- **Iterative circuit** for comparing binary numbers
  - $X = X_1X_2X_3\ldots X_n$
  - $Y = Y_1Y_2Y_3\ldots Y_n$
  - Time: $t_1t_2t_3\ldots t_n$
  - X_1 and Y_1: most significant bits



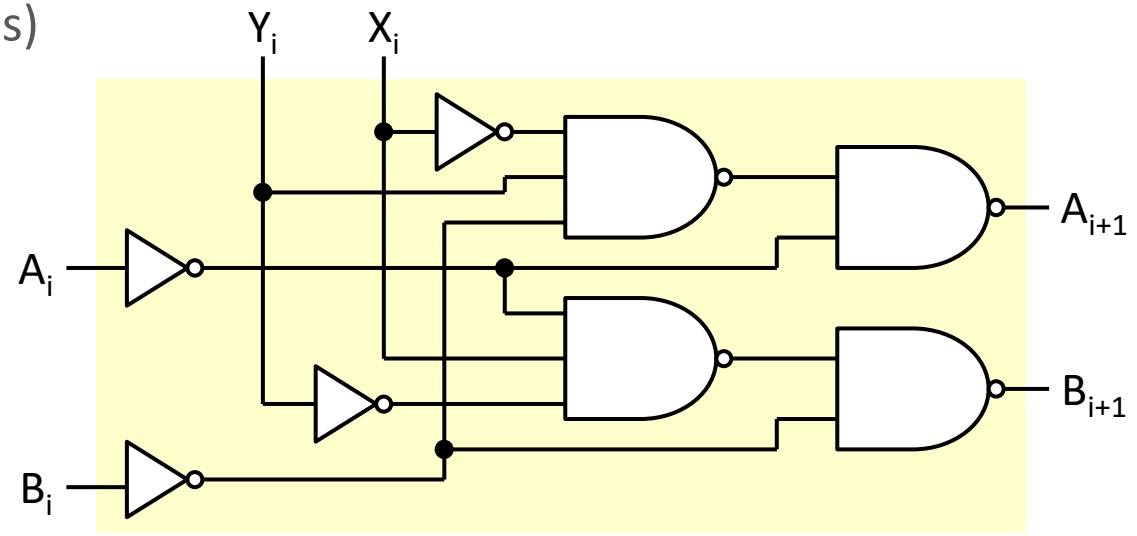
State Table and State Assignment

Present State	Next State				Output		
	X_iY_i = 00	01	11	10	Z_1	Z_2	Z_3
(X=Y) S_0	S_0	S_2	S_0	S_1	0	1	0
(X>Y) S_1	S_1	S_1	S_1	S_1	0	0	1
(X<Y) S_2	S_2	S_2	S_2	S_2	1	0	0

A_iB_i	$A_{i+1}B_{i+1}$				Output		
	X_iY_i = 00	01	11	10	Z_1	Z_2	Z_3
(X=Y) S_0	00	10	00	01	0	1	0
(X>Y) S_1	01	01	01	01	0	0	1
(X<Y) S_2	10	10	10	10	1	0	0

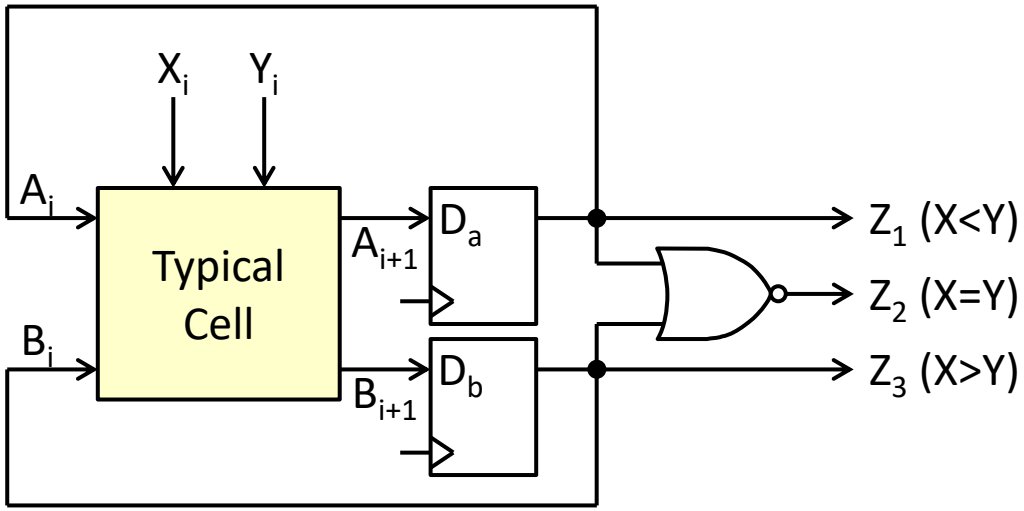
Choose Flip-Flops and Derive Equations

- Choose D flip-flops
- Derive flip-flop input equations and output equations
  - (By the Karnaugh maps)
  - $A_{i+1} = A_i + X_i'Y_iB_i'$
  - $B_{i+1} = B_i + X_iY_i'A_i'$
- Output circuit
  - $Z_1 = A_{n+1}$
  - $Z_2 = A'_{n+1}B'_{n+1}$
  - $Z_3 = B_{n+1}$



Typical Cell

Circuit Realization



Outline

- Design Example --- Code Converter
- Design of Iterative Circuits
- **Summary**

Summary

- Problem statement
- "Initial" state graph and table generation
  - Unit 14
- State reduction
  - Unit 15
- State assignment
  - Unit 15
- Choice of flip-flops
  - Unit 11
- Derivation of flip-flop input equations and output equations
  - Unit 12
- Circuit realization and timing chart

Q&A