Digital Systems Design and Laboratory
[11. Latches and Flip-Flops]

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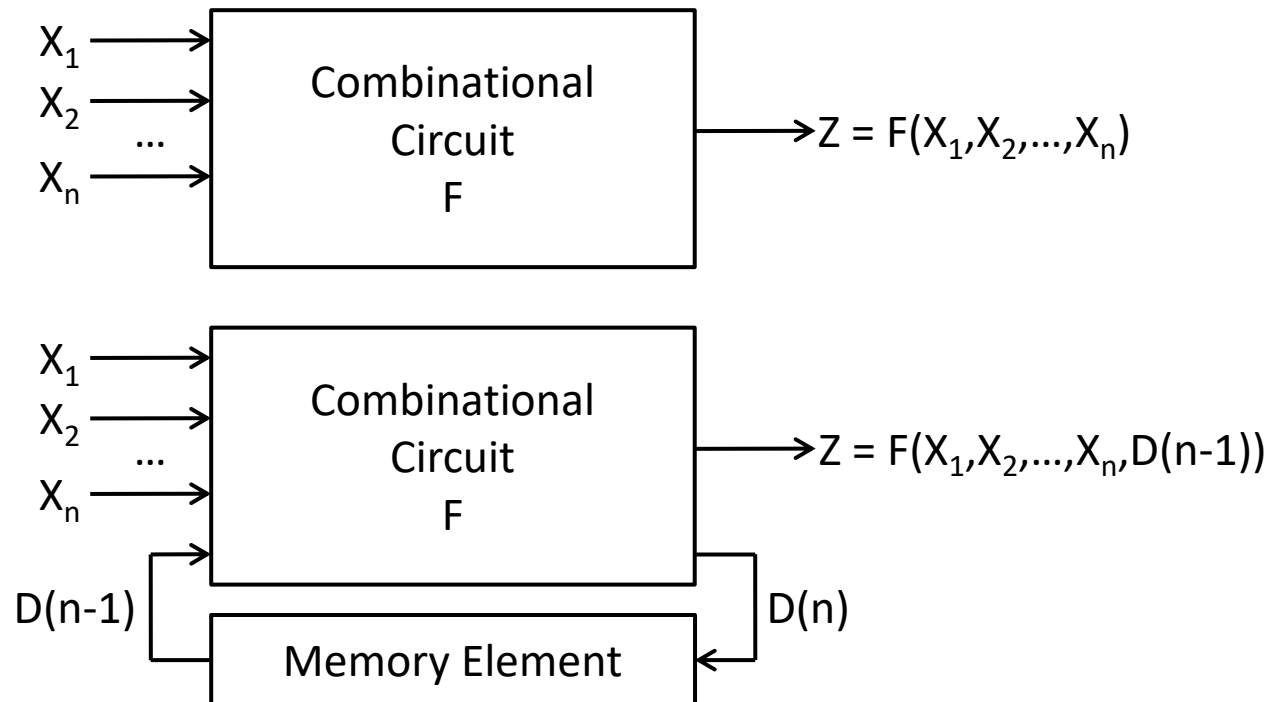
Recap: Two Types of Switching Circuits

❑ Combinational circuits (memoryless)

  ➢ Outputs depend only on **present** inputs

❑ Sequential circuits

  ➢ Outputs depend on both **present and past** inputs

  ➢ In general, sequential circuits = combinational circuits + memory

X_1, X_2, ..., X_n → Combinational Circuit F → $Z = F(X_1, X_2, ..., X_n)$

X_1, X_2, ..., X_n → Combinational Circuit F → $Z = F(X_1, X_2, ..., X_n, D(n-1))$
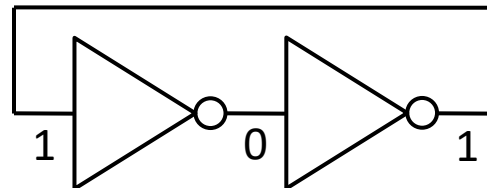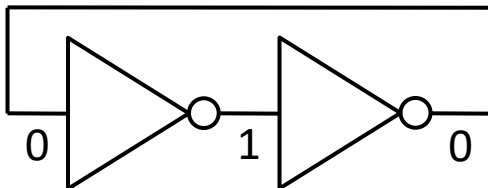
$D(n-1)$ Memory Element $D(n)$
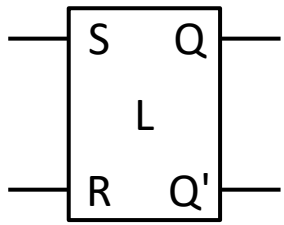
How to Remember the Past?

❑ **Feedback**

➢ The output of one of the gates is connected back into the input of another gate in the circuit so as to form a closed loop

➢ Example: inverter with feedback

- Q: How fast does the circuit oscillate?

- A: Determined by the propagation delay of the inverter

Oscillation at Inverter Output
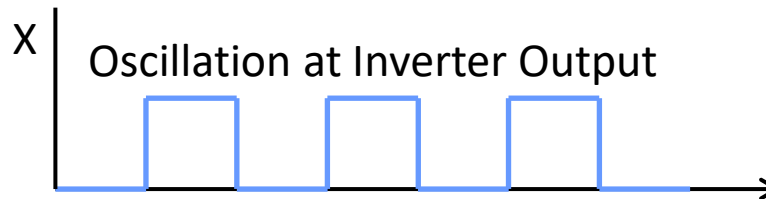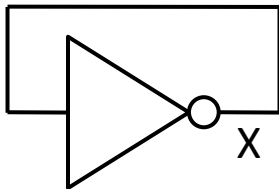
➢ Example: a feedback loop with two inverters

- Two stable states

- Latch: basic memory unit (store 1 bit)

Outline

Set-Reset (S-R) Latch (1/2)

P = 1
S = 0
R = 0
Q = 0   Stable

P = 0
S = 1
R = 0
Q = 1   Stable

P = 0
S = 0
R = 0
Q = 1   Stable

P = 1
S = 0
R = 1
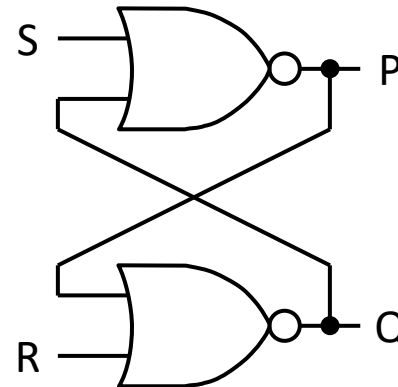Q = 0   Stable
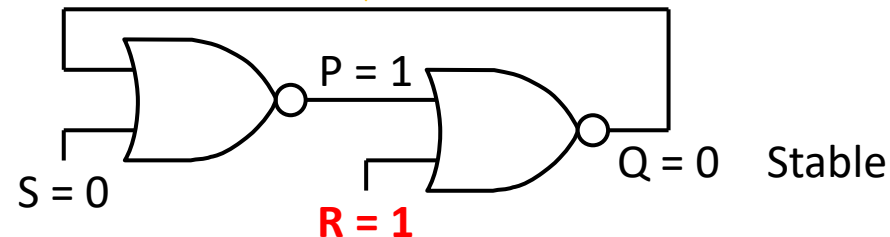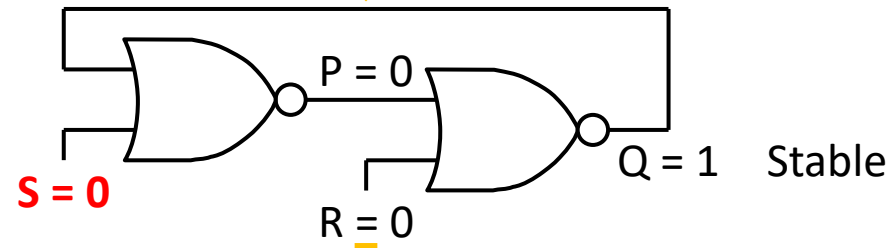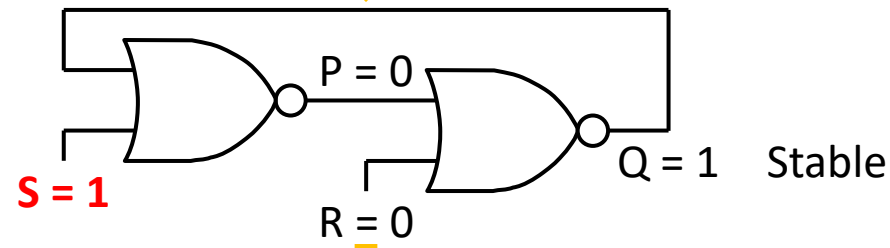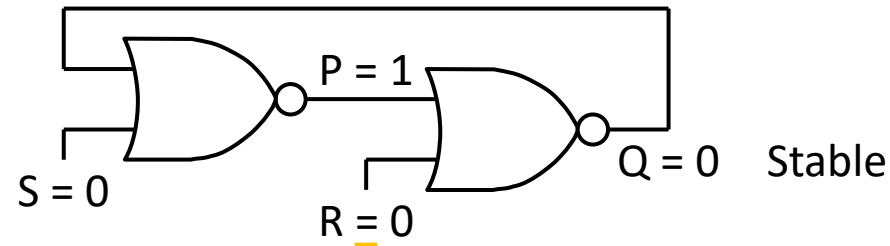
Set-Reset (S-R) Latch (2/2)

❑ Cross-coupled form
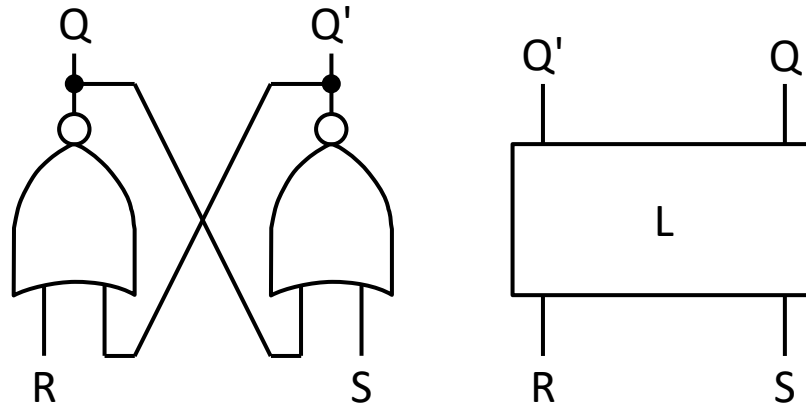
❑ S = R = 1 not allowed!

➢ Note that the outputs are Q and Q'

➢ An oscillation scenario

• Both S and R: 1 → 0

• Both P and Q: 0 → 1 → 0 → 1

– If the gate delays are equal

Next-State (Characteristic) Equation

❏ Operation

S	R	Q	Q$^+$
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	X
1	1	1	X

Unchanged

Reset to 0

Set to 1

Inputs Not Allowed

| RQ \ S	0	1
00	0	1
01	1	1
11	0	X
10	0	X

$$Q^+ = S + R'Q$$

Application: Switch Debouncing

❑ When a mechanical switch is opened or closed, switch contacts tend to vibrate before settling down

❑ Debounce with S-R latch

➢ When the switch is flipped from a to b…

➢ Work only with a "double throw" switch

- Double throw: switch between two contacts
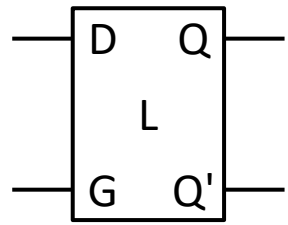- Single throw: switch between one contact and open
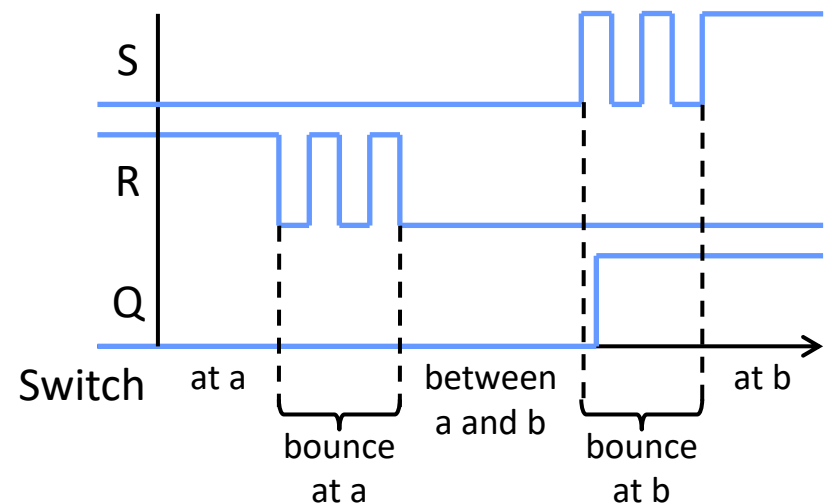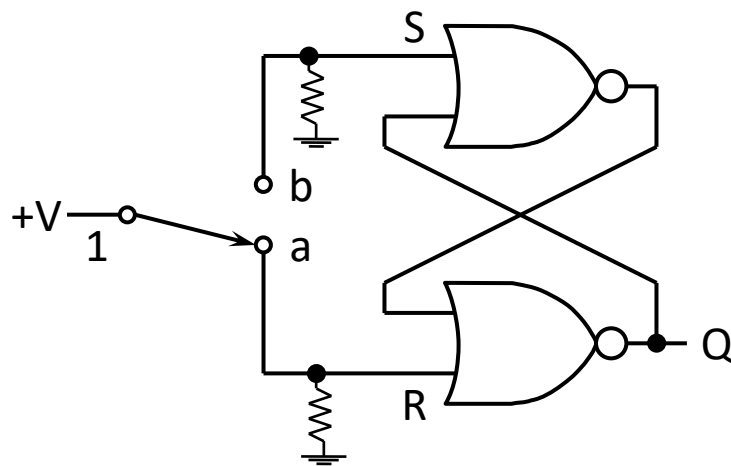
Alternative Form with NAND-Gates

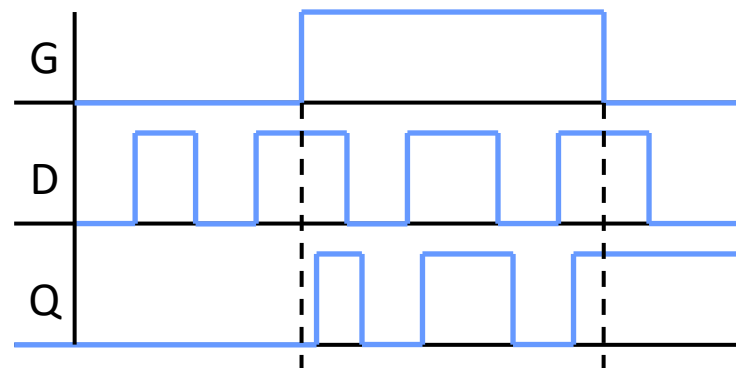❏ $\overline{S}$-$\overline{R}$ latch: active-low inputs for S & R
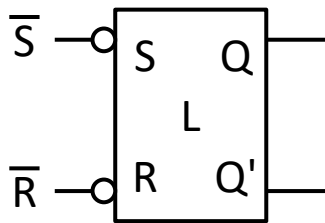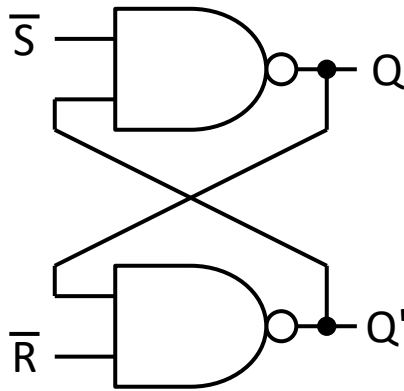
$\overline{S}$	$\overline{R}$	Q	Q^+	
1	1	0	0	Unchanged
1	1	1	1	
1	0	0	0	Reset to 0
1	0	1	0	
0	1	0	1	Set to 1
0	1	1	1	
0	0	0	X	Inputs Not Allowed
0	0	1	X	

Outline

□ Set-Reset Latch

□ **Gated D Latch**

□ Edge-Triggered D Flip-Flop

□ S-R Flip-Flop

□ J-K Flip-Flop

□ T Flip-Flop

□ Flip-Flops with Additional Inputs

Gated D Latch
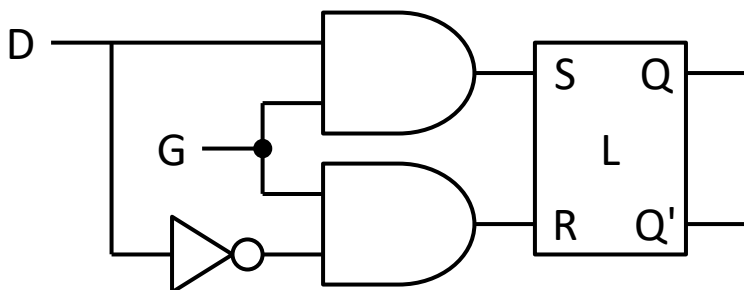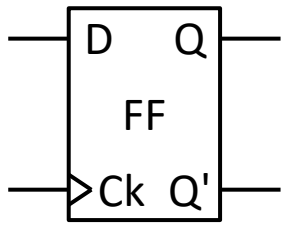
G	D	Q	Q⁺
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

Unchanged
$Q^+ = Q$

$Q^+ = D$

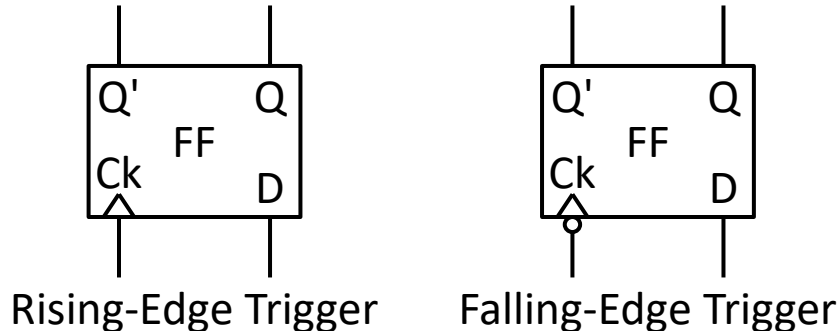| DQ \ G	0	1
00	0	0
01	1	0
11	1	1
10	0	1

$Q^+ = G'Q + GD$

Outline

□ Set-Reset Latch

□ Gated D Latch

□ **Edge-Triggered D Flip-Flop**

□ S-R Flip-Flop

□ J-K Flip-Flop
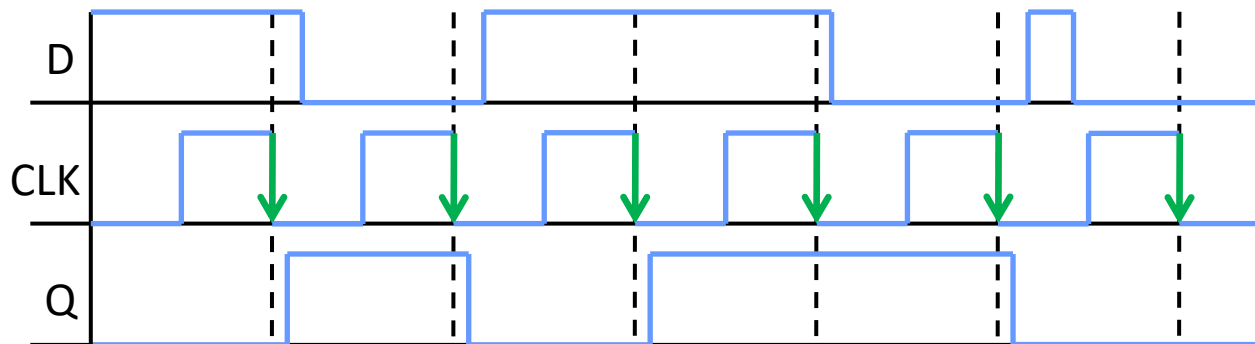
□ T Flip-Flop

□ Flip-Flops with Additional Inputs

Edge-Triggered D Flip-Flops (1/2)

❑ Output changes are aligned with clock edges

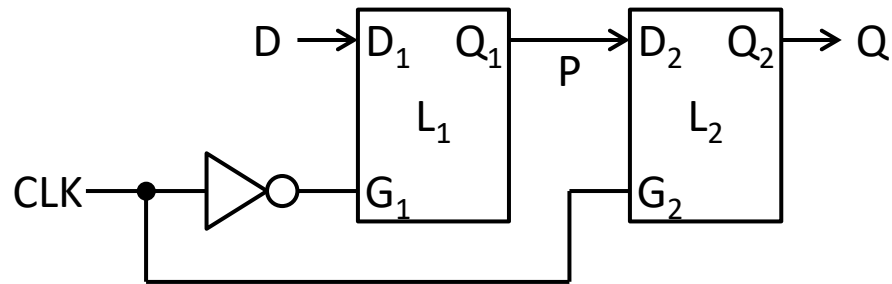➢ Positive (rising-edge) trigger

➢ Negative (falling-edge) trigger

Rising-Edge Trigger   Falling-Edge Trigger

➢ Next-state (characteristic) equation: $Q^+ = D$

➢ Timing diagram for a <u>falling-edge</u> triggered D flip-flop
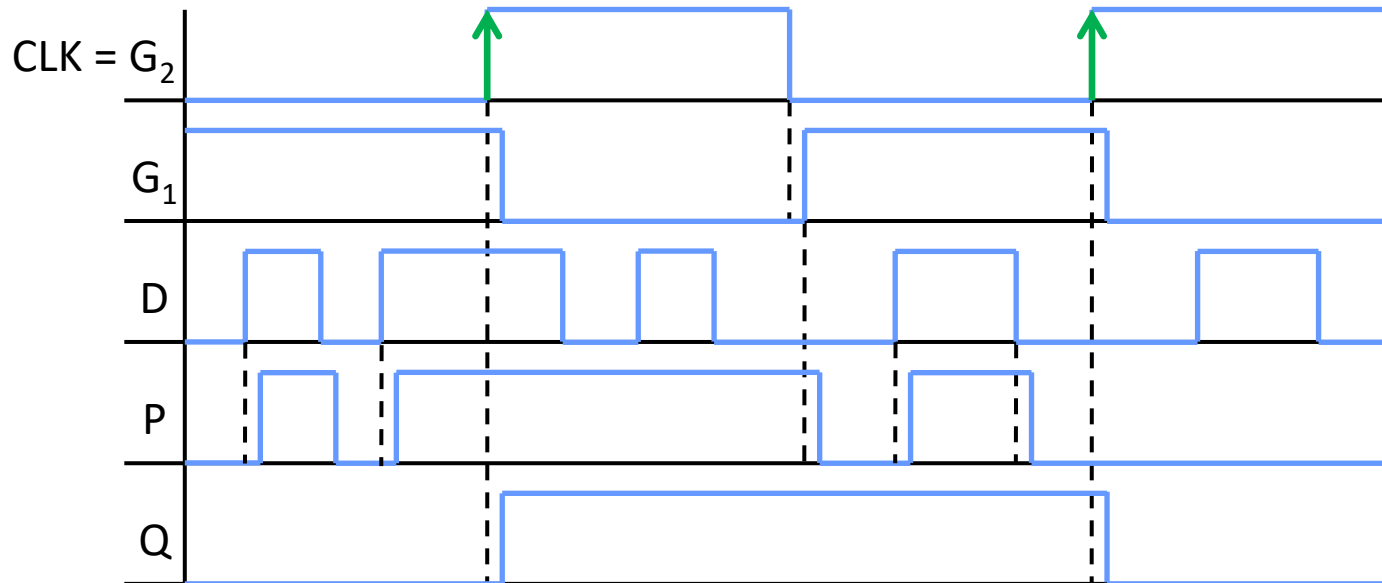
Edge-Triggered D Flip-Flops (2/2)

❑ Construct a <u>rising-edge</u> triggered D flip-flop from 2 gated D latches
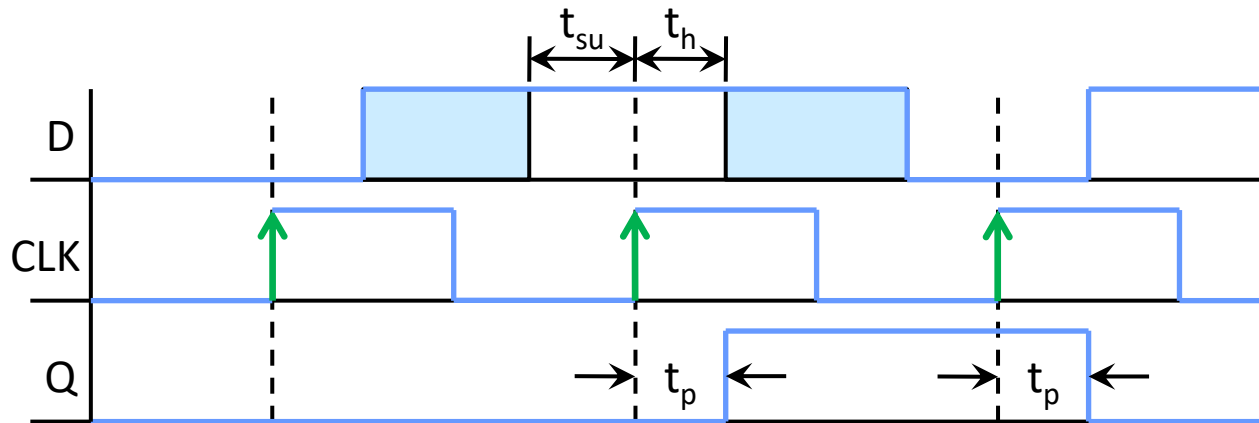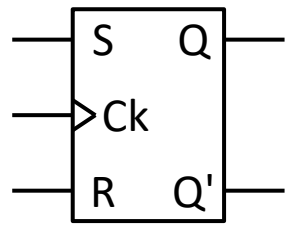
❑ Time diagram

Setup Times and Hold Times

❑ Setup time

➢ The amount of time that D must be stable before the active edge

❑ Hold time

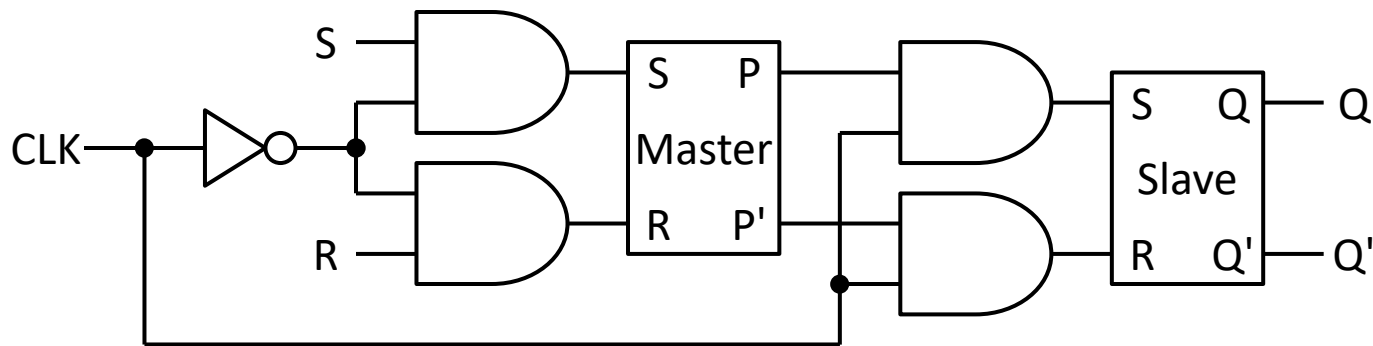➢ The amount of time that D must hold the same value after the active edge

Outline

```
┌─────────┐
│ S     Q │──
│         │
│>Ck      │
│         │
│ R     Q'│──
└─────────┘
```

❑ Set-Reset Latch

❑ Gated D Latch

❑ Edge-Triggered D Flip-Flop

❑ **S-R Flip-Flop**

❑ J-K Flip-Flop

❑ T Flip-Flop

❑ Flip-Flops with Additional Inputs

S-R Flip-Flop

- ❑ Output changes at rising edges
- ❑ Construct from 2 latches

S	R	Operation
0	0	No state change
0	1	Reset Q to 0 (after active CLK edge)
1	0	Set Q to 1 (after active CLK edge)
1	1	Not allowed

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Outline

- ❑ Set-Reset Latch
- ❑ Gated D Latch
- ❑ Edge-Triggered D Flip-Flop
- ❑ S-R Flip-Flop
- ❑ **J-K Flip-Flop**
- ❑ T Flip-Flop
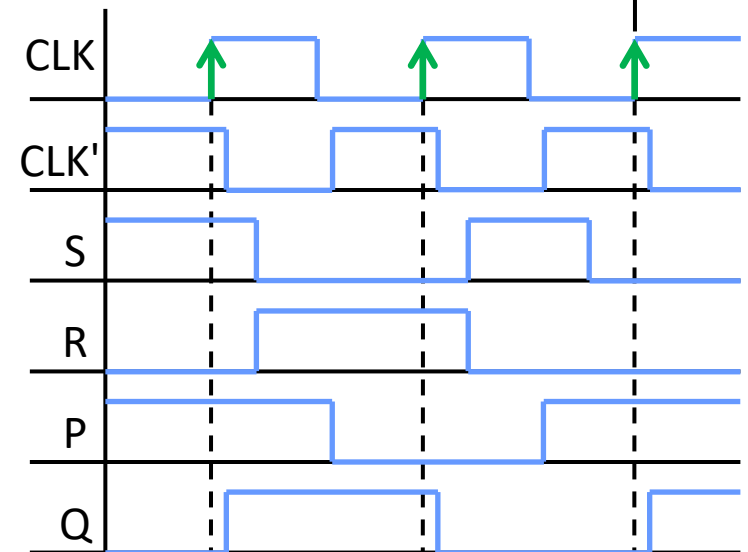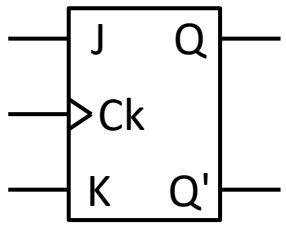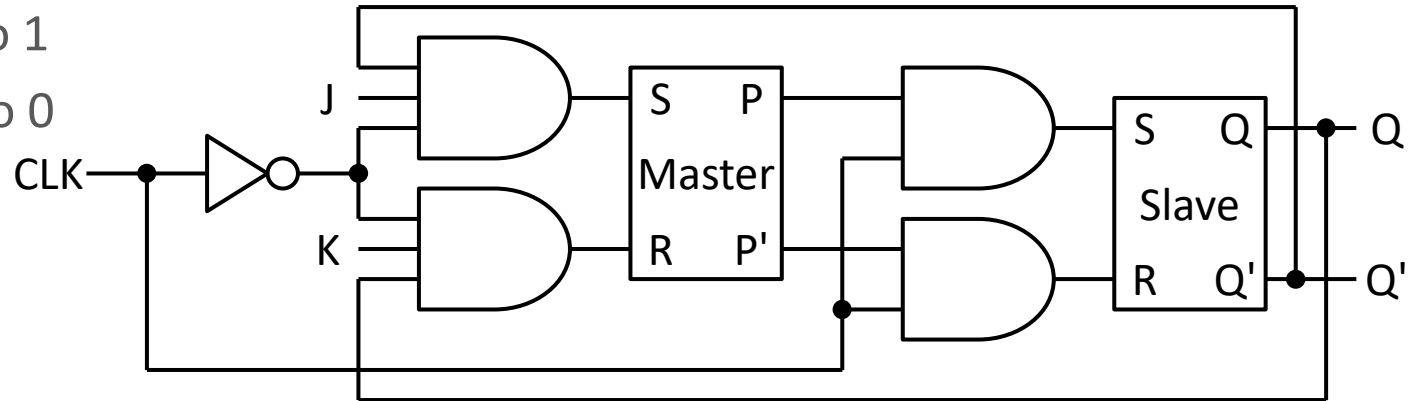- ❑ Flip-Flops with Additional Inputs
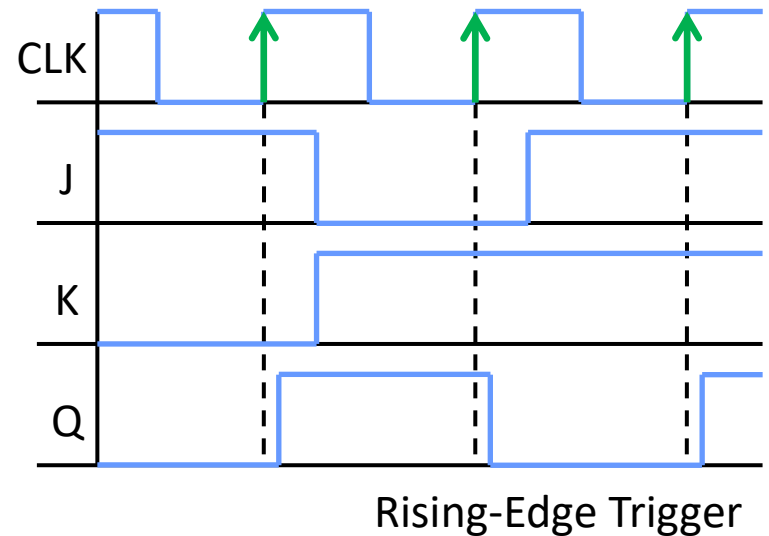
J-K Flip-Flop

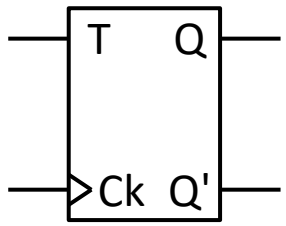❑ **Extension of S-R flip-flop**

➢ J: jump to 1

➢ K: clear to 0

J   CLK   K   S   P   Master   R   P'   S   Q   Slave   R   Q'   Q   Q'

J	K	Q	Q$^+$
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Unchanged

Clear to 0

Jump to 1

Toggle

$$Q^+ = JQ' + K'Q$$

CLK

J

K

Q

Rising-Edge Trigger

Outline
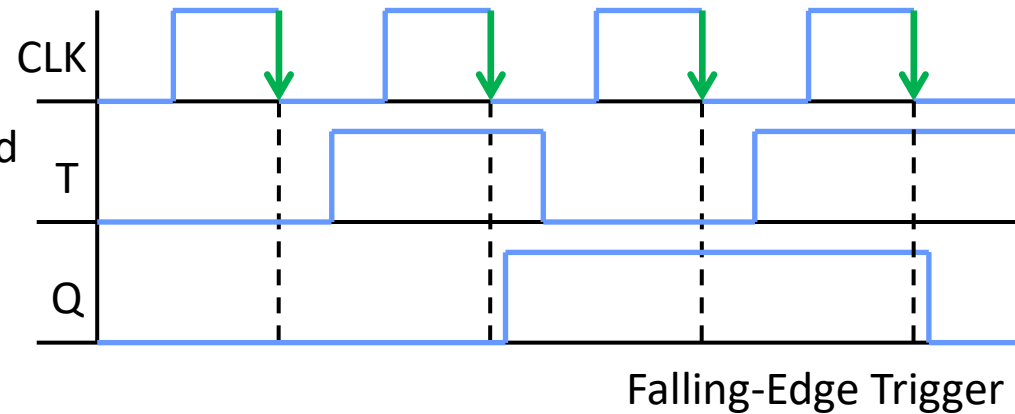
❏ Set-Reset Latch

❏ Gated D Latch

❏ Edge-Triggered D Flip-Flop

❏ S-R Flip-Flop

❏ J-K Flip-Flop

❏ **T Flip-Flop**
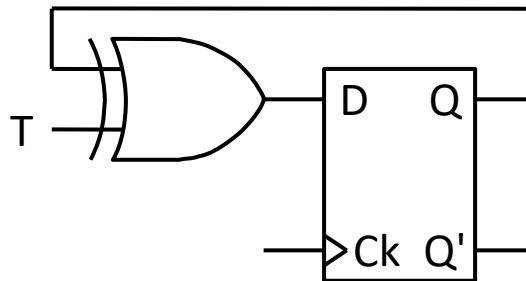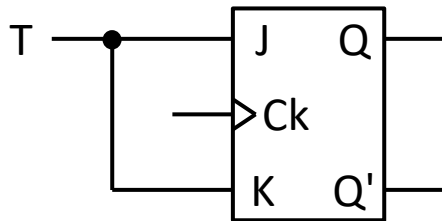
❏ Flip-Flops with Additional Inputs

T Flip-Flop

❑ T: toggle

T	Q	Q⁺	
0	0	0	Unchanged
0	1	1	
1	0	1	Toggle
1	1	0	

$$Q^+ = TQ' + T'Q$$

Falling-Edge Trigger

❑ Implementations

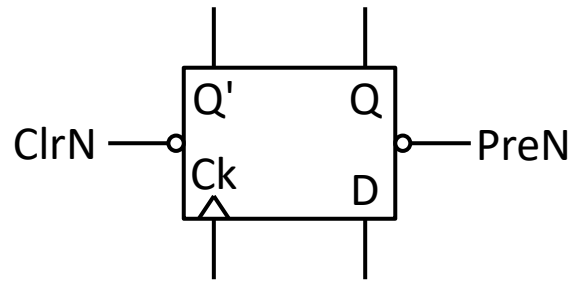# Outline

❑ Set-Reset Latch

❑ Gated D Latch

❑ Edge-Triggered D Flip-Flop

❑ S-R Flip-Flop

❑ J-K Flip-Flop

❑ T Flip-Flop

❑ **Flip-Flops with Additional Inputs**

Flip-Flops with Additional Inputs

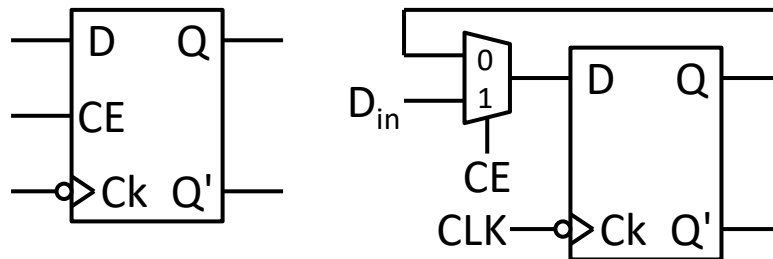❑ **Set a flip-flop to an initial state independent of the clock**

➢ Example: asynchronous Clear and Preset

Ck	D	PreN	ClrN	Q$^+$
X	X	0	0	Not Allowed
X	X	0	1	1
X	X	1	0	0
↑	0	1	1	0
↑	1	1	1	1
0, 1, ↓	X	1	1	Q (Unchange)

❑ **Let a flip-flop hold existing data even though the data input may be changing**

➢ Gated clock: gate the clock by Clock Enable (CE)

Summary

Type	Q$^+$
S-R Latch	S + R'Q
Gated D Latch	G'Q + GD
D Flip-Flop	D
S-R Flip-Flop	S + R'Q
J-K Flip-Flop	JQ' + K'Q
T Flip-Flop	TQ' + T'Q
D-CE Flip-Flop	D(CE) + Q(CE)'

Q&A