CSIE 2344: Homework 4

Due May 20 (Monday) at Noon

There are 90 points in total. Points will be deducted if no appropriate intermediate step is provided. When you submit your homework on Gradescope, please select the corresponding page(s) of each question.

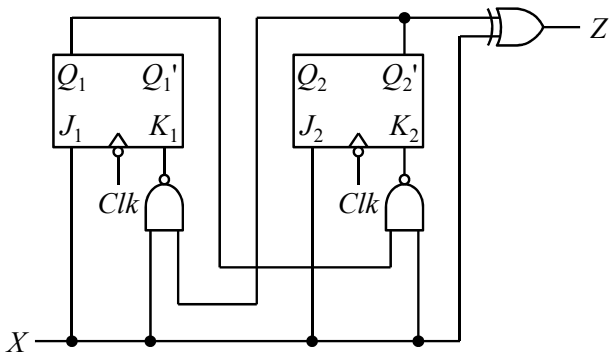
1 Counter Design (24pts)

Design a 3-bit counter which counts CBA in the sequence: 001, 011, 010, 110, 111, 101, 100, and repeats.

1. (4pts) Show the truth table and the Karnaugh map of C^+, B^+, and A^+.
2. (4pts) Use D flip-flops. Derive a minimum sum-of-products expression for D_C.
3. (4pts) Use T flip-flops. Derive a minimum sum-of-products expression for T_C.
4. (6pts) Use S-R flip-flops. Derive a minimum sum-of-products expression for S_B and R_B.
5. (6pts) Use J-K flip-flops. Derive a minimum sum-of-products expression for J_A and K_A.

2 Construction of State Table and State Graph (12pts)

Given the following circuit,



1. (6pts) Construct the state table.
2. (6pts) Construct the state graph.

3 Derivation of State Tables (12pts)

1. (6pts) A Mealy sequential circuit has one input (X) and one output (Z). $Z = 1$ if and only if the most recent input, combined with the preceding three inputs, was not a valid BCD encoding of a decimal digit; otherwise, $Z = 0$. Assume the BCD digits are received least significant bit first. Derive a state table for the circuit and explain the meaning of each state. Assume that in the reset state all previous inputs were 0. (Three states are sufficient.)
2. (6pts) Repeat for a Moore circuit ($Z = 1$ if and only if the previous four inputs were not a valid BCD digit). (Four states are sufficient.)

4 Lab 2: Part 1 (30pts)

Replace <index> in lab2.v with proper indexes, but leave the rest of the code unchanged.

1. (12pts) Print out the module mult_fast.
2. (12pts) Show the waveform with the settings in lab2.sav (should include 1750 to 1800 sec).
3. (6pts) What is the latency (worst case waiting time from the input becomes steady to the register of the last stage refreshes)?

5 Lab 2: Part 2 (12pts)

Minimize the clock cycle by changing the delays in the module mult_tb.

1. (6pts) What is the minimum clock cycle?
2. (6pts) Show the waveform with the settings in lab2.sav (should include 1750 to 1800 sec).