PRESENTATION ON 8-BIT MIPS PROCESSOR

GROUP - A05

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DEFINITION OF OUR MICROPROCESSOR

- 8-BIT RISC BASED SINGLE CORE PIPELINED MICROPROCESSOR WHICH CAN BE USED TO PERFORM VARIOUS ARITHMATIC AND LOGICAL OPERATIONS.

MOTIVATION

- TO RELATE THE THEORY AND PRACTICAL ASPECTS OF COMPUTER ORGANISATION.
- TO UNDERSTAND THE CONCEPTS OF MICROPROCESSOR WITHOUT INTERLOCKED PIPELINED STAGES(MIPS).
- WILLINGNESS TO CREATE A MICRO-PROCESSOR.
- PRACTICAL KNOWLEDGE REGARDING MIPS AND 8085.

SPECIFICATIONS

- BIT - 8
- INSTRUCTIONS - 28
- REGISTERS - 32
- ADDRESS BIT - 8
- FREQUENCY - 1MHZ
- INSTRUCTION SET ARCHITECTURE – RISC
- ADDRESSING MODE - DIRECT, REGISTER DIRECT, IMMEDIATE DIRECT
- INSTRUCTION FORMAT – I - TYPE, R - TYPE, J - TYPE

SPECIFICATIONS CONTINUED...

- **INSTRUCTION FORMATS:**

- R TYPE

Op_dec (5 bits)	Rw (5 bits)	Rb(5 bits)	Ra(5 bits)

- I TYPE

Op_dec(5 bits)	Rw(5 bits)	Rb(5 bits)	Immediate(5 bits)

- J TYPE

Op_dec(5 bits)	Jump_address(15bits)

SPECIFICATIONS CONTINUED....

- CPI –
  - FOR VERY LARGE NUMBER OF INSTRUCTIONS – 1
  - FOR OUR ADDITION PROGRAM – 1
  - FOR OUR MULTIPLICATION PROGRAM - 1.538
- SPEED-UP FACTOR - 5
- NUMBER OF PINS –
  - INPUT – 11
  - OUTPUT - 8
- CLOCK PERIOD - 1000 NANO SECOND

BLOCK DIAGRAM OF MICROPROCESSOR

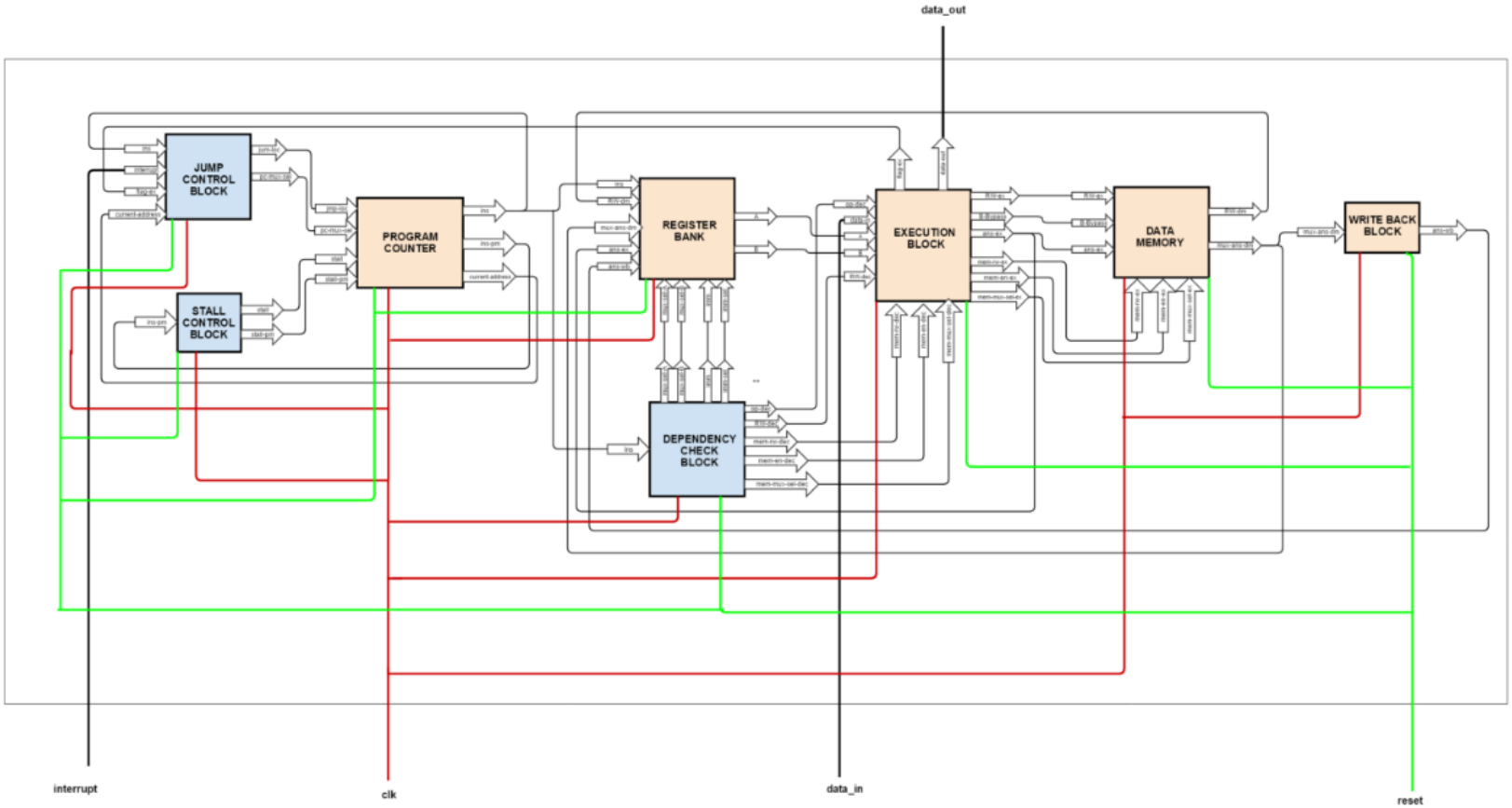
THE BLOCK DIAGRAM INCLUDES VARIOUS BLOCKS OR PARTS OF MICRO-PROCESSOR WHICH PERFORMS THEIR SPECIFIC JOBS. THESE BLOCKS ARE-

JUMP CONTROL BLOCK, STALL CONTROL BLOCK, PROGRAM COUNTER, REGISTER BANK, DEPENDENCY CHECK BLOCK, DATA MEMORY, WRITE BACK AND EXECUTION BLOCK.

CLICK HERE FOR THE BLOCK DIAGRAM

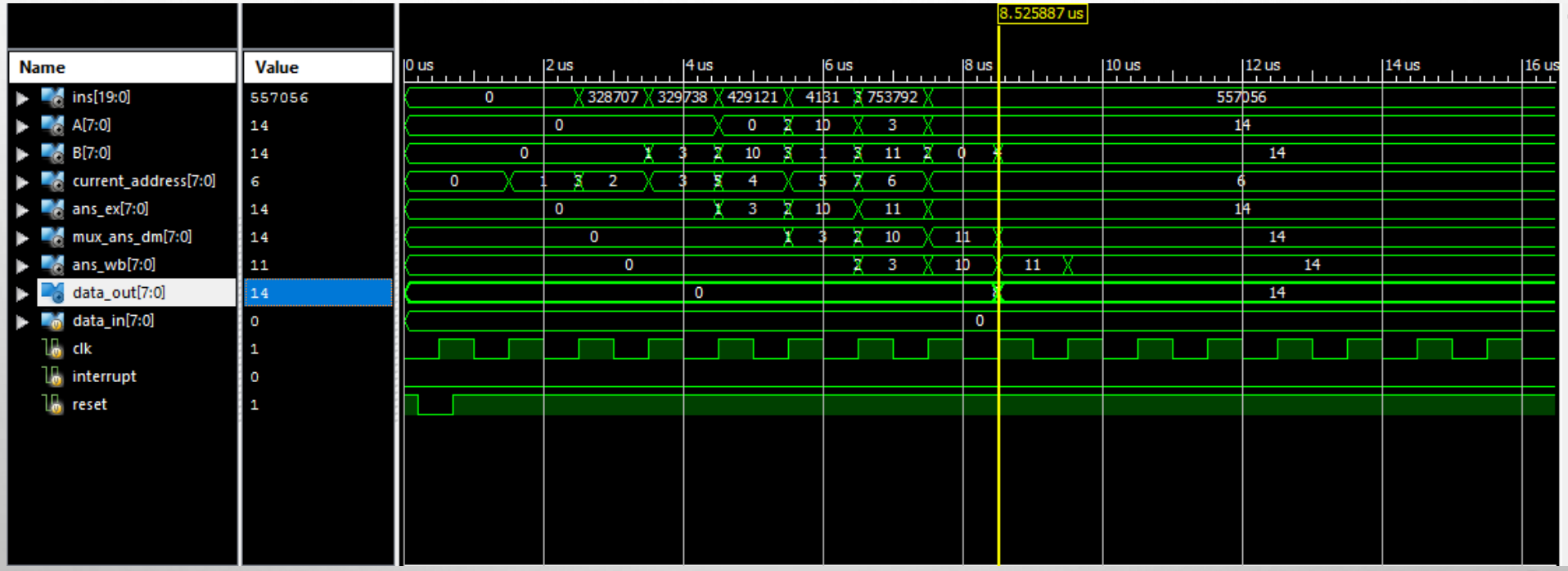
Link for the online diagram:

https://www.gliffy.com/go/share/image/snnodv6gfuwj9gk4egpr.png?utm_medium=live-embed&utm_source=googleapps

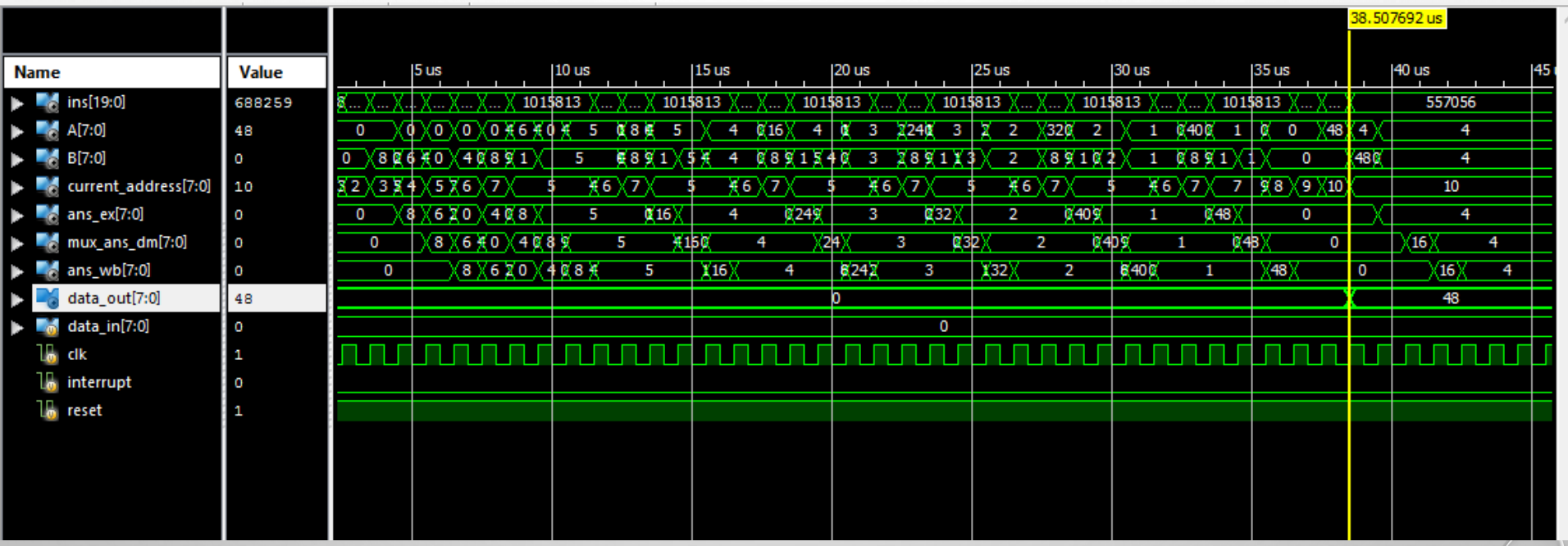


RISC BASED 8 BIT SINGLE CORE MICROPROCESSOR

OUTPUT OF ADDITION(POST-ROUTE)



OUTPUT OF MULTIPLICATION (POST-ROUTE)



ADVANTAGES OF OUR MICROPROCESSOR

- HAS MORE NUMBER OF REGISTERS THAN 8085, SO IT CAN STORE MORE DATA.
- OUR PROCESSOR IS PIPELINED.
- AS OUR PROCESSOR IS RISC BASED SO IT IS FASTER THAN 8085.

DISADVANTAGES OF OUR MICROPROCESSOR

- CLOCK PERIOD OF OUR MICROPROCESSOR IS MORE AS COMPARED TO 8085.
- OUR PROCESSOR CAN NOT COMMUNICATE WITH THE EXTERNAL WORLD.
- OUR PROCESSOR HAS LESS NUMBER OF PINS AS COMPARED TO 8085.
- AS DATA MEMORY AND PROGRAM MEMORY ARE SEPARATE IN OUR PROCESSOR IT TAKES MORE TIME TO EXECUTE A INSTRUCTION AS COMPARED TO 8085 WHICH HAS COMBINED MEMORY.
- OUR PROCESSOR HAS LESS NUMBER OF INSTRUCTIONS AS COMPARED TO 8085.

COMPARISON OF OUR DESIGN WITH 8085

8085	Processor
▪ 8 bit data bus	▪ 8 bit data bus
▪ frequency : 3-6 Mhz	▪ 1 Mhz
▪ Semi - CISC	▪ RISC
▪ Non-pipelined	▪ Pipelined
▪ 6 Registers	▪ 32 Registers
▪ 16 bit address line	▪ 20 bit address line
▪ 80 instructions	▪ 28 instructions
▪ Accumulator : 8 bit	▪ Accumulator : not present
▪Architecture : Neumann	▪Architecture : Harvard

CHALLENGES FACED DURING DESIGN AND IMPLEMENTATION

- REMOVING THE IF...ELSE BLOCKS FROM WHOLE CODE.
- SHOWING THE WARNINGS OF SOME MISSING FILES EVEN THOUGH THE FILES WERE PRESENT IN THE PROJECT FOLDER.
- DIFFERENCES BETWEEN THINKING OF GROUP MEMBERS.
- TO UNDERSTAND THE CONCEPT AND LOGIC BEHIND THE DESIGN.
- TO ANALYZE THE OUTPUT OF THE DESIGN.

FEEDBACK /SUGGESTIONS

- MANAN SIR AND PARTH SIR WERE VERY HELPFUL TO US IN ALL THE LAB SESSIONS.
- AS AN ENGINEER, WE HAD A GOOD EXPERIENCE TO EXPLORE THE INTERNAL PARTS OF A PROCESSOR.
- IF YOU CAN PLEASE TRY TO DESIGN A CODE WHICH CAN BE DUMPED ON FPGA.
- WE CAN INCLUDE THE INTERRUPT BLOCK SO AS TO TAKE ANY INTERRUPT VALUE.
- OVERALL IT WAS A GOOD EXPERIENCE.

THANK YOU...☺☺☺