Siddharth R. Kala

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Career Objective

Looking for a responsible position as a researcher with a view to utilize and enhance my research and technical skills in a dynamic, growth oriented and technologically driven organization.

Research interests

Analog and mixed signal design, ADCs, Memory Design, Filter Design.

Working Experience

Designation	Teaching Assistant
Organization	IIT Goa
Duration	From January 2018 to Present
Job Role	Conducting Analog Circuits lab

Designation	Project Staff
Organization	NIT GOA
Duration	From September 2016 to December 2016
Job Role	Worked on 10 Bit Successive approximation (SAR) ADC; project was sponsored by SMDP.

Publications

2018 Siddharth R. K., Nithin Kumar Y. B., Vasantha M. H., Edoardo Bonizzoni, "A Low-Power Auxiliary Circuit for Level-Crossing ADCs in IoT-Sensor Applications", *2018 IEEE International Symposium of Circuits and Systems (ISCAS)*, Florence, Italy, 2018. [*accepted*]

2017 Siddharth R. K., Nithin Kumar Y. B., Vasantha M. H., 2017, Dynamic comparator with method for optimizing speed, Indian Patent Application 201721029618, filed August 2017. [*Patent Pending*]

2017 Sumit Khalapure, Siddharth R. K., Y.B.N. Kumar, M.H. Vasantha, "Design of 5-Bit Flash ADC Using Multiple Input Standard Cell Gates for Large Input Swing, *2017 IEEE Computer Society Annual Symposium on VLSI (ISVLSI),pp. 585-588, Bochum, Germany, 2017.*

2017 Mayur S. M., Siddharth R. K., Y.B.N. Kumar, M.H. Vasantha, "Design of Low Power 4- Bit 400MS/s Standard Cell Based Flash ADC, *2017 IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, pp. 600-603, Bochum, Germany, 2017.

2016 Mayur S. M., Siddharth R. K., Y.B.N. Kumar, M.H. Vasantha,"Design of Low Power 5-Bit Hybrid Flash ADC", *2017 IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, pp. 343-348, Pittsburg, PA, 2016.

2016 Saurabh B. K., Siddharth R. K., Y.B.N. Kumar,S. Patidar, M.H. Vasantha,"Design and Implementation of Tunable Bandpass Filter for Biomedical Applications, *2016 IEEE International Symposium on Nanoelectronic and Information Systems (iNIS)*, pp. 43-46, Gwalior, India, 2016.

Academic projects

Present Research

Title	Design of Asynchronous ADC for energy-aware systems
Tool	Cadence-Virtuoso, MATLAB
Description	Uniform sampling scheme takes equal number of samples from the low activity zone (regions where slope is small) and high activity zone (large slope regions). Hence to minimize the effect of slope overload and save energy, ultimately energy, a non-uniform sampling scheme has been chosen so that more samples are taken from the high activity zone. Thus, asynchronous ADC can prove to be better solution for energy-aware designs.

M.Tech

Title	Asynchronous Hybrid Analog to Digital Converters (ADCs)
Tool	Cadence - Virtuoso, MATLAB
Description	This work tends to use a nonuniform sampling whose sampling instances depends on the amplitude of the sampled input voltage. Input voltages near to most significant bit (MSB) will have a lesser delay than input voltages near least significant bit (LSB). During the operation of one comparator, other comparators are disconnected form the power supply. This reduces power consumption but increases the conversion time by introducing the delay.

B.Tech

Title	GSM based design of the industrial automation.
Tool	Keil
Description	This work focuses on facing the current issues of catching fire in industries/home. It senses smoke, fire, increase in the temperature and gas leakage and initiates the buzzer/alarm and sending the message to the controller us- ing GSM wherever he/she may be. It also displays a warning message in the industry and can informing the police or fire station in case of an emergency.

Technical skills

Languages	C, VHDL, Assembly languages (8085, 8086, 8051).
Automation tools	Cadence-virtuoso, ATLAS, Xilinx, MATLAB, Visual-TCAD.

Educational qualifications

Year	Degree and Institute	Grade
2017 - Present	PhD in VLSI National Institute of Technology, Goa	CGPA: 9.0/10
2014 - 2016	Master of Technology in VLSI National Institute of Technology, Goa	CGPA: 9.27/10
2009 - 2013	Bachelor of Technology in ECE Government Engineering College, Patan, Gujarat.	CGPA: 8.06/10
2007 - 2009	H.S.C. (MPC) St. Francis Of Assisi Convent High School, Navsari, Gujarat (GHSEB).	Percentage: 79.40 %
2002 - 2007	S.S.C Seventh Day Adventist English High School, Navsari, Gujarat	Percentage: 70.01 %

Workshops attended

- Four days Instruction Enhancement Programme (IEP) on “High Level Design to silicon”at IIT Roorkee from 24th-27th February, 2018.
- Five days Instruction Enhancement Programme (IEP) on “Analog IC Design” at IIT Madras from 29th January to 2nd February, 2018.
- Three days training on “Cadence tools training”at PSG College of Technology, Coimbatore from 23rd-25th January, 2017.
- Five days Gian course “Low Power Nyquist-rate Data Converter”at NIT Goa from 6th-10th March, 2017.
- Nine days workshop on “Xilinx Training Tools in association with Corel Technologies”at NIT Goa from 2nd-10th December, 2016.

Acheivements

- Secured 80.00% in 8th National IT Aptitude Test.
- Secured 50.74 marks and 643/1000 score in GATE-2014 with a rank of 2989 out of 3,76,367 students.

Extracurricular activities

- Obtained a certificate of social service from “GLOBAL CANCER CONCERN INDIA”for raising resources for the cause of cancer sufferers.
- Worked as volunteer for Unnat Bharat, Swachh Bharat Campaigns, orientation program for freshers and convocations conducted in NIT Goa

Personal skills

Hardworking, good leadership and presentation skills

Hobbies

Reading, Traveling and Playing Chess.

References

- Dr. M.H. Vasantha
  HOD, Dept. of ECE, NIT Goa
  Email: vasanthmh@nitgoa.ac.in
- Dr. Y.B.Nithin Kumar
  Assistant professor, Dept. of ECE, NIT Goa
  Email: nithin.shastri@gmail.com