Charudatta Gurudas Korde

Research Scholar(PhD)
National Institute of Technology
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Research interests

Digital VLSI design, Machine Learning, Deep Neural Network, Field Programmable Gate Arrays.

Academic projects

Title FPGA based algorithm implementation.
Tool MATLAB, Spyder, Vivado
Description To design Generative Adversarial Network(GAN) and its variant using python based Deep Neural Network(DNN) library namely Keras. The studies is conducted by varying parameters of GANs to get stable and robust network. The designed network will be implemented on FPGA to reduce power consumption and to get speed up comparable to GPU.

Publications

2018 Barve, S Raveendran S, Korde C ,Panigrahi T, Nithin Kumar Y, Vasantha M "FPGA implementation of square and cube architecture using vedic mathematics, *Proceedings - 2018 IEEE 4th International Symposium on Smart Electronic Systems, iSES 2018*.

2017 Korde C. G., Chandrasekhar, E. and Shenvi, N., "Multifractal analysis of ionospheric disturbances triggered by earthquakes, *18th Annual conference of the International Association of Mathematical Geosciences (IAMG 2017)*,Perth, Australia,September, 2017(POSTER).

Educational qualifications

Year	Degree and Institute	Grade
2018 - Present	PhD in VLSI National Institute of Technology, Goa	CGPA: 8.6/10
2015 - 2017	Master of Engineering in Microelectronics Goa College of Engineering, Goa.	CGPA: 8.0/10
2011 - 2015	Bachelor of Technology in EEE Goa College of Engineering, Goa.	Percentage: 76%

Technical skills

Languages	MATLAB, Verilog, Python, C, Julia, VHDL, Cuda.
Hardware Platforms	Nvidia GPU, Raspberry Pi, Arduino, FPGA (Basys 3, ZedBoard).
Tools	Quartus, MATLAB, Vivado HLX, Spyder (Anaconda).
Feilds	Deep Neural Networks, Machine Vision - Image Processing, Evolutionary Algorithms, Fuzzy Logic, Cryptography and Network Security, Neural Networks , Fractals.

Work Experience

september 2019 - march 2020

Title	Software Validation Engineer
Tool	Quartus 19.3, 19.4, 20.1
Description	I interned with Intel Banglore Bellandur SSR4. I worked on testing and validation of the Quartus tool for Partial Reconfiguration and Heraichial Design flows.

Work

- Github: https://github.com/charudatta10
- Website: https://deathsta.webs.com/

References

- Dr. M.H. Vasantha
  Associate professor, Dept. of ECE, NIT Goa
  Email: vasanthmh@nitgoa.ac.in
- Dr. Y.B.Nithin Kumar
  HOD, Dept. of ECE, NIT Goa
  Email: nithin.shastri@gmail.com