BPC-NDI

Auxiliary Arithmetic Unit

Final Report

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Document Change Log

Version	Date	Author(s)	Description of Changes
1.0	14.1.2024	Kučera, Charvot	First version

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1 INTRODUCTION

This document is part of the documentation for the Auxiliary Arithmetic Unit (AAU), which was a topic for semestral project in the BPC-NDI course. As it is a final report, document describes several things. As the first, development of the AAU is presented and its architecture is also briefly discussed. Subsequently, the document focuses on the description of the design verification and its results are presented in detail.

2 APPLICABLE AND REFERENCED DOCUMENTS

The applicable and reference documents used during document preparation are listed in tables bellow. If exact date of issue is unknown the 1st day of the month is used. If either month is unknown the 1st of January is used. If revision of the document is unknown number 0 is used.

2.1 List of applicable documents

The following documents of the exact issue and/or revision shown form a part of this document to the extend specification herein. Where no issue is shown the latest issue is applicable.

Table 1: List of applicable documents

Ref.	Name	Document Number	Version
AD01	Requirement Specification	AAU-RS-BUT-0001	2.1

2.2 List of referenced documents

The following documents are for reference and/or guideline only.

Table 2: List of referenced documents

Ref.	Name	Document Number	Version
RD01	Requirement Specification	AAU-RS-BUT-0001	2.1

3 DEFINITIONS AND LIST OF ABBREVIATIONS

The formal part of the document, we recommend drawing inspiration from a similar chapter in the specification request.

3.1 Definitions

In description of individual testcases used for design verification the following terms are used:

- **Empty packet** - means a packet where both frames are 0.

Each verification test has its number which is in the following format: tc_*tested-block*_xxx

- tc stands for Test Case
- *tested-block* is substitute for abbreviation of block to which is test case related
- xxx is substitute for three digit number of the test
- Example: tc_spi_001

3.2 Writing Numbers

Numbers in this document are written mainly in human-readable format, that means number with decimal point interpreted in ten-base system, eg. -3.75. For the proccesing in the AAU, numbers are converted to proper binary form in VHDL procedure and vica-versa for number received from the AAU.

3.3 Units

Only SI units are used in the text.

3.4 Abbreviations

AAU	Auxiliary Arithmetic Unit
CLK	Clock
CS	Chip Select
DDF	Double D Flip-Flop
DUT	Device Under Test
FPGA	Field-Programmable Gate Array
FSM	Finite State Machine
HDL	Hardware Description Language
ISE	Integrated Synthesis Environment
LSB	Least Significant Bit
MCU	Microcontroller Unit
MISO	Master In Slave Out
MOSI	Master Out Slave In

P&R Place and Route

SCLK Signal CLK

SI Système International

SPI Serial Peripheral Interface

STA Static Timing Analyses

TB Test Bench

VHDL VHSIC Hardware Description Language

4 PROJECT PRESENTATION

In the project, an Auxiliary Arithmetic Unit (AAU) is incorporated as an enhancement to a basic microcontroller (MCU) for arithmetic tasks. The AAU is connected to the MCU via a Serial Peripheral Interface (SPI), with the MCU acting as the master and the AAU as the slave in the communication schema. Data transmission is carried out from the master to the slave, and the AAU independently returns the results of arithmetic operations in the subsequent packet. The AAU is designed to perform two arithmetic operations: addition and multiplication, with numbers being processed in a fixed-point format.

While the master unit drives the data transfer, there is a possibility of errors occurring in the link. Therefore, it is essential to verify the completeness of incoming data before carrying out arithmetic operations and transmitting the results.

5 DEVELOPMENT PLAN

The development plan, as shown in Figure 1, includes a structured approach to project implementation. First, requirements as specified in AD01 are identified, followed by an architecture design process that includes the creation of functional blocks and simulations. This phase is followed by integration into the final circuit and subsequent verification to ensure that all specifications are met. If inconsistencies are found during verification, a cyclic process is initiated that returns to the design phase for necessary changes and further verification until the criteria are met. Upon successful verification, the design is considered complete.

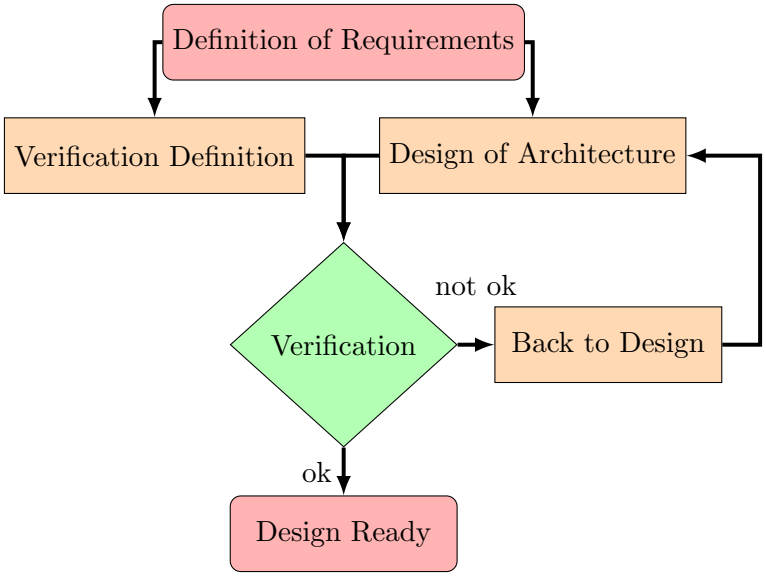

Figure 1: Development Diagram

6 DESIGN DESCRIPTION

In Figure 2, the block diagram of the AAU unit architecture is shown. The individual blocks within the AAU are further described in more detail in the following subsections.

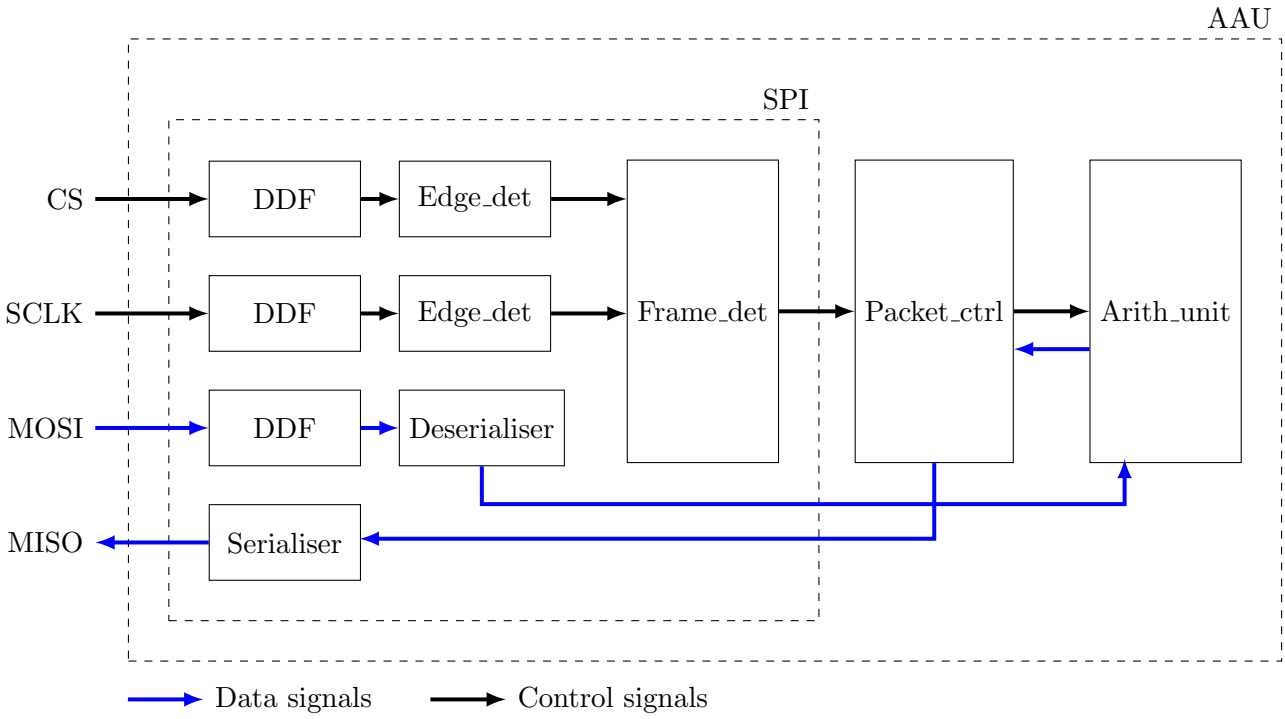

Figure 2: Architecture block diagram.

6.1 SPI interface

The SPI is the block that handles communication with the master, receiving and sending packets. It is also responsible for detecting an error frame.

6.1.1 DDF

The Double D Flip-Flop (DDF) is crucial for managing asynchronous signals, specifically for meeting the requirement REQ_AAU_G_004. It ensures that the asynchronous inputs are synchronized with the FPGA's clock, minimizing the risk of metastability.

6.1.2 Edge detector

Detects rising or falling edges and generate a single pulse on the corresponding output signal.

6.1.3 Serializer/Deserializer

The Deserializer converts serial data from the MOSI bus to parallel data. The Serializer converts parallel data to serial data for sending to the MISO bus. The core of both modules is a shift register which also guarantees the fulfilment of the requirement REQ_AAU_G_003 because the MISO pin (which is the only one output signal) is connected directly to the output of that register.

6.1.4 Frame detector

This block is responsible for detection of valid or an erroneous frame. It detects frame start, counts received bits and after detection of frame end it checks the frame length.

6.2 Packet control

Ensures packets are received and sent correctly. In case of receiving an invalid packet, it is considered a empty packet. For controlling the process a FSM is used, its diagram is shown in Figure 3. Packet control block is able to control data flow in both directions and reset Arithmetical unit.

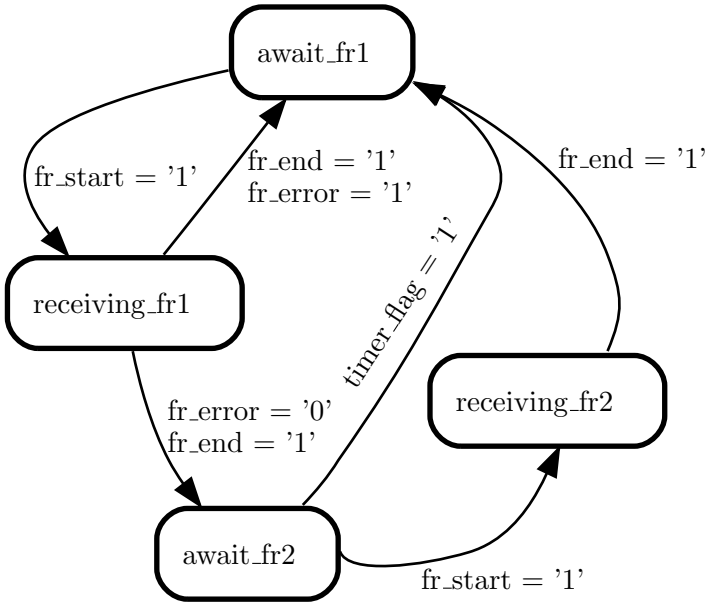

Figure 3: FSM diagram for Packet control.

6.3 Arithmetic unit

Performs sum and product calculations from received data, rounding and flooring the results as defined in the referenced documentation.

7 VERIFICATION PLAN

The verification plan is designed to systematically evaluate the design against its predefined requirements. Verification is carried out through three main methods: documentation review (R), simulation (S) and analysis (A).

In the documentation check, the verification process consists of referring to specific sections of the document that match and satisfy the requirements. This approach ensures that all documented aspects of the design comply with the set criteria.

Verification through simulation uses test vectors that are systematically applied to the design to elicit responses that are then evaluated to determine if the design meets the necessary requirements.

7.1 Verification Matrix

In Table 3

Table 3: Verification Matrix.

REQ ID	Name	Ver. method			Verification of Requirement	Fulfilled
		R	S	A		
REQ_AAU_G_001	Target technology	Y	-	-	Section 8.1	Y
REQ_AAU_G_002	Synchronous design	Y	-	-	Section 8.1.2	Y
REQ_AAU_G_003	Output signals	Y	-	-	Section 6.1.3	Y
REQ_AAU_G_004	Input signals	Y	-	-	Section 6.1.1	Y
REQ_AAU_G_005	FSM Safe Implementation	Y	-	-	Section 8.1.1	Y
REQ_AAU_G_006	Documentation	Y	-	-		Y
REQ_AAU_F_010	Auxiliary Arithmetic Unit	Y	-	-	tc_au_001	Y
REQ_AAU_F_011	Format of numbers	-	Y	-	tc_spi_002	Y
REQ_AAU_F_012	Number rounding	-	Y	-	tc_au_001	Y
REQ_AAU_F_013	Overflow of arithmetic operations	-	Y	-	tc_au_001	Y
REQ_AAU_I_020	SPI clock frequency	-	Y	-	tc_spi_002	Y
REQ_AAU_I_021	Bit ordering	-	Y	-	tc_spi_001	Y
REQ_AAU_I_022	Incomplete frame	-	Y	-	tc_pckctrl_001	Y
REQ_AAU_I_023	Link reset	-	Y	-	tc_pckctrl_001	Y
REQ_AAU_I_024	Packet format	-	Y	-	tc_spi_001	Y

7.2 Description of the Verification Environment

This chapter describes the structure of the verification environment and the function of its individual components. Similarly to the design description, initially, the overall structure is presented seen in Figure 4, and the data transfer between individual components is described. Then, the individual components are presented in more detail.

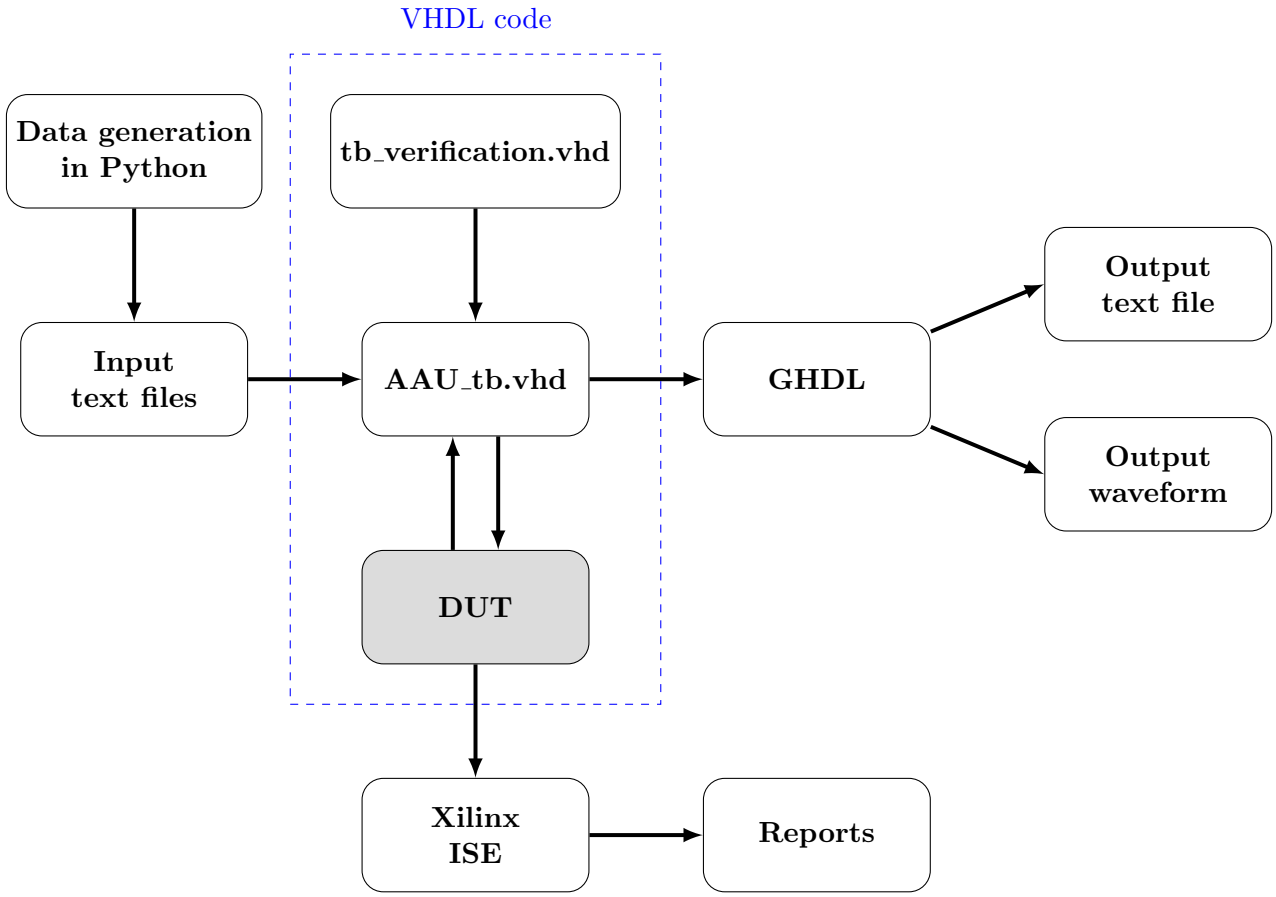

Figure 4: Block diagram of the verification environment.

Python script generates testing vectors for multiple test-cases as well as the correct arithmetic results for later verification. This generated data is stored in text files (**Input text files**), for groups of related requests, which are then read by test bench **AAU_tb.vhd**. This test-bench uses `record`s and `procedure`s, `function`s and `constant`s defined in custom VHDL `package` (**tb_verification.vhd**). Furthermore, this test bench interacts with the **DUT**, simulating it for the defined test cases. The outputs of these simulations are **Output text file and Output waveform**. In the next step **DUT** is analysed in **Xilinx ISE** which produces **Reports**.

7.2.1 Data generation in Python

This python script (listing 8 in Appendix B) generates a list of numbers from two input numbers written in float format, with corresponding requirement. It generates their sum and product in fixed-point arithmetic with 16 bit numbers, where whole part is 8 bits and fractional part is 8 bits, just like AAU. It also computes the product by simple multiplication, which is used to test the functionality of the floor method. Sets of generated numbers for independent test cases are converted to float format and written to a corresponding Input text file.

7.2.2 Input text file

The results from the **Python** script are stored in this file. Where all the numbers and requirements are on a separate line, because of the way VHDL reads input files.

7.2.3 AAU_tb.vhd

This file deals with reading input text files and writing results to output text files. Simulations for all test-cases are performed here.

7.2.4 tb_verification.vhd

This file contains defined records, constants, procedures and functions and is used in AAU_tb.vhd. The `record` is used for defining `packet`, which contains both frames data of type `real`, and `SPI_bus_t`, which contains all SPI signals of type `std_logic`. The `constant`s are used for defining CLK and SCLK period and for bit width of the design, because the whole design is written parametrically by passing a generic parameter `g_DATA_SIZE` to all modules. The `procedure`s are used for sending and receiving data packets and validating the correctness of the communication process. The `function`s are used for data conversion from `real` to `std_logic_vector` and vice versa. This conversions are useful, so that the numbers can be entered into procedures in a human readable format, instead of 16 bit binary numbers, and the results will be also converted back into this readable format.

7.2.5 Output text file and Output waveform

These two blocks are the output of the simulation. The Output text file stores formatted results of each test-case. Waveform is the output of the simulator, where the waveform of the signals over time can be seen and analysed.

7.2.6 DUT

The DUT (Device Under Test) is an already designed AAU that is being tested. Its design is described in Section 6.

7.2.7 Xilinx ISE

Xilinx ISE is a software tool for the creating HDL designs and their synthesis and analysis. It is used to implement the design on the target technology, also the STA is done. Xilinx ISE generates detailed reports of the performed steps.

7.2.8 Reports

Reports are files generated after synthesis, STA and design implementation. More information can be seen in Section 8.1.

7.2.9 GHDL

GHDL is an open-source simulator for the VHDL language. It's been used for simulations in this project. Simulations were done for VHDL 2008 standard, but the code is compatible with VHDL 93 standard, except for the `to_string` function, which is only used to read and write from input and output text files.

7.3 Verification Tests

In this chapter, all tests for verifying the functionality of the design (to meet requirements) are listed.

Test Number: tc_au_001	
Name of Test	Correct arithmetic operations
Test Description	The purpose of this test is to verify that **DUT** gets and returns numbers in correct format and performs arithmetic operations according to related requirements. Test is done by sending different combinations of input numbers to match all possible scenarios.
Reflected Requirements	REQ_AAU_F_010, REQ_AAU_F_012, REQ_AAU_F_013
Test Procedure	1. Reset DUT 2. Start generating clock signals: system clock . . . 50 MHz SCLK . . . 1 MHz 3. TB: Loop throw the input numbers from text file: • TB: Send valid packet with a pair of input numbers. • TB: Send empty packet and receive results packet from DUT. • TB: Validate results according to python generated correct numbers. • TB: Add report to output text file. 4. Check output text file for possible errors.
Output file	Listing 4 in Appendix A

Test Number: tc_spi_001

Name of Test	Packet and frame format
Test Description	This test ensures that **DUT** uses correct packet format for receiving input numbers and sending arithmetic results back on the SPI bus.
Reflected Requirements	REQ_AAU_F_011, REQ_AAU_I_021, REQ_AAU_I_024
Test Procedure	1. Reset DUT 2. Start generating clock signals: system clock . . . 50 MHz SCLK . . . 1 MHz 3. TB: Send valid packet with numbers 15.12109375, -3.50 4. TB: Send empty packet and receive results packet from DUT. 5. TB: Validate results according to python generated correct numbers. 6. TB: Add report to output text file. 7. Check output text file for possible errors. 8. View generated waveforms of the SPI bus. • Check the transmition on MOSI and MISO, LSB should be first. • Numbers should be in 2nd complement format. • Check result packet, sumation result should be first followed by multiplication result.
Output file	Listing 5 in Appendix A
Output waveform	Figure 6 in Appendix A

Test Number: tc_spi_002

Name of Test	SPI clock frequency
Test Description	The purpose of the test is to ensure the correct function of DUT with multiple SPI clock frequencies.
Reflected Requirements	REQ_AAU_I_020
Test Procedure	1. Reset DUT 2. Start generating clock signals: system clock . . . 50 MHz SCLK . . . 1 MHz 3. TB: Loop throw the input numbers from text file: • TB: Send valid packet with a pair of input numbers. • TB: Send empty packet and receive results packet from DUT. • TB: Validate results according to python generated correct numbers. • TB: Add report to output text file. 4. TB: Change SCLK period to match frequency of 100 kHz. 5. TB: Reset DUT and repeat sequence above for the same numbers. 6. TB: Change SCLK period to match frequency of 10 kHz. 7. TB: Reset DUT and repeat sequence above for the same numbers. 8. Check output text file for possible errors.
Output file	Listing 6 in Appendix A

Test Number: tc_pckctrl_001

Name of Test	Detection of Erroneous Frame on SPI Bus
Test Description	This test verify a correct function of **packet_control** module of DUT. This module should detect frame with wrong number of bits and also packet with too long delay between its frames. Those packets should be discarded. In the test correct packet and multiple erroneous will be provided to DUT and the reaction will me monitored.
Reflected Requirements	REQ_AAU_I_022, REQ_AAU_I_023
Test Procedure	*If not specified, delay between frames is* 1 μs *and between packets is* 1 μs. *For getting DUT response a valid empty packet is sent and than the result is verified.* 1. Reset DUT 2. Start generating clock signals: system clock . . . 50 MHz SCLK . . . 1 MHz 3. TB: Send a valid packet to ensure a proper function on the start. 4. TB: Receive response and verify it. 5. TB: Send packet with shorter both frames (8 bit). 6. TB: Send packet with shorter second frame (8 bit). 7. TB: Send packet with longer both frames (20 bit). 8. TB: Send packet with longer second frames (20 bit). 9. TB: Verify responses, **all results from the steps above should be empty**. 10. TB: Send packet with shorter first frame (8 bit). 11. TB: Send packet with longer first frame (20 bit). 12. TB: Send packet with 1.2 ms delay between frames. 13. TB: Verify responses. In those three scenarios the first frame of the packet is ignored as expected. Because of that, the second frame is from the DUT perspective perceived as the first frame and all following frames are shifted. In place where TB expect to be the multiplication result (zero) is actually result of sumation of number from second frame and first zero of the empty frame. This behaviour is in compliance with the requirements.

8 IMPLEMENTATION RESULTS

After successful verification (done by simulation) is necessary to finally implement design for the target technology which is FPGA Xilinx Spartan 3, according to REQ_AAU_G_001. Xilinx ISE is used for the implementation because it is the only environment that supports the target technology.

First step is to proper set the environment. To match all the requirements, settings from the Table 4 were applied.

Table 4: Xilinx ISE settings applied.

Design properties	
Family	Spartan3
Device	XC3S200
Package	FT256
VHDL Source Analysis Standard	VHDL-93
Synthesis Options	
Optimization Goal	Speed
Optimization Effort	Normal
Use Synthesis Constraints File	YES
HDL Options	
FSM Encoding Algorithm	Auto
Safe Implementation	YES

8.1 ISE reports

All relevant reports from Xilinx ISE are placed in the Appendix. For better orientation, they are also listed in Table 5. Important parts of the reports are also discussed in following subsections.

Table 5: List of Xilinx ISE reports.

Report name	**Reference**
Synthesis Report	Listing 9 in Appendix C
STA Report	Listing 10 in Appendix C
Place and Route Report	Listing 11 in Appendix C

8.1.1 FSM Safe Implementation

Below in Listing 1 a snippet from Synthesis Report can be seen confirming REQ_AAU_G_005

Listing 1: Snippet from Synthesis Report (AAU.syr).

```
...
---- Source Options
FSM Encoding Algorithm             : Auto
Safe Implementation                : Yes
...
---------------------------
 State          | Encoding
---------------------------
 await_fr1      | 00
 receiving_fr1  | 01
 await_fr2      | 10
 receiving_fr2  | 11
---------------------------
...
```

8.1.2 Synchronous design

Below in Listing 2 a snippet from Synthesis Report can be seen confirming REQ_AAU_G_002

Listing 2: Snippet from Synthesis Report (AAU.syr).

```
...
Asynchronous Control Signals Information:
----------------------------------------
No asynchronous control signals found in this design
...
```

8.1.3 Static Time Analysis

STA is executed after Synthesis and P&R so the timing estimate is better than the one from Synthesis. From the Listing 3 can be seen the timing constraint used in the simulation and also the simulated value of minimal possible CLK period 11.528 ns which correspond to frequency of 86.75 MHz. The system works on frequency of 50 MHz so there is a significant design margin.

Listing 3: Snippet from STA Report (AAU.twr).

```
...
 Timing constraint: TS_clk = PERIOD TIMEGRP "clk" 50 MHz HIGH 50%;
 For more information, see Period Analysis in the Timing Closure User Guide (
   UG612).
  16427 paths analyzed, 476 endpoints analyzed, 0 failing endpoints
  0 timing errors detected. (0 setup errors, 0 hold errors, 0 component
    switching limit errors)
  Minimum period is  11.528ns.
...
```

A Output Results

Listing 4: tc-au-001.log

```
---------------
REQ_AAU_F_012:
For numbers:  0.01171875 and 0.50000000
Add res. was: 0.51171875, Should be: 0.51171875, raw: 0.51171875
Mul res. was: 0.00390625, Should be: 0.00390625, raw: 0.00585937
PASSED
---------------
REQ_AAU_F_012:
For numbers:  0.01171875 and -0.50000000
Add res. was: -0.48828125, Should be: -0.48828125, raw: -0.48828125
Mul res. was: -0.00781250, Should be: -0.00781250, raw: -0.00585937
PASSED
---------------
REQ_AAU_F_012:
For numbers:  0.01171875 and 0.25000000
Add res. was: 0.26171875, Should be: 0.26171875, raw: 0.26171875
Mul res. was: 0.00000000, Should be: 0.00000000, raw: 0.00292969
PASSED
---------------
REQ_AAU_F_013:
For numbers:  120.00000000 and 90.00000000
Add res. was: 127.99609375, Should be: 127.99609375, raw: 210.00000000
Mul res. was: 127.99609375, Should be: 127.99609375, raw: 10800.00000000
PASSED
---------------
REQ_AAU_F_013:
For numbers:  -90.00000000 and -100.00000000
Add res. was: -128.00000000, Should be: -128.00000000, raw: -190.00000000
Mul res. was: 127.99609375, Should be: 127.99609375, raw: 9000.00000000
PASSED
---------------
REQ_AAU_F_013:
For numbers:  -100.12500000 and 1.50000000
Add res. was: -98.62500000, Should be: -98.62500000, raw: -98.62500000
Mul res. was: -128.00000000, Should be: -128.00000000, raw: -150.18750000
PASSED
---------------
REQ_AAU_F_013:
For numbers:  120.00000000 and 2.00000000
Add res. was: 122.00000000, Should be: 122.00000000, raw: 122.00000000
Mul res. was: 127.99609375, Should be: 127.99609375, raw: 240.00000000
PASSED
```

Listing 5: tc-spi-001.log

```
---------------
REQ_AAU_F_011:
For numbers:  15.12109375 and -3.50000000
In binary:  0000111100011111 and 1111110010000000
Add res. was: 11.62109375, Should be: 11.62109375, raw: 11.62109375
In binary:  0000101110011111
Mul res. was: -52.92578125, Should be: -52.92578125, raw: -52.92382812
In binary:  1100101100010011
PASSED
For requirements verificaton please see output waveform file.
```

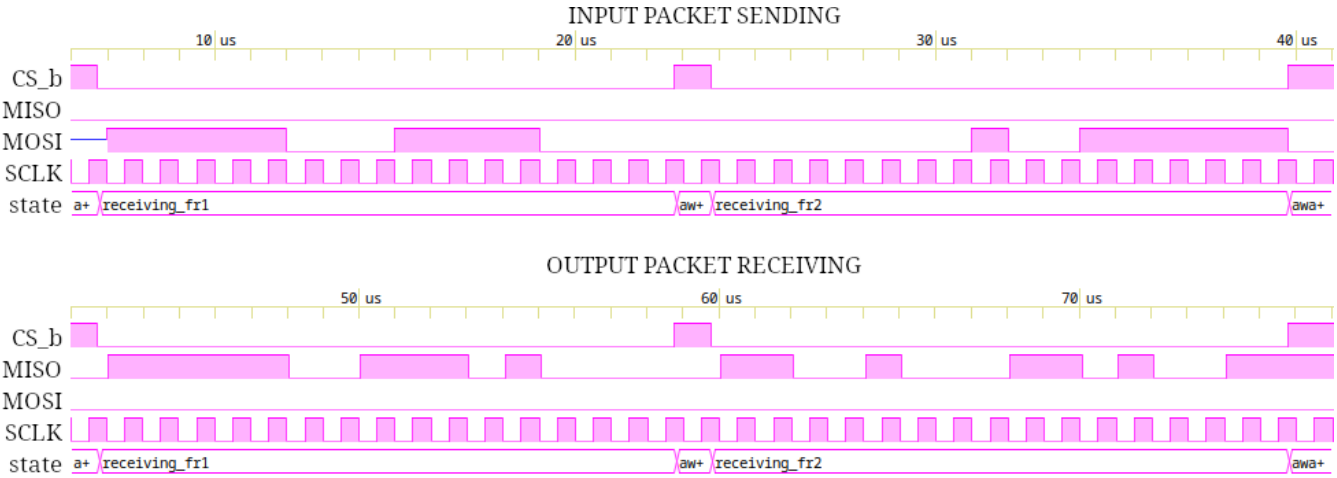

Figure 5: Waveform from tc-spi-001

Listing 6: tc-spi-002.log

```
---------------
REQ_AAU_I_020 for SCLK: 1000000000 fs:
For numbers:  15.12109375 and -3.50000000
Add res. was: 11.62109375, Should be: 11.62109375, raw: 11.62109375
Mul res. was: -52.92578125, Should be: -52.92578125, raw: -52.92382812
PASSED
---------------
REQ_AAU_I_020 for SCLK: 1000000000 fs:
For numbers:  100.25000000 and -40.00000000
Add res. was: 60.25000000, Should be: 60.25000000, raw: 60.25000000
Mul res. was: -128.00000000, Should be: -128.00000000, raw: -4010.00000000
PASSED
---------------
REQ_AAU_I_020 for SCLK: 1000000000 fs:
For numbers:  69.42187500 and 1.69140625
Add res. was: 71.11328125, Should be: 71.11328125, raw: 71.11328125
Mul res. was: 117.41796875, Should be: 117.41796875, raw: 117.42059326
PASSED
---------------
REQ_AAU_I_020 for SCLK: 10000000000 fs:
For numbers:  15.12109375 and -3.50000000
Add res. was: 11.62109375, Should be: 11.62109375, raw: 11.62109375
Mul res. was: -52.92578125, Should be: -52.92578125, raw: -52.92382812
PASSED
---------------
REQ_AAU_I_020 for SCLK: 10000000000 fs:
For numbers:  100.25000000 and -40.00000000
Add res. was: 60.25000000, Should be: 60.25000000, raw: 60.25000000
Mul res. was: -128.00000000, Should be: -128.00000000, raw: -4010.00000000
PASSED
---------------
REQ_AAU_I_020 for SCLK: 10000000000 fs:
For numbers:  69.42187500 and 1.69140625
Add res. was: 71.11328125, Should be: 71.11328125, raw: 71.11328125
Mul res. was: 117.41796875, Should be: 117.41796875, raw: 117.42059326
PASSED
---------------
REQ_AAU_I_020 for SCLK: 100000000000 fs:
For numbers:  15.12109375 and -3.50000000
Add res. was: 11.62109375, Should be: 11.62109375, raw: 11.62109375
Mul res. was: -52.92578125, Should be: -52.92578125, raw: -52.92382812
PASSED
---------------
REQ_AAU_I_020 for SCLK: 100000000000 fs:
For numbers:  100.25000000 and -40.00000000
Add res. was: 60.25000000, Should be: 60.25000000, raw: 60.25000000
Mul res. was: -128.00000000, Should be: -128.00000000, raw: -4010.00000000
PASSED
---------------
REQ_AAU_I_020 for SCLK: 100000000000 fs:
For numbers:  69.42187500 and 1.69140625
Add res. was: 71.11328125, Should be: 71.11328125, raw: 71.11328125
Mul res. was: 117.41796875, Should be: 117.41796875, raw: 117.42059326
PASSED
```

Listing 7: tc-pckctrl-001.log

```
---------------
REQ_AAU_I_022 for bit size 1=16 and bit size 2=16:
For numbers:  6.50000000 and 15.25000000
Add res. was: 21.75000000, Should be: 21.75000000, raw: 21.75000000
Mul res. was: 99.12500000, Should be: 99.12500000, raw: 99.12500000
PASSED
---------------
REQ_AAU_I_022 for bit size 1=8 and bit size 2=8:
For numbers:  6.50000000 and 15.25000000
Add res. was: 0.00000000, Should be: 0.00000000, raw: 21.75000000
Mul res. was: 0.00000000, Should be: 0.00000000, raw: 99.12500000
PASSED
---------------
REQ_AAU_I_022 for bit size 1=16 and bit size 2=8:
For numbers:  6.50000000 and 15.25000000
Add res. was: 0.00000000, Should be: 0.00000000, raw: 21.75000000
Mul res. was: 0.00000000, Should be: 0.00000000, raw: 99.12500000
PASSED
---------------
REQ_AAU_I_022 for bit size 1=20 and bit size 2=20:
For numbers:  6.50000000 and 15.25000000
Add res. was: 0.00000000, Should be: 0.00000000, raw: 21.75000000
Mul res. was: 0.00000000, Should be: 0.00000000, raw: 99.12500000
PASSED
---------------
REQ_AAU_I_022 for bit size 1=8 and bit size 2=16:
For numbers:  6.50000000 and 15.25000000
Add res. was: 0.00000000, Should be: 0.00000000, raw: 21.75000000
Mul res. was: 15.25000000, Should be: 15.25000000, raw: 99.12500000
PASSED
---------------
REQ_AAU_I_023 delay between frames=1200000000000 fs:
For numbers:  6.50000000 and 15.25000000
Add res. was: 0.00000000, Should be: 0.00000000, raw: 21.75000000
Mul res. was: 15.25000000, Should be: 15.25000000, raw: 99.12500000
PASSED
```

B Python script

Listing 8: Script for generating data

```
def main():
    # generate_nbit(4)
    generate_nbit(16, 12)
    # number     <-128, 127.99609375> for n=16
    # tc_au_001 - Correct arithmetic operations
    tc_au_001 = [
        [0.01171875, 0.5, 'REQ_AAU_F_012'], # Number rounding
        [0.01171875, -0.5, 'REQ_AAU_F_012'],# Number rounding
        [0.01171875, 0.25, 'REQ_AAU_F_012'],# Number rounding
        [120.0, 90.0, 'REQ_AAU_F_013'],     # Overflow - Add, Mul oflw
        [-90.0, -100.0, 'REQ_AAU_F_013'],   # Overflow - Add uflw, Mull oflw
        [-100.125, 1.5, 'REQ_AAU_F_013'],   # Overflow - Mul uflw
        [120.0, 2.0, 'REQ_AAU_F_013'],      # Overflow - Mul oflw
    ]
    generate_nbit(16,customDataset=tc_au_001,name='input-data-tc-au-001')
    # tc_spi_001 - Packet and frame format
    tc_spi_001 = [ [15.12109375, -3.50, 'REQ_AAU_F_011'] ]
    generate_nbit(16,customDataset=tc_spi_001,name='input-data-tc-spi-001')
    # tc_spi_002 - desc
    tc_spi_002 = [
        [15.12109375, -3.50, 'REQ_AAU_I_020'],          # Clock freq
        [100.25, -40.0, 'REQ_AAU_I_020'],          # Clock freq
        [69.421875, 1.69140625, 'REQ_AAU_I_020'],          # Clock freq
    ]
    generate_nbit(16,customDataset=tc_spi_002,name='input-data-tc-spi-002')
# Function generates data for assertion in VHDL testbench
# Desired format is fixed point number with decimal point in the middle of the bits
# Parameters:
#   n   ... number of bits for number generation, e.g. for n=4 generated nubers will be between -2 and 1.75
#   nth ... take only 2**nth element (to generate smaller dataset), default 0 (taking every number)
#       ! WARNING: function always taking the last number, does not depend on nth parameter
def generate_nbit(n, nth=0, customDataset=None,name='default'):
    binary_numbers = [(i-(2**n)/2)*2**-(n/2) for i in range(2**n)]
    testCases = []
    if(customDataset==None):
        for i,numA in enumerate(binary_numbers):
            if(i % (2**nth) == 0 or i==(2**n)-1):
                for j,numB in enumerate(binary_numbers):
                    if(j % (2**nth) == 0 or j==(2**n)-1):
                        testCases.append(['NOT_REQ_TEST_',numA,numB,sumNums(numA,numB,n),mulNums(numA,numB,n),numA+numB,numB*numA])
    else:
        for nums in customDataset:
                testCases.append([nums[2],nums[0],nums[1],sumNums(nums[0],nums[1],n),mulNums(nums[0],nums[1],n),nums[0]+nums[1],nums[0]*nums[1]])

    fileName = ""
    if(name == 'default'):
        fileName = f"data_test_{n}_{nth}_bit"
```

```
    else:
        fileName = name
    with open(fileName+'.txt', "w") as file:
        for i in testCases:
            for ii in range(len(i)):
                file.write(f"{i[ii]}\n")

    with open(fileName+"_human.txt", "w") as file:
        for i in testCases:
            file.write(f"{i[0]},{i[1]},{i[2]},{i[3]}\n")

def sumNums(numA:float,numB:float,n:int) -> float:
    min = (0-(2**n)/2)*2**-(n/2)
    max = ((2**n-1)-(2**n)/2)*2**-(n/2)
    sum = numA + numB
    if(sum > max):
        sum = max
    if(sum < min):
        sum = min

    return sum

def mulNums(numA:float,numB:float,n:int) -> float:
    min = (0-(2**n)/2)*2**-(n/2)
    max = ((2**n-1)-(2**n)/2)*2**-(n/2)
    mul = numA * numB
    if(mul > max):
        mul = max
    if(mul < min):
        mul = min

    factor = 2 ** (n / 2)
    floored_result = (mul * factor) // 1 / factor

    if floored_result == -0.0:
        floored_result = 0.0

    return floored_result

if __name__ == '__main__':
    main()s
```

C Design Reports

AAU Project Status (01/14/2024 - 11:11:16)			
Project File:	AAU.xise	**Parser Errors:**	No Errors
Module Name:	AAU	**Implementation State:**	Placed and Routed
Target Device:	xc3s200-5ft256	• **Errors:**	No Errors
Product Version:	ISE 14.7	• **Warnings:**	2 Warnings (0 new)
Design Goal:	Balanced	• **Routing Results:**	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	• **Timing Constraints:**	All Constraints Met
Environment:	System Settings	• **Final Timing Score:**	0 (Timing Report)

Device Utilization Summary [-]				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Flip Flops	129	3,840	3%	
Number of 4 input LUTs	119	3,840	3%	
Number of occupied Slices	102	1,920	5%	
Number of Slices containing only related logic	102	102	100%	
Number of Slices containing unrelated logic	0	102	0%	
Total Number of 4 input LUTs	137	3,840	3%	
Number used as logic	116			
Number used as a route-thru	18			
Number used as Shift registers	3			
Number of bonded IOBs	6	173	3%	
Number of MULT18X18s	1	12	8%	
Number of BUFGMUXs	1	8	12%	
Average Fanout of Non-Clock Nets	3.11			

Performance Summary [-]			
Final Timing Score:	0 (Setup: 0, Hold: 0, Component Switching Limit: 0)	**Pinout Data:**	Pinout Report
Routing Results:	All Signals Completely Routed	**Clock Data:**	Clock Report
Timing Constraints:	All Constraints Met		

Detailed Reports [-]					
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	ne 14. led 11:08:32 2024	0	2 Warnings (0 new)	0
Translation Report	Current	ne 14. led 11:08:49 2024	0	0	0
Map Report	Current	ne 14. led 11:09:05 2024	0	0	2 Infos (0 new)
Place and Route Report	Current	ne 14. led 11:09:15 2024	0	0	0
Power Report					
Post-PAR Static Timing Report	Current	ne 14. led 11:09:22 2024	0	0	5 Infos (0 new)

Figure 6: Xilinx Design Summary (from Xilinx ISE).

Listing 9: Synthesis Report

```
Release 14.7 - xst P.20131013 (nt)
Copyright (c) 1995-2013 Xilinx, Inc.  All rights reserved.
--> Parameter TMPDIR set to xst/projnav.tmp


Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.09 secs

--> Parameter xsthdpdir set to xst


Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.09 secs

--> Reading design: AAU.prj

TABLE OF CONTENTS
  1) Synthesis Options Summary
  2) HDL Compilation
  3) Design Hierarchy Analysis
  4) HDL Analysis
  5) HDL Synthesis
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  6) Advanced HDL Synthesis
     6.1) Advanced HDL Synthesis Report
  7) Low Level Synthesis
  8) Partition Report
  9) Final Report
  9.1) Device utilization summary
  9.2) Partition Resource Summary
  9.3) TIMING REPORT


=========================================================================
*                      Synthesis Options Summary                        *
=========================================================================
---- Source Parameters
Input File Name                    : "AAU.prj"
Input Format                       : mixed
Ignore Synthesis Constraint File   : NO

---- Target Parameters
Output File Name                   : "AAU"
Output Format                      : NGC
Target Device                      : xc3s200-5-ft256

---- Source Options
Top Module Name                    : AAU
Automatic FSM Extraction           : YES
FSM Encoding Algorithm             : Auto
Safe Implementation                : Yes
FSM Style                          : LUT
RAM Extraction                     : Yes
RAM Style                          : Auto
ROM Extraction                     : Yes
```

```
Mux Style                           : Auto
Decoder Extraction                  : YES
Priority Encoder Extraction         : Yes
Shift Register Extraction           : YES
Logical Shifter Extraction          : YES
XOR Collapsing                      : YES
ROM Style                           : Auto
Mux Extraction                      : Yes
Resource Sharing                    : YES
Asynchronous To Synchronous         : NO
Multiplier Style                    : Auto
Automatic Register Balancing        : No

---- Target Options
Add IO Buffers                      : YES
Global Maximum Fanout               : 100000
Add Generic Clock Buffer(BUFG)      : 8
Register Duplication                : YES
Slice Packing                       : YES
Optimize Instantiated Primitives    : NO
Use Clock Enable                    : Yes
Use Synchronous Set                 : Yes
Use Synchronous Reset               : Yes
Pack IO Registers into IOBs         : Auto
Equivalent register Removal         : YES

---- General Options
Optimization Goal                   : Speed
Optimization Effort                 : 1
Keep Hierarchy                      : No
Netlist Hierarchy                   : As_Optimized
RTL Output                          : Yes
Global Optimization                 : AllClockNets
Read Cores                          : YES
Write Timing Constraints            : NO
Cross Clock Analysis                : NO
Hierarchy Separator                 : /
Bus Delimiter                       : <>
Case Specifier                      : Maintain
Slice Utilization Ratio             : 100
BRAM Utilization Ratio              : 100
Verilog 2001                        : YES
Auto BRAM Packing                   : NO
Slice Utilization Ratio Delta       : 5

=========================================================================


=========================================================================
*                          HDL Compilation                              *
=========================================================================
Compiling vhdl file "Z:/home/jakub/Plocha/NDI/Projekt/src/arith_unit/
   n_bit_register.vhd" in Library work.
Architecture behavioral of Entity n_bit_register is up to date.
Compiling vhdl file "Z:/home/jakub/Plocha/NDI/Projekt/src/packet_control/timer.
   vhd" in Library work.
```

```
Architecture behavioral of Entity timer is up to date.
Compiling vhdl file "Z:/home/jakub/Plocha/NDI/Projekt/src/SPI/edge_detector.vhd
    " in Library work.
Architecture behavioral of Entity edge_detector is up to date.
Compiling vhdl file "Z:/home/jakub/Plocha/NDI/Projekt/src/SPI/ser.vhd" in
    Library work.
Architecture behavioral of Entity ser is up to date.
Compiling vhdl file "Z:/home/jakub/Plocha/NDI/Projekt/src/SPI/deser.vhd" in
    Library work.
Architecture behavioral of Entity deser is up to date.
Compiling vhdl file "Z:/home/jakub/Plocha/NDI/Projekt/src/SPI/DDF.vhd" in
    Library work.
Architecture behavioral of Entity ddf is up to date.
Compiling vhdl file "Z:/home/jakub/Plocha/NDI/Projekt/src/SPI/FDAC.vhd" in
    Library work.
Architecture behavioral of Entity fdac is up to date.
Compiling vhdl file "Z:/home/jakub/Plocha/NDI/Projekt/src/SPI/SPI.vhd" in
    Library work.
Architecture behavioral of Entity spi is up to date.
Compiling vhdl file "Z:/home/jakub/Plocha/NDI/Projekt/src/packet_control/
    packet_control.vhd" in Library work.
Architecture behavioral of Entity packet_control is up to date.
Compiling vhdl file "Z:/home/jakub/Plocha/NDI/Projekt/src/arith_unit/arith_unit
    .vhd" in Library work.
Architecture behavioral of Entity arith_unit is up to date.
Compiling vhdl file "Z:/home/jakub/Plocha/NDI/Projekt/src/AAU.vhd" in Library
    work.
Architecture behavioral of Entity aau is up to date.

=========================================================================
*                     Design Hierarchy Analysis                         *
=========================================================================
Analyzing hierarchy for entity <AAU> in library <work> (architecture <
    behavioral>) with generics.
  g_CLK_PERIOD_NS = 20
  g_DATA_SIZE = 16

Analyzing hierarchy for entity <SPI> in library <work> (architecture <
    Behavioral>) with generics.
  g_DATA_SIZE = 16

Analyzing hierarchy for entity <packet_control> in library <work> (architecture
     <Behavioral>) with generics.
  g_CLK_PERIOD_NS = 20
  g_DATA_SIZE = 16

Analyzing hierarchy for entity <arith_unit> in library <work> (architecture <
    Behavioral>) with generics.
  g_DATA_SIZE = 16

Analyzing hierarchy for entity <edge_detector> in library <work> (architecture
    <Behavioral>).

Analyzing hierarchy for entity <ser> in library <work> (architecture <
    Behavioral>) with generics.
  g_DATA_SIZE = 16
```

```
Analyzing hierarchy for entity <deser> in library <work> (architecture <
    Behavioral>) with generics.
  g_DATA_SIZE = 16

Analyzing hierarchy for entity <DDF> in library <work> (architecture <
    Behavioral>).

Analyzing hierarchy for entity <FDAC> in library <work> (architecture <
    Behavioral>) with generics.
  g_DATA_SIZE = 16

Analyzing hierarchy for entity <Timer> in library <work> (architecture <
    Behavioral>) with generics.
  g_CLK_PERIOD_NS = 20
  g_COUNT_TO_MS = 1

Analyzing hierarchy for entity <n_bit_register> in library <work> (architecture
     <Behavioral>) with generics.
  g_DATA_SIZE = 16


=========================================================================
*                            HDL Analysis                               *
=========================================================================
Analyzing generic Entity <AAU> in library <work> (Architecture <behavioral>).
  g_CLK_PERIOD_NS = 20
  g_DATA_SIZE = 16
Entity <AAU> analyzed. Unit <AAU> generated.

Analyzing generic Entity <SPI> in library <work> (Architecture <Behavioral>).
  g_DATA_SIZE = 16
Entity <SPI> analyzed. Unit <SPI> generated.

Analyzing Entity <edge_detector> in library <work> (Architecture <Behavioral>).
Entity <edge_detector> analyzed. Unit <edge_detector> generated.

Analyzing generic Entity <ser> in library <work> (Architecture <Behavioral>).
  g_DATA_SIZE = 16
Entity <ser> analyzed. Unit <ser> generated.

Analyzing generic Entity <deser> in library <work> (Architecture <Behavioral>).
  g_DATA_SIZE = 16
Entity <deser> analyzed. Unit <deser> generated.

Analyzing Entity <DDF> in library <work> (Architecture <Behavioral>).
Entity <DDF> analyzed. Unit <DDF> generated.

Analyzing generic Entity <FDAC> in library <work> (Architecture <Behavioral>).
  g_DATA_SIZE = 16
Entity <FDAC> analyzed. Unit <FDAC> generated.

Analyzing generic Entity <packet_control> in library <work> (Architecture <
    Behavioral>).
  g_CLK_PERIOD_NS = 20
  g_DATA_SIZE = 16
```

```
Entity <packet_control> analyzed. Unit <packet_control> generated.

Analyzing generic Entity <Timer> in library <work> (Architecture <Behavioral>).
  g_CLK_PERIOD_NS = 20
  g_COUNT_TO_MS = 1
Entity <Timer> analyzed. Unit <Timer> generated.

Analyzing generic Entity <arith_unit> in library <work> (Architecture <
   Behavioral>).
  g_DATA_SIZE = 16
Entity <arith_unit> analyzed. Unit <arith_unit> generated.

Analyzing generic Entity <n_bit_register> in library <work> (Architecture <
   Behavioral>).
  g_DATA_SIZE = 16
Entity <n_bit_register> analyzed. Unit <n_bit_register> generated.


=========================================================================
*                            HDL Synthesis                              *
=========================================================================

Performing bidirectional port resolution...

Synthesizing Unit <edge_detector>.
    Related source file is "Z:/home/jakub/Plocha/NDI/Projekt/src/SPI/
   edge_detector.vhd".
    Found 1-bit register for signal <reg_s>.
    Summary:
  inferred   1 D-type flip-flop(s).
Unit <edge_detector> synthesized.


Synthesizing Unit <ser>.
    Related source file is "Z:/home/jakub/Plocha/NDI/Projekt/src/SPI/ser.vhd".
    Found 17-bit register for signal <reg_q>.
    Summary:
  inferred  17 D-type flip-flop(s).
Unit <ser> synthesized.


Synthesizing Unit <deser>.
    Related source file is "Z:/home/jakub/Plocha/NDI/Projekt/src/SPI/deser.vhd
   ".
    Found 16-bit register for signal <reg_q>.
    Summary:
  inferred  16 D-type flip-flop(s).
Unit <deser> synthesized.


Synthesizing Unit <DDF>.
    Related source file is "Z:/home/jakub/Plocha/NDI/Projekt/src/SPI/DDF.vhd".
    Found 1-bit register for signal <reg_q1>.
    Found 1-bit register for signal <reg_q2>.
    Summary:
  inferred   2 D-type flip-flop(s).
```

```
Unit <DDF> synthesized.


Synthesizing Unit <FDAC>.
    Related source file is "Z:/home/jakub/Plocha/NDI/Projekt/src/SPI/FDAC.vhd".
    Found 5-bit up counter for signal <cnt_q>.
    Summary:
  inferred   1 Counter(s).
Unit <FDAC> synthesized.


Synthesizing Unit <Timer>.
    Related source file is "Z:/home/jakub/Plocha/NDI/Projekt/src/packet_control
   /timer.vhd".
    Found 1-bit register for signal <flag>.
    Found 17-bit up counter for signal <cnt_q>.
    Found 17-bit comparator less for signal <flag$cmp_lt0000> created at line
   30.
    Summary:
  inferred   1 Counter(s).
  inferred   1 D-type flip-flop(s).
  inferred   1 Comparator(s).
Unit <Timer> synthesized.


Synthesizing Unit <n_bit_register>.
    Related source file is "Z:/home/jakub/Plocha/NDI/Projekt/src/arith_unit/
   n_bit_register.vhd".
    Found 16-bit register for signal <reg_q>.
    Summary:
  inferred  16 D-type flip-flop(s).
Unit <n_bit_register> synthesized.


Synthesizing Unit <SPI>.
    Related source file is "Z:/home/jakub/Plocha/NDI/Projekt/src/SPI/SPI.vhd".
Unit <SPI> synthesized.


Synthesizing Unit <packet_control>.
    Related source file is "Z:/home/jakub/Plocha/NDI/Projekt/src/packet_control
   /packet_control.vhd".
    Found finite state machine <FSM_0> for signal <current_state>.
    -----------------------------------------------------------------------
    | States             | 4                                              |
    | Transitions        | 10                                             |
    | Inputs             | 4                                              |
    | Outputs            | 5                                              |
    | Clock              | clk                       (rising_edge)        |
    | Reset              | rst                       (positive)           |
    | Reset type         | synchronous                                    |
    | Reset State        | await_fr1                                      |
    | Power Up State     | await_fr1                                      |
    | Recovery State     | await_fr1                                      |
    | Encoding           | automatic                                      |
    | Implementation     | LUT                                            |
```

```
    ----------------------------------------------------------------------
    Summary:
  inferred   1 Finite State Machine(s).
Unit <packet_control> synthesized.


Synthesizing Unit <arith_unit>.
    Related source file is "Z:/home/jakub/Plocha/NDI/Projekt/src/arith_unit/
   arith_unit.vhd".
WARNING:Xst:646 - Signal <sig_mul_res<7:0>> is assigned but never used. This
   unconnected signal will be trimmed during the optimization process.
WARNING:Xst:646 - Signal <sig_add_res<16>> is assigned but never used. This
   unconnected signal will be trimmed during the optimization process.
    Found 17-bit adder for signal <sig_add_res>.
    Found 16x16-bit multiplier for signal <sig_mul_res>.
    Found 9-bit comparator greater for signal <sig_mul_res_reg_d$cmp_gt0000>
   created at line 120.
    Found 1-bit xor2 for signal <sig_mul_res_reg_d$xor0000> created at line
   120.
    Summary:
  inferred   1 Adder/Subtractor(s).
  inferred   1 Multiplier(s).
  inferred   1 Comparator(s).
Unit <arith_unit> synthesized.


Synthesizing Unit <AAU>.
    Related source file is "Z:/home/jakub/Plocha/NDI/Projekt/src/AAU.vhd".
Unit <AAU> synthesized.


=========================================================================
HDL Synthesis Report

Macro Statistics
# Multipliers                                          : 1
 16x16-bit multiplier                                  : 1
# Adders/Subtractors                                   : 1
 17-bit adder                                          : 1
# Counters                                             : 2
 17-bit up counter                                     : 1
 5-bit up counter                                      : 1
# Registers                                            : 15
 1-bit register                                        : 9
 16-bit register                                       : 5
 17-bit register                                       : 1
# Comparators                                          : 2
 17-bit comparator less                                : 1
 9-bit comparator greater                              : 1
# Xors                                                 : 1
 1-bit xor2                                            : 1

=========================================================================

=========================================================================
*                      Advanced HDL Synthesis                           *
```

```
=========================================================================

Analyzing FSM <FSM_0> for best encoding.
Optimizing FSM <Packet_control/current_state/FSM> on signal <current_state
   [1:2]> with user encoding.
---------------------------
 State          | Encoding
---------------------------
 await_fr1      | 00
 receiving_fr1  | 01
 await_fr2      | 10
 receiving_fr2  | 11
---------------------------

=========================================================================
Advanced HDL Synthesis Report

Macro Statistics
# FSMs                                                 : 1
# Multipliers                                          : 1
 16x16-bit multiplier                                  : 1
# Adders/Subtractors                                   : 1
 16-bit adder                                          : 1
# Counters                                             : 2
 17-bit up counter                                     : 1
 5-bit up counter                                      : 1
# Registers                                            : 106
 Flip-Flops                                            : 106
# Comparators                                          : 2
 17-bit comparator less                                : 1
 9-bit comparator greater                              : 1
# Xors                                                 : 1
 1-bit xor2                                            : 1

=========================================================================

=========================================================================
*                         Low Level Synthesis                           *
=========================================================================

Optimizing unit <AAU> ...

Optimizing unit <ser> ...

Optimizing unit <deser> ...

Optimizing unit <n_bit_register> ...

Optimizing unit <SPI> ...

Optimizing unit <packet_control> ...

Optimizing unit <arith_unit> ...

Mapping all equations...
Building and optimizing final netlist ...
```

```
Found area constraint ratio of 100 (+ 5) on block AAU, actual ratio is 5.
FlipFlop Arith_unit/Data_fr1_reg/reg_q_15 has been replicated 1 time(s)
FlipFlop Arith_unit/Data_fr2_reg/reg_q_15 has been replicated 1 time(s)

Final Macro Processing ...

Processing Unit <AAU> :
  Found 2-bit shift register for signal <SPI/CS_b_DDF/reg_q2>.
  Found 2-bit shift register for signal <SPI/SCLK_DDF/reg_q2>.
  Found 2-bit shift register for signal <SPI/MOSI_DDF/reg_q2>.
Unit <AAU> processed.

=========================================================================
Final Register Report

Macro Statistics
# Registers                                          : 126
 Flip-Flops                                          : 126
# Shift Registers                                    : 3
 2-bit shift register                                : 3

=========================================================================

=========================================================================
*                            Partition Report                           *
=========================================================================

Partition Implementation Status
-------------------------------

  No Partitions were found in this design.

-------------------------------

=========================================================================
*                             Final Report                              *
=========================================================================
Final Results
RTL Top Level Output File Name     : AAU.ngr
Top Level Output File Name         : AAU
Output Format                      : NGC
Optimization Goal                  : Speed
Keep Hierarchy                     : No

Design Statistics
# IOs                              : 6

Cell Usage :
# BELS                             : 212
#      GND                         : 1
#      INV                         : 5
#      LUT1                        : 18
#      LUT2                        : 24
#      LUT2_D                      : 1
#      LUT2_L                      : 1
#      LUT3                        : 21
```

```
#      LUT3_L                            : 16
#      LUT4                              : 48
#      LUT4_D                            : 1
#      MUXCY                             : 39
#      MUXF5                             : 3
#      VCC                               : 1
#      XORCY                             : 33
# FlipFlops/Latches                      : 129
#      FD                                : 5
#      FDR                               : 18
#      FDRE                              : 104
#      FDRSE                             : 1
#      FDSE                              : 1
# Shift Registers                        : 3
#      SRL16                             : 3
# Clock Buffers                          : 1
#      BUFGP                             : 1
# IO Buffers                             : 5
#      IBUF                              : 4
#      OBUF                              : 1
# MULTs                                  : 1
#      MULT18X18                         : 1
=========================================================================

Device utilization summary:
---------------------------

Selected Device : 3s200ft256-5

 Number of Slices:                       99  out of   1920     5%
 Number of Slice Flip Flops:            129  out of   3840     3%
 Number of 4 input LUTs:                138  out of   3840     3%
    Number used as logic:               135
    Number used as Shift registers:       3
 Number of IOs:                           6
 Number of bonded IOBs:                   6  out of    173     3%
 Number of MULT18X18s:                    1  out of     12     8%
 Number of GCLKs:                         1  out of      8    12%

---------------------------
Partition Resource Summary:
---------------------------

  No Partitions were found in this design.

---------------------------


=========================================================================
TIMING REPORT

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.

Clock Information:
```

```
------------------
-----------------------------------+-------------------------+-------+
Clock Signal                       | Clock buffer(FF name)   | Load  |
-----------------------------------+-------------------------+-------+
clk                                | BUFGP                   | 132   |
-----------------------------------+-------------------------+-------+

Asynchronous Control Signals Information:
----------------------------------------
No asynchronous control signals found in this design

Timing Summary:
---------------
Speed Grade: -5

   Minimum period: 9.952ns (Maximum Frequency: 100.480MHz)
   Minimum input arrival time before clock: 6.035ns
   Maximum output required time after clock: 6.216ns
   Maximum combinational path delay: No path found

Timing Detail:
--------------
All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default period analysis for Clock 'clk'
  Clock period: 9.952ns (frequency: 100.480MHz)
  Total number of paths / destination ports: 16430 / 307
-------------------------------------------------------------------------
Delay:               9.952ns (Levels of Logic = 4)
  Source:            Arith_unit/Data_fr1_reg/reg_q_15_1 (FF)
  Destination:       Arith_unit/Data_mul_res_reg/reg_q_0 (FF)
  Source Clock:      clk rising
  Destination Clock: clk rising

  Data Path: Arith_unit/Data_fr1_reg/reg_q_15_1 to Arith_unit/Data_mul_res_reg/
   reg_q_0
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDRE:C->Q             3   0.626   0.771  Arith_unit/Data_fr1_reg/
   reg_q_15_1 (Arith_unit/Data_fr1_reg/reg_q_15_1)
     MULT18X18:A17->P29    3   4.098   1.066  Arith_unit/Mmult_sig_mul_res (
   Arith_unit/sig_mul_res<29>)
     LUT3:I0->O            1   0.479   0.704  Arith_unit/
   sig_mul_res_reg_d_and000132 (Arith_unit/sig_mul_res_reg_d_and000132)
     LUT4:I3->O           16   0.479   1.074  Arith_unit/
   sig_mul_res_reg_d_and000182 (Arith_unit/sig_mul_res_reg_d_and000182)
     LUT4:I3->O            1   0.479   0.000  Arith_unit/sig_mul_res_reg_d<9>1
   (Arith_unit/sig_mul_res_reg_d<9>)
     FDRE:D                    0.176          Arith_unit/Data_mul_res_reg/
   reg_q_9
    ----------------------------------------
    Total                      9.952ns (6.337ns logic, 3.615ns route)
                                       (63.7% logic, 36.3% route)
```

```
=========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'clk'
  Total number of paths / destination ports: 170 / 104
-------------------------------------------------------------------------
Offset:              6.035ns (Levels of Logic = 3)
  Source:            rst (PAD)
  Destination:       Arith_unit/Data_fr1_reg/reg_q_0 (FF)
  Destination Clock: clk rising

  Data Path: rst to Arith_unit/Data_fr1_reg/reg_q_0
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             37   0.715   1.894  rst_IBUF (rst_IBUF)
     LUT3:I0->O             1   0.479   0.000  sig_arith_rst2 (sig_arith_rst2)
     MUXF5:I0->O           66   0.314   1.741  sig_arith_rst_f5 (sig_arith_rst)
     FDRE:R                     0.892          Arith_unit/Data_mul_res_reg/
   reg_q_0
    ----------------------------------------
    Total                      6.035ns (2.400ns logic, 3.635ns route)
                                       (39.8% logic, 60.2% route)

=========================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'
  Total number of paths / destination ports: 1 / 1
-------------------------------------------------------------------------
Offset:              6.216ns (Levels of Logic = 1)
  Source:            SPI/Serializer/reg_q_0 (FF)
  Destination:       MISO (PAD)
  Source Clock:      clk rising

  Data Path: SPI/Serializer/reg_q_0 to MISO
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDRE:C->Q             1   0.626   0.681  SPI/Serializer/reg_q_0 (SPI/
   Serializer/reg_q_0)
     OBUF:I->O                  4.909          MISO_OBUF (MISO)
    ----------------------------------------
    Total                      6.216ns (5.535ns logic, 0.681ns route)
                                       (89.0% logic, 11.0% route)

=========================================================================


Total REAL time to Xst completion: 3.00 secs
Total CPU time to Xst completion: 3.14 secs

-->

Total memory usage is 123756 kilobytes

Number of errors   :    0 (   0 filtered)
Number of warnings :    2 (   0 filtered)
Number of infos    :    0 (   0 filtered)
```

Listing 10: STA Report

```
--------------------------------------------------------------------------------

Release 14.7 Trace  (nt)
Copyright (c) 1995-2013 Xilinx, Inc.  All rights reserved.

C:\xilinx\14.7\ISE_DS\ISE\bin\nt\unwrapped\trce.exe -intstyle ise -v 3 -s 5 -n
3 -fastpaths -xml AAU.twx AAU.ncd -o AAU.twr AAU.pcf -ucf AAU.ucf -ucf SPI.ucf

Design file:              AAU.ncd
Physical constraint file: AAU.pcf
Device,package,speed:     xc3s200,ft256,-5 (PRODUCTION 1.39 2013-10-13)
Report level:             verbose report

Environment Variable      Effect
--------------------      ------
NONE                      No environment variables were set
--------------------------------------------------------------------------------


INFO:Timing:3412 - To improve timing, see the Timing Closure User Guide (UG612)
   .
INFO:Timing:2752 - To get complete path coverage, use the unconstrained paths
   option. All paths that are not constrained will be reported in the
   unconstrained paths section(s) of the report.
INFO:Timing:3339 - The clock-to-out numbers in this timing report are based on
   a 50 Ohm transmission line loading model.  For the details of this model,
   and for more information on accounting for different loading conditions,
   please see the device datasheet.
INFO:Timing:3390 - This architecture does not support a default System Jitter
   value, please add SYSTEM_JITTER constraint to the UCF to modify the Clock
   Uncertainty calculation.
INFO:Timing:3389 - This architecture does not support 'Discrete Jitter' and
   'Phase Error' calculations, these terms will be zero in the Clock
   Uncertainty calculation.  Please make appropriate modification to
   SYSTEM_JITTER to account for the unsupported Discrete Jitter and Phase
   Error.

================================================================================

Timing constraint: TS_clk = PERIOD TIMEGRP "clk" 50 MHz HIGH 50%;
For more information, see Period Analysis in the Timing Closure User Guide (
   UG612).

 16427 paths analyzed, 476 endpoints analyzed, 0 failing endpoints
 0 timing errors detected. (0 setup errors, 0 hold errors, 0 component
   switching limit errors)
 Minimum period is  11.528ns.
--------------------------------------------------------------------------------


Paths for end point Arith_unit/Data_mul_res_reg/reg_q_2 (SLICE_X36Y23.G1), 468
   paths
--------------------------------------------------------------------------------

Slack (setup path):     8.472ns (requirement - (data path - clock path skew +
```

```
   uncertainty))
  Source:               Arith_unit/Data_fr1_reg/reg_q_13 (FF)
  Destination:          Arith_unit/Data_mul_res_reg/reg_q_2 (FF)
  Requirement:          20.000ns
  Data Path Delay:      11.526ns (Levels of Logic = 4)
  Clock Path Skew:      -0.002ns (0.380 - 0.382)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Destination Clock:    clk_BUFGP rising at 20.000ns
  Clock Uncertainty:    0.000ns

  Maximum Data Path: Arith_unit/Data_fr1_reg/reg_q_13 to Arith_unit/
   Data_mul_res_reg/reg_q_2
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X33Y30.XQ      Tcko                  0.626   Arith_unit/Data_fr1_reg/
   reg_q<13>
                                                       Arith_unit/Data_fr1_reg/
   reg_q_13
    MULT18X18_X1Y3.A13   net (fanout=2)        2.087   Arith_unit/Data_fr1_reg/
   reg_q<13>
    MULT18X18_X1Y3.P24   Tmult                 3.790   Arith_unit/
   Mmult_sig_mul_res
                                                       Arith_unit/
   Mmult_sig_mul_res
    SLICE_X37Y31.G2      net (fanout=2)        1.806   Arith_unit/sig_mul_res
   <24>
    SLICE_X37Y31.Y       Tilo                  0.479   Arith_unit/
   sig_mul_res_reg_d_and00004
                                                       Arith_unit/
   sig_mul_res_reg_d_and000121
    SLICE_X37Y30.F1      net (fanout=1)        0.482   Arith_unit/
   sig_mul_res_reg_d_and000121
    SLICE_X37Y30.X       Tilo                  0.479   Arith_unit/
   sig_mul_res_reg_d_and000182
                                                       Arith_unit/
   sig_mul_res_reg_d_and000182
    SLICE_X36Y23.G1      net (fanout=16)       1.177   Arith_unit/
   sig_mul_res_reg_d_and000182
    SLICE_X36Y23.CLK     Tgck                  0.600   Arith_unit/
   Data_mul_res_reg/reg_q<3>
                                                       Arith_unit/
   sig_mul_res_reg_d<2>1
                                                       Arith_unit/
   Data_mul_res_reg/reg_q_2
    ---------------------------------------------------
   ---------------------------
    Total                                    11.526ns (5.974ns logic, 5.552ns
   route)
                                                       (51.8% logic, 48.2%
   route)

--------------------------------------------------------------------------------

Slack (setup path):     8.610ns (requirement - (data path - clock path skew +
   uncertainty))
```

```
  Source:               Arith_unit/Data_fr2_reg/reg_q_5 (FF)
  Destination:          Arith_unit/Data_mul_res_reg/reg_q_2 (FF)
  Requirement:          20.000ns
  Data Path Delay:      11.387ns (Levels of Logic = 4)
  Clock Path Skew:      -0.003ns (0.380 - 0.383)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Destination Clock:    clk_BUFGP rising at 20.000ns
  Clock Uncertainty:    0.000ns

  Maximum Data Path: Arith_unit/Data_fr2_reg/reg_q_5 to Arith_unit/
   Data_mul_res_reg/reg_q_2
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ----------------------------------------------------  -------------------
    SLICE_X36Y25.XQ      Tcko                  0.626   Arith_unit/Data_fr2_reg/
   reg_q<5>
                                                       Arith_unit/Data_fr2_reg/
   reg_q_5
    MULT18X18_X1Y3.B5    net (fanout=2)        1.948   Arith_unit/Data_fr2_reg/
   reg_q<5>
    MULT18X18_X1Y3.P24   Tmult                 3.790   Arith_unit/
   Mmult_sig_mul_res
                                                       Arith_unit/
   Mmult_sig_mul_res
    SLICE_X37Y31.G2      net (fanout=2)        1.806   Arith_unit/sig_mul_res
   <24>
    SLICE_X37Y31.Y       Tilo                  0.479   Arith_unit/
   sig_mul_res_reg_d_and00004
                                                       Arith_unit/
   sig_mul_res_reg_d_and000121
    SLICE_X37Y30.F1      net (fanout=1)        0.482   Arith_unit/
   sig_mul_res_reg_d_and000121
    SLICE_X37Y30.X       Tilo                  0.479   Arith_unit/
   sig_mul_res_reg_d_and000182
                                                       Arith_unit/
   sig_mul_res_reg_d_and000182
    SLICE_X36Y23.G1      net (fanout=16)       1.177   Arith_unit/
   sig_mul_res_reg_d_and000182
    SLICE_X36Y23.CLK     Tgck                  0.600   Arith_unit/
   Data_mul_res_reg/reg_q<3>
                                                       Arith_unit/
   sig_mul_res_reg_d<2>1
                                                       Arith_unit/
   Data_mul_res_reg/reg_q_2
    ----------------------------------------------------
   ---------------------------
    Total                                    11.387ns (5.974ns logic, 5.413ns
   route)
                                                       (52.5% logic, 47.5%
   route)

--------------------------------------------------------------------------------

Slack (setup path):     8.862ns (requirement - (data path - clock path skew +
   uncertainty))
  Source:               Arith_unit/Data_fr2_reg/reg_q_4 (FF)
```

```
  Destination:            Arith_unit/Data_mul_res_reg/reg_q_2 (FF)
  Requirement:            20.000ns
  Data Path Delay:        11.135ns (Levels of Logic = 4)
  Clock Path Skew:        -0.003ns (0.380 - 0.383)
  Source Clock:           clk_BUFGP rising at 0.000ns
  Destination Clock:      clk_BUFGP rising at 20.000ns
  Clock Uncertainty:      0.000ns

  Maximum Data Path: Arith_unit/Data_fr2_reg/reg_q_4 to Arith_unit/
   Data_mul_res_reg/reg_q_2
    Location              Delay type         Delay(ns)  Physical Resource
                                                        Logical Resource(s)
    ----------------------------------------------------  -------------------
    SLICE_X36Y25.YQ       Tcko                  0.626   Arith_unit/Data_fr2_reg/
   reg_q<5>
                                                        Arith_unit/Data_fr2_reg/
   reg_q_4
    MULT18X18_X1Y3.B4     net (fanout=2)        1.696   Arith_unit/Data_fr2_reg/
   reg_q<4>
    MULT18X18_X1Y3.P24    Tmult                 3.790   Arith_unit/
   Mmult_sig_mul_res
                                                        Arith_unit/
   Mmult_sig_mul_res
    SLICE_X37Y31.G2       net (fanout=2)        1.806   Arith_unit/sig_mul_res
   <24>
    SLICE_X37Y31.Y        Tilo                  0.479   Arith_unit/
   sig_mul_res_reg_d_and00004
                                                        Arith_unit/
   sig_mul_res_reg_d_and000121
    SLICE_X37Y30.F1       net (fanout=1)        0.482   Arith_unit/
   sig_mul_res_reg_d_and000121
    SLICE_X37Y30.X        Tilo                  0.479   Arith_unit/
   sig_mul_res_reg_d_and000182
                                                        Arith_unit/
   sig_mul_res_reg_d_and000182
    SLICE_X36Y23.G1       net (fanout=16)       1.177   Arith_unit/
   sig_mul_res_reg_d_and000182
    SLICE_X36Y23.CLK      Tgck                  0.600   Arith_unit/
   Data_mul_res_reg/reg_q<3>
                                                        Arith_unit/
   sig_mul_res_reg_d<2>1
                                                        Arith_unit/
   Data_mul_res_reg/reg_q_2
    ----------------------------------------------------
   ----------------------------
    Total                                    11.135ns (5.974ns logic, 5.161ns
   route)
                                                        (53.7% logic, 46.3%
   route)

--------------------------------------------------------------------------------


Paths for end point Arith_unit/Data_mul_res_reg/reg_q_3 (SLICE_X36Y23.F1), 468
   paths
--------------------------------------------------------------------------------
```

```
Slack (setup path):     8.485ns (requirement - (data path - clock path skew +
   uncertainty))
  Source:               Arith_unit/Data_fr1_reg/reg_q_13 (FF)
  Destination:          Arith_unit/Data_mul_res_reg/reg_q_3 (FF)
  Requirement:          20.000ns
  Data Path Delay:      11.513ns (Levels of Logic = 4)
  Clock Path Skew:      -0.002ns (0.380 - 0.382)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Destination Clock:    clk_BUFGP rising at 20.000ns
  Clock Uncertainty:    0.000ns

  Maximum Data Path: Arith_unit/Data_fr1_reg/reg_q_13 to Arith_unit/
   Data_mul_res_reg/reg_q_3
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X33Y30.XQ      Tcko                  0.626   Arith_unit/Data_fr1_reg/
   reg_q<13>
                                                       Arith_unit/Data_fr1_reg/
   reg_q_13
    MULT18X18_X1Y3.A13   net (fanout=2)        2.087   Arith_unit/Data_fr1_reg/
   reg_q<13>
    MULT18X18_X1Y3.P24   Tmult                 3.790   Arith_unit/
   Mmult_sig_mul_res
                                                       Arith_unit/
   Mmult_sig_mul_res
    SLICE_X37Y31.G2      net (fanout=2)        1.806   Arith_unit/sig_mul_res
   <24>
    SLICE_X37Y31.Y       Tilo                  0.479   Arith_unit/
   sig_mul_res_reg_d_and00004
                                                       Arith_unit/
   sig_mul_res_reg_d_and000121
    SLICE_X37Y30.F1      net (fanout=1)        0.482   Arith_unit/
   sig_mul_res_reg_d_and000121
    SLICE_X37Y30.X       Tilo                  0.479   Arith_unit/
   sig_mul_res_reg_d_and000182
                                                       Arith_unit/
   sig_mul_res_reg_d_and000182
    SLICE_X36Y23.F1      net (fanout=16)       1.164   Arith_unit/
   sig_mul_res_reg_d_and000182
    SLICE_X36Y23.CLK     Tfck                  0.600   Arith_unit/
   Data_mul_res_reg/reg_q<3>
                                                       Arith_unit/
   sig_mul_res_reg_d<3>1
                                                       Arith_unit/
   Data_mul_res_reg/reg_q_3
    ---------------------------------------------------
   ---------------------------
    Total                                    11.513ns (5.974ns logic, 5.539ns
   route)
                                                       (51.9% logic, 48.1%
   route)

--------------------------------------------------------------------------------
```

```
Slack (setup path):     8.623ns (requirement - (data path - clock path skew +
   uncertainty))
  Source:               Arith_unit/Data_fr2_reg/reg_q_5 (FF)
  Destination:          Arith_unit/Data_mul_res_reg/reg_q_3 (FF)
  Requirement:          20.000ns
  Data Path Delay:      11.374ns (Levels of Logic = 4)
  Clock Path Skew:      -0.003ns (0.380 - 0.383)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Destination Clock:    clk_BUFGP rising at 20.000ns
  Clock Uncertainty:    0.000ns

  Maximum Data Path: Arith_unit/Data_fr2_reg/reg_q_5 to Arith_unit/
   Data_mul_res_reg/reg_q_3
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X36Y25.XQ      Tcko                  0.626   Arith_unit/Data_fr2_reg/
   reg_q<5>
                                                       Arith_unit/Data_fr2_reg/
   reg_q_5
    MULT18X18_X1Y3.B5    net (fanout=2)        1.948   Arith_unit/Data_fr2_reg/
   reg_q<5>
    MULT18X18_X1Y3.P24   Tmult                 3.790   Arith_unit/
   Mmult_sig_mul_res
                                                       Arith_unit/
   Mmult_sig_mul_res
    SLICE_X37Y31.G2      net (fanout=2)        1.806   Arith_unit/sig_mul_res
   <24>
    SLICE_X37Y31.Y       Tilo                  0.479   Arith_unit/
   sig_mul_res_reg_d_and00004
                                                       Arith_unit/
   sig_mul_res_reg_d_and000121
    SLICE_X37Y30.F1      net (fanout=1)        0.482   Arith_unit/
   sig_mul_res_reg_d_and000121
    SLICE_X37Y30.X       Tilo                  0.479   Arith_unit/
   sig_mul_res_reg_d_and000182
                                                       Arith_unit/
   sig_mul_res_reg_d_and000182
    SLICE_X36Y23.F1      net (fanout=16)       1.164   Arith_unit/
   sig_mul_res_reg_d_and000182
    SLICE_X36Y23.CLK     Tfck                  0.600   Arith_unit/
   Data_mul_res_reg/reg_q<3>
                                                       Arith_unit/
   sig_mul_res_reg_d<3>1
                                                       Arith_unit/
   Data_mul_res_reg/reg_q_3
    -------------------------------------------------
   ----------------------------
    Total                                    11.374ns (5.974ns logic, 5.400ns
   route)
                                                       (52.5% logic, 47.5%
   route)

--------------------------------------------------------------------------------

Slack (setup path):     8.875ns (requirement - (data path - clock path skew +
```

```
  uncertainty))
  Source:               Arith_unit/Data_fr2_reg/reg_q_4 (FF)
  Destination:          Arith_unit/Data_mul_res_reg/reg_q_3 (FF)
  Requirement:          20.000ns
  Data Path Delay:      11.122ns (Levels of Logic = 4)
  Clock Path Skew:      -0.003ns (0.380 - 0.383)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Destination Clock:    clk_BUFGP rising at 20.000ns
  Clock Uncertainty:    0.000ns

  Maximum Data Path: Arith_unit/Data_fr2_reg/reg_q_4 to Arith_unit/
   Data_mul_res_reg/reg_q_3
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X36Y25.YQ      Tcko                  0.626   Arith_unit/Data_fr2_reg/
   reg_q<5>
                                                       Arith_unit/Data_fr2_reg/
   reg_q_4
    MULT18X18_X1Y3.B4    net (fanout=2)        1.696   Arith_unit/Data_fr2_reg/
   reg_q<4>
    MULT18X18_X1Y3.P24   Tmult                 3.790   Arith_unit/
   Mmult_sig_mul_res
                                                       Arith_unit/
   Mmult_sig_mul_res
    SLICE_X37Y31.G2      net (fanout=2)        1.806   Arith_unit/sig_mul_res
   <24>
    SLICE_X37Y31.Y       Tilo                  0.479   Arith_unit/
   sig_mul_res_reg_d_and00004
                                                       Arith_unit/
   sig_mul_res_reg_d_and000121
    SLICE_X37Y30.F1      net (fanout=1)        0.482   Arith_unit/
   sig_mul_res_reg_d_and000121
    SLICE_X37Y30.X       Tilo                  0.479   Arith_unit/
   sig_mul_res_reg_d_and000182
                                                       Arith_unit/
   sig_mul_res_reg_d_and000182
    SLICE_X36Y23.F1      net (fanout=16)       1.164   Arith_unit/
   sig_mul_res_reg_d_and000182
    SLICE_X36Y23.CLK     Tfck                  0.600   Arith_unit/
   Data_mul_res_reg/reg_q<3>
                                                       Arith_unit/
   sig_mul_res_reg_d<3>1
                                                       Arith_unit/
   Data_mul_res_reg/reg_q_3
    ---------------------------------------------------
   ---------------------------
    Total                                    11.122ns (5.974ns logic, 5.148ns
   route)
                                                       (53.7% logic, 46.3%
   route)

--------------------------------------------------------------------------------


Paths for end point Arith_unit/Data_mul_res_reg/reg_q_4 (SLICE_X38Y26.G4), 468
```

```
   paths
--------------------------------------------------------------------------------

Slack (setup path):     8.497ns (requirement - (data path - clock path skew +
   uncertainty))
  Source:               Arith_unit/Data_fr1_reg/reg_q_13 (FF)
  Destination:          Arith_unit/Data_mul_res_reg/reg_q_4 (FF)
  Requirement:          20.000ns
  Data Path Delay:      11.501ns (Levels of Logic = 4)
  Clock Path Skew:      -0.002ns (0.123 - 0.125)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Destination Clock:    clk_BUFGP rising at 20.000ns
  Clock Uncertainty:    0.000ns

  Maximum Data Path: Arith_unit/Data_fr1_reg/reg_q_13 to Arith_unit/
   Data_mul_res_reg/reg_q_4
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X33Y30.XQ      Tcko                  0.626   Arith_unit/Data_fr1_reg/
   reg_q<13>
                                                       Arith_unit/Data_fr1_reg/
   reg_q_13
    MULT18X18_X1Y3.A13   net (fanout=2)        2.087   Arith_unit/Data_fr1_reg/
   reg_q<13>
    MULT18X18_X1Y3.P24   Tmult                 3.790   Arith_unit/
   Mmult_sig_mul_res
                                                       Arith_unit/
   Mmult_sig_mul_res
    SLICE_X37Y31.G2      net (fanout=2)        1.806   Arith_unit/sig_mul_res
   <24>
    SLICE_X37Y31.Y       Tilo                  0.479   Arith_unit/
   sig_mul_res_reg_d_and00004
                                                       Arith_unit/
   sig_mul_res_reg_d_and000121
    SLICE_X37Y30.F1      net (fanout=1)        0.482   Arith_unit/
   sig_mul_res_reg_d_and000121
    SLICE_X37Y30.X       Tilo                  0.479   Arith_unit/
   sig_mul_res_reg_d_and000182
                                                       Arith_unit/
   sig_mul_res_reg_d_and000182
    SLICE_X38Y26.G4      net (fanout=16)       1.152   Arith_unit/
   sig_mul_res_reg_d_and000182
    SLICE_X38Y26.CLK     Tgck                  0.600   Arith_unit/
   Data_mul_res_reg/reg_q<5>
                                                       Arith_unit/
   sig_mul_res_reg_d<4>1
                                                       Arith_unit/
   Data_mul_res_reg/reg_q_4
    -------------------------------------------------
   ---------------------------
    Total                                    11.501ns (5.974ns logic, 5.527ns
   route)
                                                       (51.9% logic, 48.1%
   route)
```

```
--------------------------------------------------------------------------------

Slack (setup path):     8.635ns (requirement - (data path - clock path skew +
   uncertainty))
  Source:               Arith_unit/Data_fr2_reg/reg_q_5 (FF)
  Destination:          Arith_unit/Data_mul_res_reg/reg_q_4 (FF)
  Requirement:          20.000ns
  Data Path Delay:      11.362ns (Levels of Logic = 4)
  Clock Path Skew:      -0.003ns (0.123 - 0.126)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Destination Clock:    clk_BUFGP rising at 20.000ns
  Clock Uncertainty:    0.000ns

  Maximum Data Path: Arith_unit/Data_fr2_reg/reg_q_5 to Arith_unit/
   Data_mul_res_reg/reg_q_4
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X36Y25.XQ      Tcko                  0.626   Arith_unit/Data_fr2_reg/
   reg_q<5>
                                                       Arith_unit/Data_fr2_reg/
   reg_q_5
    MULT18X18_X1Y3.B5    net (fanout=2)        1.948   Arith_unit/Data_fr2_reg/
   reg_q<5>
    MULT18X18_X1Y3.P24   Tmult                 3.790   Arith_unit/
   Mmult_sig_mul_res
                                                       Arith_unit/
   Mmult_sig_mul_res
    SLICE_X37Y31.G2      net (fanout=2)        1.806   Arith_unit/sig_mul_res
   <24>
    SLICE_X37Y31.Y       Tilo                  0.479   Arith_unit/
   sig_mul_res_reg_d_and00004
                                                       Arith_unit/
   sig_mul_res_reg_d_and000121
    SLICE_X37Y30.F1      net (fanout=1)        0.482   Arith_unit/
   sig_mul_res_reg_d_and000121
    SLICE_X37Y30.X       Tilo                  0.479   Arith_unit/
   sig_mul_res_reg_d_and000182
                                                       Arith_unit/
   sig_mul_res_reg_d_and000182
    SLICE_X38Y26.G4      net (fanout=16)       1.152   Arith_unit/
   sig_mul_res_reg_d_and000182
    SLICE_X38Y26.CLK     Tgck                  0.600   Arith_unit/
   Data_mul_res_reg/reg_q<5>
                                                       Arith_unit/
   sig_mul_res_reg_d<4>1
                                                       Arith_unit/
   Data_mul_res_reg/reg_q_4
    -------------------------------------------------
   ---------------------------
    Total                                    11.362ns (5.974ns logic, 5.388ns
   route)
                                                       (52.6% logic, 47.4%
   route)

--------------------------------------------------------------------------------
```

```
Slack (setup path):     8.887ns (requirement - (data path - clock path skew +
   uncertainty))
  Source:               Arith_unit/Data_fr2_reg/reg_q_4 (FF)
  Destination:          Arith_unit/Data_mul_res_reg/reg_q_4 (FF)
  Requirement:          20.000ns
  Data Path Delay:      11.110ns (Levels of Logic = 4)
  Clock Path Skew:      -0.003ns (0.123 - 0.126)
  Source Clock:         clk_BUFGP rising at 0.000ns
  Destination Clock:    clk_BUFGP rising at 20.000ns
  Clock Uncertainty:    0.000ns

  Maximum Data Path: Arith_unit/Data_fr2_reg/reg_q_4 to Arith_unit/
   Data_mul_res_reg/reg_q_4
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X36Y25.YQ      Tcko                  0.626   Arith_unit/Data_fr2_reg/
   reg_q<5>
                                                       Arith_unit/Data_fr2_reg/
   reg_q_4
    MULT18X18_X1Y3.B4    net (fanout=2)        1.696   Arith_unit/Data_fr2_reg/
   reg_q<4>
    MULT18X18_X1Y3.P24   Tmult                 3.790   Arith_unit/
   Mmult_sig_mul_res
                                                       Arith_unit/
   Mmult_sig_mul_res
    SLICE_X37Y31.G2      net (fanout=2)        1.806   Arith_unit/sig_mul_res
   <24>
    SLICE_X37Y31.Y       Tilo                  0.479   Arith_unit/
   sig_mul_res_reg_d_and00004
                                                       Arith_unit/
   sig_mul_res_reg_d_and000121
    SLICE_X37Y30.F1      net (fanout=1)        0.482   Arith_unit/
   sig_mul_res_reg_d_and000121
    SLICE_X37Y30.X       Tilo                  0.479   Arith_unit/
   sig_mul_res_reg_d_and000182
                                                       Arith_unit/
   sig_mul_res_reg_d_and000182
    SLICE_X38Y26.G4      net (fanout=16)       1.152   Arith_unit/
   sig_mul_res_reg_d_and000182
    SLICE_X38Y26.CLK     Tgck                  0.600   Arith_unit/
   Data_mul_res_reg/reg_q<5>
                                                       Arith_unit/
   sig_mul_res_reg_d<4>1
                                                       Arith_unit/
   Data_mul_res_reg/reg_q_4
    ---------------------------------------------------
   ---------------------------
    Total                                    11.110ns (5.974ns logic, 5.136ns
   route)
                                                       (53.8% logic, 46.2%
   route)

--------------------------------------------------------------------------------
```

```
Hold Paths: TS_clk = PERIOD TIMEGRP "clk" 50 MHz HIGH 50%;
--------------------------------------------------------------------------------


Paths for end point SPI/Frame_check/cnt_q_0 (SLICE_X24Y28.BX), 1 path
--------------------------------------------------------------------------------

Slack (hold path):      0.719ns (requirement - (clock path skew + uncertainty -
    data path))
  Source:               SPI/Frame_check/cnt_q_0 (FF)
  Destination:          SPI/Frame_check/cnt_q_0 (FF)
  Requirement:          0.000ns
  Data Path Delay:      0.719ns (Levels of Logic = 0)
  Clock Path Skew:      0.000ns
  Source Clock:         clk_BUFGP rising at 20.000ns
  Destination Clock:    clk_BUFGP rising at 20.000ns
  Clock Uncertainty:    0.000ns

  Minimum Data Path: SPI/Frame_check/cnt_q_0 to SPI/Frame_check/cnt_q_0
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X24Y28.XQ      Tcko                  0.501   SPI/Frame_check/cnt_q<0>
                                                       SPI/Frame_check/cnt_q_0
    SLICE_X24Y28.BX      net (fanout=7)        0.464   SPI/Frame_check/cnt_q<0>
    SLICE_X24Y28.CLK     Tckdi       (-Th)     0.246   SPI/Frame_check/cnt_q<0>
                                                       SPI/Frame_check/cnt_q_0
    -------------------------------------------------
    ---------------------------
    Total                                      0.719ns (0.255ns logic, 0.464ns
    route)
                                                       (35.5% logic, 64.5%
    route)

--------------------------------------------------------------------------------


Paths for end point Arith_unit/Data_fr1_reg/reg_q_1 (SLICE_X34Y20.BX), 1 path
--------------------------------------------------------------------------------

Slack (hold path):      0.721ns (requirement - (clock path skew + uncertainty -
    data path))
  Source:               SPI/Deserializer/reg_q_14 (FF)
  Destination:          Arith_unit/Data_fr1_reg/reg_q_1 (FF)
  Requirement:          0.000ns
  Data Path Delay:      0.721ns (Levels of Logic = 0)
  Clock Path Skew:      0.000ns
  Source Clock:         clk_BUFGP rising at 20.000ns
  Destination Clock:    clk_BUFGP rising at 20.000ns
  Clock Uncertainty:    0.000ns

  Minimum Data Path: SPI/Deserializer/reg_q_14 to Arith_unit/Data_fr1_reg/
    reg_q_1
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
```

```
    ----------------------------------------------------  -------------------
    SLICE_X35Y20.YQ      Tcko                  0.501   SPI/Deserializer/reg_q
   <15>
                                                       SPI/Deserializer/
   reg_q_14
    SLICE_X34Y20.BX      net (fanout=3)        0.466   SPI/Deserializer/reg_q
   <14>
    SLICE_X34Y20.CLK     Tckdi       (-Th)     0.246   Arith_unit/Data_fr1_reg/
   reg_q<1>
                                                       Arith_unit/Data_fr1_reg/
   reg_q_1
    ----------------------------------------------------
   ---------------------------
    Total                                     0.721ns (0.255ns logic, 0.466ns
   route)
                                                       (35.4% logic, 64.6%
   route)

--------------------------------------------------------------------------------


Paths for end point Arith_unit/Data_fr1_reg/reg_q_13 (SLICE_X33Y30.BX), 1 path
--------------------------------------------------------------------------------

Slack (hold path):      0.721ns (requirement - (clock path skew + uncertainty -
    data path))
  Source:               SPI/Deserializer/reg_q_2 (FF)
  Destination:          Arith_unit/Data_fr1_reg/reg_q_13 (FF)
  Requirement:          0.000ns
  Data Path Delay:      0.721ns (Levels of Logic = 0)
  Clock Path Skew:      0.000ns
  Source Clock:         clk_BUFGP rising at 20.000ns
  Destination Clock:    clk_BUFGP rising at 20.000ns
  Clock Uncertainty:    0.000ns

  Minimum Data Path: SPI/Deserializer/reg_q_2 to Arith_unit/Data_fr1_reg/
   reg_q_13
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ----------------------------------------------------  -------------------
    SLICE_X32Y31.YQ      Tcko                  0.501   SPI/Deserializer/reg_q
   <3>
                                                       SPI/Deserializer/reg_q_2
    SLICE_X33Y30.BX      net (fanout=3)        0.466   SPI/Deserializer/reg_q
   <2>
    SLICE_X33Y30.CLK     Tckdi       (-Th)     0.246   Arith_unit/Data_fr1_reg/
   reg_q<13>
                                                       Arith_unit/Data_fr1_reg/
   reg_q_13
    ----------------------------------------------------
   ---------------------------
    Total                                     0.721ns (0.255ns logic, 0.466ns
   route)
                                                       (35.4% logic, 64.6%
   route)
```

```
--------------------------------------------------------------------------------


Component Switching Limit Checks: TS_clk = PERIOD TIMEGRP "clk" 50 MHz HIGH
   50%;
--------------------------------------------------------------------------------

Slack: 18.316ns (period - (min low pulse limit / (low pulse / period)))
  Period: 20.000ns
  Low pulse: 10.000ns
  Low pulse limit: 0.842ns (Twpl)
  Physical resource: SPI/SCLK_DDF/reg_q2/CLK
  Logical resource: SPI/SCLK_DDF/Mshreg_reg_q2/SRL16E/WS
  Location pin: SLICE_X24Y39.CLK
  Clock network: clk_BUFGP
--------------------------------------------------------------------------------

Slack: 18.316ns (period - (min high pulse limit / (high pulse / period)))
  Period: 20.000ns
  High pulse: 10.000ns
  High pulse limit: 0.842ns (Twph)
  Physical resource: SPI/SCLK_DDF/reg_q2/CLK
  Logical resource: SPI/SCLK_DDF/Mshreg_reg_q2/SRL16E/WS
  Location pin: SLICE_X24Y39.CLK
  Clock network: clk_BUFGP
--------------------------------------------------------------------------------

Slack: 18.316ns (period - min period limit)
  Period: 20.000ns
  Min period limit: 1.684ns (593.824MHz) (Tcp)
  Physical resource: SPI/SCLK_DDF/reg_q2/CLK
  Logical resource: SPI/SCLK_DDF/Mshreg_reg_q2/SRL16E/WS
  Location pin: SLICE_X24Y39.CLK
  Clock network: clk_BUFGP
--------------------------------------------------------------------------------



All constraints were met.


Data Sheet report:
-----------------
All values displayed in nanoseconds (ns)

Clock to Setup on destination clock clk
---------------+---------+---------+---------+---------+
               | Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock   |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
---------------+---------+---------+---------+---------+
clk            |   11.528|         |         |         |
---------------+---------+---------+---------+---------+


Timing summary:
---------------
```

```
Timing errors: 0  Score: 0  (Setup/Max: 0, Hold: 0)

Constraints cover 16427 paths, 0 nets, and 676 connections

Design statistics:
   Minimum period:  11.528ns{1}   (Maximum frequency:  86.745MHz)


------------------------------------Footnotes
   ------------------------------------
1)  The minimum period statistic assumes all single cycle delays.

Analysis completed Sun Jan 14 17:20:29 2024
--------------------------------------------------------------------------------


Trace Settings:
-------------------------
Trace Settings

Peak Memory Usage: 75 MB
```

Listing 11: Place and Route Report

```
Release 14.7 par P.20131013 (nt)
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JAKUB-NTB::  Sun Jan 14 17:20:17 2024

par -w -intstyle ise -ol high -t 1 AAU_map.ncd AAU.ncd AAU.pcf


Constraints file: AAU.pcf.
Loading device for application Rf_Device from file '3s200.nph' in environment C
   :\xilinx\14.7\ISE_DS\ISE\.
   "AAU" is an NCD, version 3.2, device xc3s200, package ft256, speed -5

Initializing temperature to 85.000 Celsius. (default - Range: 0.000 to 85.000
   Celsius)
Initializing voltage to 1.140 Volts. (default - Range: 1.140 to 1.260 Volts)


Device speed data version:  "PRODUCTION 1.39 2013-10-13".


Device Utilization Summary:

   Number of BUFGMUXs                        1 out of 8      12%
   Number of External IOBs                   6 out of 173     3%
      Number of LOCed IOBs                   0 out of 6       0%

   Number of MULT18X18s                      1 out of 12      8%
   Number of Slices                        102 out of 1920    5%
      Number of SLICEMs                      3 out of 960     1%



Overall effort level (-ol):   High
Placer effort level (-pl):    High
Placer cost table entry (-t): 1
Router effort level (-rl):    High

Starting initial Timing Analysis.  REAL time: 0 secs
Finished initial Timing Analysis.  REAL time: 0 secs


Starting Placer
Total REAL time at the beginning of Placer: 0 secs
Total CPU  time at the beginning of Placer: 0 secs

Phase 1.1  Initial Placement Analysis
Phase 1.1  Initial Placement Analysis (Checksum:1770) REAL time: 0 secs

Phase 2.7  Design Feasibility Check
Phase 2.7  Design Feasibility Check (Checksum:1770) REAL time: 0 secs

Phase 3.31  Local Placement Optimization
Phase 3.31  Local Placement Optimization (Checksum:1770) REAL time: 0 secs
```

```
Phase 4.2  Initial Clock and IO Placement
.............
Phase 4.2  Initial Clock and IO Placement (Checksum:9711de0) REAL time: 0 secs

Phase 5.36  Local Placement Optimization
Phase 5.36  Local Placement Optimization (Checksum:9711de0) REAL time: 0 secs

Phase 6.3  Local Placement Optimization
...........
Phase 6.3  Local Placement Optimization (Checksum:1b85a9f6) REAL time: 0 secs

Phase 7.5  Local Placement Optimization
Phase 7.5  Local Placement Optimization (Checksum:1b85a9f6) REAL time: 0 secs

Phase 8.8  Global Placement
.............
..
Phase 8.8  Global Placement (Checksum:a5a760c9) REAL time: 1 secs

Phase 9.5  Local Placement Optimization
Phase 9.5  Local Placement Optimization (Checksum:a5a760c9) REAL time: 1 secs

Phase 10.18  Placement Optimization
Phase 10.18  Placement Optimization (Checksum:d94575bf) REAL time: 1 secs

Phase 11.5  Local Placement Optimization
Phase 11.5  Local Placement Optimization (Checksum:d94575bf) REAL time: 1 secs

Total REAL time to Placer completion: 1 secs
Total CPU  time to Placer completion: 1 secs
Writing design to file AAU.ncd



Starting Router


Phase  1  : 730 unrouted;      REAL time: 1 secs

Phase  2  : 628 unrouted;      REAL time: 1 secs

Phase  3  : 247 unrouted;      REAL time: 1 secs

Phase  4  : 247 unrouted; (Setup:0, Hold:0, Component Switching Limit:0)
   REAL time: 2 secs

Phase  5  : 0 unrouted; (Setup:0, Hold:0, Component Switching Limit:0)     REAL
    time: 2 secs

Updating file: AAU.ncd with current fully routed design.

Phase  6  : 0 unrouted; (Setup:0, Hold:0, Component Switching Limit:0)     REAL
    time: 2 secs

Phase  7  : 0 unrouted; (Setup:0, Hold:0, Component Switching Limit:0)     REAL
    time: 2 secs
```

```
Phase  8  : 0 unrouted; (Setup:0, Hold:0, Component Switching Limit:0)     REAL
    time: 2 secs

Total REAL time to Router completion: 2 secs
Total CPU time to Router completion: 2 secs

Partition Implementation Status
-------------------------------

  No Partitions were found in this design.

-------------------------------

Generating "PAR" statistics.

**************************
Generating Clock Report
**************************

+----------------------+--------------+------+------+------------+-------------+
|        Clock Net     |   Resource   |Locked|Fanout|Net Skew(ns)|Max Delay(ns)|
+----------------------+--------------+------+------+------------+-------------+
|           clk_BUFGP  |      BUFGMUX0| No   |   80 |  0.004     |  0.884      |
+----------------------+--------------+------+------+------------+-------------+

* Net Skew is the difference between the minimum and maximum routing
only delays for the net. Note this is different from Clock Skew which
is reported in TRCE timing report. Clock Skew is the difference between
the minimum and maximum path delays which includes logic delays.

* The fanout is the number of component pins not the individual BEL loads,
for example SLICE loads not FF loads.

Timing Score: 0 (Setup: 0, Hold: 0, Component Switching Limit: 0)

Asterisk (*) preceding a constraint indicates it was not met.
   This may be due to a setup or hold violation.

--------------------------------------------------------------------------------

  Constraint                                |    Check    | Worst Case |  Best
   Case | Timing |   Timing
                                            |             |    Slack   |
   Achievable | Errors |    Score
--------------------------------------------------------------------------------

  TS_clk = PERIOD TIMEGRP "clk" 50 MHz HIGH | SETUP       |     8.472ns|
   11.528ns|       0|           0
   50%                                      | HOLD        |     0.719ns|
        |       0|           0
--------------------------------------------------------------------------------



All constraints were met.
```

```
Generating Pad Report.

All signals are completely routed.

Total REAL time to PAR completion: 2 secs
Total CPU time to PAR completion: 2 secs

Peak Memory Usage:  119 MB

Placement: Completed - No errors found.
Routing: Completed - No errors found.
Timing: Completed - No errors found.

Number of error messages: 0
Number of warning messages: 0
Number of info messages: 0

Writing design to file AAU.ncd



PAR done!
```