AAU Project Status (01/14/2024 - 11:11:16)			
Project File:	AAU.xise	**Parser Errors:**	No Errors
Module Name:	AAU	**Implementation State:**	Placed and Routed
Target Device:	xc3s200-5ft256	• **Errors:**	No Errors
Product Version:	ISE 14.7	• **Warnings:**	2 Warnings (0 new)
Design Goal:	Balanced	• **Routing Results:**	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	• **Timing Constraints:**	All Constraints Met
Environment:	System Settings	• **Final Timing Score:**	0 (Timing Report)

Device Utilization Summary				[-]
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Flip Flops	129	3,840	3%	
Number of 4 input LUTs	119	3,840	3%	
Number of occupied Slices	102	1,920	5%	
Number of Slices containing only related logic	102	102	100%	
Number of Slices containing unrelated logic	0	102	0%	
Total Number of 4 input LUTs	137	3,840	3%	
Number used as logic	116			
Number used as a route-thru	18			
Number used as Shift registers	3			
Number of bonded IOBs	6	173	3%	
Number of MULT18X18s	1	12	8%	
Number of BUFGMUXs	1	8	12%	
Average Fanout of Non-Clock Nets	3.11			

Performance Summary				[-]
Final Timing Score:	0 (Setup: 0, Hold: 0, Component Switching Limit: 0)	**Pinout Data:**	Pinout Report	
Routing Results:	All Signals Completely Routed	**Clock Data:**	Clock Report	
Timing Constraints:	All Constraints Met			

Detailed Reports					[-]
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	ne 14. led 11:08:32 2024	0	2 Warnings (0 new)	0
Translation Report	Current	ne 14. led 11:08:49 2024	0	0	0
Map Report	Current	ne 14. led 11:09:05 2024	0	0	2 Infos (0 new)
Place and Route Report	Current	ne 14. led 11:09:15 2024	0	0	0
Power Report					
Post-PAR Static Timing Report	Current	ne 14. led 11:09:22 2024	0	0	5 Infos (0 new)

Secondary Reports		[-]
Report Name	**Status**	**Generated**
Post-Synthesis Simulation Model Report	Current	ne 14. led 11:11:15 2024
Primetime Netlist Report	Current	ne 14. led 11:11:02 2024

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