**Preliminary Work / Preliminary Design Report (50 points)**

CS224

Section No.: 05

Spring 2018

Lab No.: 06

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1. **(** **5 points:** **With 2 or more errors you get 0 points. Otherwise full point.)**

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **No.** | **Cache**  **Size KB** | **N way**  **cache** | **Word**  **Size** | **Block size**  **(no. of words)** | **No. of**  **Sets** | **Tag Size**  **in bits** | **Index Size**  **(Set No.) in bits** | **Word Block**  **Offset**  **Size in bits1** | **Byte**  **Offset**  **Size in bits2** | **Block**  **Replacement**  **Policy Needed (Yes/No)** |
| 1 | 256 | 1 | 32 bits | 4 | 2^14 | 14 | 14 | 2 | 2 | NO |
| 2 | 256 | 2 | 32 bits | 4 | 2^13 | 15 | 13 | 2 | 2 | YES |
| 3 | 256 | 4 | 32 bits | 8 | 2^11 | 16 | 11 | 3 | 2 | YES |
| 4 | 256 | Full | 32 bits | 8 | 1 | 27 | 0 | 3 | 2 | YES |
| 9 | 512 | 1 | 16 bits | 4 | 2^16 | 13 | 16 | 2 | 1 | NO |
| 10 | 512 | 2 | 16 bits | 4 | 2^15 | 14 | 15 | 2 | 1 | YES |
| 11 | 512 | 4 | 16 bits | 16 | 2^12 | 15 | 12 | 4 | 1 | YES |
| 12 | 512 | Full | 16 bits | 16 | 1 | 27 | 0 | 4 | 1 | YES |

**1 Word Block Offset Size in bits:** Log2(No. of words in a block)

**2 Byte Offset Size in bits:** Log2(No. of bytes in a word)

**2**. **(5 points:** **With 2 or more errors you get 0 points. Otherwise full point.)**

|  |  |  |
| --- | --- | --- |
| **Memory Address Accessed (hex)** | **Set No.** | **Hit (yes/no)** |
| 00 00 00 28 | 01 | No |
| 00 00 00 49 | 01 | No |
| 00 00 00 6C | 01 | No |
| 00 00 00 0C | 01 | No |
| 00 00 00 0B | 01 | Yes |
| 00 00 00 0D | 01 | Yes |

**3**. **(5 points:** **With 2 or more errors you get 0 points. Otherwise full point.)**

|  |  |  |
| --- | --- | --- |
| **Memory Address Accessed (hex)** | **Set No.** | **Hit (yes/no)** |
| 00 00 00 28 | 01 | No |
| 00 00 00 49 | 01 | No |
| 00 00 00 4C | 01 | Yes |
| 00 00 00 0C | 01 | No |
| 00 00 00 0B | 01 | Yes |
| 00 00 00 0D | 01 | Yes |

**4**. **(5 points, With 1 or more errors you get 0 points. Otherwise full point.)**

L1: 1 clock cycle

L2: 2 clock cycles

Main Memory: as L2 is 2 clock cycles, 20 clock cycles

L1 miss = %20

L2 miss = %5

AMAT = L1\*HITRATE + L2\*HITRATE + MAIN\*HITRATE

= 0.8 + 0.2\*0.95\*3 + 0.2\*0.05\*1\*23

= 1.6 clock cycles

Every time we check L1, L2 so in the L2 time we add L1 clock cycle and miss rate too. Also for the main, it applies.

For 2 GHz clock = (Expected clock cycle per ins \* # of inst)/2 GHz

= 1.6\*10^12\*2\*10^9

= 800