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WM-N-BM-14 Application Note

SOURCE ORGANIZATION : USI WP/RD/WM/HW1

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Change List

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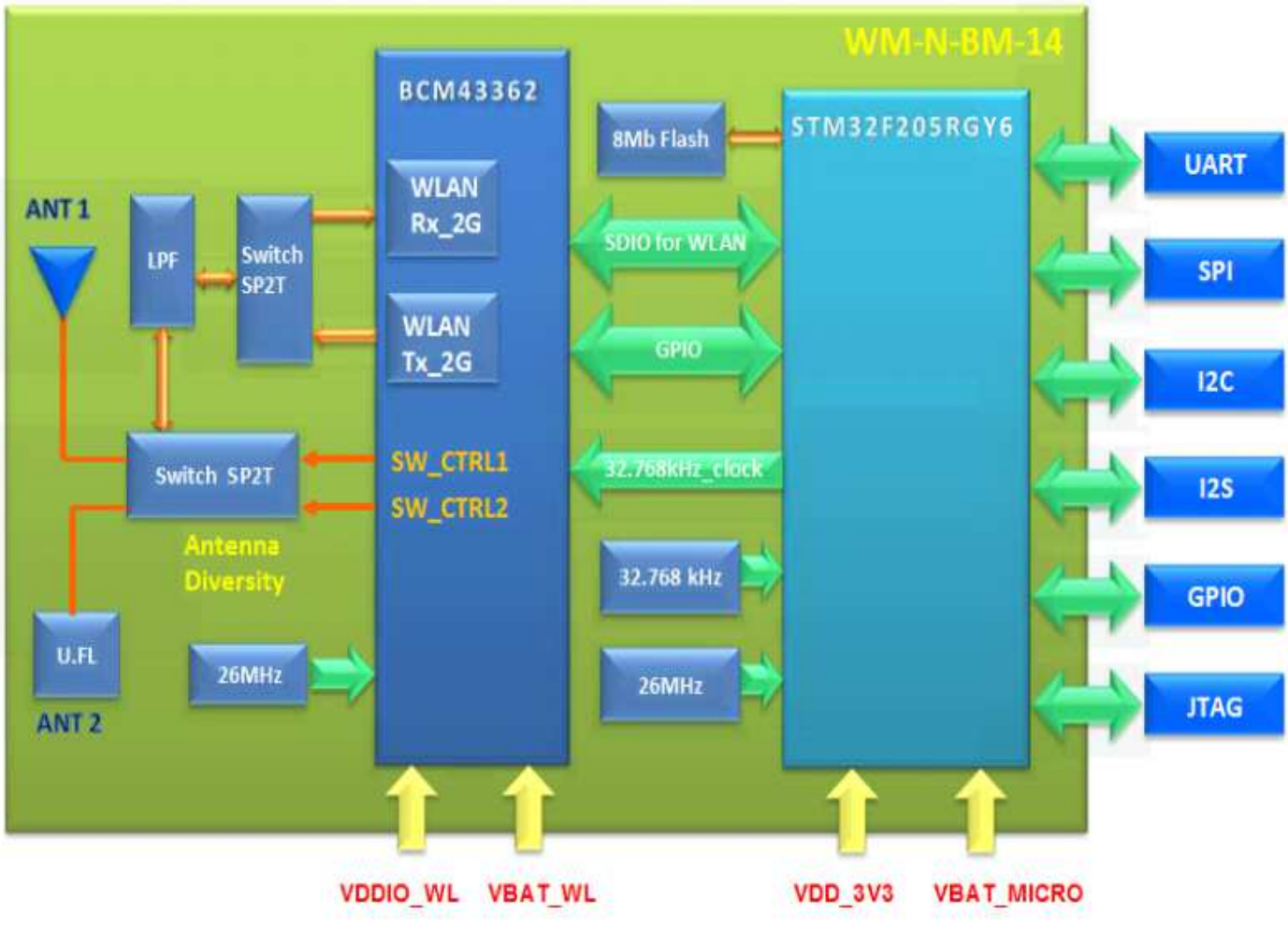
HW Application note for WM-N-BM-14

1. Introduction

WM-N-BM-14 includes WIFi and Micro-processor. The WLAN is 2.4G single band that includes 802.11b/g/n function. The application note is composed of module power plan, reference schematic description and the layout guide line for this module.



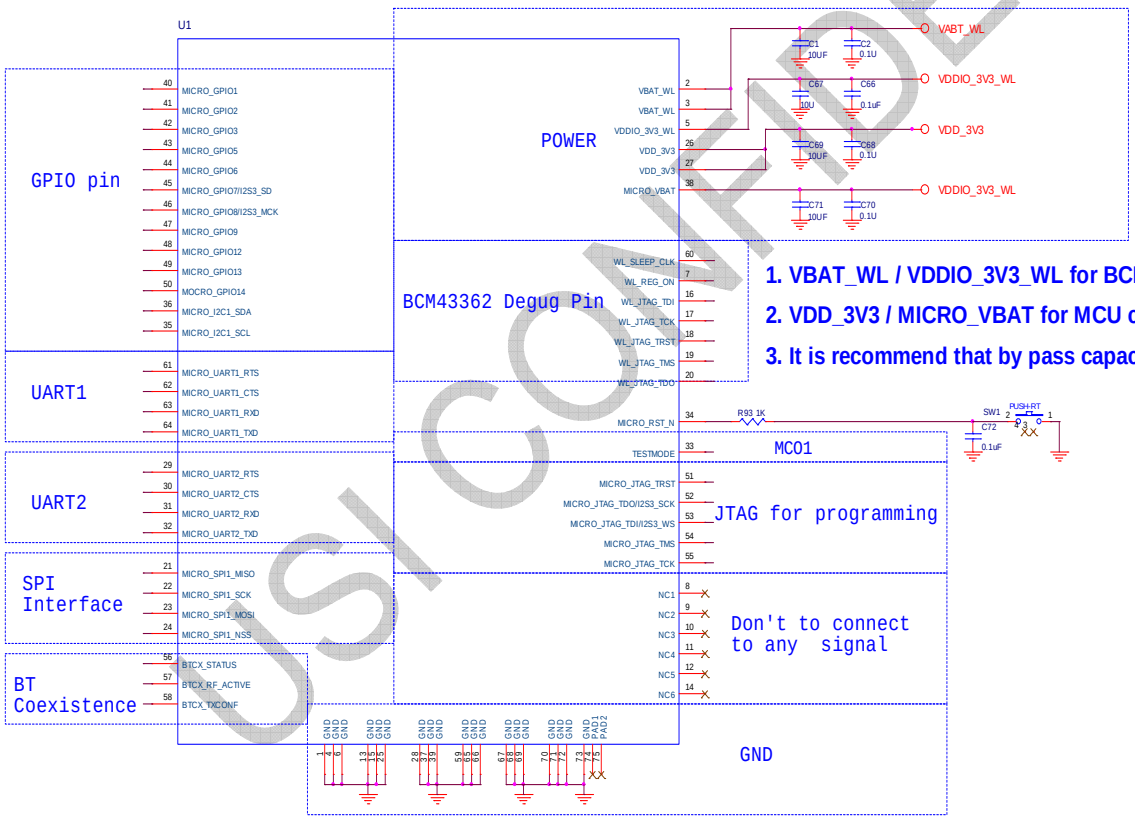
WM-N-BM-14 Module

2. Power Request

Module operational requirements voltage have VDD_WIFI, VDDIO_WIFI, VDD_3V3 and VBAT. The recommended operational voltage is shown at below table.

Symbol	Parameter	Min	Typ	Max	Unit
VBAT_WL	power supply for BCM43362	3.0	3.3	3.6	V
VDDIO_3V3_WL	host Interface power supply	3.0	3.3	3.6	V
VBAT_MICRO	backup operating voltage	3.0	3.3	3.6	V
VDD_3V3	power supply for MCU	3.0	3.3	3.6	V

3. Reference Circuit



1. VBAT_WL / VDDIO_3V3_WL for BCM43362 should be 3.0V ~ 3.6V
2. VDD_3V3 / MICRO_VBAT for MCU can be between 3.0V ~ 3.6V
3. It is recommend that by pass capacitor be placed near module output pins

Note : 1. It is highly recommended that keeping the top layer of the module mounting area as GND-plane

2. Do not route any traces underneath the module

3. Cover the module with shielding case to avoid EMI issues.

4. Layout suggestion

DC power

Use wide traces for power supply lines. Understand the maximum current carried on each power supply trace, and make the trace widths proportionate to the current (especially for long trace lengths). If possible, fill large areas with copper to distribute the highest currents. These measures minimize IR drops, line inductance, and switching transients.

- Use several plated via holes to connect power supply traces between layers. The number of vias used should be proportional to the current being routed.
- Avoid loops in the supply distribution traces. Current-carrying loops are essentially antennas radiating electromagnetic fields that may corrupt transceiver performance or cause regulatory electromagnetic interference (EMI) test failures

- The bypass capacitor for power sourceshould be as close to module pin out as possible.
- If there are two different capacitors for signal power source, please placed the one with low capacitance to be closer to module pin out.

WM-N-BM-14 Maximum current table

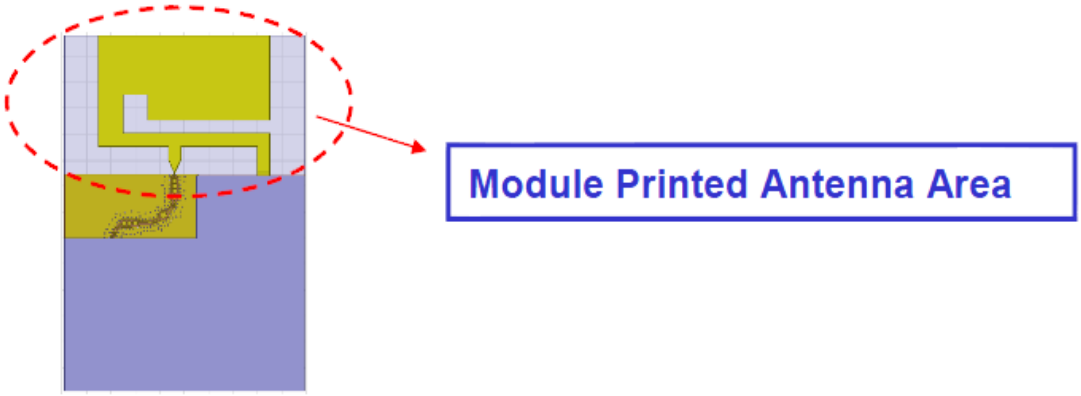
Power Consumption	MAX.
VBAT_WL	310 mA
VDDIO_3V3_WL	50 mA
VBAT_MICRO	50 mA
VDD_3V3	120 mA

Table1.

Printed Antenna

General guidelines for 2.4G printed Antenna

- **Main board antenna area under module printed antenna should be clear or empty.**
- **No signals, GND or power traces can be routed in antenna area for each layers of main board.**
- **Any metal lid, power trace or metal components should be placed far away from antenna area on main board.**
- **Keep GND plane as large as you can on main board.**



TESTMODE PIN

Pin 33 testmode (PA8, which is defined as microcontroller clock output) is capable of outputting clock signal. You can output four different clock source onto the MCO1 pin (PA8) using the configurable prescaler (from 1 to 5):

– HSI clock
– LSE clock
– HSE clock
– PLL clock

The desired clock source is selected using the MCO1PRE[2:0] and MCO1[1:0] bits, for detail information of the RCC clock configuration register (RCC_CFGR), please refre to stm32 reference menu. The reference programming manuals are also available from the STMicroelectronics website *www.st.com*.

If pin33 need to output clock , this clock signal trace this signal trace must be routed

carefully to prevent from the interfere of other clocks, power supply transients and other digital noise. And it must be routed as short and direct as possible.

5. Host Interface

5.1 Pin Mapping

WM-N-BM-14 pin mapping with STM32F205RG as below:

Pin-No	Symbol	ST32F205RGY
21	MICRO_SPI1_MISO	H5(PA6)
22	MICRO_SPI1_SCK	H6 (PA5)
23	MICRO_SPI1_MOSI	J7 (PA7)
24	MICRO_SPI1_NSS	J8 (PA4)
29	MICRO_UART2_RTS	H8 (PA1)
30	MICRO_UART2_CTS	E7 (PA0)
31	MICRO_UART2_RXD	G7 (PA2)
32	MICRO_UART2_TXD	J9 (PA2)
33	TESTMODE	E2 (PA8)
34	MICRO_RST_N	E8 (RST_L)
35	MICRO_I2C1_SCL	B5 (PB6)
36	MICRO_I2C1_SDA	A6 (PB7)
38	VBAT_MICRO	A9
40	MICRO_GPIO1	J6 (PB0)
41	MICRO_GPIO2	J5 (PB1)
42	MICRO_GPIO3	G9 (PC0)
43	MICRO_GPIO5	G8 (PC3)
44	MICRO_GPIO6	H4 (PC4)
45	MICRO_GPIO7 / I2S3_SD	A5 (PB5)
46	MICRO_GPIO8 / I2S3_MCK	F2 (PC7)
47	MICRO_GPIO9	B8 (PC13)
48	MICRO_GPIO12	F8 (PC1)
49	MICRO_GPIO13	D7 (PC2)

50	MICRO_GPIO14	G3 (PC5)
51	MICRO_JTAG_TRST	B4 (PB4)
52	MICRO_JTAG_TDO / I2S3_SCK	A4 (PB3)
53	MICRO_JTAG_TDI / I2S3_WS	A2 (PA15)
54	MICRO_JTAG_TMS	B2 (PA13)
55	MICRO_JTAG_TCK	A1 (PA14)
61	MICRO_UART1_RTS	C1 (PA12)
62	MICRO_UART1_CTS	D2 (PA11)
63	MICRO_UART1_RXD	D3 (PA10)
64	MICRO_UART1_TXD	E3 (PA9)

5.2 Interface of SPI, UART, I2C and I2S

PIN 21/22/23/24 pins for SPI interface. Table2. describes the SPI pins.

Table2. SPI Interface

Pin-No	Symbol	Pin Type	Description
21	MICRO_SPI1_MISO	I/O	SPI_MISO
22	MICRO_SPI1_SCK	I/O	SPI_SCK
23	MICRO_SPI1_MOSI	I/O	SPI_MOSI
24	MICRO_SPI1_NSS	I/O	SPI_NSS

PIN 29/30/31/32 pins for UART interface. Table3. describes the UART pins.

Table3. UART Interface

Pin-No	Symbol	Pin Type	Description
29	MICRO_UART2_RTS	I/O	UART2_RTS
30	MICRO_UART2_CTS	I/O	UART2_CTS
31	MICRO_UART2_RXD	I/O	UART2_RXD
32	MICRO_UART2_TXD	I/O	UART2_TXD
61	MICRO_UART1_RTS	I/O	UART1_RTS
62	MICRO_UART1_CTS	I/O	UART1_CTS
63	MICRO_UART1_RXD	I/O	UART1_RXD
64	MICRO_UART1_TXD	I/O	UART1_TXD

PIN 35/36 pins for I2C interface. Table4. describes the I2C pins.

Table4. I2C1 Interface

Pin-No	Symbol	Pin Type	Description
35	MICRO_I2C1_SCL	I/O	I2C_SCL
36	MICRO_I2C1_SDA	I/O	I2C_SDA

PIN 45/46/52/53 pins for I2S interface. Table5. describes the I2S pins.

Table5. I2S3 Interface

Pin-No	Symbol	Pin Type	Description
45	MICRO_GPIO7 / I2S3_SD	I/O	I2S_SD
46	MICRO_GPIO8 / I2S3_MCK	I/O	I2S_MCK
52	MICRO_JTAG_TDO / I2S3_SCK	I/O	I2S_SCK
53	MICRO_JTAG_TDI / I2S3_WS	I/O	I2S_WS

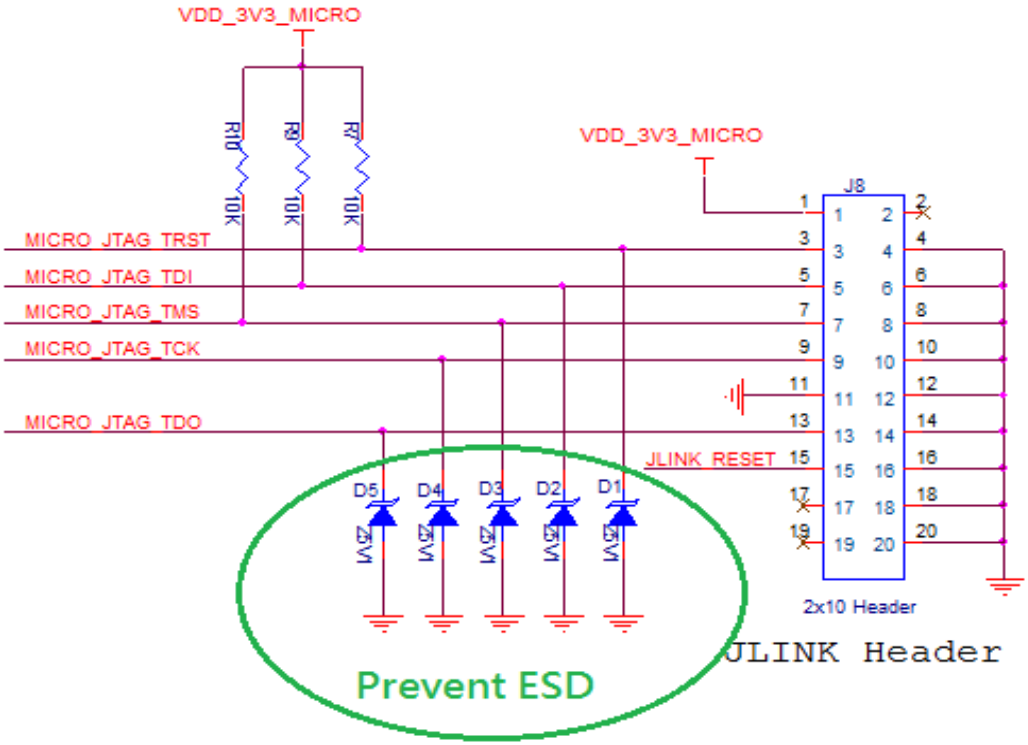
6. JTAG Interface

PIN 51~55 pins for JTAG interface that can be used for programming MCU. Table6. describes these JTAG pins.

Table6. JTAG Interface

Pin-No	Symbol	Pin Type	Description
51	MICRO_JTAG_TRST	I/O	JTAG_TRST
52	MICRO_JTAG_TDO / I2S3_SCK	I/O	JTAG_TDO
53	MICRO_JTAG_TDI / I2S3_WS	I/O	JTAG_TDI
54	MICRO_JTAG_TMS	I/O	JTAG_TMS
55	MICRO_JTAG_TCK	I/O	JTAG_TCK

We suggest customer follow the EVB design shown below. All JTAG signals should connect to 2x10 header which can link to ST-LINK/OLIMEX ARM-USB-TINY-H cable to program MCU.



Please find detail information from link as below,
https://www.olimex.com/Products/ARM/JTAG/ARM-USB-TINY-H/

ARM-USB-TINY-H

Device summary

Part number	Order Code	Description
ST-LINK/V2	ST-LINK/V2	In-circuit debugger/programmer
	ST-LINK/V2-ISOL	In-circuit debugger/programmer with digital isolation

ST-LINK/V2

ST-LINK/V2-ISOL

ST-Link/v2 Utility :

http://www.st.com/st-web-ui/static/active/en/st_prod_software_internet/resource/technical/software/utility/stsw-link004.zip

ST-Link/v2 driver :

http://www.st.com/st-web-ui/static/active/en/st_prod_software_internet/resource/technical/software/driver/st-link_v2_usbdriver.zip

7. Characteristic Option

7.1 External Coexistence Interface

WM-N-BM-14 supports the coexistence with Bluetooth or other external radios. The corresponding pins are shown below.

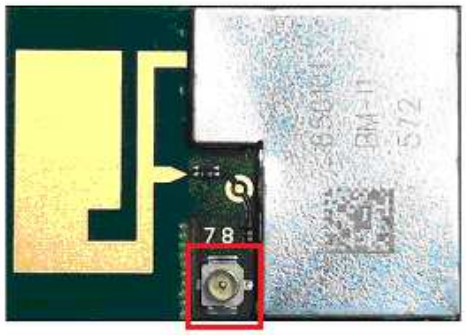
Table7. coexistence status

Pin-No	Symbol	Pin Type	Description
56	BTCX_STATUS	I	Coexistence signal indicating Bluetooth priority status and TX/RX direction.
57	BTCX_RF-ACTIVE	I	Coexistence signal indicating that Bluetooth is active.
58	BTCX_TXCONF	O	Coexistence output giving Bluetooth permission to transmit.

Multiplexed BT_Coex pins. When programmed are high impedance on power up and reset. Subsequently, they can be individually programmed to become inputs or outputs through software control. They can also be programmed to have internal pull-up or pull-down resistor.

7.2 Printed Antenna support

WM-N-BM-14 embeds on-board printed antenna as well as an external antenna port.



Antenna Connector

the wl commend also need to modify the ant setting as below:

```
wl --serial 2 up
wl --serial 2 txant 1
wl --serial 2 antdiv 1
```

7.3 Boot mode

In the STM32F205RGY6, three different boot modes can be selected through the BOOT[1:0] pins as shown in below *Table 8*.

Table 8. Boot modes

Boot mode selection pins		Boot mode	Aliasing
BOOT1	BOOT0		
x	0	Main Flash memory	Main Flash memory is selected as the boot space
0	1	System memory	System memory is selected as the boot space
1	1	Embedded SRAM	Embedded SRAM is selected as the boot space

WM-N-BM-14 set the BOOT0 to GND, the Boot mode is Main Flash memory.

7.4 MCO Output Clock VS. Low Power

By default, the microcontroller is in Run mode after a system or a power-on reset. In Run mode the CPU is clocked by HCLK and the program code is executed. Several low-power modes are available to save power when the CPU does not need to be kept running, for example when waiting for an external event. It is up to the user to select the mode that gives the best compromise between low-power consumption, short startup time and available wakeup sources.

The devices feature three low-power modes:

- Sleep mode (Cortex™-M3 core stopped, peripherals kept running)
- Stop mode (all clocks are stopped)
- Standby mode (1.2 V domain powered off)

The microcontroller clock output (MCO) is available in STM32 RUN, SLEEP or STOP mode . Customer can use this MCO1 pin to provide 32.768KHZ clock to BCM43362. But it is necessary for setting MCU “PC6” as input ; MCU “PA8” as output LSE clock.