Charles Block

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Education

2022-Present **Ph.D. Computer Science**, *University of Illinois*, Urbana-Champaign
NSF Graduate Research Fellow, advised by Dr. Josep Torrellas. Research topics include computer architecture and distributed systems.

2022-2024 **M.S. Computer Science**, *University of Illinois*, Urbana-Champaign

2018-2022 **B.S. Electrical & Computer Engineering with Honors**, *University of Texas*, Austin

Industry Experience

Summer 2024 **Apple Inc**, *CPU Architecture/Performance Intern*
- Investigated novel memory ordering techniques and their impact on next-generation CPUs.
- Developed enhancements to trace-based performance simulators and tooling.
- Identified and addressed performance simulation bugs to accurately model RTL.

Summer 2022 **Intel Corporation**, *Design Validation Intern*
- Supported CPU validation in the Advanced Architecture Development Group.
- Debugged core RTL & software infrastructure to address performance and power issues.
- Improved run-time performance of long- and often-running validation jobs by 20x.

Summer 2021 **Microsoft Corporation**, *Software Development Intern (Azure)*
- Initiated development of a distributed service to supplement PostgreSQL databases.
- Developed a new distributed, in-memory storage backend for PostgreSQL.
- Developed software using the C and Rust programming languages.

Summer of 2019 & 2020 **Amazon Robotics**, *Firmware Development Intern*
- Supported firmware development for the Amazon Scout robotics project.
- Integrated various sensors, MCUs, and SoCs using both embedded Linux and bare-metal C.
- Developed/evaluated a real-time object detection and tracking system on an embedded SoC.

Summer 2018 **TyRex Group, LTD**, *Engineering Intern*

Academic & Leadership Experience

2023-Present **i-acoma Group at UIUC**, *Graduate Researcher*
- Working with Professor Josep Torrellas on HPC architectures and distributed systems.
- Supercomputer-scale distributed algorithms for sparse matrix kernels.
- Multi-agent reinforcement learning for multi-core architectures.

2021-2022 **Lu Research Group at UT Austin**, *Research Assistant*
- Worked with Professor Nanshu Lu to develop wearable low-power biomedical sensors.
- Developed measurement circuitry for experiments with novel pressure sensor technology.

2018-2022 **Longhorn Racing - Solar Vehicle Team**
- Oversaw manufacturing of composite materials, electronic systems, and structural components.
- Led development of embedded hardware and software for vehicle control and power.
- Developed lessons & mentored other students for designing circuits and software.

Spring of 2020 & 2021 **Intro to Embedded Systems at UT Austin (EE319K)**, *Teaching Assistant*
- Assisted in teaching and lab supervision for a freshman embedded systems course.

Awards

2022 **NSF Graduate Research Fellowship**, *National Science Foundation*

2022 **Wing Kai Cheng Fellowship**, *University of Illinois Urbana-Champaign*

2020 & 2021 **Dr. Ariane L. Beck and Mr. Eric Sebesta Endowed Scholarship**, *UT Austin ECE*

Relevant Coursework

- Machine Learning for Compilers & Architecture (Charith Mendis, *UIUC*)
- Parallel Computer Architecture (Josep Torrellas, *UIUC*)
- Microarchitecture (Yale Patt, *UT Austin*)
- System-on-Chip Design (Andreas Gerstlauer, *UT Asutin*)
- ML Algorithm & Hardware Co-Design (Mattan Erez & Michael Orshansky, *UT Austin*)

Publications

[1] L. Scalco de Vasconcelos, Y. Yan, P. Maharjan, S. Kumar, M. Zhang, B. Yao, H. Li, S. Duan, E. Li, E. Williams, S. Tiku, P. Vidal, R. S. Solorzano-Vargas, W. Hong, Y. Du, Z. Liu, F. Iwane, **C. Block**, A. T. Repetski, P. Tan, P. Wang, M. G. Martín, J. d. R. Millán, X. He, and N. Lu, "On-scalp printing of personalized electroencephalography e-tattoos," *Cell Biomaterials*, 2024.

[2] I. Ranawaka, M. T. Hussain, **C. Block**, G. Gerogiannis, J. Torrellas, and A. Azad, "Distributed-memory parallel algorithms for sparse matrix and sparse tall-and-skinny matrix multiplication," in *Proceedings of the International Conference for High Performance Computing, Networking, Storage, and Analysis*, ser. SC '24. IEEE Press, 2024.

[3] V. Suresh, B. Mishra, Y. Jing, Z. Zhu, N. Jin, **C. Block**, P. Mantovani, D. Giri, J. Zuckerman, L. P. Carloni, and S. V. Adve, "Mozart: Taming taxes and composing accelerators with shared-memory," in *Proceedings of the 2024 International Conference on Parallel Architectures and Compilation Techniques*, ser. PACT '24, 2024, p. 183–200.

[4] K.-H. Ha, Z. Li, S. Kim, H. Huh, Z. Wang, H. Shi, **C. Block**, S. Bhattacharya, and N. Lu, "Stretchable hybrid response pressure sensors," *Matter*, vol. 7, no. 5, 2024.

[5] **C. Block**, G. Gerogiannis, C. Mendis, A. Azad, and J. Torrellas, "Two-face: Combining collective and one-sided communication for efficient distributed spmm," in *Proceedings of the 29th ACM International Conference on Architectural Support for Programming Languages and Operating Systems, Volume 2*, ser. ASPLOS '24, 2024.