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ECE 6780-003

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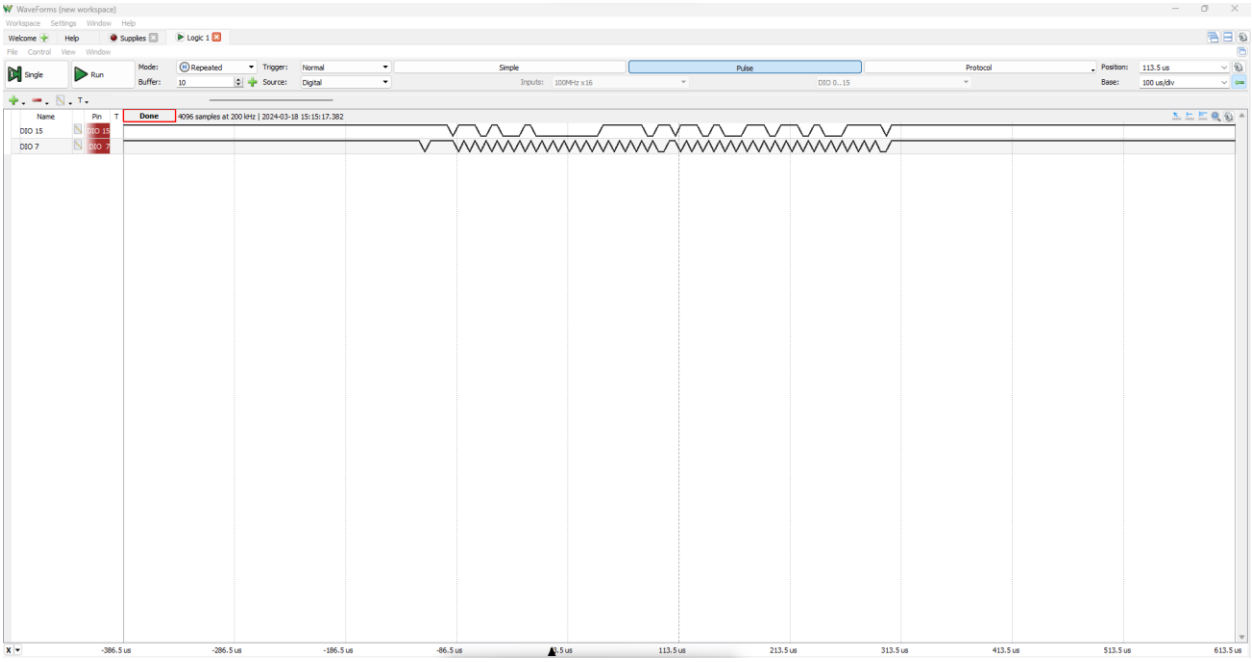
Post-lab 05 Questions

5.2 — Postlab 5. Please answer the following questions about I2C and the lab, and submit your source code.



1. What does the AUTOEND bit in the CR2 register do? Why don't you want to use it when you'll be needing a restart condition?

Bit 25 **AUTOEND**: Automatic end mode (master mode)
This bit is set and cleared by software.
0: software end mode: TC flag is set when NBYTES data are transferred, stretching SCL low.
1: Automatic end mode: a STOP condition is automatically sent when NBYTES data are transferred.
Note: This bit has no effect in slave mode or when the RELOAD bit is set.

The AUTOEND bit in the CR2 register helps you avoid manually sending a STOP condition after an I2C transmission wraps up. But, if you're planning on doing a restart—where you immediately start another transfer without releasing the bus—AUTOEND would not allow for a smooth transition between transfers. Thus, if we want to do a restart condition, it's better if we just handle the STOP ourselves and not use AUTOEND.

2. This lab used standard-mode 100 kHz I2C speed. What values would you write in the TIMINGR if we were using 400 kHz fast-mode?

// Configure TIMINGR register for 400 kHz fast-mode

I2C2->TIMINGR |= (3 << 28); // PSC = 3

I2C2->TIMINGR |= (0x0D << 20); // SCLDEL = 0x0D

I2C2->TIMINGR |= (0x02 << 16); // SDADEL = 0x02

I2C2->TIMINGR |= (0x0F << 8); // SCLH = 0x0F

I2C2->TIMINGR |= (0x13 << 0); // SCLL = 0x13

3. This lab used blocking code. To implement it completely as non-blocking you would replace all of the wait loops with interrupts. Most flags in the I2C peripheral can trigger an interrupt if the proper enable bit is set. Find the interrupt enable bits that match the following flags:

• TC: in CR1 - Bit 6 TCIE: Transfer complete interrupt enable

• NACKF: in CR1 - NACKIE: Not acknowledge received Interrupt enable

• TXIS (transmit interrupt): in CR1 - Bit 1 TXIE: TX Interrupt enable

• ARLO: in CR1 - Bit 0 PE: Peripheral enable – we would set this to 0 based on the documentation for ARLO.

Bit 9 **ARLO**: Arbitration lost

This flag is set by hardware in case of arbitration loss. It is cleared by software by setting the ARLOCF bit.

Note: This bit is cleared by hardware when PE = 0.

4. The gyro can operate in three full-scale/measurement ranges, measured in degrees-per-second (dps). What are these three ranges?

Symbol	Parameter	Test condition	Min.(1)	Typ.(2)	Max.(1)	Unit
FS	Measurement range(3)	User-selectable		±245		dps
				±500		
				±2000		

5. What is the I2C address of the gyro when the SDO pin is low? The lab has the pin set high, read the I2C section of the gyro datasheet.

“When the SDO pin is connected to ground, the LSb value is ‘0’ (address 1101000b)”