APS3R

Energy Efficient Embedded Microcontroller

advanced processing solutions

The APS3R from Cortus is an ultra low power, low interrupt latency, silicon efficient 32 bit microcontroller core designed to efficiently run high level languages such as C and C++.

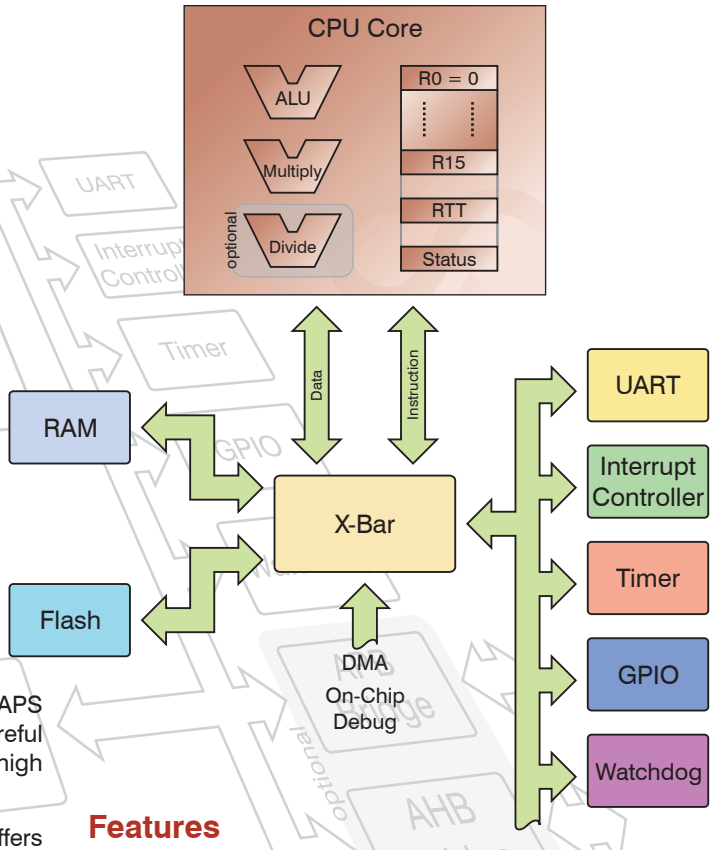
Ideal for applications requiring energy efficiency yet high performance such as wireless communications, sensing, SIM cards, touchscreen controllers and security applications.

The APS3R has a very small silicon footprint, from 8700 gates, and ultra low power consumption. This offers industry leading performance in terms of both DMIPS/μW and DMIPS/mm^2.

As a member of the Cortus APS family of processors the APS3R shares the key architectural features of the other processors, with a common toolchain and IDE, bus interface and peripheral set.

The ASP3R is fully upwards compatible with other APS processors. The modern RISC architecture and careful design ensures that the APS3R can achieve a high maximum clock frequency, F_{max}.

This 32 bit CPU is an ideal 8 bit replacement, and offers considerable advantages over 8 bit processors, in terms of performance, code density, power consumption and silicon footprint.



Performance

- CoreMark 1:1·21
- DMIPS 2·29 DMIPS/MHz
- At least 400MHz in 90nm

Implementation Results

	F_{max}	Area	Power
65nm (TSMC) low power	689 MHz	0·023 mm^2	1·71 μW/MHz
90nm (UMC)	526 MHz	0·049 mm^2	11·61 μW/MHz
130nm (UMC)	357 MHz	0·083 mm^2	16·85 μW/MHz

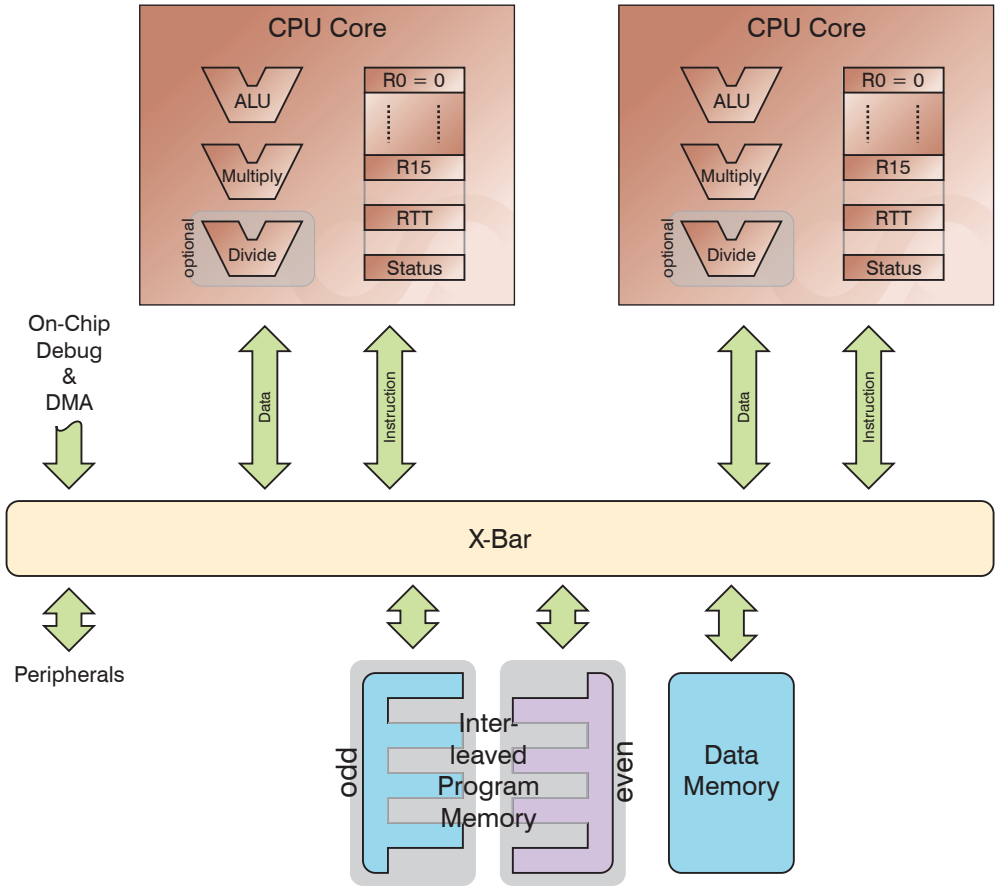
CoreMark 1.0 : 1.208312 / GCC4.5.3 20120201 (Cortus Eval) -mmul -flto -O3 -funroll-all-loops -finline-limit=500 -IC:/cortus-ide/toolchain/aps3/include -DPERFORMANCE_RUN=1 -Wl,--noinhibit-exec -Wl,--relax / STACK

Features

- Low Power RISC Core
- Very Small Silicon Footprint
- High F_{max}
- Excellent Code Density
- Fully 32 bit
- 5-7 Stage Pipeline
- Integer Multiply
- Full Toolchain and IDE at No Cost
- Full Peripheral Set

The APS3R has been designed to ensure high throughput, most instructions (including loads and stores) execute in a single cycle due to the 5-7 pipeline with out-of-order completion.

The simple, vectored, interrupt structure ensures low latency, real time, response to external events with a minimum of overhead. Up to 251 external user interrupts are supported.



Peripherals

The APS3R shares the low latency, high speed APS bus architecture with other members of the processor family. Cortus offers a wide choice of peripherals developed specifically for the APS family ranging from UARTs, Counters/Timers to Ethernet MACs and USB2.0 blocks all supplied with examples and driver code. Also available are bridges to and from AHB-Lite™.

A wide range of peripherals are available including:

- Counter
- Timer with Capture and PWM
- UART
- GPIO
- SPI
- I2C
- Watchdog
- USB 2.0 Device & OTG
- Ethernet 10/100 MAC
- AHB-Lite™ Bridge, master and slave

Ecosystem

The APS3R benefits from the shared ecosystem surrounding the APS family. It has a complete software development environment including toolchain for C and C++, a complete adapted IDE based on one of the most widely used IDEs - Eclipse. Debugging is fully supported with an integrated instruction set simulator, the Cortus on-chip-debuging hardware and an Ethernet connected JTAG interface - the EtherTag. Ports of various RTOSs are available such as FreeRTOS, Micrium μC/OS, μCLinux…

Going Further

The APS3R can be enhanced with either the optional 3 stage parallel multiplier or a divider. This delivers a performance figure of 1·92 CoreMarks/MHz. It is also possible to use the APS3 in a dual core configuration, for example a simple system with interleaved memory yields a CoreMark figure of 3·51 CoreMarks/MHz.

Upgrade Older Cores

The APS3R is an ideal upgrade for subsystems designed with older 8 bit or 16 bit cores. With APS3R there is no need to use assembly code and ANSI C or C++ offer greater productivity and lower risk.

Furthermore the APS3R has a silicon footprint similar to many 8 bit cores. With considerably more processing performance per cycle, fewer cycles are needed driving down power consumption. A 32 bit APS3R core delivers better code density and can save up to 55% in code memory area.

Applications

The APS3R is suited to a wide variety of applications, such as:

- SIM Cards
- Touchscreen Controllers
- Wireless Communication
- Image Processing
- Smart Metering
- Bluetooth
- Automotive Sensor Control
- Security Applications

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