ATSAMW25-MR210PB

IEEE 802.11 b/g/n SmartConnect Wi-Fi Module

PRELIMINARY DATASHEET

Description

The Atmel® | SMART SAMW25 module is based on the industry-leading low-power 2.4GHz IEEE® 802.11 b/g/n Wi-Fi® ATWINC1500 SoC (System on Chip) combined with the ARM® Cortex®-M0+ based microcontroller technology from Atmel.

This turnkey system provides an integrated software solution with application and security protocols such as TLS and integrated network services (TCP/IP stack) which are all available through Atmel Studio 6 integrated development environment (IDE). The Atmel SmartConnect modules offer the ideal solutions for designers seeking to add Wi-Fi connectivity with minimal previous experience in 802.11, IP Stack, or RF. Atmel SmartConnect Wi-Fi opens the door of the Internet of Things (IoT) to the vast array of battery-powered devices and applications requiring the integration of WLAN connectivity without compromising on cost or power consumption. While we compete with other Wi-Fi modules on size, RF performance, cost, and other characteristics, the Atmel SmartConnect product family has a distinctive advantage when it comes to power consumption and power saving modes. The ATSAMW25 device is a standalone end point, where a complete small application can be executed on the module by itself.

Features

Key features with SAMW25 Wireless connectivity solution:

- Certified Wi-Fi ATWINC1500B-MU-T with SAMD21 MCU
- IEEE 802.11 b/g/n 20MHz (1x1) solution
- Single spatial stream in 2.4GHz ISM band
- Compact footprint: 33.863 x 14.882mm
- Radio:
  - Output power - 802.11b /11Mbps: 17dBm ±1dB
  - 802.11g /54Mbps: 16dBm ±1dB @ EVM -28dB
  - 802.11n /72Mbps: 14dBm ±1dB @ EVM -30dB
- Application processor:
  - Atmel SAM D21 ARM Cortex M0+ based microcontroller
  - 256KB embedded Flash and 32KB SRAM
  - Full-Speed USB Device and embedded Host

- CryptoAuthentication™ ATECC508 (optional) I/O operating voltage: 2.7 to 3.6V
- Power Amplifier and On-board Switching Regulator operating voltage: 2.7 to 4.3V
- Power states supported:
  - Provision (AP/Sniffer) IDLE LISTEN
  - IDLE
  - SUSPEND
- Extreme low-power, on-chip low-power sleep oscillator
- Serial Host Interface SPI or UART
- Software Upgrade Over-the-Air (OTA)
- FCC, CE, IC, and TELEC Certified; RoHS compliant
- Security protocols; WPA/WPA2 Personal, TLS, and SSL
- Network services; DHCP, DNS, TCP/IP (IPv4), UDP, HTTP, and HTTPS

Target Applications

- IoT applications
- Smart appliances
- Multimedia streaming
- Safety and security
- Home automation
- Consumer electronics
- Industrial automation

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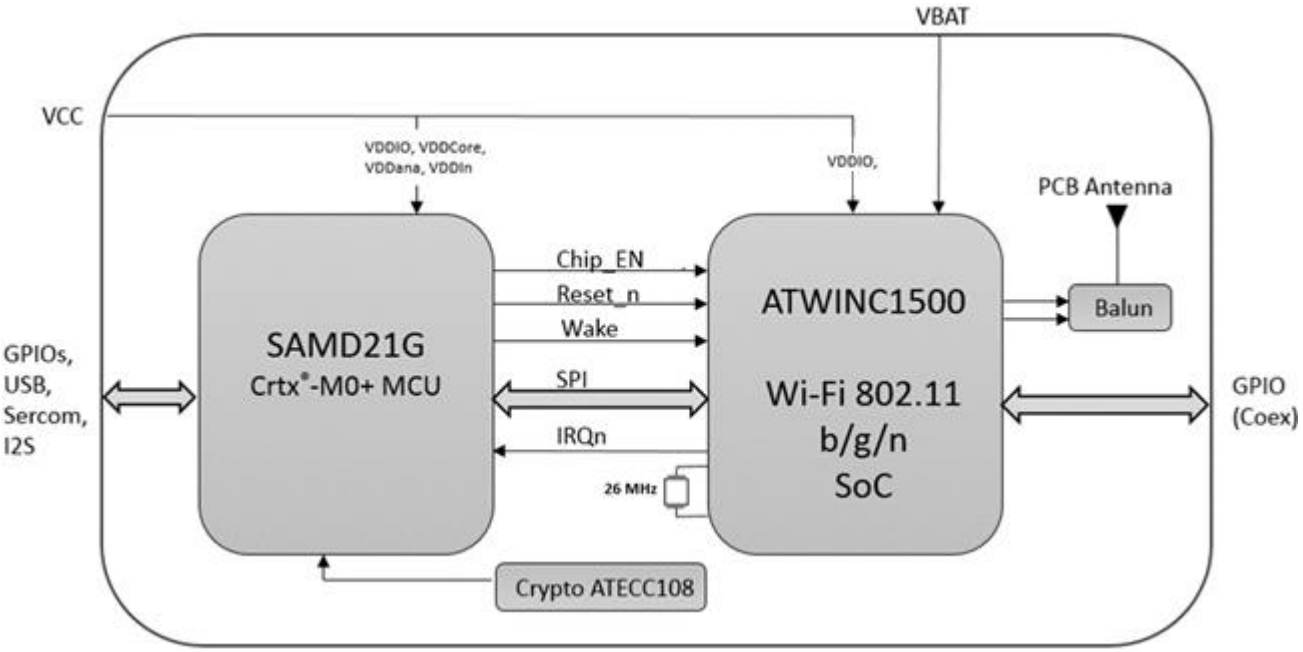
1 Block Diagram

Figure 1-1. ATSAMW25 Block Diagram



2 Ordering Information and IC Marking

Table 2-1. Ordering Details

Atmel ordering code	Package
ATSAMW25-MR210PB	ATWINC1500 + SAM D21 module. Tray Packing.
ATSAMW25-MR510PA	ATWINC1500 + SAM D21 + ATECC508 module. Tray Packing.
ATSAMW25-XPRO	Xplained board evaluation kit

3 Pinout and Package Information

3.1 Pin Description

Figure 3-1. Pin Assignment

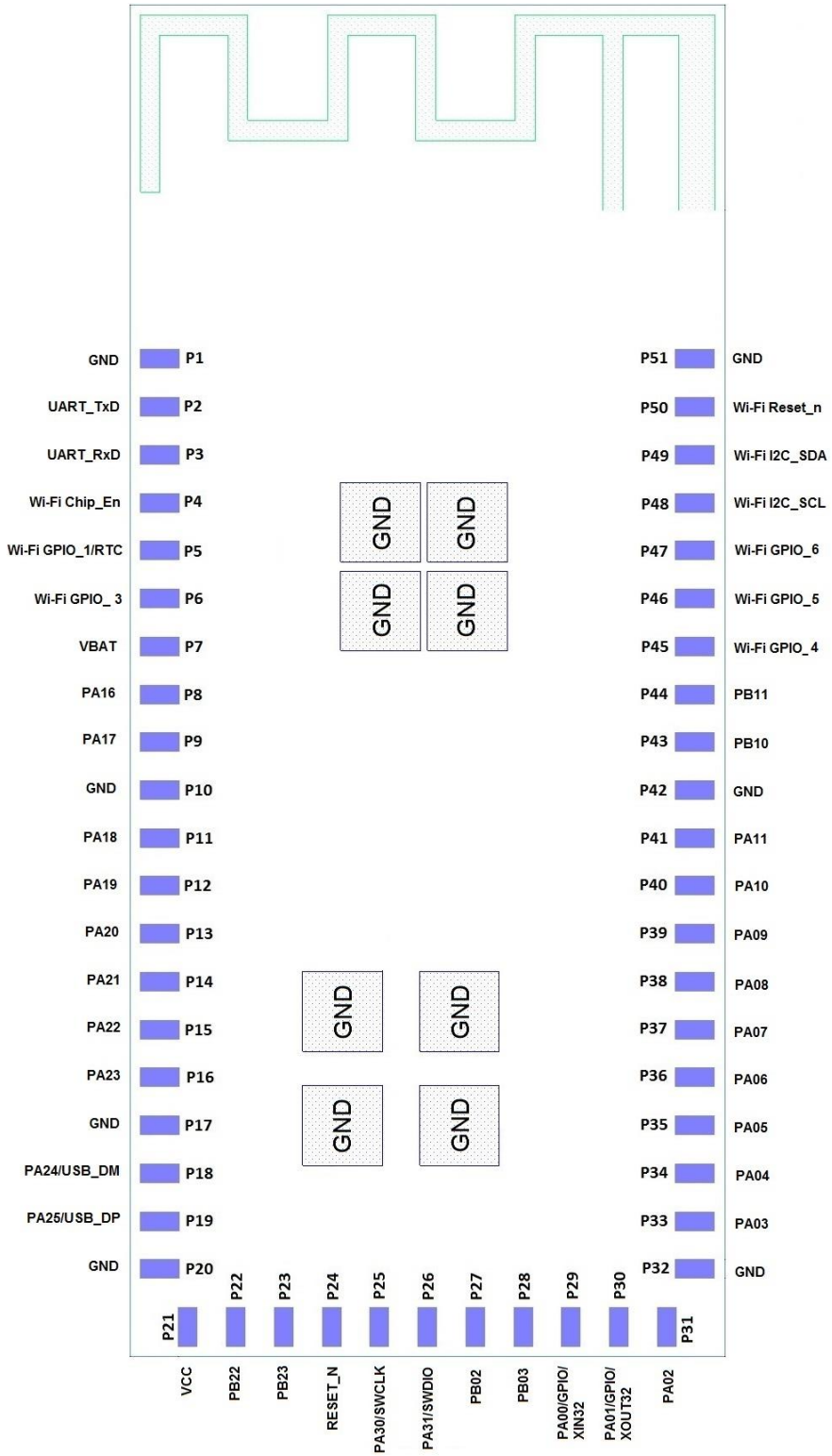


Table 3-1. Pin Description

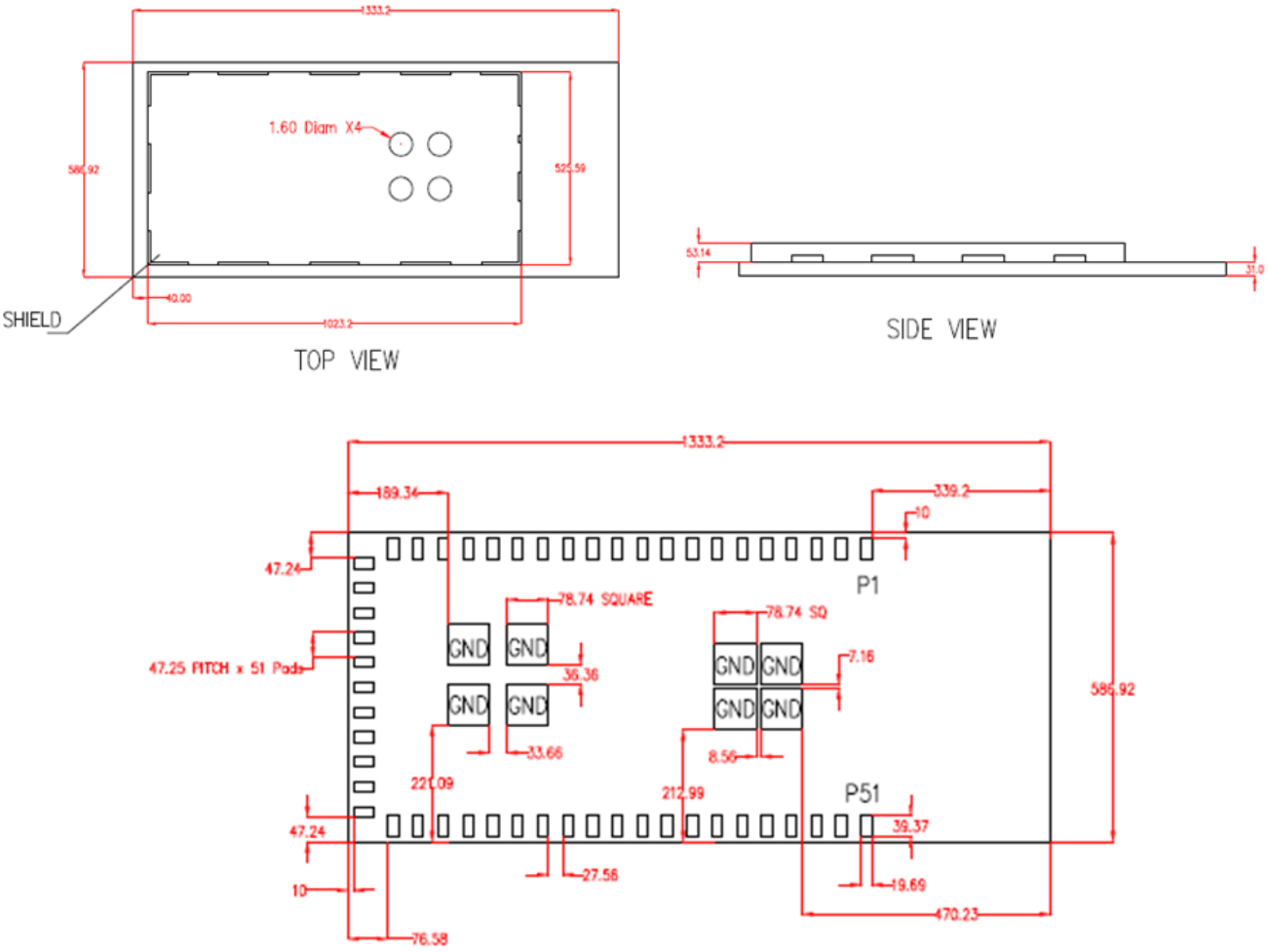
Pin #	Pin description	I/O type	Function (default)	Programmable pull-up/-down resistor
1	GND	N/A	Common ground	
2	UART_TxD	ATWINC1500 output	Currently used only for Atmel debug. Not for customer use. Leave unconnected.	Yes – pull-up
3	UART_RxD	ATWINC1500 input	Currently used only for Atmel debug. Not for customer use. Leave unconnected.	Yes – pull-up
4	Wi-Fi Chip_En	ATWINC1500 input	Currently used only for Atmel debug. Not for customer use. Leave unconnected.	No
5	Wi-Fi GPIO_1/RTC	ATWINC1500 I/O	ATWINC1500 General purpose I/O. Can also be used to input a 32.768KHz Real Time Clock for accurate timing of Wi-Fi sleep intervals	Yes – pull-up
6	Wi-Fi GPIO_3	-	ATWINC1500 General purpose I/O	Yes – pull-up
7	VBAT	Power	Supply for Wi-Fi RF Power Amplifier and Internal 1.3V Switching Regulator	
8	PA16	See SAM D21G datasheet	See SAM D21G datasheet	Yes
9	PA17	See SAM D21G datasheet	See SAM D21G datasheet	Yes
10	GND	Power	Ground	
11	PA18	See SAM D21G datasheet	See SAM D21G datasheet	Yes
12	PA19	See SAM D21G datasheet	See SAM D21G datasheet	Yes
13	PA20	See SAM D21G datasheet	See SAM D21G datasheet	Yes
14	PA21	See SAM D21G datasheet	See SAM D21G datasheet	Yes
15	PA22	See SAM D21G datasheet	See SAM D21G datasheet	Yes
16	PA23	See SAM D21G datasheet	See SAM D21G datasheet	Yes
17	GND	Power	Ground	
18	PA24/USB_DM	See SAM D21G datasheet	Host Interface USB Data minus pin	Yes
19	PA25/USB_DP	See SAM D21G datasheet	Host Interface USB Data Plus pin	Yes
20	GND	Power	Ground	
21	VCC	Power	Power supply for I/O	
22	PB22	See SAM D21G datasheet	See SAM D21G datasheet	Yes
23	PB23	See SAM D21G datasheet	See SAM D21G datasheet	Yes
24	RESET_N	Input see SAM D21G datasheet	System Reset. Low level on this pin resets the entire module.	Yes
25	PA30/SWCLK	See SAM D21G datasheet	Cortex Serial Wire Debug Interface CLK	Yes

Pin #	Pin description	I/O type	Function (default)	Programmable pull-up/-down resistor
26	PA31/SWDIO	See SAM D21G datasheet	Cortex Serial Wire Debug Interface Data I/O	Yes
27	PB02	See SAM D21G datasheet	See SAM D21G datasheet	Yes
28	PB03	See SAM D21G datasheet	See SAM D21G datasheet	Yes
29	PA00/GPIO/XIN32	See SAM D21G datasheet	See SAM D21G datasheet	Yes
30	PA01/GPIO/XOUT32	See SAM D21G datasheet	See SAM D21G datasheet	Yes
31	PA02	I/O	See SAM D21G datasheet	Yes
32	GND	Power	Ground	Yes
33	PA03	See SAM D21G datasheet	See SAM D21G datasheet	Yes
34	PA04	See SAM D21G datasheet	See SAM D21G datasheet	Yes
35	PA05	See SAM D21G datasheet	See SAM D21G datasheet	Yes
36	PA06	See SAM D21G datasheet	See SAM D21G datasheet	Yes
37	PA07	See SAM D21G datasheet	See SAM D21G datasheet	Yes
38	PA08	See SAM D21G datasheet	See SAM D21G datasheet	Yes
39	PA09	See SAM D21G datasheet	See SAM D21G datasheet	Yes
40	PA10	See SAM D21G datasheet	See SAM D21G datasheet	Yes
41	PA11	See SAM D21G datasheet	See SAM D21G datasheet	Yes
42	GND	Power	Ground	
43	PB10	See SAM D21G datasheet	See SAM D21G datasheet	Yes
44	PB11	See SAM D21G datasheet	See SAM D21G datasheet	Yes
45	Wi-Fi GPIO_4	ATWINC1500 I/O	ATWINC1500 General purpose I/O	Yes – pull-up
46	Wi-Fi GPIO_5	ATWINC1500 I/O	ATWINC1500 General purpose I/O	Yes – pull-up
47	Wi-Fi GPIO_6	ATWINC1500 I/O	ATWINC1500 General purpose I/O	Yes – pull-up
48	Wi-Fi I2C_SCL	ATWINC1500 I/O	Currently used only for Atmel debug. Not for customer use. Leave unconnected.	Yes – pull-up
49	Wi-Fi I2C_SDA	ATWINC1500 I/O	Currently used only for Atmel debug. Not for customer use. Leave unconnected.	Yes – pull-up
50	Wi-Fi Reset_n	ATWINC1500 Input	Currently used only for Atmel debug. Not for customer use. Leave unconnected.	No
51	GND	Power	Ground	

3.2 Package Description

The ATSAMW25-MR210PB package information.

Figure 3-2. SAMW25 MR210PB Package



SCALE: 1:1 or AS NOTED	DATE: 10/17/14	DRAWN: V. IRLANDA	TITLE: ATMEL CORP (LAKE FOREST) SAMW25–MR210PA PACKAGE OUTLINE DRAWING	
DIMENSIONAL UNIT: MILS	UNTOLERANCED DIMENSIONS ±3 Mils	ENGINEER: V. IRLANDA		
PROJECTION UNLESS SPECIFIED	ANGLE ±1°	CHECKED: V. IRLANDA		
		APPROVED:		
		CAD NAME:	DRAWING NUMBER:	REV. 1 / SHEET: 1 OF 1

4 Electrical Specifications

4.1 Absolute Ratings

All typical values are measured at T = 25°C unless otherwise specified. All minimum and maximum values are valid across operating temperature and voltage unless otherwise specified.

Table 4-1. Absolute Maximum Ratings

Parameters	Minimum	Maximum	Unit
VBAT power supply voltage	0	5.0	V
VCC power supply voltage	0	3.63	
Pin voltage with respect to GND and VCC	GND-0.3	VCC+0.3	
Storage temperature range	-40	+125	°C

Table 4-2. General Operating Ratings

Parameters	Minimum	Typical	Maximum	Unit
VBATT	3.0	3.6	4.3	°C
VCC	2.7	3.30	3.6	
Operating temperature range	-40	25	85	

Table 4-3. Physical Characteristics

Parameters	Value	Comments
Size	33.863 x 14.882mm	-
Connector pins pitch	See module footprint	-

Table 4-4. I/O Pins Characteristics

Characteristic	Minimum	Typical	Maximum	Unit
Input Low Voltage V_{IL}	-0.30		0.65	V
Input High Voltage V_{IH}	VCC-0.60		VCC+0.30	
Output Low Voltage V_{OL}			0.45	
Output High Voltage V_{OH}	VCC-0.50			
Output Loading			20	pF
Digital Input Load			6	
Pull-up Resistor	76K	90K	104K	Ω

I/O pin characteristics for pins 5, 45, 46, and 47 (for all other I/O, see the SAM D21G datasheet).

4.2 Recommended Operating Conditions

Table 4-5. Recommended Operating Conditions

Characteristic	Symbol	Minimum	Typical	Maximum	Unit
I/O supply voltage	VCC	2.7	3.3	3.6	V
Battery supply voltage	VBATT	3.0	3.6	4.3	
Operating temperature		-40		85	ºC

Notes: 1. I/O supply voltage is applied to the following pins: VDDIO_A and VDDIO.
2. Battery supply voltage is applied to following pins: VDD_BATT_PPA, VDD_BATT_PA, and VBATT_BUCK.

4.3 DC Electrical Characteristics

Table 4-6 provides the DC characteristics for the ATSAMW25 digital pads.

Table 4-6. DC Electrical Characteristics

Characteristic	Minimum	Maximum	Unit
Input Low Voltage V_{IL}	-0.30	0.65	V
Input High Voltage V_{IH}	VCC-0.60	VCC+0.30	
Output Low Voltage V_{OL}		0.45	
Output High Voltage V_{OH}	VCC-0.50		
Output Loading		20	pF
Digital Input Load		6	
Pad Drive Strength (regular pads[1])	8	13.5	mA
Pad Drive Strength (high-drive pads[1])	16	27	

Note: 1. The following are high-drive pads: I2C_SCL, I2C_SDA; all other pads are regular.

5 Application and Core Subsystems

5.1 Host Processor

The Atmel | SMART SAM D ARM Cortex-M0+ based microcontroller (MCU) series builds on decades of innovation and experience in embedded Flash microcontroller technology. It not only sets a new benchmark for flexibility and ease-of-use but also combines the performance and energy efficiency of an ARM Cortex-M0+ based MCU with an optimized architecture and peripheral set. The Atmel | SMART SAM D gives you a truly differentiated general-purpose microcontroller that is ideal for many low-power, cost-sensitive industrial, and consumer applications.

5.1.1 Host MCU Description

A rich set of peripherals, flexibility, and ease-of-use combined with low power consumption make the Atmel SAM D21 ideal for a wide range of home automation, consumer, metering, and industrial applications.

- ARM Cortex-M0+ based MCU running up to 48MHz
- 256KB embedded Flash and 32KB SRAM
- DMA and Event system
- Six flexible serial communication modules (SERCOM)
- Full-speed USB device and embedded Host
- 12-bit ADC (SAM D21G: 14 channels); 10-bit DAC
- Hardware touch support

5.1.2 Host MCU Key Features

- Low power consumption, down to 70µA/MHz
- Enhanced Analog Performance
  - ADC with offset and gain correction
  - Averaging, oversampling, and decimation
  - Flexible DAC
  - New low-power internal oscillators
  - ±2% accuracy over operating range
- Digital Innovations
  - Programmable Event System
  - Enhanced TC for Control Applications
  - Programmable SERCOM module
  - I^2C / SPI / USART / LIN2 / IrDA
  - Full Speed USB Device and Host
  - No external components needed
  - 6-12 channel DMA with CRC module
  - PTC Hardware touch module
  - I^2S module with PDM support

5.2 Wi-Fi Core Processor

ATWINC1500B has a Cortus APS3 32-bit processor. This processor performs many of the MAC functions, including but not limited to association, authentication, power management, security key management, and MSDU aggregation/de-aggregation. In addition, the processor provides flexibility for various modes of operation, such as STA and AP modes.

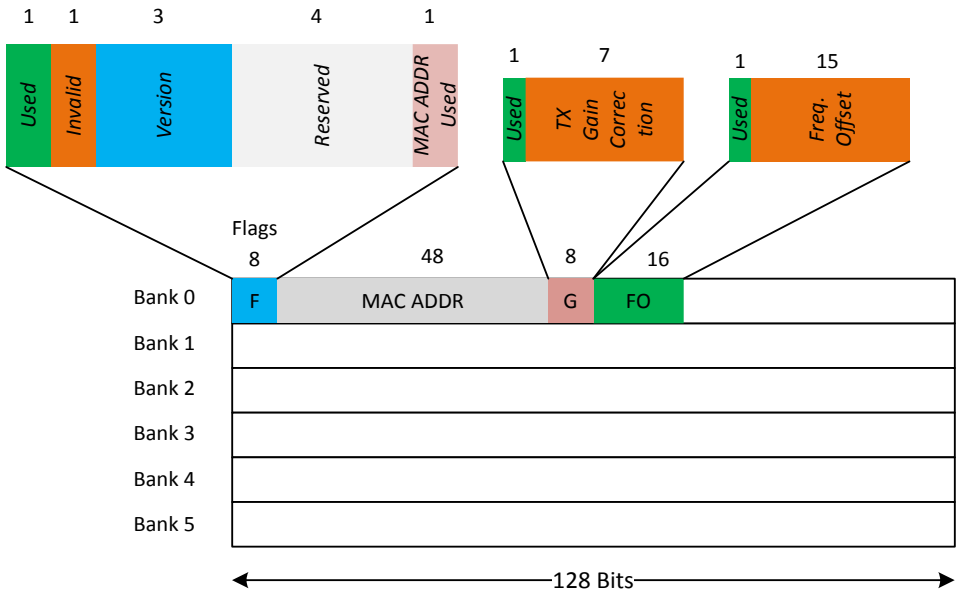
5.2.1 Memory Subsystem

The APS3 core uses a 128KB instruction/boot ROM along with a 128KB instruction RAM and a 64KB data RAM. ATWINC1500B also has 8Mb of flash memory, which can be used for system software. In addition, the device uses a 128KB shared RAM, accessible by the processor and MAC, which allows the APS3 core to perform various data management tasks on the TX and RX data packets.

5.2.2 Non-volatile Memory (eFuse)

ATWINC1500B has 768 bits of non-volatile eFuse memory that can be read by the CPU after device reset. This non-volatile one-time-programmable (OTP) memory can be used to store customer-specific parameters, such as MAC address; various calibration information, such as TX power, crystal frequency offset, etc.; and other software-specific configuration parameters. The eFuse is partitioned into six 128-bit banks. Each bank has the same bit map, which is shown in Figure 5-1. The purpose of the first 80 bits in each bank is fixed, and the remaining 48 bits are general-purpose software dependent bits, or reserved for future use. Since each bank can be programmed independently, this allows for several updates of the device parameters following the initial programming, e.g. updating MAC address. Refer to ATWINC1500B Programming Guide for the eFuse programming instructions.

Figure 5-1. eFuse Bit Map



6 WLAN Subsystem

The WLAN subsystem is composed of the Media Access Controller (MAC) and the Physical Layer (PHY). The following two subsections describe the MAC and PHY in detail.

6.1 MAC

6.1.1 Features

The ATWINC1500B IEEE802.11 MAC supports the following functions:

- IEEE 802.11b/g/n
- IEEE 802.11e WMM® QoS EDCA/PCF multiple access categories traffic scheduling
- Advanced IEEE 802.11n features:
  - Transmission and reception of aggregated MPDUs (A-MPDU)
  - Transmission and reception of aggregated MSDUs (A-MSDU)
  - Immediate Block Acknowledgement
  - Reduced Interframe Spacing (RIFS)
- Support for IEEE802.11i and WFA security with key management
  - WEP 64/128
  - WPA-TKIP
  - 128-bit WPA2 CCMP (AES)
- Support for WAPI security
- Advanced power management
  - Standard 802.11 Power Save Mode
  - Wi-Fi Alliance WMM-PS (U-APSD)
- RTS-CTS and CTS-self support
- Supports either STA or AP mode in the infrastructure basic service set mode
- Supports independent basic service set (IBSS)

6.1.2 Description

The ATWINC1500B MAC is designed to operate at low power while providing high data throughput. The IEEE 802.11 MAC functions are implemented with a combination of dedicated data path engines, hardwired control logic, and a low-power, high-efficiency microprocessor. The combination of dedicated logic with a programmable processor provides optimal power efficiency and real-time response while providing the flexibility to accommodate evolving standards and future feature enhancements. Dedicated data path engines are used to implement data path functions with heavy computational. For example, an FCS engine checks the CRC of the transmitting and receiving packets, and a cipher engine performs all the required encryption and decryption operations for the WEP, WPA-TKIP, WPA2 CCMP-AES, and WAPI security requirements. Control functions, which have real-time requirements, are implemented using hardwired control logic modules. These logic modules offer real-time response while maintaining configurability via the processor. Examples of hardwired control logic modules are the channel access control module (implements EDCA/HCCA, Beacon TX control, inter-frame spacing, etc.), protocol timer module (responsible for the Network Access Vector, back-off timing, timing synchronization function, and slot management), MPDU handling module, aggregation/de-aggregation module, block ACK controller (implements the protocol requirements for burst block communication), and TX/RX control FSMs (coordinate data movement between PHY-MAC interface, cipher engine, and the DMA interface to the TX/RX FIFOs).ø

The MAC functions implemented solely in software on the microprocessor have the following characteristics:

- Functions with high memory requirements or complex data structures. Examples are association table management and power save queuing.
- Functions with low computational load or without critical real-time requirements. Examples are authentication and association.
- Functions which need flexibility and upgradeability. Examples are beacon frame processing and QoS scheduling.

6.2 PHY

6.2.1 Features

The ATWINC1500B IEEE802.11 PHY supports the following functions:

- Single antenna 1x1 stream in 20MHz channels
- Supports IEEE 802.11b DSSS-CCK modulation: 1, 2, 5.5, and 11Mbps
- Supports IEEE 802.11g OFDM modulation: 6, 9, 12,18, 24, 36, 48, and 54Mbps
- Supports IEEE 802.11n HT modulations MCS0-7, 20MHz, 800 and 400ns guard interval: 6.5, 7.2, 13.0, 14.4, 19.5, 21.7, 26.0, 28.9, 39.0, 43.3, 52.0, 57.8, 58.5, 65.0, and 72.2Mbps
- IEEE 802.11n mixed mode operation
- Per packet TX power control
- Advanced channel estimation/equalization, automatic gain control, CCA, carrier/symbol recovery, and frame detection

6.2.2 Description

The ATWINC1500B WLAN PHY is designed to achieve reliable and power-efficient physical layer communication specified by IEEE 802.11 b/g/n in single stream mode with 20MHz bandwidth. Advanced algorithms have been employed to achieve maximum throughput in a real world communication environment with impairments and interference. The PHY implements all the required functions such as FFT, filtering, FEC (Viterbi decoder), frequency and timing acquisition and tracking, channel estimation and equalization, carrier sensing, and clear channel assessment, as well as the automatic gain control.

6.3 Radio

6.3.1 Receiver Performance

Radio performance under typical conditions: VBAT = 3.3V; VDDIO = 3.3V; Temp.: 25°C @ RF pins

Table 6-1. Receiver Performance

Parameter	Description	Minimum	Typical	Maximum	Unit
Frequency		2,412		2,484	MHz
Sensitivity 802.11b	1Mbps DSS		-98		dBm
	2Mbps DSS		-94		dBm
	5.5Mbps DSS		-92		dBm
	11Mbps DSS		-88		dBm

Parameter	Description	Minimum	Typical	Maximum	Unit
Sensitivity 802.11g	6Mbps OFDM		-90		dBm
	9Mbps OFDM		-89		dBm
	12Mbps OFDM		-88		dBm
	18Mbps OFDM		-85		dBm
	24Mbps OFDM		-83		dBm
	36Mbps OFDM		-80		dBm
	48Mbps OFDM		-76		dBm
	54Mbps OFDM		-74		dBm
Sensitivity 802.11n (BW=20MHz)	MCS 0		-89		dBm
	MCS 1		-87		dBm
	MCS 2		-85		dBm
	MCS 3		-82		dBm
	MCS 4		-77		dBm
	MCS 5		-74		dBm
	MCS 6		-72		dBm
	MCS 7		-70.5		dBm
Maximum Receive Signal Level	1-11Mbps DSS		0		dBm
	6-54Mbps OFDM		0		dBm
	MCS 0 – 7		0		dBm
Adjacent Channel Rejection	1Mbps DSS (30MHz offset)		50		dB
	11Mbps DSS (25MHz offset)		43		dB
	6Mbps OFDM (25MHz offset)		40		dB
	54Mbps OFDM (25MHz offset)		25		dB
	MCS 0 – 20MHz BW (25MHz offset)		40		dB
	MCS 7 – 20MHz BW (25MHz offset)		20		dB
Cellular Blocker Immunity	776-794MHz CDMA		-14		dBm
	824-849MHz GSM		-10		dBm
	880-915MHz GSM		-10		dBm
	1710-1785MHz GSM		-15		dBm
	1850-1910MHz GSM		-15		dBm
	1850-1910MHz WCDMA		-24		dBm
	1920-1980MHz WCDMA		-24		dBm

Measured at RF pin assuming 50Ω differential; RF performance guaranteed for temperature range -30 to 85ºC. 1dB derating in performance at -40ºC.

6.3.2 Transmitter Performance

Radio performance under typical conditions: VBAT = 3.3V; VDDIO = 3.3V; Temp.: 25°C @ RF pins

Table 6-2. Transmitter Performance

Parameter	Description	Minimum	Typical	Maximum	Unit
Frequency		2,412		2,484	MHz
Output Power[1], ON_Transmit_High_Power Mode	802.11b 1Mbps		18.5		dBm
	802.11b 11Mbps		19.5		dBm
	802.11g 6Mbps		18.5		dBm
	802.11g 54Mbps		16.5		dBm
	802.11n MCS 0		17.0		dBm
	802.11n MCS 7		14.5		dBm
Output Power[1], ON_Transmit_Low_Power Mode	802.11b 1Mbps		17.0		dBm
	802.11b 11Mbps		17.5		dBm
	802.11g 6-18Mbps		16.0		dBm
	802.11g >18Mbps		N/A		dBm
	802.11n MCS 0-3		14.5		dBm
	802.11n >MCS 3		N/A		dBm
TX Power Accuracy			±1.5[2]		dB
Carrier Suppression			30.0		dBc
Out of Band Transmit Power	76-108		-125		dBm/Hz
	776-794		-125		dBm/Hz
	869-960		-125		dBm/Hz
	925-960		-125		dBm/Hz
	1570-1580		-125		dBm/Hz
	1805-1880		-125		dBm/Hz
	1930-1990		-125		dBm/Hz
	2110-2170		-125		dBm/Hz
Harmonic Output Power	2nd			-41	dBm/MHz
	3rd			-41	dBm/MHz

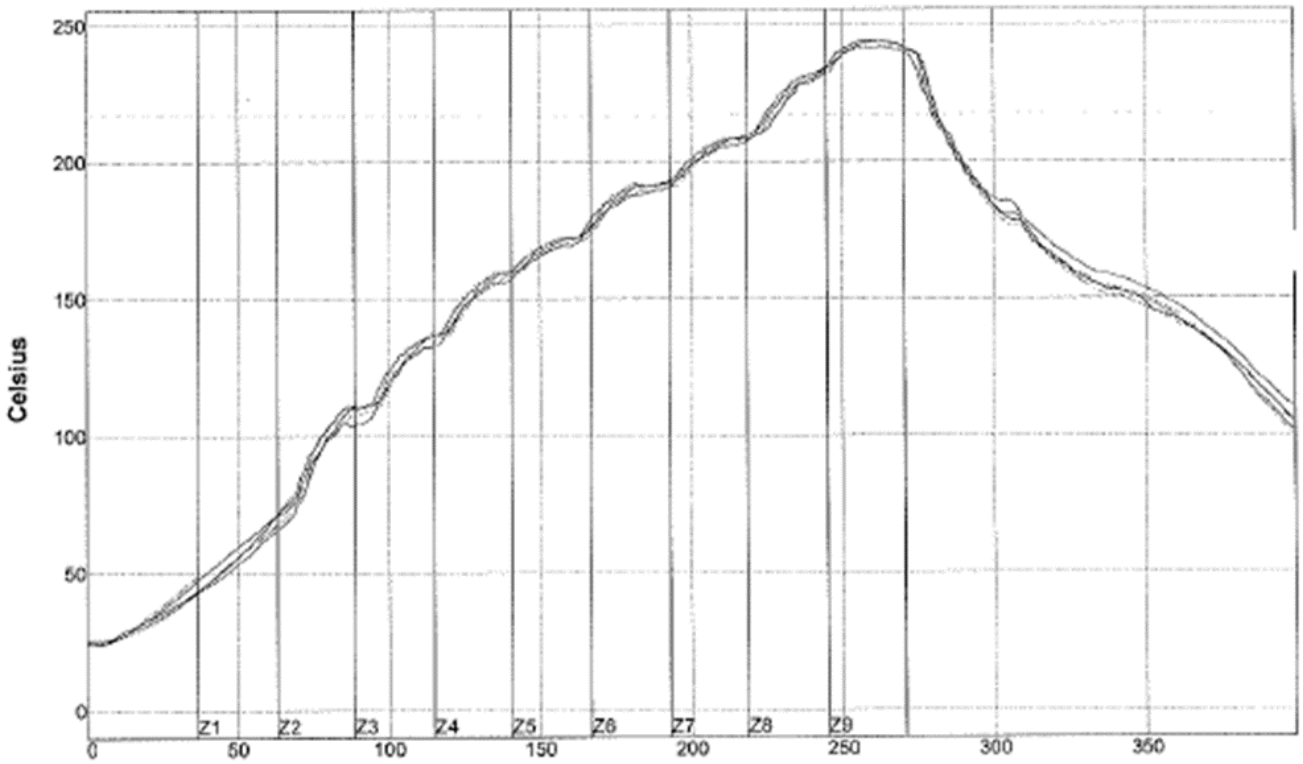
Notes: 1. Measured at 802.11 spec compliant EVM/Spectral Mask.
2. Measured after RF matching network. See reference design.

7 Recommended Reflow Profile

Setpoints (Celsius)

Zone	1	2	3	4	5	6	7	8	9
Top	200	140	160	180	180	210	220	265	265
Bottom	200	140	160	180	180	210	220	265	265

Conveyor Speed (cm/min): 65.0



PWI= 64%	Max Rising Slope		Max Falling Slope		Soak Time 150-200C		Reflow Time /217C		Peak Temp	
<TC2>	1.17	-41%	-3.92	-30%	74.60	-51%	54.87	-56%	242.73	-23%
<TC3>	1.19	-40%	-2.68	13%	75.03	-50%	54.99	-56%	241.73	-31%
<TC4>	1.18	-41%	-4.09	-35%	74.83	-51%	54.90	-56%	244.28	-12%
<TC5>	1.19	-40%	-3.63	-20%	73.47	-55%	53.11	-64%	244.22	-13%
<TC6>	1.17	-41%	-4.04	-34%	73.63	-55%	55.09	-55%	243.92	-15%
Delta	0.02		1.41		1.56		1.98		2.55	

Process Window:

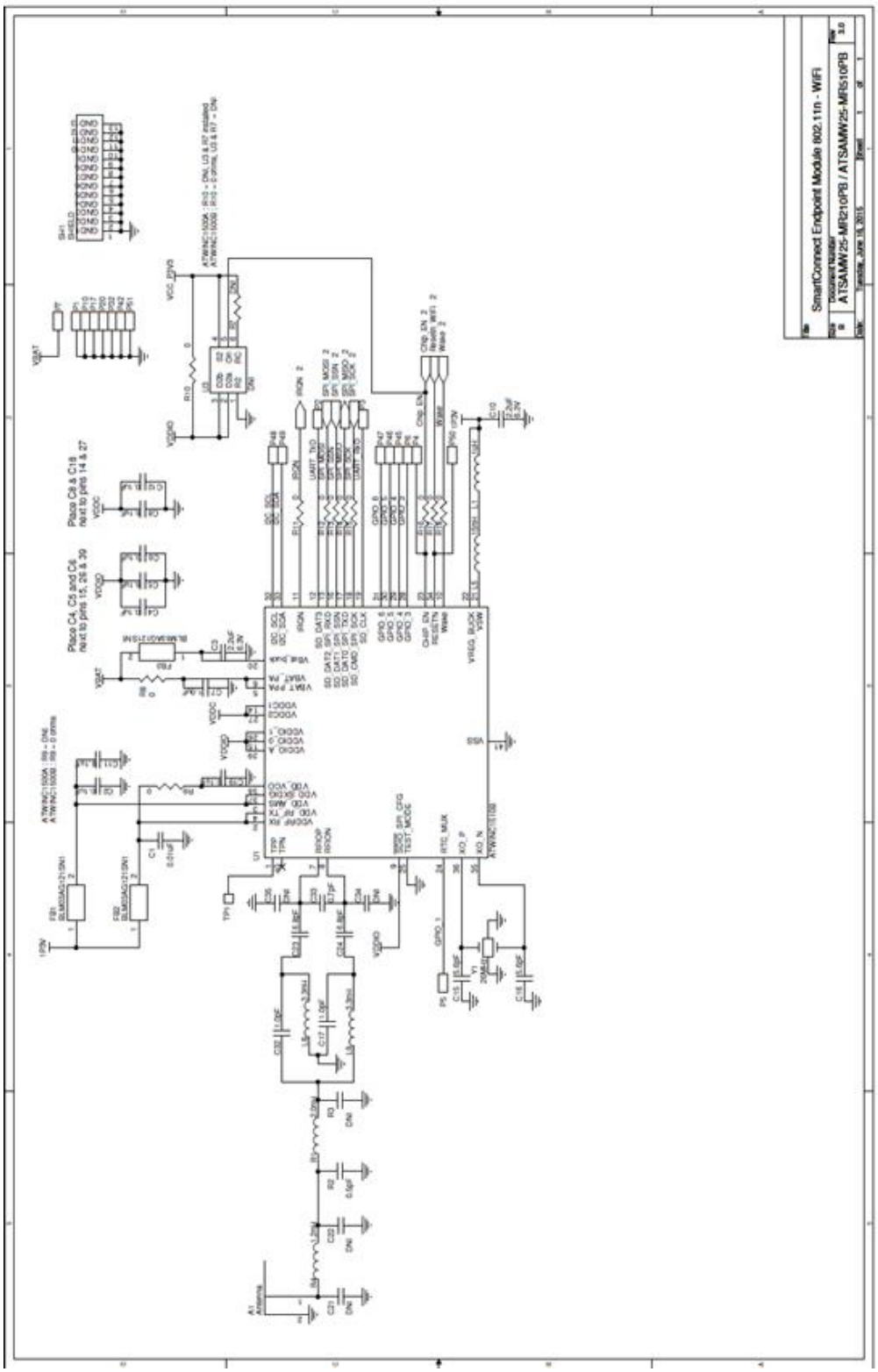
Solder Paste: RoHS

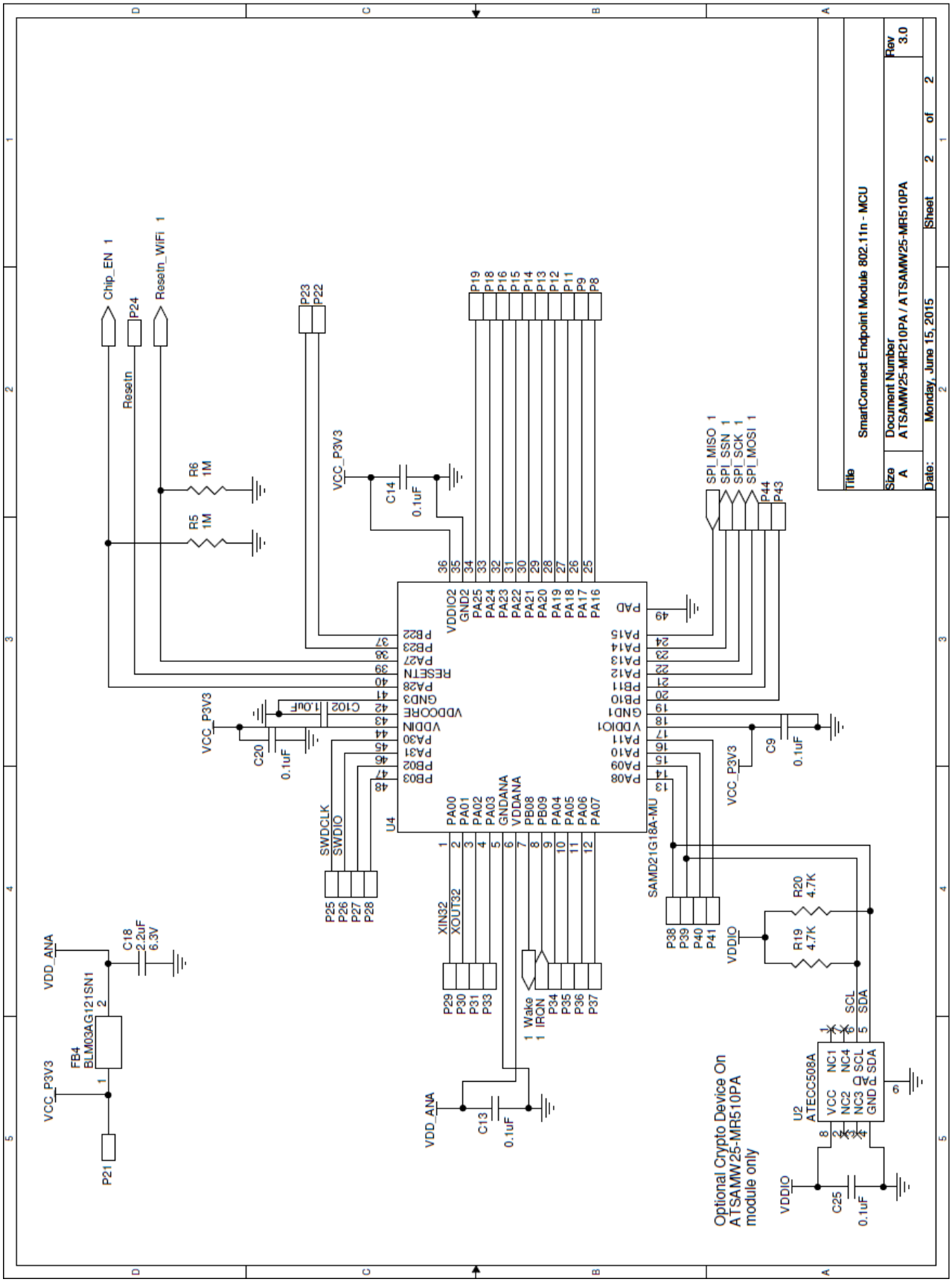
Statistic Name	Low Limit	High Limit	Units
Max Rising Slope (Target=2.0)	0	3	Degrees/Second
(Calculate Slope over 90 Seconds)			
Max Falling Slope	-6	-0.1	Degrees/Second
(Calculate Slope over 6 Seconds)			
Soak Time 150-200C	60	120	Seconds
Time Above Reflow - 217C	45	90	Seconds
Peak Temperature	232	260	Degrees Celsius

8 Module Schematic

The ATSAMW25-MR210PB/MR510PB Module schematic is shown in Figure 8-1.

Figure 8-1. ATSAMW25-MR210PB/MR510 Module Schematic




SmartConnect Endpoint Module 802.11n - MCU
Document Number
ATSAMW25-MR210PA / ATSAMW25-MR510PA
Rev 3.0
Monday, June 15, 2015
Sheet 2 of 2
SAMD21G18A-MU
ATECC508A
Optional Crypto Device On ATSAMW25-MR510PA module only
VCC_P3V3
VDD_ANA
VDDIO
Chip_EN_1
ResetIn_WiFi_1
ResetIn
SPI_MISO_1
SPI_SSN_1
SPI_SCK_1
SPI_MOSI_1
SWDCLK
SWDIO
XIN32
XOUT32
Wake
IRQN
SCL
SDA

9 Bill of Materials (BOM)

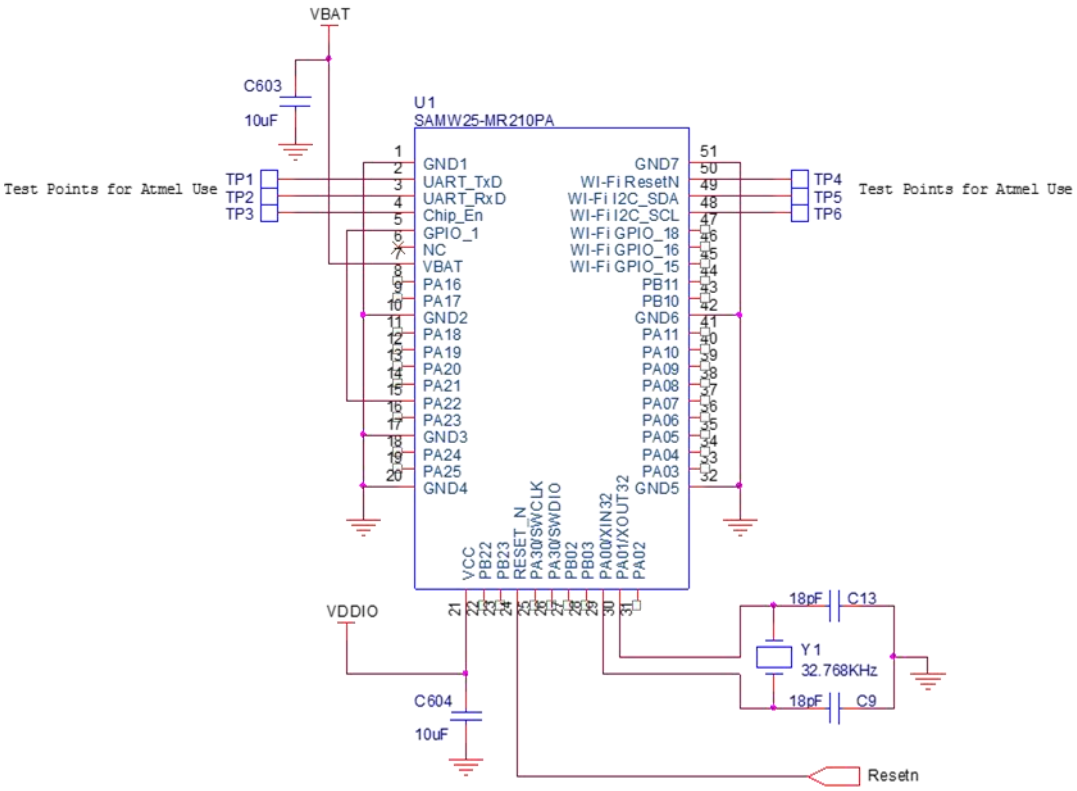
SmartConnect Endpoint Module 802.11n - WiFi Revised: Monday, June 15, 2015
SAMW25-MR510PB Revision: 1

Bill Of Materials

Item	Qty	Reference	Value	Description	Manufacturer	Part Number	Footprint
1	1	A1	Antenna	Antenna, Printed PCB, Inverted F		Non-Component	PCB F
2	1	C1	0.01uF	CAP,CER,0.01uF,10%,X5R,0201,10V,-55-125C	Murata	GRM033R61A103KA01D	0201
3	13	C2,C4,C5,C6,C8,C9,C11, C12,C13,C14,C19,C20,C25	0.1uF	CAP,CER,0.1uF,10%,X5R,0201,6.3V,-55-125C	Murata	GRM033R60J104KE19D	0201
4	3	C3,C10,C18	2.2uF	CAP,CER,2.2uF,10%,X5R,0402,6.3V,-55-85C	TDK	C1005X5R0J225K	0402
5	2	C7,C102	1.0uF	CAP,CER,1.0uF,10%,X5R,0402,6.3V,-55-85C	GRM155R60J105KE19D	GRM155R60J105KE19D	0402
6	2	C15,C16	5.6pF	CAP,CER,5.6pF,+/-0.5pF,NPO,0201,25V,-55-125C	Murata	GRM0335C2A5R6DA01D	0201
7	2	C17,C32	1.0pF	CAP,CER,1.0pF,+/-0.1pF,NPO,0201,25V,-55-125C	Murata	GRM0335C1E1R0BA01J	0201
8	1	C21	DNI	CAP,CER,1.0pF,+/-0.1pF,NPO,0201,25V,-55-125C	Murata	GRM0335C1E1R0BA01J	0201
9	1	C22	DNI	CAP,CER,0.5pF,+/-0.1pF,NPO,0201,25V,-55-125C	Murata	500RGRM0335C1ER50BA0	0201
10	2	C23,C24	6.8pF	CAP,CER,6.8pF,+/-0.5pF,NPO,0201,25V,-55-125C	TDK	C0603C0G1E6R8D030BA	0201
11	1	C33	0.7pF	CAP,CER,0.7pF,+/-0.05pF,NPO,0201,25V,-55-125C	TDK	C0603C0G1E0R7W030BF	0201
12	2	C34,C35	DNI	CAP,CER,0.5pF,+/-0.1pF,NPO,0201,25V,-55-125C	Murata	500RGRM0335C1ER50BA01D07S0R5AV4T	0201
13							
14	4	FB1,FB2,FB3,FB4	BLM03AG121SN1	FERRITE,120 OHM @100MHz,200mA,0201,-55-125C	Murata	BLM03AG121SN1	0201
15	1	L1	1uH	POWER INDUCTOR,1uH,20%,940mA,0.125ohms,0603,shielded,-40-85c	Murata	LQM18PN1R0MFRL	0603
16	1	L5	15nH	INDUCTOR,Multilayer,15nH,5%,350mA,Q=8@100MHz,0402	Murata	LQG15HS15NJ02D	0402
17	2	L8,L9	3.3nH	Inductor,3.3nH,+/-0.2nH,Q=13@500MHz,SRF=8.1GHz,0201,-55-125C	Taiyo Yuden	HKQ0603S3N3C-T	0201
18	51	P1,P2,P3,P4,P5,P6,P7,P8, P9,P10,P11,P12,P13,P14, P15,P16,P17,P18,P19,P20, P21,P22,P23,P24,P25,P26, P27,P28,P29,P30,P31,P32, P33,P34,P35,P36,P37,P38, P39,P40,P41,P42,P43,P44, P45,P46,P47,P48,P49,P50, P51	PAD_0.7x1.2	LGA Module Pad, 0.7mm x 1.2mm		Non-Component	PAD_0.7mmx1.2mm
19	1	R1	2.0nH	Inductor,2.0nH,+/-0.2nH,Q=13@500MHz,SRF=8.1GHz,0201,-55-125C	Taiyo Yuden	HKQ0603S2N0C-T	0201
20	1	R2	0.5pF	CAP,CER,0.5pF,+/-0.1pF,NPO,0201,25V,-55-125C	Murata	GRM0335C1ER50BA0	0201
21	1	R3	DNI	CAP,CER,0.5pF,+/-0.1pF,NPO,0201,25V,-55-125C	Murata	GRM0335C1ER50BA0	0201
22	1	R4	1.2nH	Inductor,1.2nH,+/-0.1nH,Q=14@500MHz,SRF=6GHz,0201,-55-125C	Murata	LQP03TN1N2B02D	0201
23	2	R5,R6	1M	RESISTOR,Thick Film,1M,5%,0201	Vishay	CRCW0201-105J	0201
24	1	R7	DNI	RESISTOR,Thick Film,1M,5%,0201	Vishay	CRCW0201-105J	0201
25	11	R8,R9,R10,R11,R12,R13, R14,R15,R16,R17,R18	0	RESISTOR,Thick Film,0 ohm,0201	Panasonic	ERJ-1GN0R00C	0201
26	2	R19,R20	4.7K	RESISTOR,Thick Film,4.7K,5%,0201	Vishay	CRCW0201-472J	0201
27	1	SH1	SHIELD	Shield			SHIELD
28	1	TP1	DNI	Test Point,Surface Mount,0.030"sq.		Non-Component	
29	1	U1	ATWINC1510B	IC, WiFi + 8GB FLASH 40QFN	Atmel	ATWINC1510B	40QFN
30	1	U2	ATECC508A	IC, Memory, Crypto Authentication, 8UDFN	Atmel	ATECC508A-MAHWF-T	8UDFN
31	1	U3	DNI	IC, Load Switch,1.8V-12V In,RDSon=0.3ohm@2.5V,SC70-6	Vishay	SI1865DDL	SC70-6
32	1	U4	SAMD21G18A-MU	MCU,	Atmel	SAMD21G18A-MU	48QFN
33	1	Y1	26MHz	CRYSTAL,26MHz,CL=7pF,10ppm,-40-85C,ESR=50,3.2x2.5mm	Tatien	A0183-X-002-3	2.0mm x 2.5mm

10 Application Schematic

Figure 10-1. Connections for the ATSAMW25



The basic power supply connections for the ATSAMW25 module are shown in Figure 10-1. The test points shown (TP1 – TP6) should be added in case Atmel is required to debug the design.

The Wi-Fi chip can use its own internal oscillator for a Real Time Clock (RTC) or it can use an external 32.768KHz clock provided on the RTC pin. Using an external clock derived from a crystal oscillator can be used as a more accurate sleep timer for the Wi-Fi chip than its own internal oscillator. This in turn can reduce sleep current. If power consumption during sleep is a priority then a 32.768KHz crystal can be added to the SAM D21 module as shown in the reference design. The design shown above displays a connection from pin 15 (PA22) to pin 5 (GPIO_1).

GPIO_1 is the input pin for the Wi-Fi's Real Time Clock. PA22 can be configured to output a 32.768KHz RTC clock – derived from the 32.768KHz crystal - to be used as the source for the Wi-Fi's RTC. If cost is a priority versus power consumption, then the 32.768KHz crystal can be left off of the design and the PA22 – GPIO_1 connection can be deleted.

11 Design Guidelines

It is critical to follow the recommendations listed below to achieve the best RF performance:

- When the module is placed on the motherboard, a provision for the antenna must be made. There should be nothing under the portion of the module which contains the antenna. This means the antenna should not be placed directly on top of the motherboard PCB. This can be accomplished by, for example, placing the module at the edge of the board such that the module edge with the antenna extends beyond the main board edge by 6.5mm. Alternatively, a cutout in the motherboard can be provided under the antenna. The cutout should be at least 22 x 6.5mm. Ground vias spaced 2.5mm apart should be placed all around the perimeter of the cutout. No large components should be placed near the antenna.
- Keep away from antenna, as far as possible, large metal objects to avoid electromagnetic field blocking
- Do not enclose the antenna within a metal shield
- Keep any components which may radiate noise or signals within the 2.4 – 2.5GHz frequency band far away from the antenna, or better yet, shield those components. Any noise radiated from the main board in this frequency band will degrade the sensitivity of the module.
- The main board should have a solid ground plane. Each ground pin of the module (including each of the center ground pads) should have a via placed either in the pad or right next to the pad going down to the ground plane.
- Place a 10µF decoupling capacitor from VBAT to ground right next to pin 7. Place another 10µF capacitor from VCC to ground right next to pin 21.
- Contact Atmel for assistance if any other placement is required

12 Reference Documentation and Support

12.1 Reference Documents

Atmel offers a set of collateral documentation to ease integration and device ramp.

The following list of documents available on Atmel web or integrated into development tools.

Table 12-1. Reference Documents

Title	Content
Datasheet	This document
Design Files	User Guide, Schematic, PCB layout, Gerber, BOM, and System notes on: RF/Radio Full Test Report, radiation pattern, design guidelines, temperature performance, ESD.
Package	How to use package: Out of the Box starting guide, HW limitations and notes, SW Quick start guidelines.
Platform Getting started Guide	Best practices and recommendations to design a board with the product, including: Antenna Design for Wi-Fi (layout recommendations, types of antennas, impedance matching, using a power amplifier etc.), SPI/UART protocol between Wi-Fi SoC and the Host MCU.
HW Design Guide	Integration guide with clear description of: High level Arch, overview on how to write a networking application, list all API, parameters and structures. Features of the device, SPI/handshake protocol between device and host MCU, with flow/sequence/state diagram, timing.
SW Design Guide	Explain in details the flow chart and how to use each API to implement all generic use cases (e.g. start AP, start STA, provisioning, UDP, TCP, http, TLS, p2p, errors management, connection/transfer recovery mechanism/state diagram) - usage and sample application note.

For a complete listing of development-support tools and documentation, visit http://www.atmel.com/ or contact the nearest Atmel field representative.

12.2 Related Documents

[1] ATSAM D21 Datasheet:
Web page: http://www.atmel.com/products/microcontrollers/arm/sam-d.aspx?tab=documents.
Document: Atmel SAM D21 Datasheet (.pdf file).
Then select the required device (ATSAMD21E18A) and get the latest datasheet (.pdf file).

[2] ATWINC1500B Datasheet.

[3] ATSAM W25 Network Controller Programming Guide.

[4] ATSAM W25 Starter Kit User Guide.

13 Revision History

Doc Rev.	Date	Comments
42618A	11/2015	Initial document release.

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