

1 General

1.1 Introduction and Intended Use (Informative)

This standard describes an interface between a main module, referred to as master, and extension modules, referred to as slaves, in the model. These can be sound modules, extended function

- 5 outputs, or other function modules. The SUSI is an abbreviation for “Serial User Standard Interface”.



The SUSI logo is a trademark of Dietz Elektronik GmbH & Co.KG. It can be used freely on compatible products.

- 10 This document replaces and supersedes TI-9.2.3 Serial User Standard Interface for DCC.

1.2 References

This standard should be interpreted in the context of the following NMRA Standards, Technical Notes, and Technical Information.

1.2.1 Normative

- 15
- S-9.1.1.3 21MTC Decoder Interface
 - S-9.1.1.4 PluX Decoder Interface
 - S-9.1.1.5 Next18 and Next18S Decoder Interface
 - S-9.2.1 DCC Extended Packet Formats

1.2.2 Informative

- 20
- TI-9.2.3 Serial User Standard Interface for DCC
 - RCN-600 SUSI bus
 - RCN-601 SUSI-BiDi
 - RCN-602 SUSI Bus Configuration Variables

1.3 Terminology

Term	Definition
SUSI	Abbreviation for “Serial User Standard Interface”

25 1.4 Requirements

In order to meet this standard, all mechanical and electrical characteristics as well as the defined commands shall be observed. It is not necessary to support all commands of the interface. This applies to both master and slave modules. The description of the respective product shall list the implemented functions. A component tolerance of 10% is permissible for all resistance values.

30 2 Mechanical properties

There are three different plug systems, which also differ in their electrical characteristics.

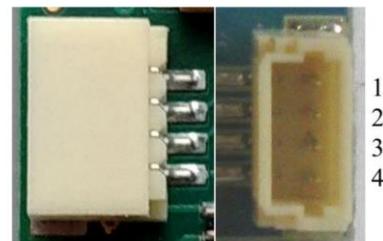
Designation	Master Connector(s)	Slave Connector(s)	Current Capacity
classicSUSI	JST SM04B-SRSS-TB JST BM04B-SRSS-TB	JST 04SR3S JST SRH-04V-SB	1000mA
microSUSI	JST SM04BXRS-ETB	JST 04XSR-36S	200mA
powerSUSI	Würth 62000511622 Würth 62000511722 Würth 620305124822 Würth 620105131822	Würth 620005113322	2000mA

“classicSUSI” is the interface that has been known since 2003 and is mainly used in H0 scale.

“microSUSI” is a small design introduced in 2017, e.g. for N scale. “powerSUSI” was added in 2018 for larger scales and modules with higher power requirements. The three versions are described in more detail in the following sections. Alternatively, solder pads can be provided for the connection instead of a plug. Additionally, it is also possible to connect a SUSI module to a decoder interface as described in S-9.1.2.3, S-9.1.2.4, and S-9.1.2.5.

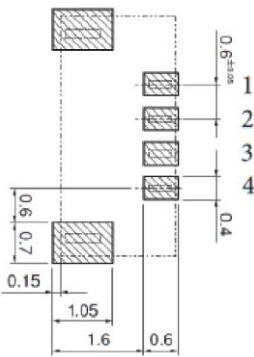
2.1 classicSUSI Interface

40 A 4-pin connector system from JST. The recommended pin header on the master is JST SM04-SRSS-TB (horizontal) or JST BM04B-SRSS-TB (vertical). The matching cable connectors are JST 04SR3S or JST SRH-04V-SB.



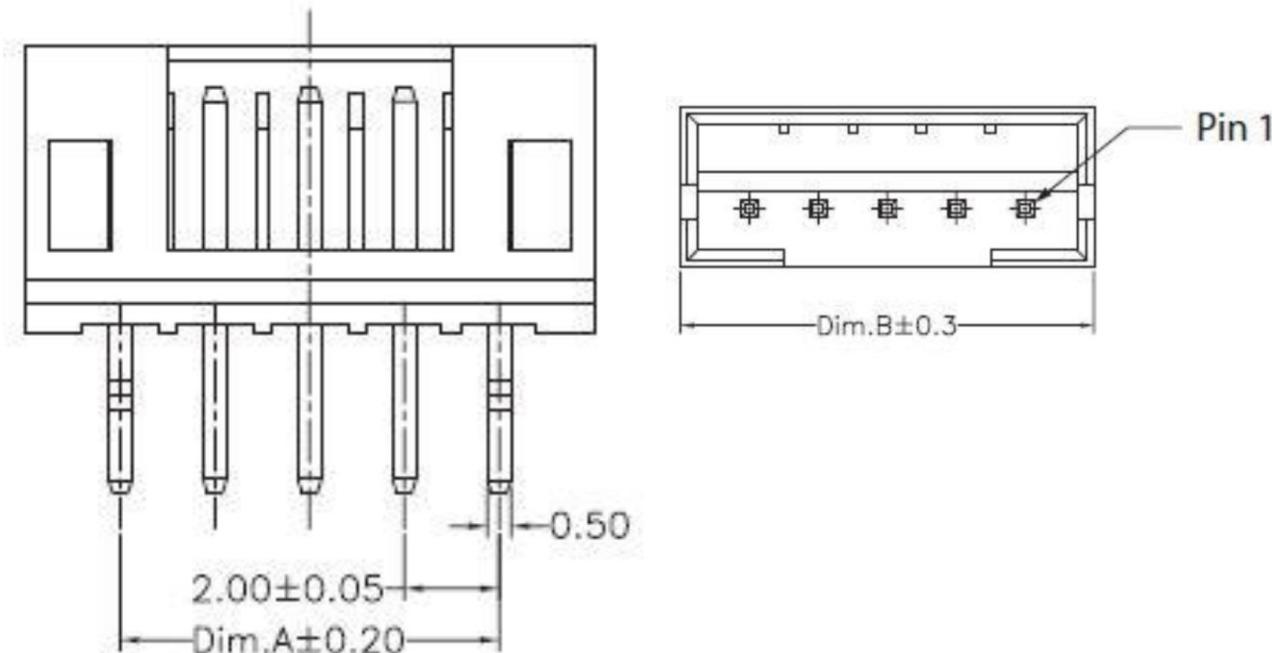
2.2 microSUSI Interface

- 45 A 4-pin connector system from JST. The recommended pin header on the master is JST SM04BXSRS-ETB. The matching cable connector is JST 04XSR-36S.



2.3 powerSUSI Interface

- 50 A 5-pin connector system from Würth Electronik (WR-WTB) with a 2.0mm pitch is used. The recommended pin header on the master is 62000511622 (through hole vertical), 62000511722 (through hole horizontal), 620305124022 (surface mount vertical), 620105131822 (surface mount horizontal). The matching cable connector is 620005113322.



3 Electrical Properties

3.1 classicSUSI Interface

The maximum load capacity is 1000mA.

Pin	Description
1	Ground (decoder negative side of rectifier)
2	Data
3	Clock
4	Plus (decoder positive side of rectifier)

65 3.2 microSUSI Interface

The maximum load capacity is 200mA.

Pin	Description
1	Ground (decoder negative side of rectifier)

2	Data
3	Clock
4	Plus (decoder positive side of rectifier)

3.3 powerSUSI Interface

The maximum load capacity is 2000mA.

Pin	Description
1	Trigger (open collector/drain signal or contact to ground for synchronization)
2	Ground (decoder negative side of rectifier)
3	Data
4	Clock
5	Plus (decoder positive side of rectifier)

- 70 The powerSUSI interface, with its higher load capacity, is also suitable for steam generators and the additional trigger signal enables wheel-synchronized steam burst without constantly sending trigger commands. The trigger is active on the falling edge. The pull-up resistor for the open collector/drain trigger signal is located on the SUSI module (slave), and is connected to VCC of the SUSI module (slave). It should be a value between 4.7kΩ and 22kΩ.

3.4 Decoder Interface

When using a standard decoder interface to connect a SUSI slave, the specifications in S-9.1.1.3, S-9.1.1.4, and S-9.1.1.5 shall be observed.

Signal	S-9.1.1.3 (21MTC)	S-9.1.1.4 (PluX22)	S-9.1.1.5 (Next18/Next18S)
Ground	20	5	5 and 14
Data	6	4	13
Clock	5	3	4
Plus	16	9	6 and 15

3.5 Common Properties

Recommended cable colors for the 4-pin interfaces. These are recommendations and are not evaluated for conformance.

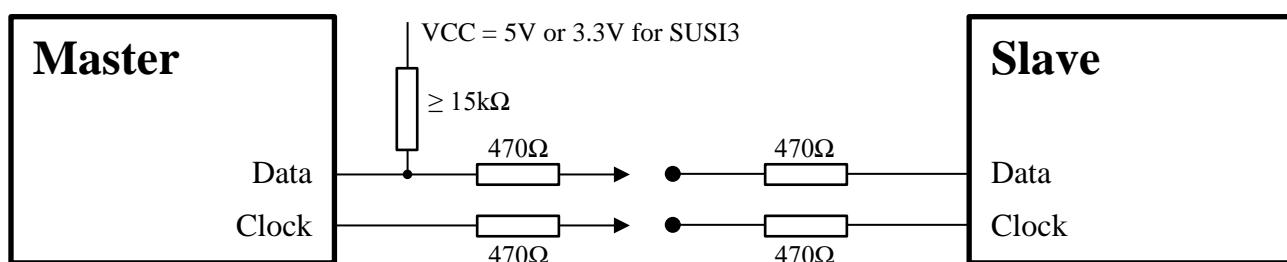
Pin	Description	Color
1	Ground	Black
2	Data	Grey
3	Clock	Blue
4	Plus	Red

Up to 3 slave modules can be connected to a master. The slave modules are connected in parallel. Appropriate adapter cables or distribution modules are required.

If the load capacity of the master may be lower than the maximum specified. If the load capacity of the master is lower, it shall be specified in the product documentation. The maximum current consumption that flows through the bus connection shall be specified for each slave module. If more current is required in a slave module, it shall be separately supplied with power. When connecting several slaves to the master, the master's total load capacity must not be exceeded.

A reverse polarity protection diode should be installed in series on the positive connection of the slave to prevent a defect in the event of reverse polarity. The diode may be omitted if one of the standard decoder interfaces described in Section 3.4 above.

A logic level high shall not fall below the value of $0.7 \times VCC$. Both lines contain a series resistance of 470Ω on the master and the slave. The data line has a pull-up resistance of $\geq 15k\Omega$ to VCC on the master.



3.6 Logic Level of the Interface

Levels corresponding to $VCC = 5V$ and $VCC = 3.3V$ are permitted. The following rules apply:

- The supported levels shall be specified in the product documentation.
- Each slave shall tolerate 5V levels.
- A slave for microSUSI shall also accept 3.3V levels.
- A slave that also accepts 3.3V levels **may** be marked with "SUSI3".
- A master that only supplies 3.3V levels **shall** be marked with "SUSI3".
 - Only masters with microSUSI socket are excluded from this requirement.

For the user, this means that only slaves with "SUSI3" marking can be safely operated on a master with SUSI3 marking. If masters and slaves are used with a microSUSI socket and plug,

compatibility is ensured. If a master with $VCC=3.3V$ is still required to deliver 5V levels, a level adjustment circuit is required. A suggestion can be found in Appendix ...

4 Protocol

The data transmission is synchronous unidirectional. All packets are two or three 8-bit bytes. The clock is low in the inactive state. Data is sent on the rising edge and shall be valid on the falling edge. The data shall be read on the falling edge.

Future extensions shall only be two byte packets. The exception mentioned are the commands that begin with the command code 0111XXXX. These are programming commands for CV manipulation with 3 bytes that are taken directly 1:1 from the DCC protocol.

The high or low period of the clock pulse shall be $\geq 10\mu s$, the total period for one bit may not exceed $500\mu s$. When reading a CV bank using SUSI BiDi commands, the total period for one bit may not exceed $100\mu s$. The master always supplies the clock pulse for data transmission. The first bit transmitted is the LSB (bit 0).

Since a single interference pulse on the clock line leads to a permanent data shift during synchronous transmission, a special timing is used for synchronization. $8ms \pm 1ms$ after a complete byte has arrived, all bits that have arrived so far are deleted and the slave is reset. This applies both internal and external of a command sequence.

125 Individual bytes of a command shall follow one another within 7ms. Further commands can be sent seamlessly, ie without a time gap, provided they follow the previous last command byte faster than 7ms. Otherwise the next command shall not begin until 9ms after the last byte sent.

For synchronization, the master shall insert a clock gap of at least 9ms after no more than 20 commands. When the reading a CV bank using SUSI BiDi commands, up to 50 commands can be transmitted without a break.

130 Commands that expect a response shall be confirmed by the slave with an acknowledge (ACK), if the response is positive, by pulling the data line to ground via the 470Ω series resistor. The acknowledge shall be $\geq 1ms$ and $\leq 2ms$, and shall be completed no later than 20ms after the falling clock edge of the last bit. After 20ms, without a complete acknowledge, the master can abort the command with a negative response. A master shall accept acknowledge pulses of $\geq 0.5ms$ and $\leq 7ms$ as valid. Shorter pulses should be considered invalid to suppress interference.

When accessing CVs 897 to 899 and 1020 to 1024, several slaves can respond with an acknowledge. In this case, the master shall always wait the full 20ms and shall not send the next byte immediately after a successful received acknowledge.

140 Error detection and/or correction is not provided because the cables are generally very short. It is recommended that they be no longer than 20cm between master and slave modules.

If slave modules do not receive valid commands within 100ms after reset, they may automatically start in an alternative mode without SUSI command control.

5 Commands

145 The data bytes are basically derived from DCC commands of S-9.2.1. This allows for very simple forwarding of DCC commands to the slave modules. A more detailed description of the individual command bits can be found in S-9.2.1. Commands are sent to the slaves when required, e.g. when data is currently being received in the master. Every active function or driver command should be repeated at least every 200ms, even without new data being received, in order to enable safe operation even in the event of faults. If the master has no external data reception, it can also independently generate commands based on specific operating states (e.g. in analog mode).

Command		Data Byte(s)	Notes
Function Group 1	0x60	000F0F4F3F2F1	F0 is always sent in FG1.
Function Group 2	0x61	F ₁₂ F ₁₁ F ₁₀ F ₉ F ₈ F ₇ F ₆ F ₅	F5 – F8 and F9 – F12 are combined into one command
Function Group 3	0x62	F ₂₀ F ₁₉ F ₁₈ F ₁₇ F ₁₆ F ₁₅ F ₁₄ F ₁₃	
Function Group 4	0x63	F ₂₈ F ₂₇ F ₂₆ F ₂₅ F ₂₄ F ₂₃ F ₂₂ F ₂₁	
Function Group 5	0x64	F ₃₆ F ₃₅ F ₃₄ F ₃₃ F ₃₂ F ₃₁ F ₃₀ F ₂₉	
Function Group 6	0x65	F ₄₄ F ₄₃ F ₄₂ F ₄₁ F ₄₀ F ₃₉ F ₃₈ F ₃₇	
Function Group 7	0x66	F ₅₂ F ₅₁ F ₅₀ F ₄₉ F ₄₈ F ₄₇ F ₄₆ F ₄₅	
Function Group 8	0x67	F ₆₀ F ₅₉ F ₅₈ F ₅₇ F ₅₆ F ₅₅ F ₅₄ F ₅₃	
Function Group 9	0x68	F ₆₈ F ₆₇ F ₆₆ F ₆₅ F ₆₄ F ₆₃ F ₆₂ F ₆₁	
Binary State Short Form	0x6D	DL ₆ L ₅ L ₄ L ₂ L ₁ L ₀	D = 0: function L switched off D = 1: function L switched on L = 1 – 127: Function number L: = 0: broadcast, all functions 1 to 127 off (D = 0) or on (D = 1)
Binary State Long Form Low Byte	0x6E	DL ₆ L ₅ L ₄ L ₂ L ₁ L ₀	Commands are always sent as a pair of binary state long form low and high byte. The low byte command shall be sent first If the two commands do not follow one another directly, they shall be ignored.
Binary State Long Form High Byte	0x6F	DH ₆ H ₅ H ₄ H ₂ H ₁ H ₀	D = 0: binary state L switched off D = 1: binary state L switched on L: low order bits of binary state 1 to 32,767 H: high order bits of binary state 1 to 32,767 H & L = 0: broadcast, all binary states 1 to 32,767 off (D = 0) or on (D = 1)
Direct Command 1	0x40	X ₈ X ₇ X ₆ X ₅ X ₄ X ₃ X ₂ X ₁	
Direct Command 2	0x41	X ₁₆ X ₁₅ X ₁₄ X ₁₃ X ₁₂ X ₁₁ X ₁₀ X ₉	

Command		Data Byte(s)	Notes
Direct Command 3	0x42	X ₂₄ X ₂₃ X ₂₂ X ₂₁ X ₂₀ X ₁₉ X ₁₈ X ₁₇	Direct commands are used to directly control outputs and other functions after applying the function table in the master. A bit= 1 means the corresponding output is switched on.
Direct Command 4	0x43	X ₃₂ X ₃₁ X ₃₀ X ₂₉ X ₂₈ X ₂₇ X ₂₆ X ₂₅	
Trigger Pulse	0x21	00000001	Command used to synchronize a steam burst. It is sent once per steam burst. Bits 1 to 7 are reserved for future use (sent as 0 by master, ignored by slave).
Current	0x23	S ₇ S ₆ S ₅ S ₄ S ₂ S ₁ S ₀	Current consumed by the motor. The valid range is -128 to 127 in 2's complement format calibrated to a manufacturer specific CV in the master. Negative values mean feedback, as is possible with modern electric locomotives.
“Actual” Velocity	0x24	RG ₆ G ₅ G ₄ G ₂ G ₁ G ₀	The speed and direction corresponding to the actual or target motor condition. G is to be normalized to the Vmax scale set in the master.
“Target” Velocity	0x25	RG ₆ G ₅ G ₄ G ₂ G ₁ G ₀	<p>G = 0: locomotive is not moving</p> <p>G = 1 – 127: normalized speed</p> <p>R = 0: reverse direction</p> <p>R = 1: forward direction</p> <p>These commands are not recommended for new designs. Slaves should instead evaluate commands 0x50 to 0x52. Masters that use different implementations of commands 0x24 and 0x25 for reasons of compatibility with existing products are still compliant to the standard.</p>
Load Balancing	0x26	P ₇ P ₆ P ₅ P ₄ P ₂ P ₁ P ₀	<p>The load state can be detected via motor voltage (Back-EMF), current, or power.</p> <p>0: no load</p> <p>127: maximum load</p> <p>Negative values are also possible and transmitted in 2's complement. Negative values mean less load than operating on flat terrain. G is to be normalized to the Vmax scale set in the master.</p>

Command		Data Byte(s)	Notes
“Actual” Velocity	0x50	RG ₆ G ₅ G ₄ G ₂ G ₁ G ₀	<p>The speed and direction corresponding to the actual motor condition. This is a control value in relation to “target” speed, i.e. after adjusting the speed ramp, the actual and target should be the same (regulated state).</p> <p>G = 0: locomotive is not moving</p> <p>G = 1 – 127: normalized speed</p> <p>R = 0: reverse direction</p> <p>R = 1: forward direction</p>
“Target” Velocity	0x51	RG ₆ G ₅ G ₄ G ₂ G ₁ G ₀	<p>The internal speed of the “master” normalized to 127 levels based on received speed converted via the characteristic curve (CVs 67 to 94, CV2, 6, and 5; and other CVs that determine the speed of the locomotive). This means that the highest value that can be achieved using CVs 94 and/or CV5 or other corresponding CVs is normalized to 127. CV’s for acceleration and braking, such as CVs 3, 4, 23, and 24, are not included in the calculation.</p> <p>G = 0: locomotive is not moving</p> <p>G = 1 – 127: normalized speed</p> <p>R = 0: reverse direction</p> <p>R = 1: forward direction</p> <p>Since different decoders use different methods to determine the maximum speed, there may be slightly different implementations. It is most important that the commands for actual and target speed behave the same.</p>
“DCC” Velocity	0x52	RG ₆ G ₅ G ₄ G ₂ G ₁ G ₀	This value is directly as received by the master from the system. No adjustment is made by any CVs. 14 and 28 speed step commands from the system are normalized to 128 speed step values 0 – 127.
Analog Function Group	0x28 – 0x2F	A ₇ A ₆ A ₅ A ₄ A ₂ A ₁ A ₀	The eight commands in this group allow the transmission of eight different analog values.

Command		Data Byte(s)	Notes
Direct Command 1 for Analog	0x30	D ₇ D ₆ D ₅ D ₄ D ₂ D ₁ D ₀	<p>Set basic functions in analog mode without using a function assignment.</p> <p>Bit 0: sound on/off</p> <p>Bit 1: upgrade/dismantling</p> <p>Bits 2 – 6: reserved</p> <p>Bit 7: reduced volume</p>
Direct Command 2 for Analog			<p>Set basic functions in analog mode without using a function assignment.</p> <p>Bit 0: peak signal</p> <p>Bit 1: end signal</p> <p>Bit 2: parking light</p> <p>Bits 3 – 7: reserved</p>

6 Document History

Date	Description
9-Jun-2024	First Revision

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