Index Number – 210098R

Name – De Silva A.P.C.

Assigned Task –

Understanding the concepts and then designing & developing a 2 to 4 decoder.

Then Designing and developing a 3 to 8 decoder using 2 to 4 decoders.

After that, designing and developing 8 to 1 multiplexer using a 3 to 8 decoder after properly identifying the relevant logic circuit.

(Verification of the specific functionalities through simulations is included in each one of them.)

VHDL codes –

Decoder_2_to_4.vhd

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 03/21/2023 09:43:25 PM
-- Design Name:
-- Module Name: Decoder_2_to_4 - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
```

```
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Decoder_2_to_4 is
   Port ( I : in STD_LOGIC_VECTOR (1 downto 0);
          EN : in STD_LOGIC;
          Y : out STD_LOGIC_VECTOR (3 downto 0));
end Decoder_2_to_4;

architecture Behavioral of Decoder_2_to_4 is

begin
Y(0)<= not I(0)and not I(1)and EN;
Y(1)<= not I(1)and I(0)and EN;
Y(2)<= I(1)and not I(0)and EN;
Y(3)<= I(0)and I(1)and EN;

end Behavioral;
```

TB_Decoder_2_to_4.vhd

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 03/22/2023 12:10:51 AM
```

```
-- Design Name:
-- Module Name: TB_Decoder_2_to_4 - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity TB_Decoder_2_to_4 is
--  Port ( );
end TB_Decoder_2_to_4;

architecture Behavioral of TB_Decoder_2_to_4 is
COMPONENT Decoder_2_to_4
        PORT( I : in STD_LOGIC_VECTOR (1 downto 0);
              EN : in STD_LOGIC;
              Y : out STD_LOGIC_VECTOR (3 downto 0));
END COMPONENT;
 signal I0,I1 : STD_LOGIC ;
signal Y0,Y1,Y2,Y3 : STD_LOGIC ;
signal EN :  STD_LOGIC;
begin
UUT: Decoder_2_to_4 PORT MAP(
I(0) => I0,
```

```
I(1) => I1,
Y(0) => Y0,
Y(1) => Y1,
Y(2) => Y2,
Y(3) => Y3,
EN => EN);

process
begin
   EN <='0';
   I0 <= '0';
   I1 <= '0';

   WAIT FOR 100 ns;
   I0 <= '1';

   WAIT FOR 100 ns;
   I0 <= '0';
   I1 <= '1';

   WAIT FOR 100 ns;
   I0 <= '1';

   WAIT FOR 100 ns;
   I0 <= '0';
   I1 <= '0';
   EN <= '1';

   WAIT FOR 100 ns;
   I0 <= '1';

   WAIT FOR 100 ns;
   I0 <= '0';
   I1 <= '1';

   WAIT FOR 100 ns;
   I0 <= '1';
   WAIT;
end process;
end Behavioral;
```

Decoder_3_to_8.vhd

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 03/22/2023 02:58:34 AM
-- Design Name:
-- Module Name: Decoder_3_to_8 - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Decoder_3_to_8 is
    Port ( I : in STD_LOGIC_VECTOR (2 downto 0);
           EN : in STD_LOGIC;
           Y : out STD_LOGIC_VECTOR (7 downto 0));
end Decoder_3_to_8;

architecture Behavioral of Decoder_3_to_8 is
component Decoder_2_to_4
```

```
port(
I: in STD_LOGIC_VECTOR;
EN: in STD_LOGIC;
Y: out STD_LOGIC_VECTOR );
end component;
signal I0,I1 : STD_LOGIC_VECTOR (1 downto 0);
signal Y0,Y1 : STD_LOGIC_VECTOR (3 downto 0);
signal en0,en1, I2 : STD_LOGIC;
begin
Decode_2_to_4_0 : Decoder_2_to_4
port map(
I => I0,
EN => en0,
Y => Y0 );
Decode_2_to_4_1 : Decoder_2_to_4
port map(
I => I1,
EN => en1,
Y => Y1 );
en0 <= NOT(I(2)) AND EN;
en1 <= I(2) AND EN;
I0 <= I(1 downto 0);
I1 <= I(1 downto 0);
I2 <= I(2);
Y(3 downto 0) <= Y0;
Y(7 downto 4) <= Y1;
end Behavioral;
```

TB_Decoder_3_to_8.vhd

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 03/22/2023 03:00:12 AM
-- Design Name:
-- Module Name: TB_Decoder_3_to_8 - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
```

```
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity TB_Decoder_3_to_8 is
--  Port ( );
end TB_Decoder_3_to_8;

architecture Behavioral of TB_Decoder_3_to_8 is
COMPONENT Decoder_3_to_8
        PORT( I : in STD_LOGIC_VECTOR (2 downto 0);
              EN : in STD_LOGIC;
              Y : out STD_LOGIC_VECTOR (7 downto 0));
END COMPONENT;
 signal I0,I1,I2 : STD_LOGIC ;
signal Y0,Y1,Y2,Y3,Y4,Y5,Y6,Y7 : STD_LOGIC ;
signal EN :  STD_LOGIC;
begin
UUT: Decoder_3_to_8 PORT MAP(
I(0) => I0,
I(1) => I1,
I(2) => I2,
Y(0) => Y0,
Y(1) => Y1,
Y(2) => Y2,
Y(3) => Y3,
Y(4) => Y4,
```

```
Y(5) => Y5,
Y(6) => Y6,
Y(7) => Y7,
EN => EN);

process
begin
   EN <='0';
   I0 <= '0';
   I1 <= '1';
   I2 <= '0';
   WAIT FOR 100 ns;
      I2 <= '1';

   WAIT FOR 100 ns;
      I0 <= '1';
      I2 <= '0';
   WAIT FOR 100 ns;
      EN <='1';
      I0 <= '0';
      I2 <= '0';
   WAIT FOR 100 ns;
       I2 <= '1';

   WAIT FOR 100 ns;
      I0 <= '1';
      I2 <= '0';


      WAIT FOR 100 ns;
            I0 <= '1';
            I1 <= '0';
            I2 <= '1';

   WAIT;
end process;
end Behavioral;
```

Mux_8_to_1.vhd

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 03/22/2023 01:32:17 PM
-- Design Name:
-- Module Name: Mux_8_to_1 - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Mux_8_to_1 is
   Port ( S : in STD_LOGIC_VECTOR (2 downto 0);
          D : in STD_LOGIC_VECTOR (7 downto 0);
          EN : in STD_LOGIC;
          Y : out STD_LOGIC);
end Mux_8_to_1;

architecture Behavioral of Mux_8_to_1 is
```

```
component Decoder_3_to_8
port(
I: in STD_LOGIC_VECTOR;
EN: in STD_LOGIC;
Y: out STD_LOGIC_VECTOR );
end component;
signal Decoder_in : STD_LOGIC_VECTOR(7 downto 0);
begin
Decode_3_to_8_0 : Decoder_3_to_8
port map(
   I => S,
   EN =>EN,
   Y=> Decoder_in
);
Y <= (D(0) and Decoder_in(0)) or
    (D(1) and Decoder_in(1)) or
    (D(2) and Decoder_in(2)) or
    (D(3) and Decoder_in(3)) or
    (D(4) and Decoder_in(4)) or
    (D(5) and Decoder_in(5)) or
    (D(6) and Decoder_in(6)) or
    (D(7) and Decoder_in(7));

end Behavioral;
```

TB_Mux_8_to_1.vhd

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 03/22/2023 02:21:05 PM
-- Design Name:
-- Module Name: TB_Mux_8_to_1 - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
```

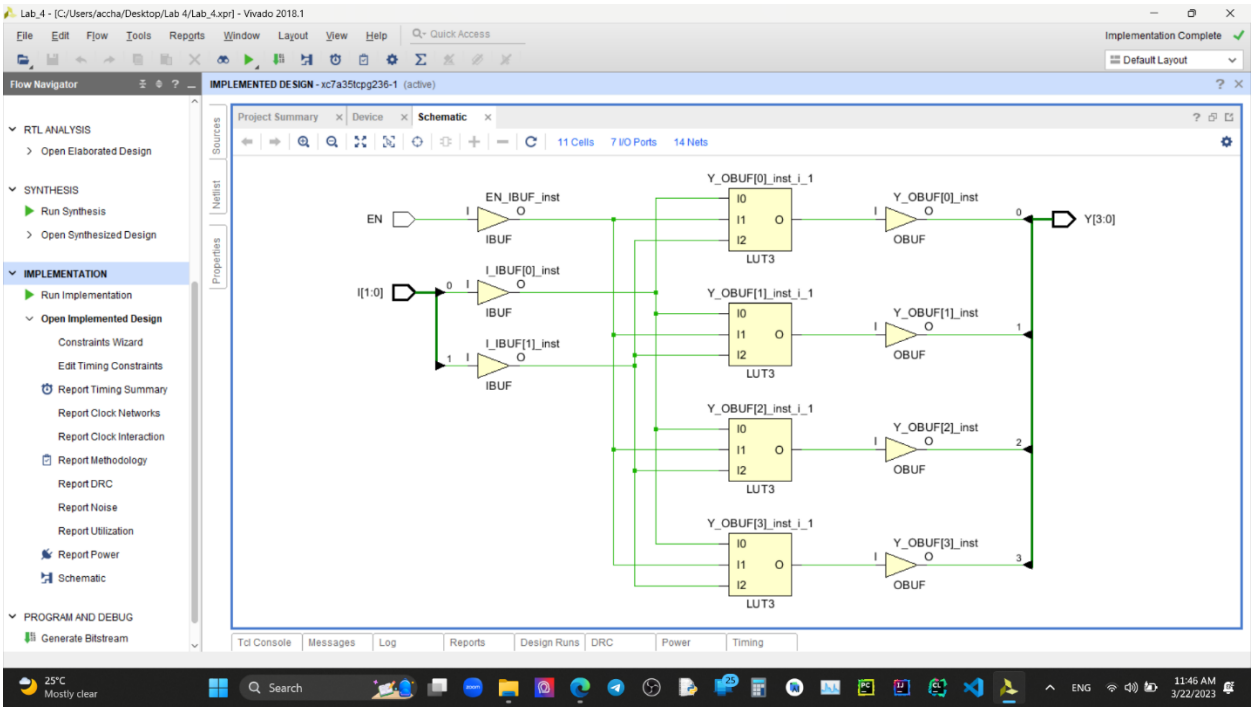
```
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity TB_Mux_8_to_1 is
--  Port ( );
end TB_Mux_8_to_1;

architecture Behavioral of TB_Mux_8_to_1 is
COMPONENT Mux_8_to_1
        PORT( S : in STD_LOGIC_VECTOR (2 downto 0);
              D : in STD_LOGIC_VECTOR (7 downto 0);
              EN : in STD_LOGIC;
              Y : out STD_LOGIC);
END COMPONENT;

signal S0,S1,S2 : STD_LOGIC ;
signal D0,D1,D2,D3,D4,D5,D6,D7 : STD_LOGIC ;
signal EN,Y :  STD_LOGIC;
begin

UUT: Mux_8_to_1 PORT MAP(
S(0) => S0,
S(1) => S1,
S(2) => S2,
D(0) => D0,
D(1) => D1,
D(2) => D2,
D(3) => D3,
```

```
D(4) => D4,
D(5) => D5,
D(6) => D6,
D(7) => D7,
Y=>Y,
EN => EN);

process
begin
   EN <='0';
   S0 <= '0';
   S1 <= '1';
   S2 <= '0';
   D0 <= '0';
   D1 <= '1';
   D2 <= '0';
   D3 <= '0';
   D4 <= '1';
   D5 <= '1';
   D6 <= '1';
   D7 <= '1';

   WAIT FOR 100 ns;
      S2 <= '1';

   WAIT FOR 100 ns;
      S0 <= '1';
      S2 <= '0';

   WAIT FOR 100 ns;
      EN <='1';
      S0 <= '0';

   WAIT FOR 100 ns;
      S2 <= '1';

   WAIT FOR 100 ns;
      S0 <= '1';
      S2 <= '0';

   WAIT FOR 100 ns;
     S0 <= '0';
     D2 <= '1';
     D3 <= '1';
```

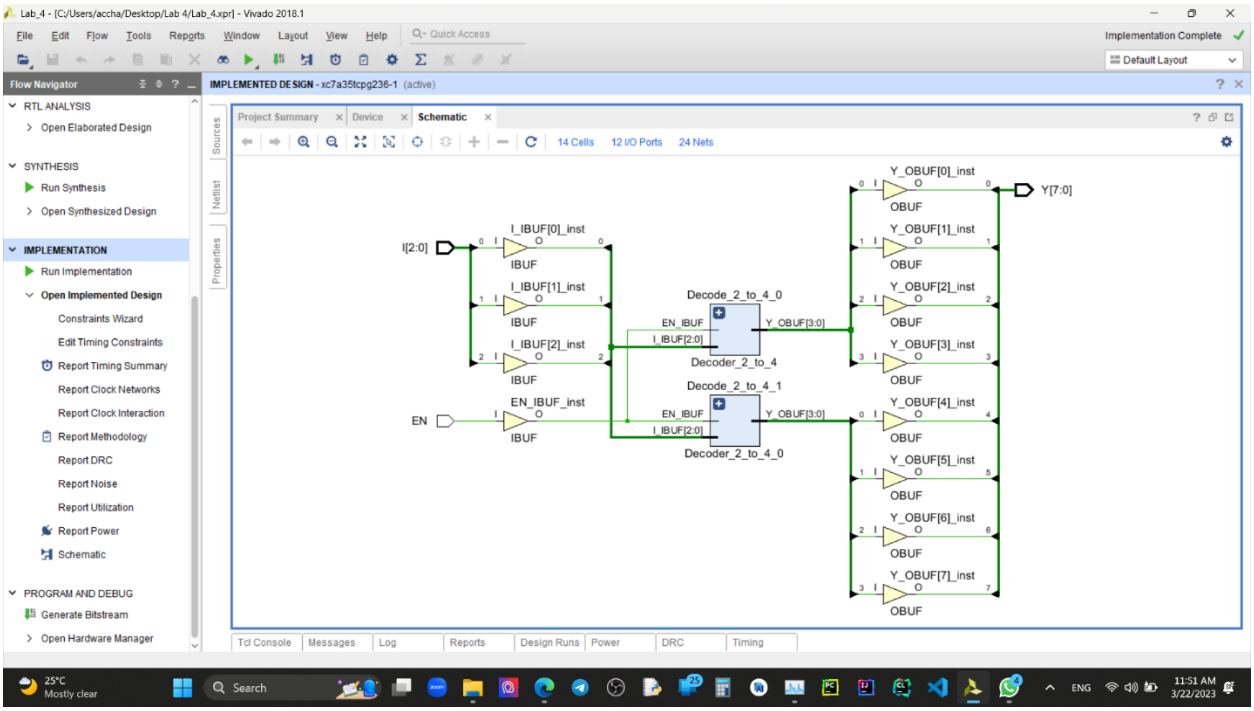
```
    D6 <= '0';
    D7 <= '0';

  WAIT FOR 100 ns;
    S2 <= '1';

  WAIT FOR 100 ns;
    S0 <= '1';
    S2 <= '0';
  WAIT;
end process;
end Behavioral;
```

Design Schematics –

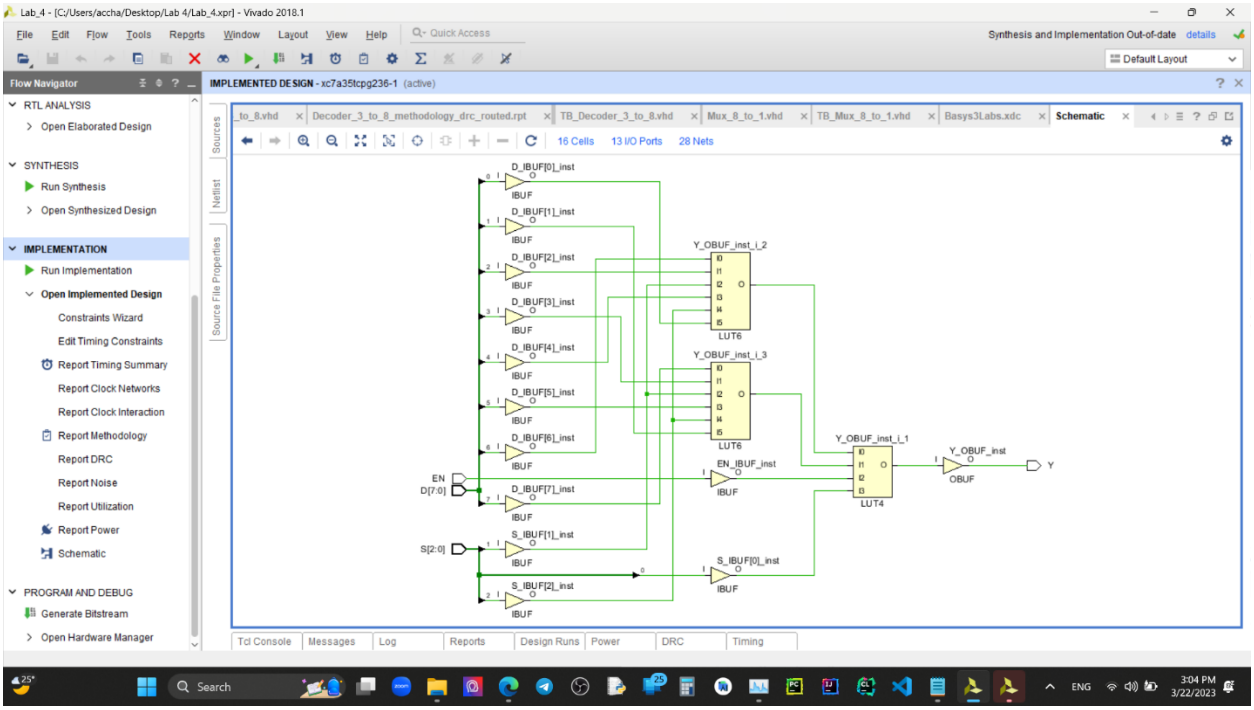
2 to 4 Decoder –



3 to 8 Decoder –

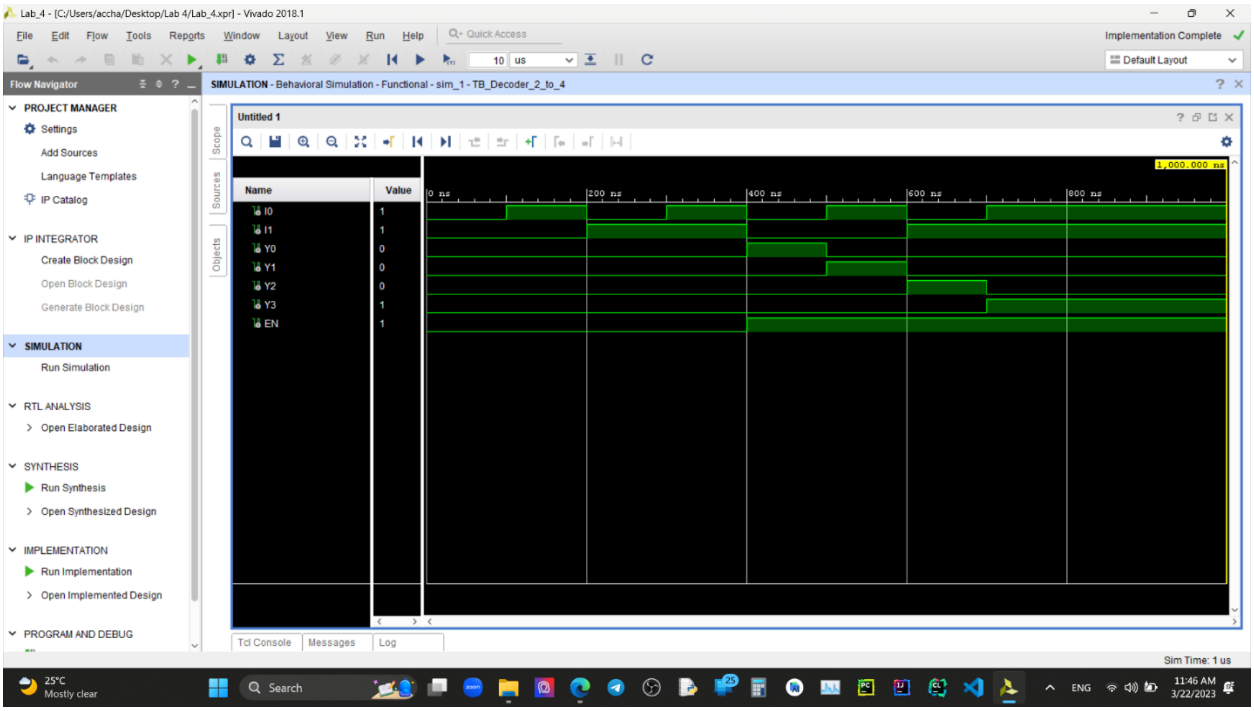


8 to 1 Multiplexer –

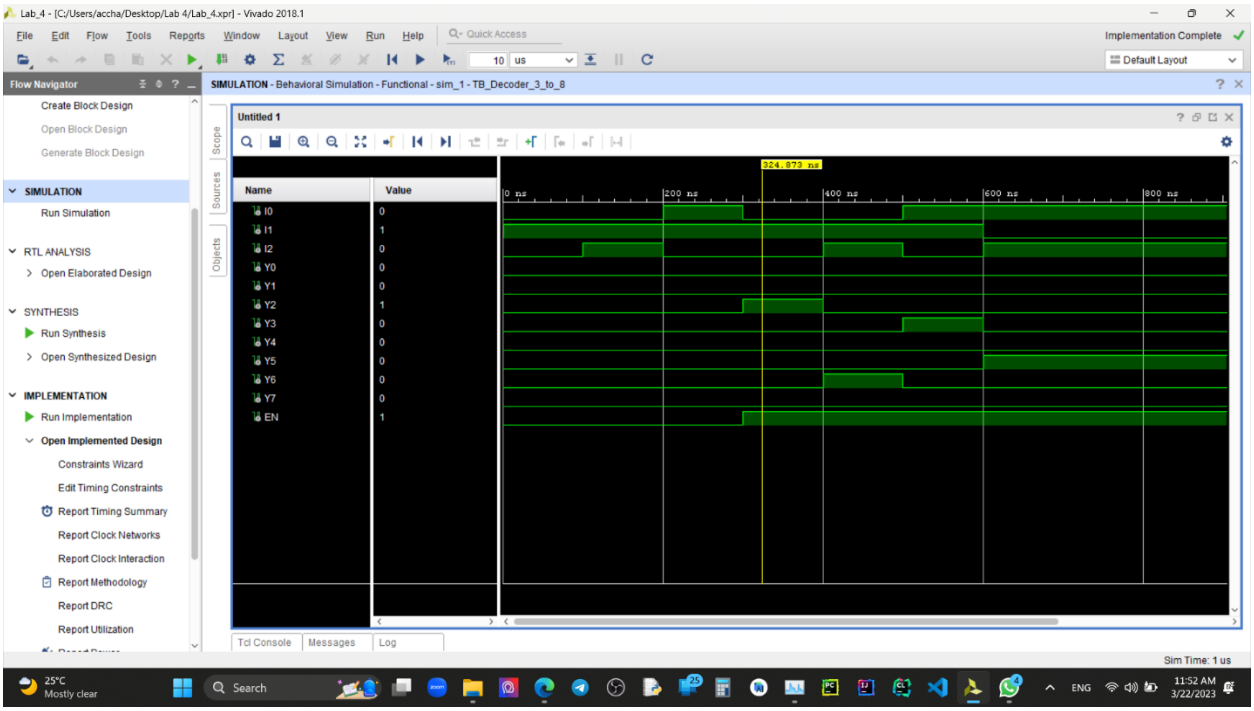


Timing diagrams –

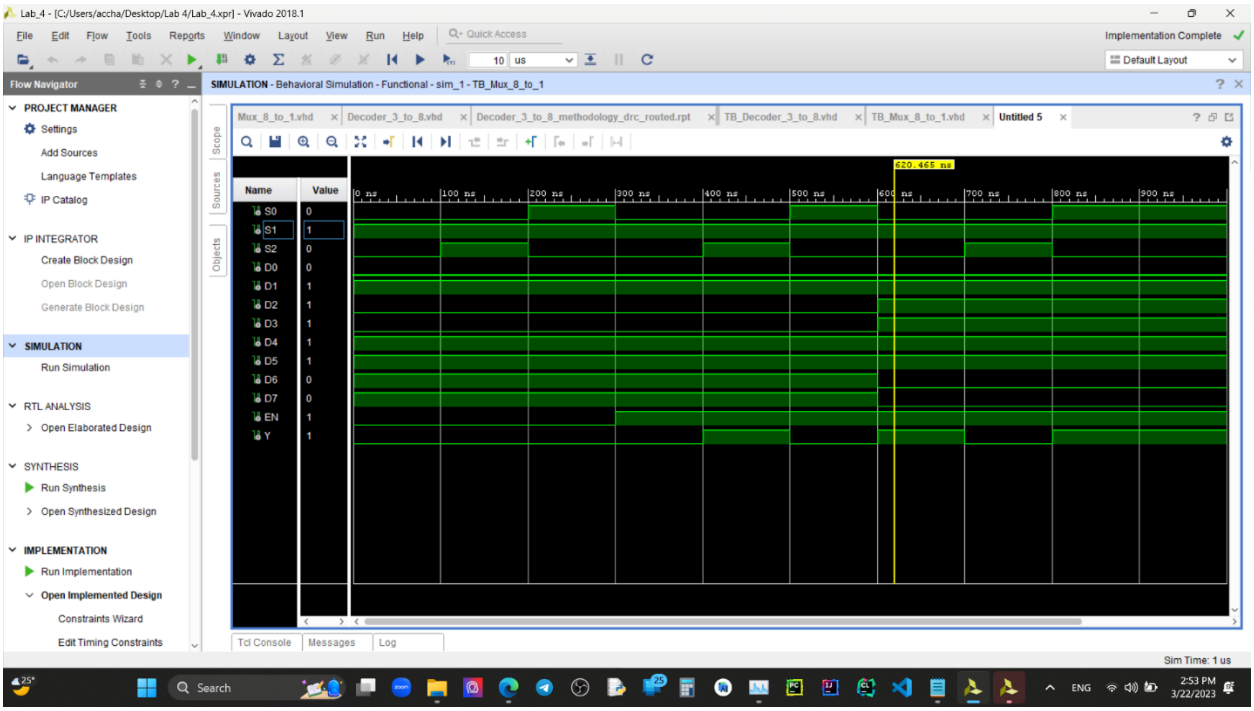
2 to 4 Decoder –



3 to 8 Decoder –



8 to 1 Multiplexer –



(First En was set to 0 for first 300 ns to check its functionality. Then It was set to 1. In first 600ns, D7 to D0 has values 1 1 1 1 0 0 1 0 respectively and then for the sake of accuracy more tests were done by setting D7 to D0 to values 0 0 1 1 1 1 1 0 . The values of S0-S2 is in the way instructed.)

Conclusion –

Designing a 2 to 4 decoder, then using that decoder to develop a 3 to 8 decoder, and then using the 3 to 8 decoder to design an 8 to 1 multiplexer is a great exercise in comprehending the hierarchical design process in digital logic.

We can create specific components of the circuit that can be reused in larger designs by dividing a complex problem into smaller, more manageable subproblems. This strategy makes it simpler and easier to test and debug the designs while also reducing the complexity of the overall design.