Name – De Silva APC

Index – 210098R

Group – In21 CSE

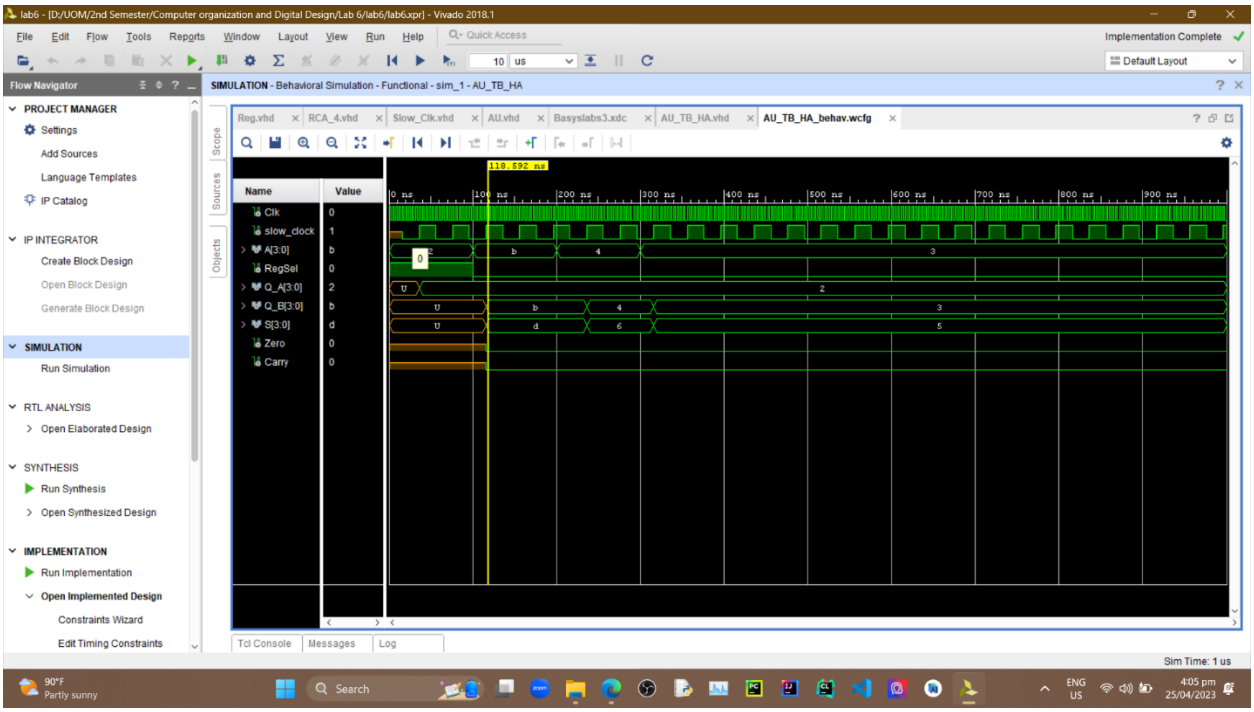
Assigned Lab Task –

Main task was to design and develop an (4-bit) Arithmetic unit and then testing it via simulation. The arithmetic unit is deigned to be capable of adding to numbers stored in two registers. This task had the use of the components been designed and developed in previous lab sessions after importing them.

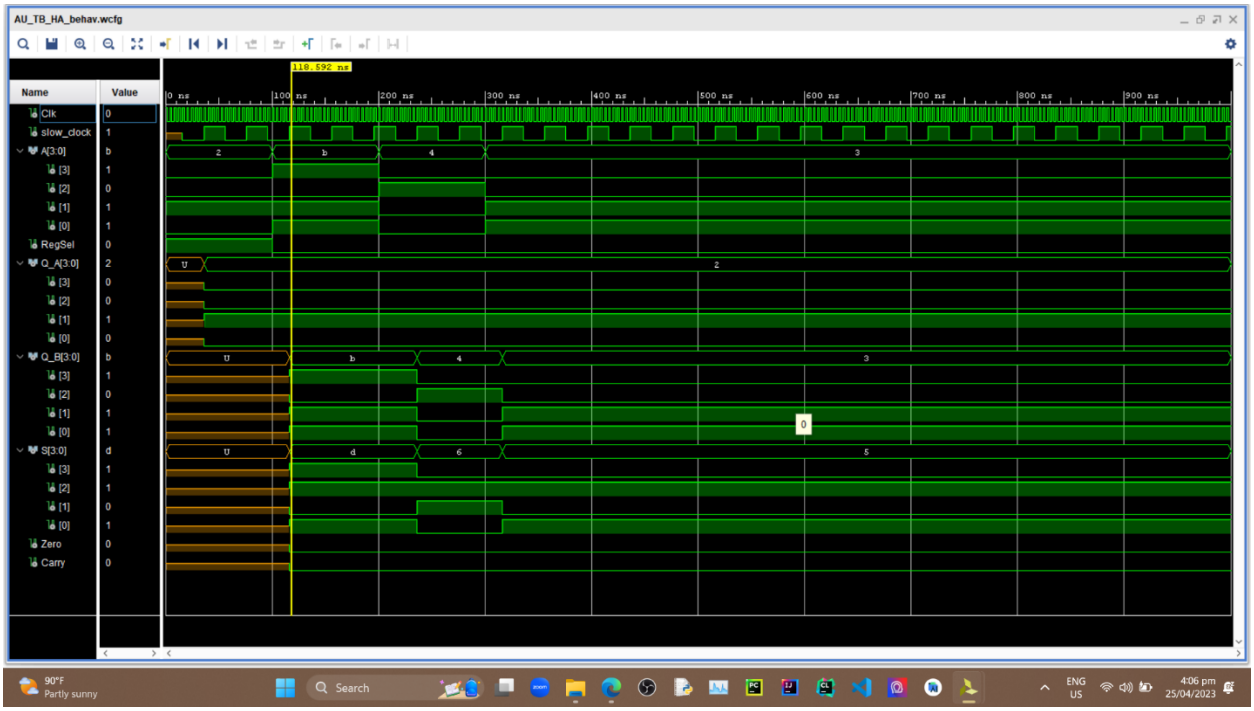
Conclusions –

A basic functionality of an Arithmetic logic unit which supports 4 bits. Use of components that already been developed and designed in a larger scale project as modules.

Screenshots of the simulation(Extended and Archieved) –



(Extended) -



All VHDL Codes –

AU_TB_HA.vhd

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 04/25/2023 03:17:04 PM
-- Design Name:
-- Module Name: AU_TB_HA - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
```

```
-- Additional Comments:
--
----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity AU_TB_HA is
--  Port ( );
end AU_TB_HA;

architecture Behavioral of AU_TB_HA is
component AU
    Port ( A : in STD_LOGIC_VECTOR (3 downto 0);
        RegSel : in STD_LOGIC;
        Clk : in STD_LOGIC;
        S : out STD_LOGIC_VECTOR (3 downto 0);
        Zero : out STD_LOGIC;
        Carry : out STD_LOGIC);
end component;
signal A,S : STD_LOGIC_VECTOR (3 downto 0) :="0000" ;
signal RegSel,Clk,Zero,Carry : STD_LOGIC := '0';
begin
UUT : AU
   PORT MAP(
      A => A,
      S =>S,
      Regsel => Regsel,
      Clk => Clk,
      Zero => Zero,
      Carry =>Carry
   );
process
begin
   Clk <= not(Clk);
   wait for 2ns;
end process;

process
```

```
begin
   A<= "0010";
   RegSel <= '1';
   wait for 100ns;

   RegSel <= '0';
   A<= "1011";
   wait for 100ns;
   A <= "0100";
   wait for 100ns;
   A <= "0011";
   wait;



end process;
end Behavioral;
```

AU.vhd

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 04/25/2023 02:16:58 PM
-- Design Name:
-- Module Name: AU - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
```

```
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity AU is
   Port ( A : in STD_LOGIC_VECTOR (3 downto 0);
          RegSel : in STD_LOGIC;
          Clk : in STD_LOGIC;
          S : out STD_LOGIC_VECTOR (3 downto 0);
          Zero : out STD_LOGIC;
          Carry : out STD_LOGIC);
end AU;

architecture Behavioral of AU is
component Slow_Clk
Port ( Clk_in : in STD_LOGIC;
          Clk_out : out STD_LOGIC);
end component;

component RCA_4
Port ( A0 : in STD_LOGIC;
          A1 : in STD_LOGIC;
          A2 : in STD_LOGIC;
          A3 : in STD_LOGIC;
          B0 : in STD_LOGIC;
          B1 : in STD_LOGIC;
          B2 : in STD_LOGIC;
          B3 : in STD_LOGIC;
          C_in : in STD_LOGIC;
          S0 : out STD_LOGIC;
          S1 : out STD_LOGIC;
          S2 : out STD_LOGIC;
          S3 : out STD_LOGIC;
          C_out : out STD_LOGIC);
end component;

component Reg
 Port ( D : in STD_LOGIC_VECTOR (3 downto 0);
          En : in STD_LOGIC;
          Clk : in STD_LOGIC;
          Q : out STD_LOGIC_VECTOR (3 downto 0));
  end component;
signal slow_clock : STD_LOGIC;
signal En_A,En_B,C_out : STD_LOGIC;
signal Q_A, Q_B,S_RCA : STD_LOGIC_VECTOR (3 downto 0);
begin
```

```
Slow_Clk_0 : Slow_Clk
   PORT MAP(
   Clk_in => Clk,
   Clk_out => slow_clock
   );


Reg_A : Reg
   PORT MAP(
   D=>A,
   En=>En_A,
   Clk=>slow_clock,
   Q =>Q_A
   );

Reg_B : Reg
   PORT MAP(
   D=>A,
   En=>En_B,
   Clk=>slow_clock,
   Q =>Q_B
   );

RCA_4_0 : RCA_4
   PORT MAP(
   A0=>Q_A(0),
   A1=>Q_A(1),
   A2=>Q_A(2),
   A3=>Q_A(3),
   B0=>Q_B(0),
   B1=>Q_B(1),
   B2=>Q_B(2),
   B3=>Q_B(3),
   C_in=>'0',
   S0=>S_RCA(0),
   S1=>S_RCA(1),
   S2=>S_RCA(2),
   S3=>S_RCA(3),
   C_out=>C_out
   );
   Carry <= C_out;
   S <= S_RCA;
   Zero <= not(S_RCA(0)) and not(S_RCA(1)) and not(S_RCA(2)) and not(S_RCA(3) and not(C_out));
   EN_A <= Regsel;
   En_B <= Not(Regsel);
end Behavioral;
```

Slow_Clk.vhd

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 04/08/2023 07:25:00 PM
-- Design Name:
-- Module Name: Slow_Clk - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Slow_Clk is
    Port ( Clk_in : in STD_LOGIC;
           Clk_out : out STD_LOGIC);
end Slow_Clk;

architecture Behavioral of Slow_Clk is

signal count : integer := 1;
signal clk_status : std_logic := '0';

begin
```

```
    process (Clk_in) begin
        if(rising_edge(Clk_in)) then
            count <= count+1;
            if(count = 5)then   -- Counting frequency scaler(Reduced to 5 to simulation purposes.IF not 5M.)
                clk_status <= not clk_status;
                Clk_out <= clk_status;
                count<=1;
            end if;
        end if;
    end process;

end Behavioral;
```

RCA_4.vhd

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 03/18/2023 11:27:04 AM
-- Design Name:
-- Module Name: RCA_4 - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;
```

```
entity RCA_4 is
   Port ( A0 : in STD_LOGIC;
          A1 : in STD_LOGIC;
          A2 : in STD_LOGIC;
          A3 : in STD_LOGIC;
          B0 : in STD_LOGIC;
          B1 : in STD_LOGIC;
          B2 : in STD_LOGIC;
          B3 : in STD_LOGIC;
          C_in : in STD_LOGIC;
          S0 : out STD_LOGIC;
          S1 : out STD_LOGIC;
          S2 : out STD_LOGIC;
          S3 : out STD_LOGIC;
          C_out : out STD_LOGIC);
end RCA_4;

architecture Behavioral of RCA_4 is
component FA
       port(
       A: in std_logic;
       B: in std_logic;
       C_in : in std_logic;
       S: out std_logic;
       C_out : out std_logic);
   end component;

   SIGNAL FA0_S, FA0_C , FA1_S,FA1_C, FA2_S, FA2_C, FA3_S, FA3_C
   : std_logic;
begin
   FA_0 : FA
      port map (
         A => A0,
         B => B0,
         C_in => '0',
         S=> S0,
         C_out => FA0_C);
    FA_1 : FA
      port map (
         A => A1,
         B => B1,
         C_in => FA0_C,
         S=> S1,
         C_out => FA1_C);
   FA_2 : FA
      port map (
         A => A2,
         B => B2,
         C_in => FA1_C,
```

```
        S=> S2,
        C_out => FA2_C);
    FA_3 : FA
      port map (
        A => A3,
        B => B3,
        C_in => FA2_C,
        S=> S3,
        C_out => C_out);
end Behavioral;
```

Reg.vhd

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 04/25/2023 02:01:44 PM
-- Design Name:
-- Module Name: Reg - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
```

```
--use UNISIM.VComponents.all;

entity Reg is
    Port ( D : in STD_LOGIC_VECTOR (3 downto 0);
           En : in STD_LOGIC;
           Clk : in STD_LOGIC;
           Q : out STD_LOGIC_VECTOR (3 downto 0));
end Reg;

architecture Behavioral of Reg is

begin
process (Clk) begin
 if (rising_edge(Clk)) then -- respond when clock rises
 if En = '1' then -- Enable should be set
 Q <= D;
 end if;
 end if;
end process;


end Behavioral;
```

THE END OF THE REPORT