Name – De Silva APC

Index – 210098R

Group – In21 CSE

Assigned Lab Task –

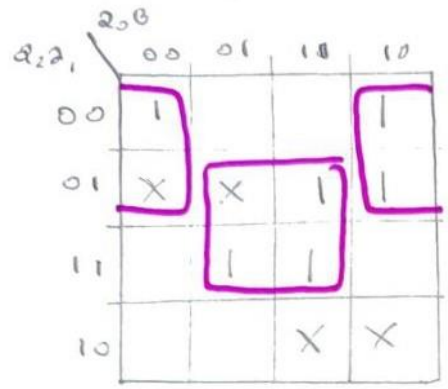
Using the provided code and info, firstly designing a D flipflop and testing it via simulation. Then implementing the “Slow Clock” to obtain a slower clock that we need using the provided 100MHz clock of Basys board and then testing it via simulation. Finally designing the 3bit Counter that counts in the direction specified via an input using both slow clock and the d flipflops.

Completed Truth Table -

Q_t			**Button (B)**	Q_{t+1}			D_2	D_1	D_0
Q_2	Q_1	Q_0		Q_2	Q_1	Q_0			
0	0	0	0	0	0	1	0	0	1
0	0	0	1	1	0	0	1	0	0
0	0	1	0	0	1	1	0	1	1
0	0	1	1	0	0	0	0	0	0
0	1	1	0	1	1	1	1	1	1
0	1	1	1	0	0	1	0	0	1
1	1	1	0	1	1	0	1	1	0
1	1	1	1	0	1	1	0	1	1
1	1	0	0	1	0	0	1	0	0
1	1	0	1	1	1	1	1	1	1
1	0	0	0	0	0	0	0	0	0
1	0	0	1	1	1	0	1	1	0

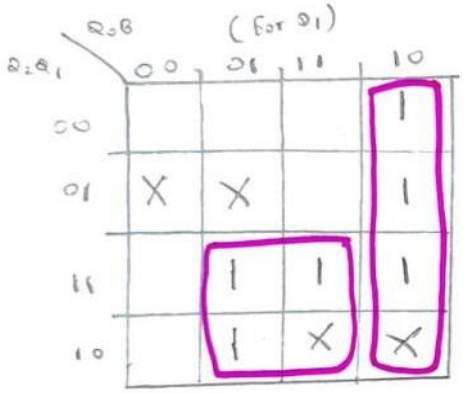
Simplified Expressions for D_0, D_1 and D_2 -

(For D_0)



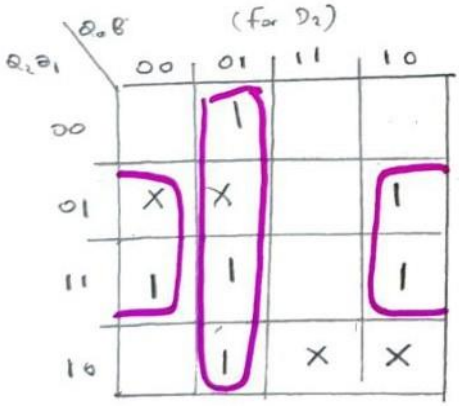
$D_0 = Q_1B + \bar{B}\bar{Q}_1$

(For D_1)



$D_1 = Q_2B + Q_0\bar{B}$

(For D_2)



$D_2 = \bar{Q}_0B + \bar{B}Q_1$

All VHDL Codes –

D_FF.vhd

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 04/08/2023 05:21:53 PM
-- Design Name:
-- Module Name: D_FF - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity D_FF is
    Port ( D : in STD_LOGIC;
           Res : in STD_LOGIC;
           Clk : in STD_LOGIC;
           Q : out STD_LOGIC;
```

```
        Qbar : out STD_LOGIC );
end D_FF;

architecture Behavioral of D_FF is

begin

   process (Clk) begin
      if (rising_edge(Clk)) then
         if Res = '1' then
            Q <='0';
            Qbar <= '1';
         else
            Q <= D;
            Qbar <= not D;
         end if;
      end if;
   end process;

end Behavioral;
```

D_FF_Sim.vhd

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 04/08/2023 05:33:01 PM
-- Design Name:
-- Module Name: D_FF_Sim - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
```

```
--------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity D_FF_Sim is
--  Port ( );
end D_FF_Sim;

architecture Behavioral of D_FF_Sim is
COMPONENT D_FF
   PORT( D,Res,Clk : IN STD_LOGIC;
         Q,Qbar : OUT STD_LOGIC);
END COMPONENT;
SIGNAL D,Res,Clk : std_logic;
SIGNAL Q,Qbar    : std_logic;
begin
UUT : D_FF PORT MAP(
      D => D,
      Res => Res,
      Clk => Clk,
      Q => Q,
      Qbar => Qbar
);

process
begin
      D <= '0';
      Res <= '0';
      Clk <= '0';
      WAIT FOR 100 ns;

      D <= '1';
      WAIT FOR 100 ns;
```

```
D <= '0';
Res <= '1';
WAIT FOR 100 ns;

D <= '1';
WAIT FOR 100 ns;

D <= '0';
Res <= '0';
WAIT FOR 30 ns;

Clk <= '1';
WAIT FOR 40 ns;

Clk <= '0';
WAIT FOR 30 ns;

D <= '1';
WAIT FOR 30 ns;

Clk <= '1';
WAIT FOR 40 NS;

Clk <= '0';
WAIT FOR 30 NS;

D <= '0';
Res <= '1';
WAIT FOR 30 ns;

Clk <= '1';
WAIT FOR 40 ns;

Clk <= '0';
WAIT FOR 30 ns;

 D <= '1';
 WAIT FOR 30 NS;

 Clk <= '1';
 WAIT FOR 40 NS;

 Clk <= '0';
```

```
        WAIT;

    end process;

end Behavioral;
```

Slow_Clk.vhd

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 04/08/2023 07:25:00 PM
-- Design Name:
-- Module Name: Slow_Clk - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;
```

```
entity Slow_Clk is
   Port ( Clk_in : in STD_LOGIC;
          Clk_out : out STD_LOGIC);
end Slow_Clk;

architecture Behavioral of Slow_Clk is

signal count : integer := 1;
signal clk_status : std_logic := '0';

begin

   process (Clk_in) begin
      if(rising_edge(Clk_in)) then
         count <= count+1;
         if(count = 5)then   -- Counting frequency scaler(Reduced to 5 to simulation purposes.IF not 5M.)
            clk_status <= not clk_status;
            Clk_out <= clk_status;
            count<=1;
         end if;
      end if;
   end process;

end Behavioral;
```

Slow_Clk_Sim.vhd

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 04/08/2023 07:30:53 PM
-- Design Name:
-- Module Name: Slow_Clk_Sim - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
```

```
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Slow_Clk_Sim is
--  Port ( );
end Slow_Clk_Sim;

architecture Behavioral of Slow_Clk_Sim is
COMPONENT Slow_Clk
   PORT( Clk_in : IN STD_LOGIC;
         Clk_out : OUT STD_LOGIC);
END COMPONENT;
SIGNAL Clk_in  : std_logic;
SIGNAL Clk_out : std_logic;
begin
UUT : Slow_Clk PORT MAP(
      Clk_in => Clk_in,
      Clk_out => Clk_out
      );

process
begin

Clk_in <= '0';
WAIT FOR 10 ns;

Clk_in <= '1';
```

```
WAIT FOR 10 ns;

Clk_in <= '0';
WAIT FOR 10 ns;

Clk_in <= '1';
WAIT FOR 10 ns;

Clk_in <= '0';
WAIT FOR 10 ns;

Clk_in <= '1';
WAIT FOR 10 ns;

Clk_in <= '0';
WAIT FOR 10 ns;

Clk_in <= '1';
WAIT FOR 10 ns;

Clk_in <= '0';
WAIT FOR 10 ns;

Clk_in <= '1';
WAIT FOR 10 ns;

Clk_in <= '0';
WAIT FOR 10 ns;

Clk_in <= '1';
WAIT FOR 10 ns;

Clk_in <= '0';
WAIT FOR 10 ns;

Clk_in <= '1';
WAIT FOR 10 ns;

Clk_in <= '0';
WAIT FOR 10 ns;

Clk_in <= '1';
WAIT FOR 10 ns;
```

```
Clk_in <= '0';
WAIT FOR 10 ns;

Clk_in <= '1';
WAIT FOR 10 ns;

Clk_in <= '0';
WAIT FOR 10 ns;

Clk_in <= '1';
WAIT FOR 10 ns;

Clk_in <= '0';
WAIT FOR 10 ns;

Clk_in <= '1';
WAIT FOR 10 ns;

Clk_in <= '0';
WAIT FOR 10 ns;

Clk_in <= '1';
WAIT FOR 10 ns;

Clk_in <= '0';
WAIT FOR 10 ns;

Clk_in <= '1';
WAIT FOR 10 ns;

Clk_in <= '0';
WAIT FOR 10 ns;

Clk_in <= '1';
WAIT FOR 10 ns;

Clk_in <= '0';
WAIT FOR 10 ns;

Clk_in <= '1';
WAIT FOR 10 ns;

Clk_in <= '0';
WAIT FOR 10 ns;
```

```
Clk_in <= '1';
WAIT FOR 10 ns;

Clk_in <= '0';
WAIT FOR 10 ns;

Clk_in <= '1';
WAIT FOR 10 ns;

Clk_in <= '0';
WAIT FOR 10 ns;

Clk_in <= '1';
WAIT FOR 10 ns;

Clk_in <= '0';
WAIT FOR 10 ns;

Clk_in <= '1';
WAIT FOR 10 ns;

Clk_in <= '0';
WAIT FOR 10 ns;

Clk_in <= '1';
WAIT FOR 10 ns;

Clk_in <= '0';
WAIT FOR 10 ns;

Clk_in <= '1';
WAIT FOR 10 ns;

Clk_in <= '0';
WAIT FOR 10 ns;

Clk_in <= '1';
WAIT FOR 10 ns;

Clk_in <= '0';
WAIT FOR 10 ns;

Clk_in <= '1';
```

```
WAIT FOR 10 ns;

Clk_in <= '0';
WAIT FOR 10 ns;

Clk_in <= '1';
WAIT FOR 10 ns;

Clk_in <= '0';
WAIT FOR 10 ns;

Clk_in <= '1';
WAIT FOR 10 ns;

Clk_in <= '0';
WAIT FOR 10 ns;

Clk_in <= '1';
WAIT FOR 10 ns;

Clk_in <= '0';
WAIT FOR 10 ns;

Clk_in <= '1';
WAIT FOR 10 ns;

Clk_in <= '0';
WAIT FOR 10 ns;

Clk_in <= '1';
WAIT FOR 10 ns;

Clk_in <= '0';
WAIT FOR 10 ns;

Clk_in <= '1';
WAIT FOR 10 ns;

Clk_in <= '0';
WAIT FOR 10 ns;

Clk_in <= '1';
WAIT FOR 10 ns;
```

```
Clk_in <= '0';
WAIT FOR 10 ns;

Clk_in <= '1';
WAIT FOR 10 ns;

Clk_in <= '0';
WAIT FOR 10 ns;

Clk_in <= '1';
WAIT FOR 10 ns;

Clk_in <= '0';
WAIT FOR 10 ns;

Clk_in <= '1';
WAIT FOR 10 ns;

Clk_in <= '0';
WAIT FOR 10 ns;

Clk_in <= '1';
WAIT FOR 10 ns;

Clk_in <= '0';
WAIT FOR 10 ns;

Clk_in <= '1';
WAIT FOR 10 ns;

Clk_in <= '0';
WAIT FOR 10 ns;

Clk_in <= '1';
WAIT FOR 10 ns;

Clk_in <= '0';
WAIT FOR 10 ns;

Clk_in <= '1';
WAIT FOR 10 ns;

Clk_in <= '0';
WAIT FOR 10 ns;
```

```
Clk_in <= '1';
WAIT FOR 10 ns;

Clk_in <= '0';
WAIT FOR 10 ns;

Clk_in <= '1';
WAIT FOR 10 ns;

Clk_in <= '0';
WAIT FOR 10 ns;

Clk_in <= '1';
WAIT FOR 10 ns;


Clk_in <= '0';

WAIT;

end process;


end Behavioral;
```

Counter.vhd

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 04/08/2023 08:32:19 PM
-- Design Name:
-- Module Name: Counter - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
```

```
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Counter is
   Port ( Dir : in STD_LOGIC;
          Res : in STD_LOGIC;
          Clk : in STD_LOGIC;
          Q : out STD_LOGIC_VECTOR (2 downto 0):="000");
end Counter;

architecture Behavioral of Counter is

 component D_FF
 port (
 D : in STD_LOGIC;
 Res: in STD_LOGIC;
 Clk : in STD_LOGIC;
 Q : out STD_LOGIC;
 Qbar : out STD_LOGIC);
 end component;

 component Slow_Clk
 port (
 Clk_in : in STD_LOGIC;
 Clk_out: out STD_LOGIC);
 end component;
```

```
 signal D0, D1, D2 : std_logic; -- Internal signals
 signal Q0, Q1, Q2 : std_logic; -- Internal signals
 signal Clk_slow : std_logic; -- Internal clock

begin
 Slow_Clk0 : Slow_Clk
 port map (
 Clk_in => Clk,
 Clk_out => Clk_slow);

 D0 <= ((not Q2) and (not Dir)) or (Q1 and Dir);
 D1 <= ((Q2 and Dir) or (Q0 and (not Dir)));
 D2 <= (((not Q0)and Dir) or ((not Dir) and Q1));

 D_FF0 : D_FF
 port map (
    D => D0,
    Res => Res,
    Clk => Clk_slow,
    Q => Q0);
 D_FF1 : D_FF
 port map (
    D => D1,
    Res => Res,
    Clk => Clk_slow,
    Q => Q1);
 D_FF2 : D_FF
 port map (
   D => D2,
   Res => Res,
   Clk => Clk_slow,
   Q => Q2);

Q(0) <= Q0;
Q(1) <= Q1;
Q(2) <= Q2;

end Behavioral;
```

Counter_sim.vhd

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 04/08/2023 09:07:18 PM
-- Design Name:
-- Module Name: Counter_sim - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Counter_sim is
--  Port ( );
end Counter_sim;

architecture Behavioral of Counter_sim is
COMPONENT Counter
    PORT( Dir,Res,Clk : IN STD_LOGIC;
```

```
        Q : OUT STD_LOGIC_VECTOR (2 downto 0));
END COMPONENT;
SIGNAL Dir,Res,Clk  : std_logic;
SIGNAL Q : std_logic_vector (2 downto 0);
begin
UUT : Counter PORT MAP(
      Dir => Dir,
      Res => Res,
      Clk =>Clk,
      Q =>Q
      );

process
begin

res <= '0';
dir <= '0';
Clk <= '0';
WAIT FOR 10 ns;

res <= '0';
dir <= '0';
Clk <= '1';
WAIT FOR 10 ns;
res <= '0';
dir <= '0';
Clk <= '0';
WAIT FOR 10 ns;

res <= '0';
dir <= '0';
Clk <= '1';
WAIT FOR 10 ns;
res <= '0';
dir <= '0';
Clk <= '0';
WAIT FOR 10 ns;

res <= '0';
dir <= '0';
Clk <= '1';
WAIT FOR 10 ns;
res <= '0';
dir <= '0';
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```
Clk <= '0';
WAIT FOR 10 ns;

res <= '0';
dir <= '0';
Clk <= '1';
WAIT FOR 10 ns;
res <= '0';
dir <= '0';
Clk <= '0';
WAIT FOR 10 ns;

res <= '0';
dir <= '0';
Clk <= '1';
WAIT FOR 10 ns;
res <= '0';
dir <= '0';
Clk <= '0';
WAIT FOR 10 ns;

res <= '0';
dir <= '0';
Clk <= '1';
WAIT FOR 10 ns;
res <= '0';
dir <= '0';
Clk <= '0';
WAIT FOR 10 ns;

res <= '0';
dir <= '0';
Clk <= '1';
WAIT FOR 10 ns;
res <= '0';
dir <= '0';
Clk <= '0';
WAIT FOR 10 ns;

res <= '0';
dir <= '0';
Clk <= '1';
WAIT FOR 10 ns;
res <= '0';
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```
dir <= '0';
Clk <= '0';
WAIT FOR 10 ns;

res <= '0';
dir <= '0';
Clk <= '1';
WAIT FOR 10 ns;
res <= '0';
dir <= '0';
Clk <= '0';
WAIT FOR 10 ns;

res <= '0';
dir <= '0';
Clk <= '1';
WAIT FOR 10 ns;
res <= '0';
dir <= '0';
Clk <= '0';
WAIT FOR 10 ns;

res <= '0';
dir <= '0';
Clk <= '1';
WAIT FOR 10 ns;
res <= '0';
dir <= '0';
Clk <= '0';
WAIT FOR 10 ns;

res <= '0';
dir <= '0';
Clk <= '1';
WAIT FOR 10 ns;
res <= '0';
dir <= '0';
Clk <= '0';
WAIT FOR 10 ns;

res <= '0';
dir <= '0';
Clk <= '1';
WAIT FOR 10 ns;
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```
res <= '0';
dir <= '0';
Clk <= '0';
WAIT FOR 10 ns;

res <= '0';
dir <= '0';
Clk <= '1';
WAIT FOR 10 ns;
res <= '0';
dir <= '0';
Clk <= '0';
WAIT FOR 10 ns;

res <= '0';
dir <= '0';
Clk <= '1';
WAIT FOR 10 ns;
res <= '0';
dir <= '0';
Clk <= '0';
WAIT FOR 10 ns;

res <= '0';
dir <= '0';
Clk <= '1';
WAIT FOR 10 ns;
res <= '0';
dir <= '0';
Clk <= '0';
WAIT FOR 10 ns;

res <= '0';
dir <= '0';
Clk <= '1';
WAIT FOR 10 ns;
res <= '0';
dir <= '0';
Clk <= '0';
WAIT FOR 10 ns;

res <= '0';
dir <= '0';
Clk <= '1';
```

```
WAIT FOR 10 ns;
res <= '0';
dir <= '0';
Clk <= '0';
WAIT FOR 10 ns;

res <= '0';
dir <= '0';
Clk <= '1';
WAIT FOR 10 ns;
res <= '0';
dir <= '0';
Clk <= '0';
WAIT FOR 10 ns;

res <= '0';
dir <= '0';
Clk <= '1';
WAIT FOR 10 ns;
res <= '0';
dir <= '0';
Clk <= '0';
WAIT FOR 10 ns;

res <= '0';
dir <= '0';
Clk <= '1';
WAIT FOR 10 ns;
res <= '0';
dir <= '0';
Clk <= '0';
WAIT FOR 10 ns;

res <= '0';
dir <= '0';
Clk <= '1';
WAIT FOR 10 ns;
res <= '0';
dir <= '0';
Clk <= '0';
WAIT FOR 10 ns;

res <= '0';
dir <= '0';
```

```
Clk <= '1';
WAIT FOR 10 ns;
res <= '0';
dir <= '0';
Clk <= '0';
WAIT FOR 10 ns;

res <= '0';
dir <= '0';
Clk <= '1';
WAIT FOR 10 ns;
res <= '0';
dir <= '0';
Clk <= '0';
WAIT FOR 10 ns;

res <= '0';
dir <= '0';
Clk <= '1';
WAIT FOR 10 ns;
res <= '0';
dir <= '0';
Clk <= '0';
WAIT FOR 10 ns;

res <= '0';
dir <= '0';
Clk <= '1';
WAIT FOR 10 ns;
res <= '0';
dir <= '0';
Clk <= '0';
WAIT FOR 10 ns;

res <= '0';
dir <= '0';
Clk <= '1';
WAIT FOR 10 ns;
res <= '0';
dir <= '0';
Clk <= '0';
WAIT FOR 10 ns;

res <= '0';
```

```
dir <= '0';
Clk <= '1';
WAIT FOR 10 ns;
res <= '0';
dir <= '0';
Clk <= '0';
WAIT FOR 10 ns;

res <= '0';
dir <= '0';
Clk <= '1';
WAIT FOR 10 ns;
res <= '0';
dir <= '0';
Clk <= '0';
WAIT FOR 10 ns;

res <= '0';
dir <= '0';
Clk <= '1';
WAIT FOR 10 ns;
res <= '0';
dir <= '0';
Clk <= '0';
WAIT FOR 10 ns;

res <= '0';
dir <= '0';
Clk <= '1';
WAIT FOR 10 ns;
res <= '0';
dir <= '0';
Clk <= '0';
WAIT FOR 10 ns;

res <= '0';
dir <= '0';
Clk <= '1';
WAIT FOR 10 ns;
res <= '0';
dir <= '0';
Clk <= '0';
WAIT FOR 10 ns;
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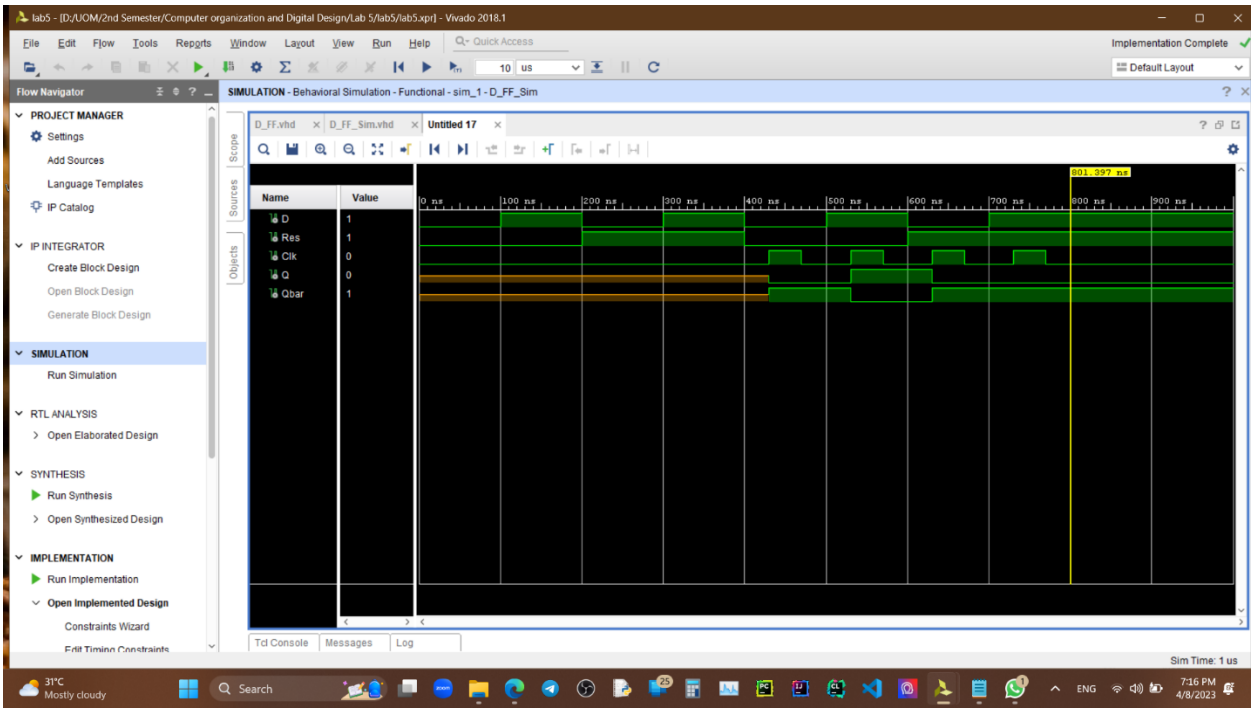
```
res <= '0';
dir <= '0';
Clk <= '1';
WAIT FOR 10 ns;
res <= '0';
dir <= '0';
Clk <= '0';
WAIT FOR 10 ns;

res <= '0';
dir <= '0';
Clk <= '1';
WAIT FOR 10 ns;
res <= '0';
dir <= '0';
Clk <= '0';
WAIT FOR 10 ns;

res <= '0';
dir <= '0';
Clk <= '1';
WAIT FOR 10 ns;
res <= '0';
dir <= '0';
Clk <= '0';
WAIT FOR 10 ns;

res <= '0';
dir <= '0';
Clk <= '1';
WAIT FOR 10 ns;
res <= '0';
dir <= '0';
Clk <= '0';
WAIT FOR 10 ns;

res <= '0';
dir <= '0';
Clk <= '1';
WAIT FOR 10 ns;
res <= '0';
dir <= '0';
Clk <= '0';
WAIT FOR 10 ns;
```

```
res <= '0';
dir <= '0';
Clk <= '1';
WAIT FOR 10 ns;
res <= '0';
dir <= '0';
Clk <= '0';
WAIT FOR 10 ns;

res <= '0';
dir <= '0';
Clk <= '1';
WAIT FOR 10 ns;
res <= '0';
dir <= '0';
Clk <= '0';
WAIT FOR 10 ns;

res <= '0';
dir <= '0';
Clk <= '1';
WAIT FOR 10 ns;
res <= '0';
dir <= '0';
Clk <= '0';
WAIT FOR 10 ns;

res <= '0';
dir <= '0';
Clk <= '1';
WAIT FOR 10 ns;
res <= '0';
dir <= '0';
Clk <= '0';
WAIT FOR 10 ns;

res <= '0';
dir <= '0';
Clk <= '1';
WAIT FOR 10 ns;
res <= '0';
dir <= '0';
Clk <= '0';
```

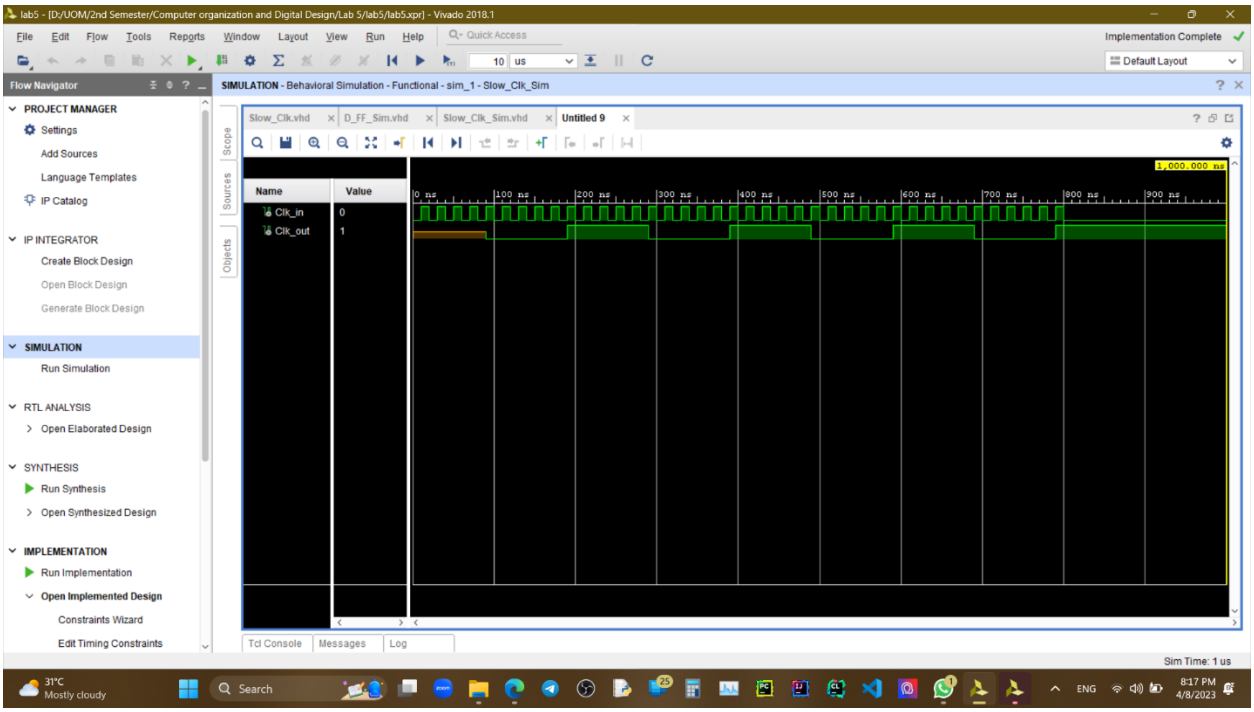
```
WAIT FOR 10 ns;

res <= '0';
dir <= '0';
Clk <= '1';
WAIT FOR 10 ns;
res <= '0';
dir <= '0';
Clk <= '0';
WAIT FOR 10 ns;

res <= '0';
dir <= '0';
Clk <= '1';
WAIT FOR 10 ns;
Clk <= '0';

WAIT;

end process;
end Behavioral;
```

Timing diagrams –

Simulating D Flip Flop –

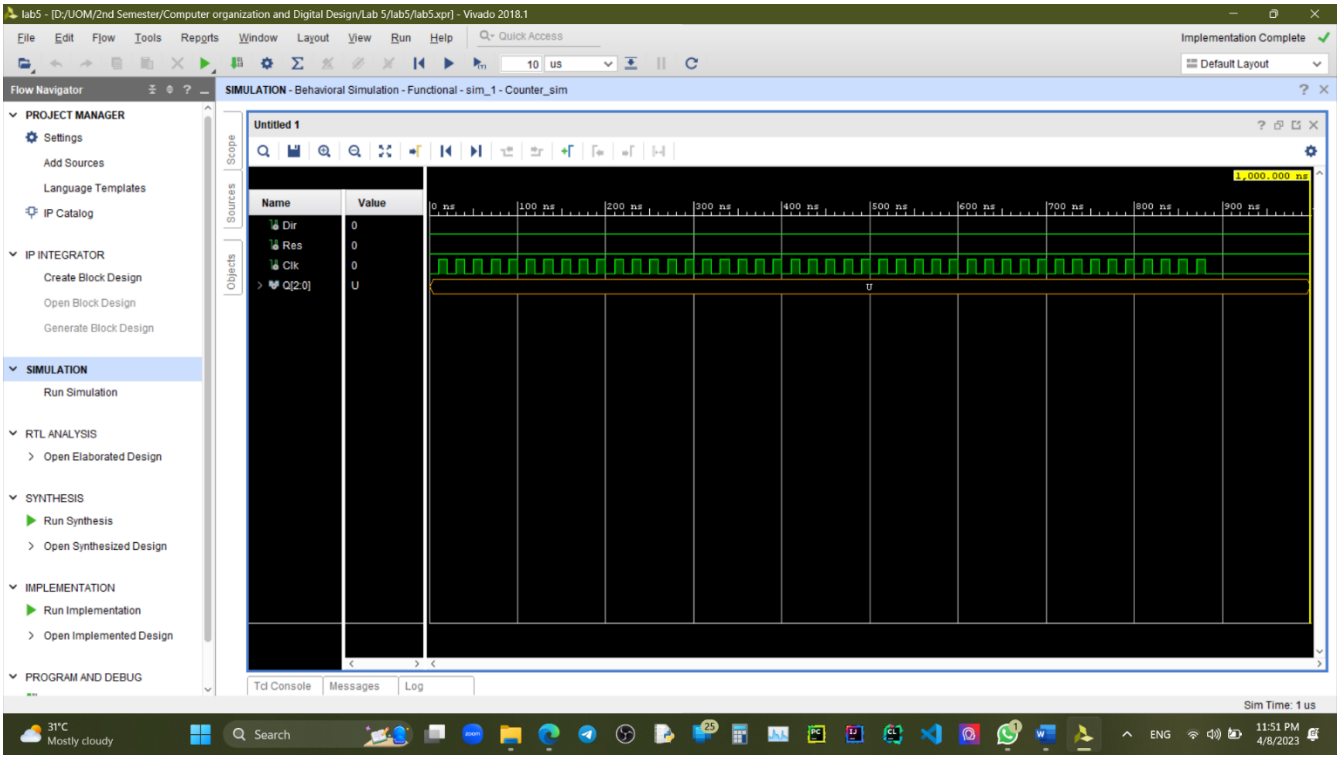


Simulating Slow Clock –



(Didn’t initialize any values for Q and Qbar in D flipflop and Clk_out in Slow Clock explicitly) *

Counter (Failed) –



Conclusions –

In conclusion, this lab exercise involved designing a D flip-flop and testing it via simulation. The next step was to implement a “Slow Clock” using the provided 100MHz clock of the Basys board and test it via simulation. Finally, a 3-bit counter was designed that counts in the direction specified via an input using both the slow clock and the D flip-flops. This exercise provided hands-on experience in designing and testing digital circuits using simulation tools. But sadly failed to successfully implement the final step, counter.