Name – De Silva A.P.C.

Index No – 210098R

Group – CSE

Assigned lab task - Design and develop a half adder, full adder and a Ripple carry adder using Vivado. Here, the Full adder should be implemented using two half adders and then the 4 bit ripple adder should be implemented using full adders.

Truth tables and Boolean expressions simplification –

Half adder

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Using sum of the products method: Sum = A'B+AB' (i.e. A XOR B) , Carry = A.B

Full adder

A	B	C_{in}	Sum	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Using sum of the products method: Sum = $A'B'C_{in} + A'BC' + AB'C_{in}' + ABC_{in}$

$= A'(B'C_{in} + BC'_{in}) + A(B'C'_{in} + BC_{in})$

$= A(B \text{ XOR } C_{in}) + A(B \text{ XOR } C)'$

$= A \text{ XOR } (B \text{ XOR } C) = A \text{ XOR } B \text{ XOR } C$

Then using a Kmap :

BC_{in}

A

	00	01	11	10
0	0	1	1^3	2
1	4	1^5	1^7	6

$C_{out} = AB + BC_{in} + AC_{in}$

HA.VHD

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 03/18/2023 12:32:39 AM
-- Design Name:
-- Module Name: HA - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------
```

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity HA is
    Port ( A : in STD_LOGIC;
           B : in STD_LOGIC;
           S : out STD_LOGIC;
           C : out STD_LOGIC);
end HA;

architecture Behavioral of HA is

begin
S <= A xor B ;
C <= A and B ;
end Behavioral;
```

TB_HA.VHD

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 03/18/2023 12:38:30 AM
-- Design Name:
-- Module Name: TB_HA - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
```

```
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity TB_HA is
--  Port ( );
end TB_HA;

architecture Behavioral of TB_HA is
COMPONENT HA
    PORT(A,B : IN STD_LOGIC;
         S,C : OUT STD_LOGIC);
END COMPONENT;
SIGNAL A,B : std_logic;
SIGNAL S,C : std_logic;
begin
UUT: HA PORT MAP(
A => A,
B => B,
S => S,
C => C
);
```

```
process
begin
   A <= '0';
   B <= '0';

   WAIT FOR 100 ns;
   B <= '1';
   WAIT FOR 100 ns;
   A <= '1';
   B <= '0';
   WAIT FOR 100 ns;
   B <= '1';
   WAIT;
end process;
end Behavioral;
```

FA.VHD

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 03/18/2023 12:58:43 AM
-- Design Name:
-- Module Name: FA - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
```

```
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity FA is
   Port ( A : in STD_LOGIC;
          B : in STD_LOGIC;
          C_in : in STD_LOGIC;
          S : out STD_LOGIC;
          C_out : out STD_LOGIC);
end FA;

architecture Behavioral of FA is
component HA
   port (
   A: in std_logic;
   B: in std_logic;
   S:out std_logic;
   C: out std_logic);
end component;
signal HA0_S, HA0_C,HA1_S, HA1_C : std_logic;
begin
HA_0 : HA
   port map (
   A => A,
   B => B,
   S => HA0_S,
   C => HA0_C);
HA_1 : HA
       port map (
       A => HA0_S,
       B => C_in,
       S => HA1_S,
       C => HA1_C);
S <= HA1_S;
C_out <= HA0_C or HA1_C;
end Behavioral;
```

TB_FA.VHD

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 03/18/2023 01:49:53 AM
```

```
-- Design Name:
-- Module Name: TB_FA - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity TB_FA is
--  Port ( );
end TB_FA;

architecture Behavioral of TB_FA is
COMPONENT FA
   PORT(A,B,C_in : IN STD_LOGIC;
        S,C_out : OUT STD_LOGIC);
END COMPONENT;
SIGNAL A,B,C_in : std_logic;
SIGNAL S,C_out : std_logic;
begin
UUT: FA PORT MAP(
A => A,
B => B,
S => S,
C_in => C_in,
C_out => C_out
);
process
begin
   A <= '0';
   B <= '0';
   C_in <= '0';
   WAIT FOR 100 ns;
   C_in <= '1';
```

```
   WAIT FOR 100 ns;
   B <= '1';
   C_in <= '0';
   WAIT FOR 100 ns;
   C_in <= '1';
   WAIT FOR 100 ns;
   A <= '1';
   B <= '0';
   C_in <= '0';
   WAIT FOR 100 ns;
   C_in <= '1';
   WAIT FOR 100 ns;
   B <= '1';
   C_in <= '0';
   WAIT FOR 100 ns;
   C_in <= '1';
   WAIT;
end process;
end Behavioral;
```

RCA_4.VHD

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 03/18/2023 11:27:04 AM
-- Design Name:
-- Module Name: RCA_4 - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
```

```
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity RCA_4 is
   Port ( A0 : in STD_LOGIC;
          A1 : in STD_LOGIC;
          A2 : in STD_LOGIC;
          A3 : in STD_LOGIC;
          B0 : in STD_LOGIC;
          B1 : in STD_LOGIC;
          B2 : in STD_LOGIC;
          B3 : in STD_LOGIC;
          C_in : in STD_LOGIC;
          S0 : out STD_LOGIC;
          S1 : out STD_LOGIC;
          S2 : out STD_LOGIC;
          S3 : out STD_LOGIC;
          C_out : out STD_LOGIC);
end RCA_4;

architecture Behavioral of RCA_4 is
component FA
       port(
       A: in std_logic;
       B: in std_logic;
       C_in : in std_logic;
       S: out std_logic;
       C_out : out std_logic);
   end component;

   SIGNAL FA0_S, FA0_C , FA1_S,FA1_C, FA2_S, FA2_C, FA3_S, FA3_C
   : std_logic;
begin
   FA_0 : FA
      port map (
         A => A0,
         B => B0,
         C_in => '0',
         S=> S0,
         C_out => FA0_C);
    FA_1 : FA
      port map (
         A => A1,
         B => B1,
         C_in => FA0_C,
         S=> S1,
         C_out => FA1_C);
   FA_2 : FA
      port map (
         A => A2,
```

```
        B => B2,
        C_in => FA1_C,
        S=> S2,
        C_out => FA2_C);
   FA_3 : FA
      port map (
        A => A3,
        B => B3,
        C_in => FA2_C,
        S=> S3,
        C_out => C_out);
end Behavioral;
```

TB_4_RCA.VHD

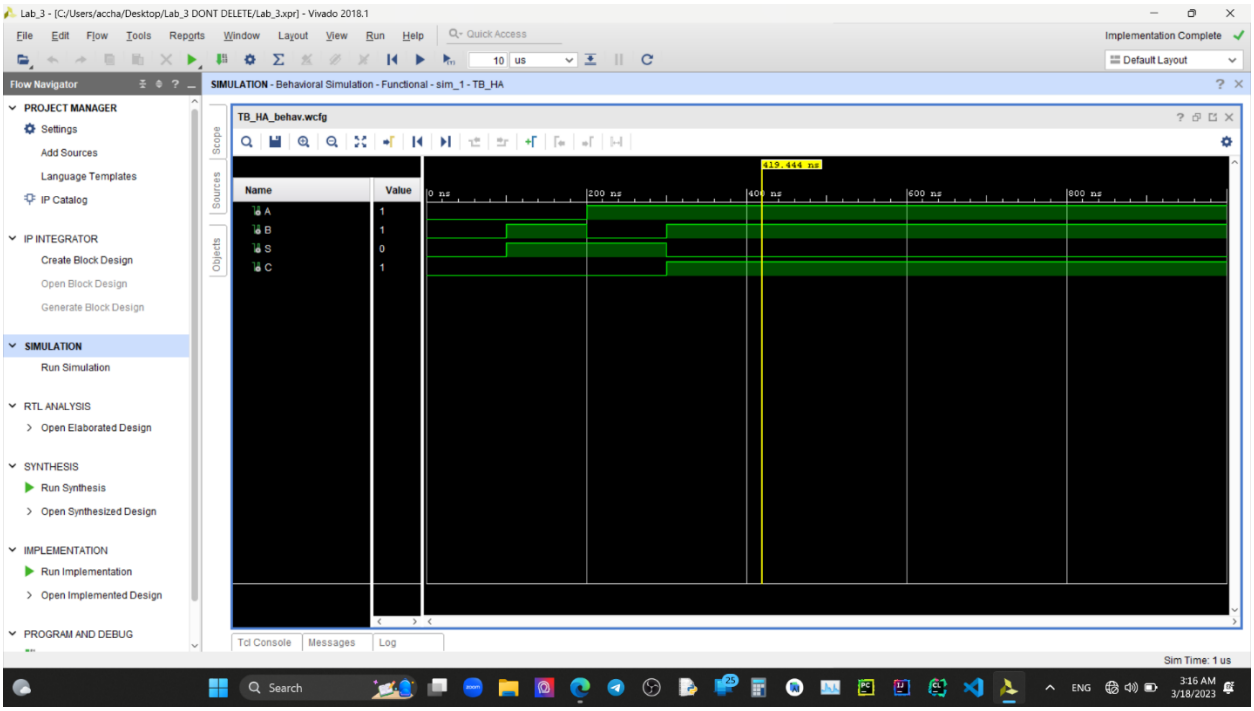
```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 03/18/2023 11:36:31 AM
-- Design Name:
-- Module Name: TB_4_RCA - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity TB_4_RCA is
```

```
--  Port ( );
end TB_4_RCA;

architecture Behavioral of TB_4_RCA is
COMPONENT RCA_4
   PORT(A0,A1,A2,A3,B0,B1,B2,B3,C_in : IN STD_LOGIC;
       S0,S1,S2,S3,C_out: OUT STD_LOGIC);
END COMPONENT;
SIGNAL A0,A1,A2,A3,B0,B1,B2,B3,C_in: std_logic;
SIGNAL S0,S1,S2,S3,C_out : std_logic;
begin
UUT: RCA_4 PORT MAP(
A0 => A0,
A1 => A1,
A2 => A2,
A3 => A3,
B0 => B0,
B1 => B1,
B2 => B2,
B3 => B3,
C_in => C_in,
C_out => C_out,
S0 => S0,
S1 => S1,
S2 => S2,
S3 => S3
);
process
begin
   A0 <= '0';
   A1 <= '1';
   A2 <= '0';
   A3 <= '0';
   B0 <= '1';
   B1 <= '0';
   B2 <= '1';
   B3 <= '1';
   C_in <= '0';
   WAIT FOR 100 ns;
      A0 <= '0';
      A1 <= '1';
      A2 <= '0';
      A3 <= '1';
      B0 <= '1';
      B1 <= '1';
      B2 <= '0';
      B3 <= '0';
      C_in <= '0';
   WAIT FOR 100 ns;
      A0 <= '0';
      A1 <= '1';
      A2 <= '1';
      A3 <= '1';
      B0 <= '1';
```

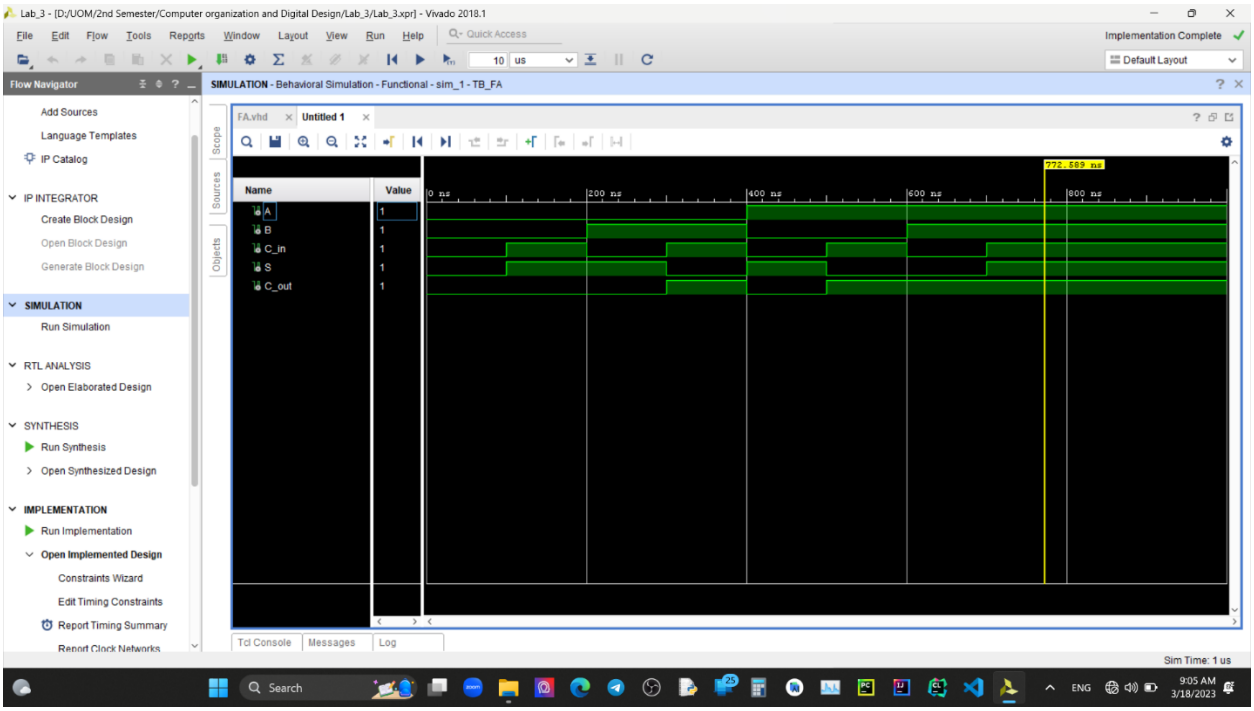
```
      B1 <= '0';
      B2 <= '1';
      B3 <= '1';
      C_in <= '0';

   WAIT FOR 100 ns;
     A0 <= '1';
     A1 <= '1';
     A2 <= '1';
     A3 <= '1';
     B0 <= '0';
     B1 <= '0';
     B2 <= '1';
     B3 <= '1';
     C_in <= '0';
    WAIT FOR 100 ns;
       A0 <= '1';
       A1 <= '0';
       A2 <= '0';
       A3 <= '1';
       B0 <= '0';
       B1 <= '0';
       B2 <= '0';
       B3 <= '1';
       C_in <= '0';
     WAIT FOR 100 ns;
     A0 <= '1';
     A1 <= '1';
     A2 <= '0';
     A3 <= '1';
     B0 <= '1';
     B1 <= '1';
     B2 <= '0';
     B3 <= '0';
     C_in <= '0';
   WAIT;
end process;
end Behavioral;
```

Timing diagrams –

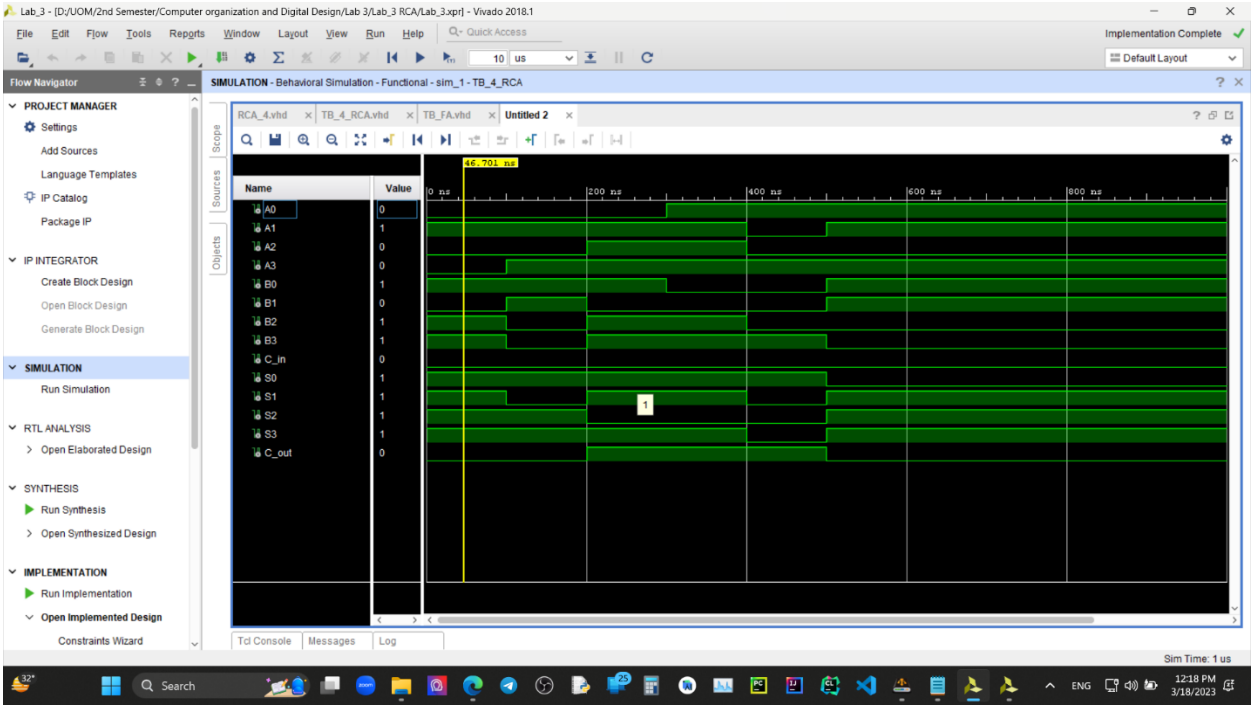
Half adder –



Full Adder –



RCA –



Discussion – After an operation if there is an overflow there is no way to represent that using only three LEDs. For an example if we add 1000 and 1011, this will output only 0011 without notifying about the remaining carry bit. To indicate about the carry bit we need that extra LED.

Conclusion - We can use basic components to build more complex components. Here we build a half adder using basic logic, then built a full adder using half adders and then build RCA using the full adders.