Hand Gesture Detection Using Compact CNN Accelerator IP

Reference Design

FPGA-RD-02046 Version 1.0

September 2018

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1. Introduction

The Hand Gesture Detection using Compact CNN Accelerator Reference Design document describes how to implement a Hand Gesture Detection design on the iCE40™ UltraPlus FPGA. This design utilizes the Lattice Radiant Compact CNN Accelerator IP core, which is optimized for Convolutional Neural Network implementations.

2. Related Documentation

In addition to using this guide to help you get started developing CNN solutions on your device, you can refer to other applicable documents that may contain more detailed information that is beyond the scope of this guide.

The following documents can be obtained from the Lattice website:

- Lattice SensAI Neural Network Compiler Software (FPGA-UG-02052) - This document explains how to create the firmware file, which contains the command sequence as well as weights that go into the CNN Accelerator IP Core.
- Compact CNN Accelerator IP Core User Guide (FPGA-IPUG-02038) - This document provides additional details about the CNN IP Core contained in this design.
- Lattice Radiant Software User Guide - This document describes the main features, usage, and key concepts of the Lattice Radiant software, which is used in creating this reference design.

3. Software Requirements

The following software requirements are required in order to design and use the Hand Gesture Reference Design:

- Radiant Software 1.0 or greater - This is used to build the reference design.
- Radiant Programmer tool - This is used to program the bitstream to the External SPI Flash on the board.
- Compact CNN Accelerator IP Core - This is used to create the CNN Accelerator Engine.
- Lattice SensAI Neural Network Compiler Software – This is used to generate the firmware file from the TensorFlow/Caffe outputs.

4. Hardware Requirements

The reference design is targeted to support the Himax HM01B0 UPDuino Shield board, but can be modified for use in other HW as needed. This hardware requires a mini-USB cable in order to program.

5. Directory Structure

Figure 5.1 shows the directory structure of the **Hand Gesture Detection Using Compact CNN Accelerator IP – Project Files**. The figure also details the files contained in each folder.

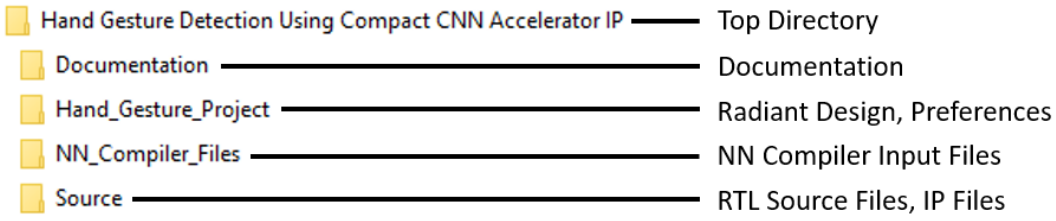

Figure 5.1. Hand Gesture Detection Directory Structure

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6. Hand Gesture Detection Reference Design Overview

6.1. Block Diagram

This section describes the Hand Gesture Detection block diagram and each top block module, as shown in Figure 6.1.

Note: Different PAR iterations can give different results. Try more than one PAR iteration to acquire the best results.

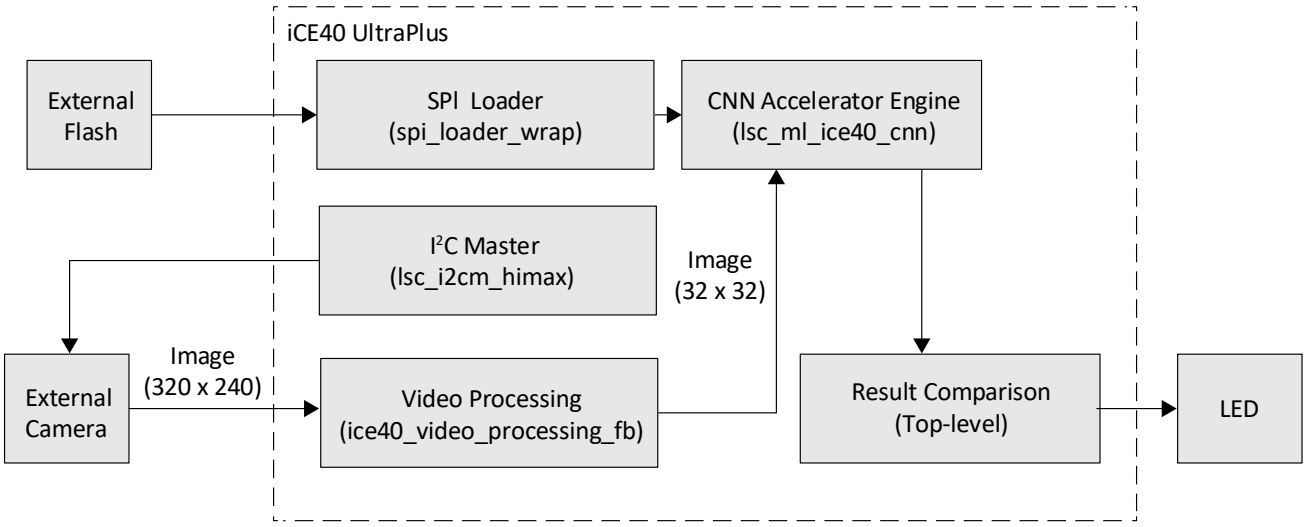

Figure 6.1. Hand Presence Detection Block Diagram

The reference design shows an implementation of a machine learning design using the CNN Soft IP Engine. There are two main inputs that go into the CNN Accelerator Engine, which then outputs four values that are evaluated to determine whether an open hand, a closed hand, or nothing is detected in a specific area.

6.2. Top Level Blocks

This section discusses in detail the top-level modules that makes up the Hand Gesture Detection Reference Design. Each top-level module includes the Verilog (.v) or IP Catalog (.ipx) files. These files are in the source directory of the .zip file.

6.2.1. Top-Level Module – Hand Gesture_Top.v

This is the top-level module contains all the blocks and connections found in Figure 6.1.

6.2.2. CNN Accelerator Engine – lsc_ml_ice40_cnn.ipx

This block contains the CNN Accelerator Engine. In this design, the engine is configured to Memory Type: DUAL SPRAM, ML_TYPE: CNN, SCRATCH SIZE: 1K. Refer to the Compact CNN Accelerator IP Core User Guide (FPGA-IPUG-02038) for details. The .ipx file takes the firmware file from the External SPI Flash and the processed image to output the desired result.

6.2.3. SPI Loader – spi_loader_wrap.v & spi_loader_spram.v

This module reads the external flash for the firmware file. The firmware file is then outputted into the CNN Accelerator IP Core. The SPI loader is configured to read the firmware file at address 20'h20000. The Lattice Neural Network compiler tool generates the firmware file.

Firmware files are located in the **NN_Compiler_Files** directory for you to generate your own firmware file.

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6.2.4. I2S Master – i2cm_himax.v

This module communicates with the Himax Camera and configures it upon boot up to make sure that it outputs the correct image. The Himax Camera is configured to output a 1 x 320 x 240 image.

6.2.5. Video Preprocessing – ice40_himax_video_process_fb_gray.v

This module stores takes the Himax Camera image output and downscales it to 1 x 32 x 32. This downscaled image is then sent to the CNN Accelerator IP core when it is requested.

6.2.6. UART – lsc_uart.v (not shown in block diagram)

With the top level parameter, EN_UART = 1, we can use UART in order to see what the camera is observing. This is mostly for centering the camera and debugging. In the design, it is default enabled. If you wish to conserve power/resources, you can turn off this feature.

6.2.7. Result Comparison/LED – Done in top level

This module captures the output of the Compact CNN Accelerator Engine and provides the result. The output is in four clock cycles, which represents in order: None, Open, Close and Others. These four values are then compared to each other and the one with the highest value outputs its LED light.

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7. Generating the Firmware File

To generate the Hand Gesture Firmware file:

1. Using the files located in the **NN_Compiler_Files** directory, create a new project in SensAI and apply the following settings as shown in Figure 7.1.
   - **Framework — TensorFlow**
   - **Device — UltraPlus**
   - **Class — CNN**
   - **Network File — handGesture.pb**
   - **Image/Video/Audio Data — B1039.jpg**
2. Click **Next**.

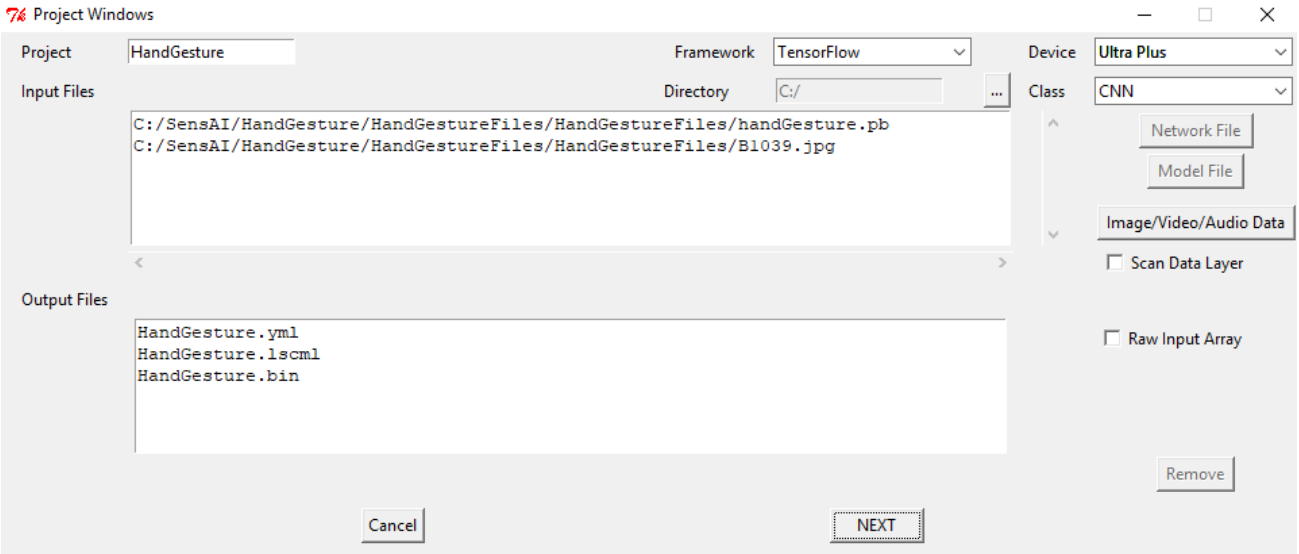

Figure 7.1. SensAI Project Settings Part 1

3. In the second section, apply the Neural Network engine settings as shown in Figure 7.2:
   - **On-Chip Memory Block Size — 65536**
   - **Mean Value — 0**
   - **Scale Value — 1.0**
4. Click **OK**.

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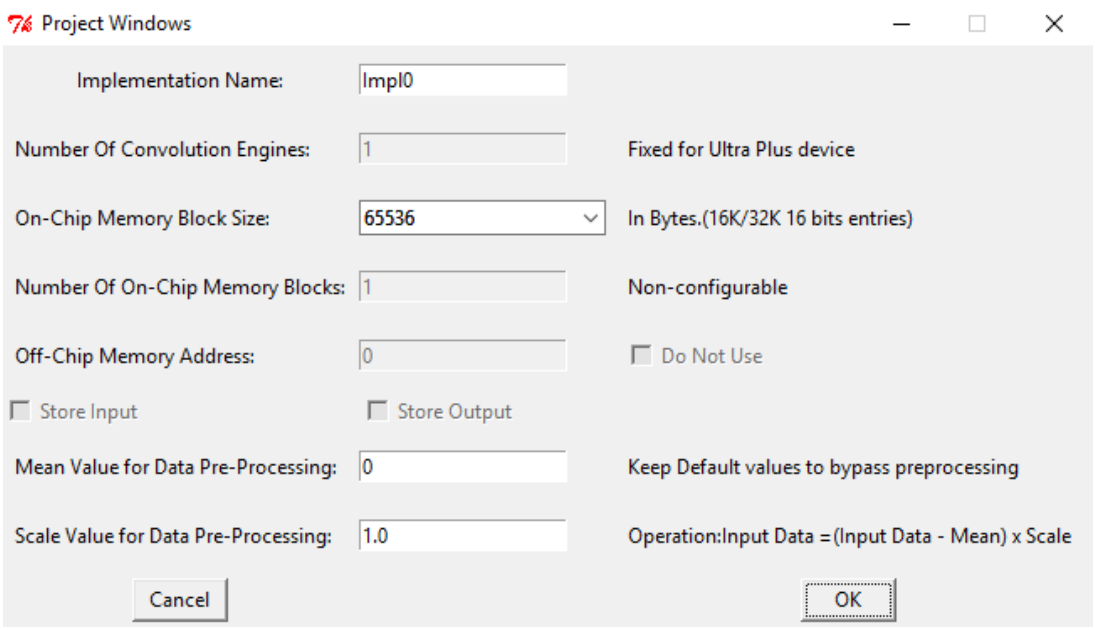

Figure 7.2. SensAI Project Settings Part 2

5. Note that this reference design requires fractional bit changes to fine-tune the accuracy of the design. After analyzing the network, edit the fractional bit for each layer. Figure 7.3 shows the change of the fractional bit.

Impl0

Blobs	Signed Data Format(Analyzed)	Stored Data Format(User Edit)	Required Memory Bytes	MAE_Simulation
data	5.10	11.4	16384	
fire1/conv3x3/	5.10	11.4	16384	
fire1/bn/batch	5.10	13.2	16384	
fire1/bn/batch	5.10	5.10	16384	
fire1/Relu	5.10	5.10	16384	
fire1/pool/Max	5.10	5.10	16384	
fire2/conv3x3/	7.8	15.0	16384	
fire2/bn/batch	7.8	13.2	16384	
fire2/bn/batch	7.8	13.2	16384	
fire2/Relu	7.8	13.2	16384	
fire3/conv3x3/	6.9	13.2	16384	
fire3/bn/batch	6.9	12.3	16384	
fire3/bn/batch	6.9	12.3	16384	
fire3/Relu	6.9	12.3	16384	
fire3/pool/Max	6.9	12.3	16384	
fire4/conv3x3/	6.9	13.2	16384	
fire4/bn/batch	6.9	11.4	16384	
fire4/bn/batch	6.9	12.3	16384	
fire4/Relu	6.9	12.3	16384	
fire5/conv3x3/	6.9	12.3	16384	
fire5/bn/batch	6.9	11.4	16384	
fire5/bn/batch	6.9	11.4	16384	
fire5/Relu	6.9	11.4	16384	
fire5/pool/Max	6.9	11.4	16384	
fire6/conv3x3/	5.10	11.4	16384	
fire6/bn/batch	5.10	10.5	16384	
fire6/bn/batch	5.10	11.4	16384	
fire6/Relu	5.10	11.4	16384	
fire6/pool/Max	5.10	11.4	16384	
logit/add	4.11	11.4	16384	

Figure 7.3. Fractional Bit Change

6. After changing the fractional bit, save the project file and reanalyze the design.
7. Click **Compile** to generate the Firmware file.

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Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Revision 1.0, September 2018

Section	Change Summary
All	Initial release.

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