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# Voltage regulator

## Goals

- Design a voltage regulator for positive voltages
- Understand efficiency and regulation of a regulator
- Appreciate some fine points of small signal “ground”
- Understand how to compensate errors due to opamp input bias currents

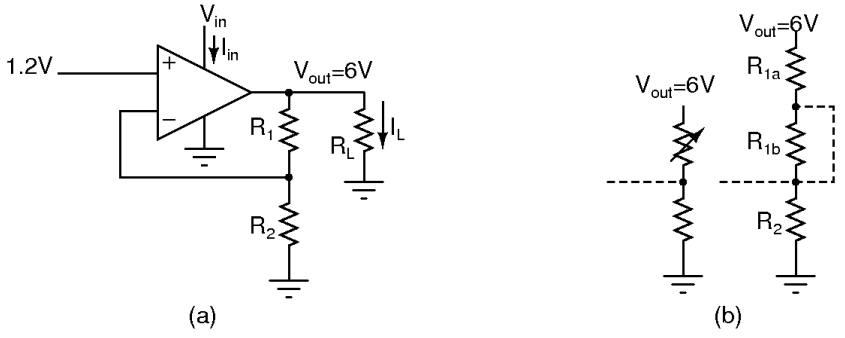
## Reference material

- Revisit problem 9 of this problem set [http://www.ee.iitm.ac.in/vlsi/_media/courses/ee3002_2014/ee3002prob8.pdf] from EE3002: Analog Circuits [http://www.ee.iitm.ac.in/vlsi/courses/ee3002_2014/start])

## Specifications

- $V_{in}$=9V, $V_{out}$=6V unless mentioned otherwise
- 1.2V reference voltage(from a dc source)

## Principle



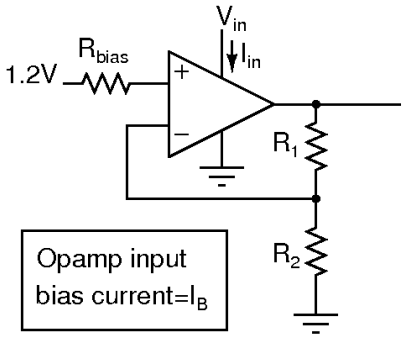

- A voltage regulator is simply a feedback driven voltage controlled voltage source shown above. The input is a temperature stable dc reference(from a bandgap reference, a Zener diode, or a string of forward biased

diodes). The feedback resistor can be made variable to have a variable supply such as the one on your bench. In your implementation, realize output voltages of 3V and 6V by shorting out a part of $R_1$ as shown above.

- The amplifier used in the voltage regulator need not be a general purpose opamp. It needs to meet the following criteria:
  - The efficiency of a regulator is $V_{out}I_{out}/V_{in}I_{in}$. $V_{out}$ and $V_{in}$ are given by the specifications. To maximize efficiency, $I_{out}$ should be close to $I_{in}$. i.e. the bias currents in the circuit must be minimized.
  - To minimize $V_{in}$ required to obtain a given $V_{out}$, the opamp should have the upper swing limit close to the supply rail. This is achieved by having a single transistor in the common emitter(or common source) configuration-i.e. a single saturation voltage drop-between $V_{in}$ and $V_{out}$. Such a regulator is known as a low dropout regulator, LDO for short(dropout = $V_{in}$-$V_{out}$).

- In your case, the "opamp" will be realized using bipolar transistors. Therefore, transistors in the input differential pair draw a bias current $I_B$. Determine the output voltage in presence of bias currents. How would you overcome this error?

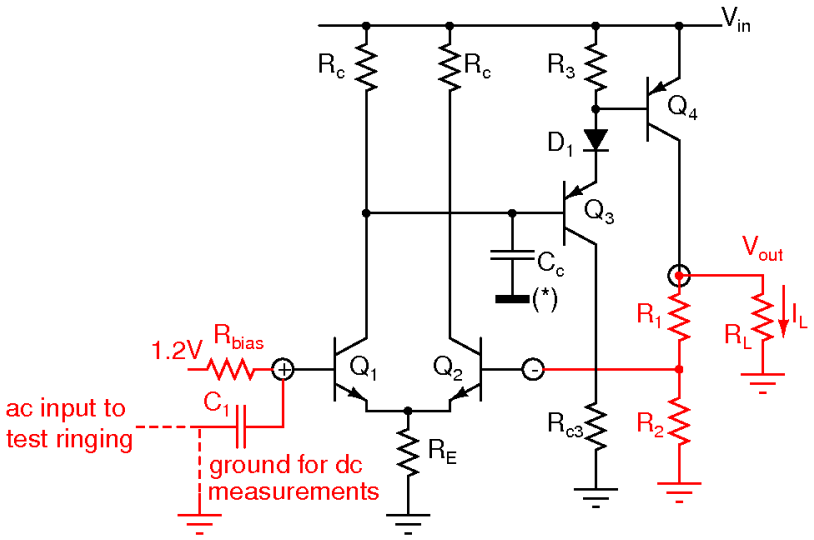
# Exercise




(c)

- The above figure shows a scheme for reducing error due to bias currents. What value will you set $R_{bias}$ to?

# Experiments




(*): small signal ground; where should this be connected?
components in red are external to the "opamp"

(d)

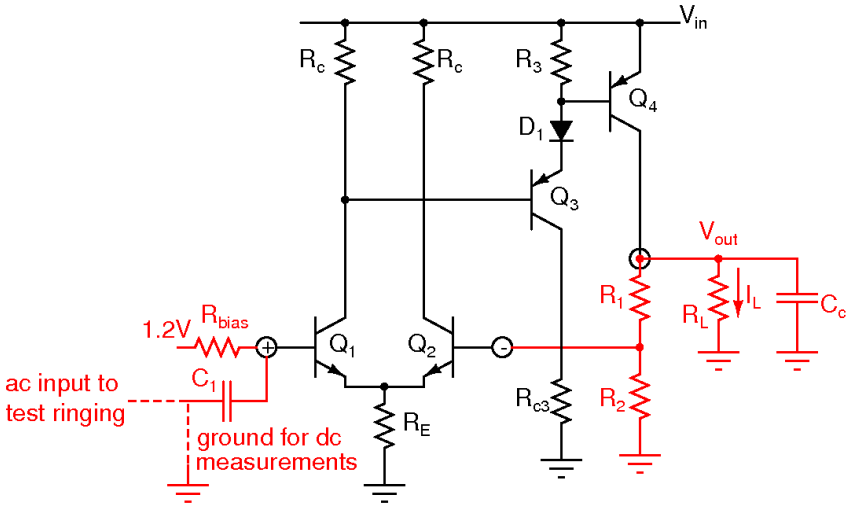
- The above figure shows the complete schematic of the opamp. $C_c$ is a compensation capacitor. In the small signal picture, $C_c$ should be conencted between the base of $Q_3$ and ground. Where should it be connected in the large signal picture? (Hint: think about what happens to the output voltage if there is a jump in the power supply voltage). You can use a diode connected transistor in place of $D_1$

- Design the circuit to meet the following requirements. For operating point calculations, you can assume $\beta=\infty$.
  - In no load condition($R_L=\infty$), quiescent currents through $Q_{1,2,3}$ and the feedback branch $R_1$,$R_2$ are equal
  - Quiescent $V_{CE3}$ should be 2 to 3V.
  - Efficiency when $R_L=125\Omega$ and $V_{out}=6V$ is $0.96*V_{out}/V_{in}$.
  - $C_c$ should be adjusted as described below.

- Optimizing the dc operating point: Calculate the resistor values to meet the specifications above. If you try to realize these exact values with series parallel combinations of resistors, the assembly can get quite messy. Therefore:
  - Use the nearest standard values available. At most, go for a combination of two resistors for each.
  - For the feedback network, use five identical resistors, with four in parallel or series as appropriate to realize the ratio accurately
  - Ensure that the collector resistances of $Q_{1,2}$ are identical.
  - Build the circuit, compensate it if necessary and measure the dc voltages $V_{c1,c2}$ at the collectors of $Q_{1,2}$.
  - If $V_{c1}$ is different from $V_{c2}$, the differential pair is not perfectly balanced. $Q_1$'s collector voltage is fixed by the dc operating point of the following stages. $Q_2$'s current needs to be reduced by $(V_{c1}-V_{c2})/R_c$.
  - To do this, measure the voltage $V_E$ at the emitter coupled node and adjust $R_E$ such that $V_E/R_{E,new} = V_E/R_E-(V_{c1}-V_{c2})/R_c$.
  - Again, use the nearest standard value if possible. Ignore mismatch between $V_{c1}$ and $V_{c2}$ if it is 100mV or less.

- Wire up the amplifier and apply a small signal square wave riding around 1.2V at the reference input and $R_L=\infty$. Does the amplifier settle without ringing? If not, compensate the loop using a capacitor $C_c$ as shown in the figure-connect it to the appropriate small signal ground determined above. Start from small values of $C_c$ and adjust the value to get 5% overshoot. Change $R_L$ to 125Ω. Does the ringing get better or worse? Why?

- Test the regulator with load(dc test):
  - Determine the output voltages for $R_L=\infty$, 2kΩ, 500Ω, 125Ω. For the last case, the resistor may become quite hot. Use a parallel or series combination of a few resistors of appropriate value to realize 125Ω.
  - Determine the output voltages for $V_{in}$=8V, 9V, 10V. Determine the line regulation $\Delta V_{out}/\Delta V_{in}$ for $R_L$=500Ω. The variation in output voltage with the input voltage is known as line regulation.
  - Determine the minimum $V_{in}$ required to get $V_{out}$=6V under full load(125Ω).
  - What happens if there is a load capacitor $C_L$ across $R_L$? Is there a value of $C_L$ beyond which the circuit oscillates?



(e)

- An alternative method for frequency compensation of the regulator is shown above. What is the required value of the compensation capacitor $C_c$? Determine the value as before. At which load condition will you do this($R_L=\infty$ or $R_L=125\Omega$) to cover all load conditions? LM2940 is compensated in this manner.
- Demonstrate the circuit with a 3V output.
- What is the reason for the relatively poor load regulation? Can you increase the loop gain to improve this? (Hint: bootstrapping may be used to increase the apparent load resistance of the differential amplifier stage. How would you implement it here?).

# Applications

- Linear voltage regulators, such as the ones on your bench are made of circuits like this one. They also include the voltage reference generator. The “pass transistor” $Q_4$ is of sufficient rating for the maximum output current(You may be able to see large pass transistors mounted on heatsinks on the backside of some of the power supplies in the lab). Multiple buffer stages may be required(such as $Q_3$) to drive the base current of $Q_4$. Usually the feedback loops have more stages for more gain. For tracking dual power supplies, there is effectively another feedback circuit that looks like an inverting amplifier with the positive $V_{out}$ as the input. On modern integrated circuits housing entire systems, like large portions of a radio, it is common to find even upto a dozen LDOs powering various blocks. LM2940 is an example of a commercially available LDO. Page 12 of the datasheet has the schematic diagram.

# Additional information

The choice of a 1.2V reference is not arbitrary. A temperature stable voltage reference can be realized using bipolar transistors. Its output equals 1.2V(= bandgap of silicon extrapolated to absolute zero). For more information about this, see

- Chapter 11, “Design of CMOS Analog Integrated Circuits”, Behzad Razavi.
- Problem 4 in this assignment [http://www.ee.iitm.ac.in/~nagendra/EE539/200801/assignments/hw08.pdf] of EE539.
- Analog IC Design [http://nptel.ac.in/courses/117106030/] on NPTEL. Lectures on voltage references.