

BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE , PILANI K. K. BIRLA Goa Campus
First Semester 2020 - 2021
CS F342 Computer Architecture
Lab - 4

Implement **single cycle datapath** for the following instructions.

ALU Control Unit : -

Input : ALUOp , Instruction[5:0]

Output : Operation

| ALUOp | Instruction | Operation |
|-------|-------------|-----------|
| | | |
| 00 | XXXXXX | 0010 |
| X1 | XXXXXX | 0110 |
| 1X | XX0000 | 0010 |
| | XX0010 | 0110 |
| | XX0100 | 0000 |
| | XX0101 | 0001 |
| | XX1010 | 0111 |

Control Circuit : -

Input : Instruction[31-26]

Output : RegDst , Branch , MemRead , MemtoReg , ALUOp , MemWrite , ALUSrc , RegWrite , Jump

| Instructions | RegDst | Branch | MemRead | MemToReg | ALUOp | MemWrite | ALUSrc | RegWrite | Jump |
|--------------|--------|--------|---------|----------|-------|----------|--------|----------|------|
| | | | | | | | | | |
| 000000 | 1 | 0 | 0 | 0 | 10 | 0 | 0 | 1 | 0 |
| 001000 | 0 | 0 | 0 | 0 | 00 | 0 | 1 | 1 | 0 |
| 100011 | 0 | 0 | 1 | 1 | 00 | 0 | 1 | 1 | 0 |
| 101011 | x | 0 | 0 | x | 00 | 1 | 1 | 0 | 0 |
| 000100 | x | 1 | 0 | x | 01 | 0 | 0 | 0 | 0 |
| 000010 | x | 0 | x | x | xx | x | x | x | 1 |

ALU :-

Input : ALUIn1 , ALUIn2

Output : Zero , ALUout

| Instruction | ALUout |
|-------------|--------------------------------|
| | |
| 0000 | ALUIn1 & ALUIn2 |
| 0001 | ALUIn1 ALUIn2 |
| 0010 | ALUIn1 + ALUIn2 |
| 0110 | ALUIn1 - ALUIn2 |
| 0111 | If(ALUIn1 < ALUIn2) then 32'd1 |
| | If(ALUIn1 > ALUIn2) then 32'd0 |
| 1100 | ~(ALUIn1 ALUIn2) |

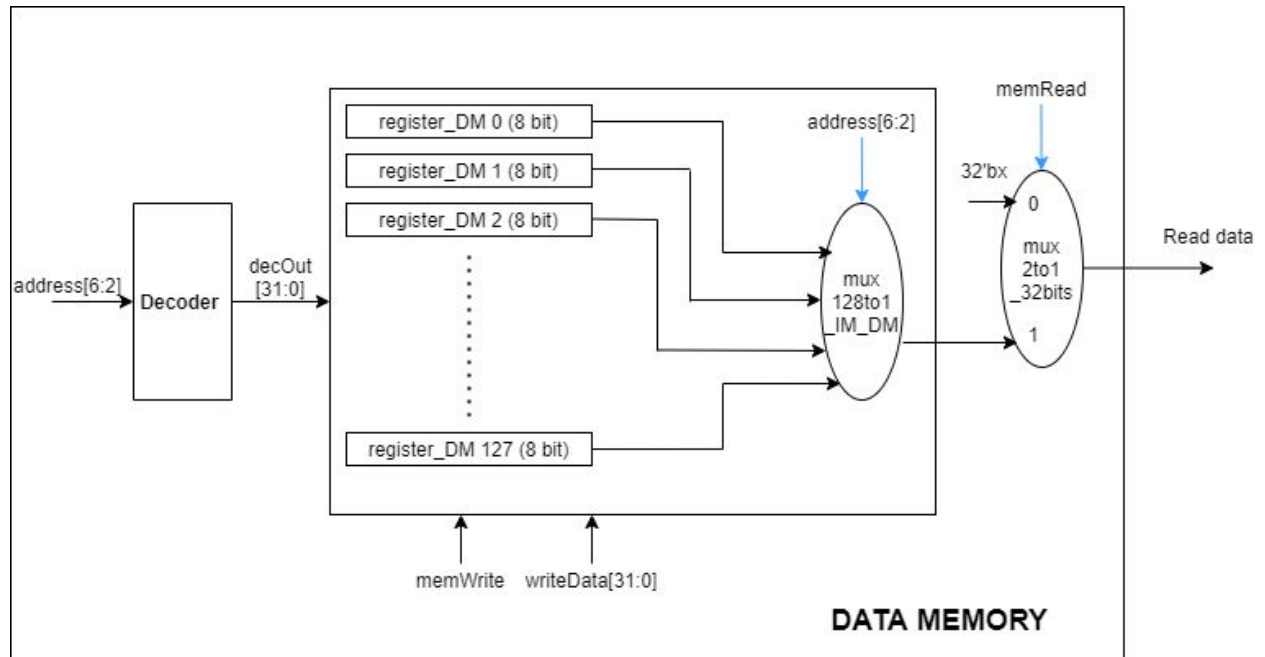
| ALUOut | Zero |
|----------|------|
| | |
| 32'b0 | 1 |
| != 32'b0 | 0 |

Data Memory :-

Input : Address[6:2] , Write Data , memWrite , memRead, clk , reset

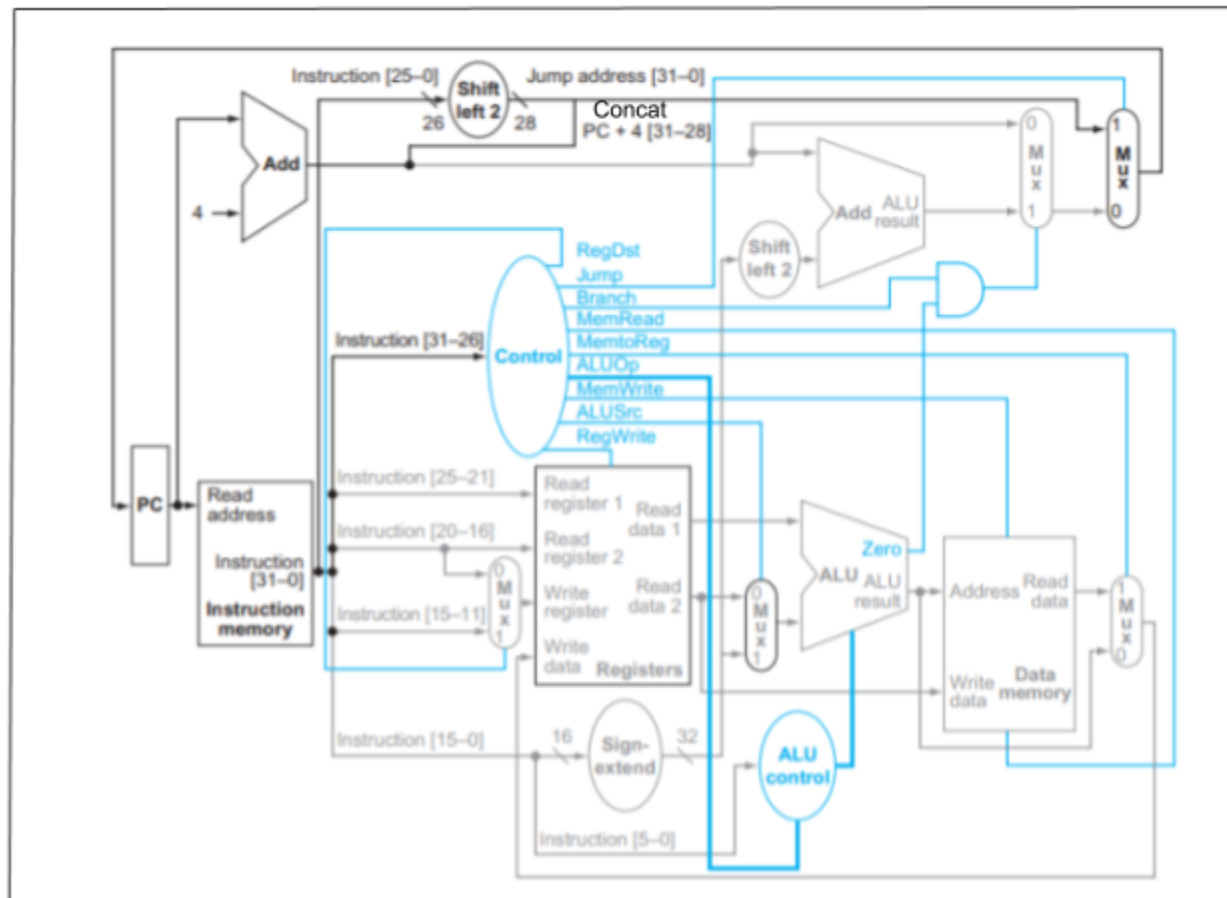
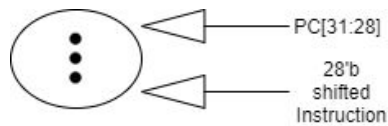
Output : Read Data

[Data Memory circuit diagram](#) :-



Single cycle datapath circuit diagram([Circuit diagram](#)) :-

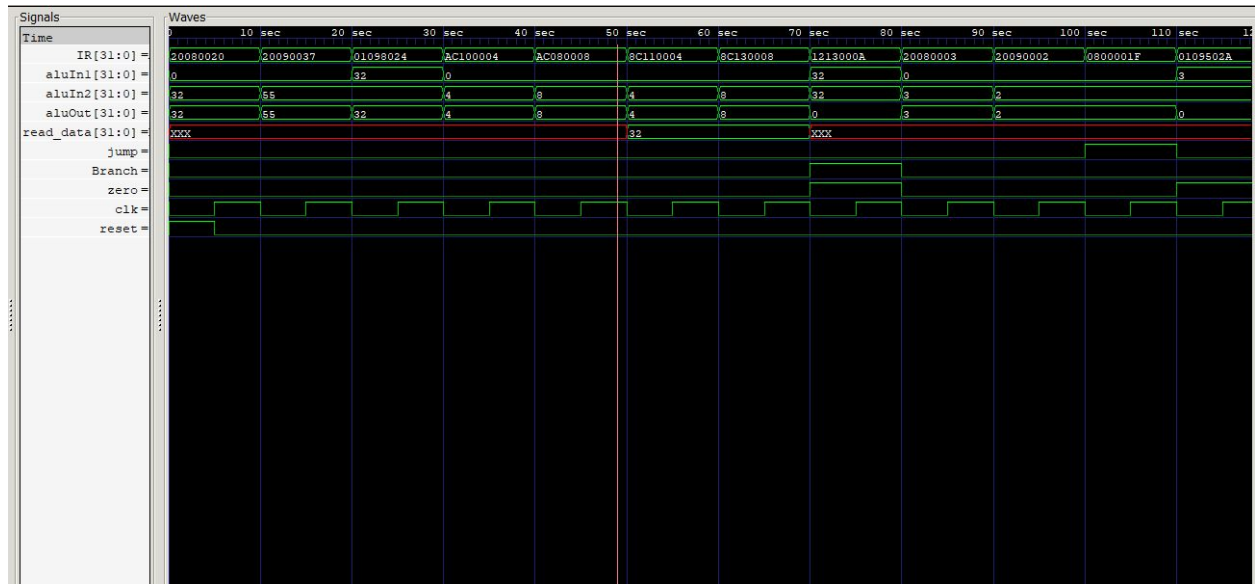
Note:- The [31:28] bits of PC+4 are being concatenated with the left shifted 28 bits of the Instruction. The zoomed in diagram is as follows:



↑ ↑
Clk Reset

Expected Outcome ([Expected Outcome Link](#)):-

1. Convert IR[31:0] to hexadecimal base for comparison.
2. Rest all are on decimal base.



Marking Scheme:

- 2 Marks - IR[31:0]
- 1 Mark - aluIn1 , aluIn2 , aluOut
- 1 Mark - read_data

Submission Method:

1. Save your singleCycle.v source file as **<Your ID>_Lab4.v**
NOTE: Change yourID to your 13 digit BITS ID in the testbench
2. Save the vcd dump file generated as **<Your ID>_Lab4.vcd** (this will already be called **<Your ID>_Lab4.vcd** since you have changed it in the testbench)
3. Save your GTKWave output as **<Your ID>_Lab4.gtkw** using the 'Save As' option in File->Write

Create a **zip file** containing the above 3 files and submit it on Quanta. **Do not create archives in other formats (rar, tar.gz etc).**

Once uploaded on Quanta, remember to **submit for grading**. **Do not leave it as a draft.**

NOTE: In case you are using a case statement with a don't care, use casex instead of case. For example casex xx000 instead of case xx000.