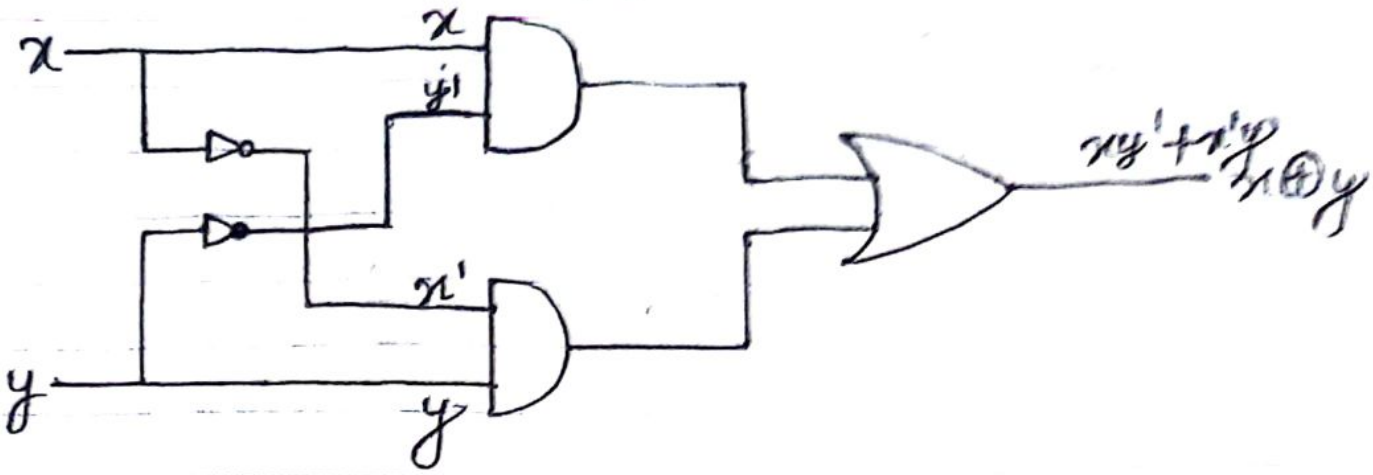
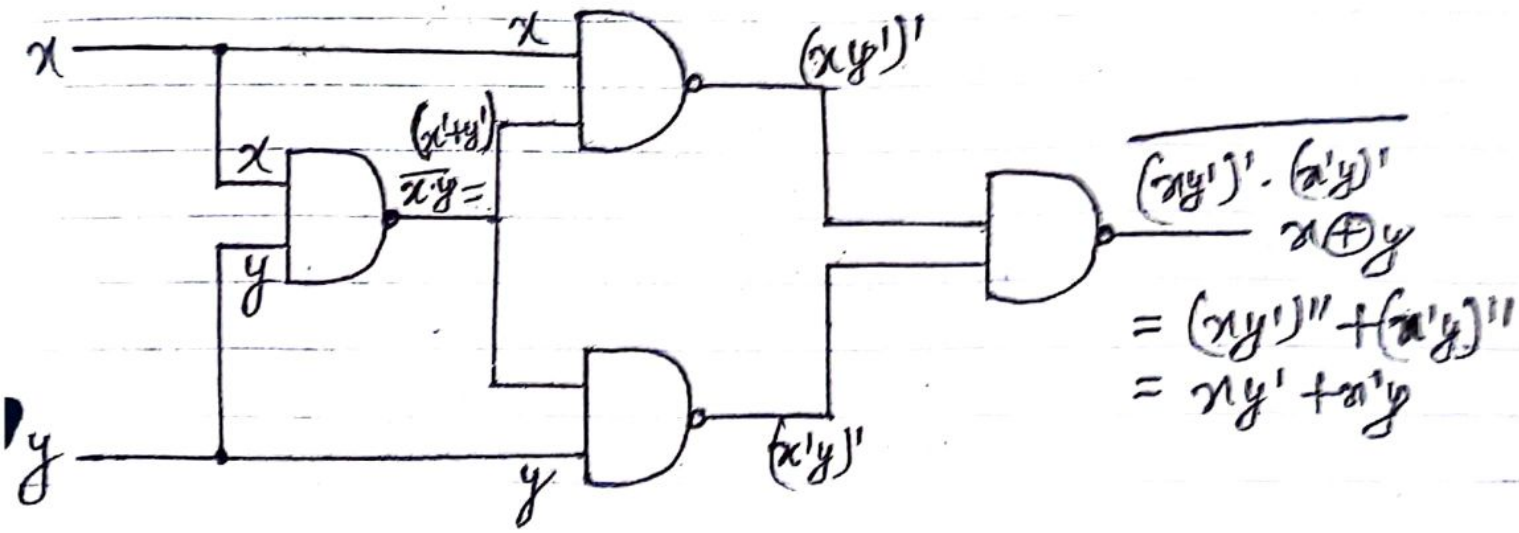


Fig: Implementation of XOR with AND-OR NOT gates



Error detection code:

An error detection code is a binary code that detects digital errors during transmission. The detected errors cannot be corrected but their presence is indicated. If error occur frequently at random, the particular erroreous information is transmitted again.

The most common error detection code used is the parity bit. A parity bit is an extra bit include with a binary message to make the total number of 1's either odd or even.

During transfer of information from one location to another, the parity bit is handled as follows:

At the sending end, the message is applied to parity generator, where the required parity bit is generated. The message, including the parity bit, is transmitted to its destination.

At the receiving end, all the incoming bits are applied to a parity checker that checks the proper parity adopted (odd or even). An error is detected if the checked parity does not confirm (same) to the adopted parity. The parity method detects the presence of one, three or any odd number of errors. An even number of errors is not detected.

There are two types of parity generator as:

(1) Even parity generator.
(2) Odd parity generator.

The circuit that generates the parity bit in the transmitter is called parity generator.

The circuit that checks the parity in the receiver is called parity checker.

(1) Even parity generator :

Let us consider that the three bit data is to be transmitted with an even parity b The three inputs are A, B & C and P is the output parity bit. In even parity generator, 1 is placed in the parity bit in order to make the total number of 1's even.

3 bit message			Even parity bit (P)	
A	B	C	P	
0	0	0	0	0
0	0	1	1	1
0	1	0	1	2
0	1	1	0	3
1	0	0	1	4
1	0	1	0	5
1	1	0	0	6
1	1	1	1	7

The K-map simplification for 3-bit messag even parity generator is,

A \ BC	B'C'	B'C	BC	BC'
A'	0 0	1 1	0 3	1 2
A	1 4	0 5	1 7	0 6

$$P = A'B'C + A'BC' + AB'C' + ABC$$
$$= A'(B'C + BC') + A(B'C' + BC)$$
$$= A'(B \oplus C) + A\overline{(B \oplus C)}$$
$$= A'x + Ax' \quad (\text{Assume } B \oplus C = x)$$
$$= A \oplus x$$
$$= A \oplus B \oplus C$$

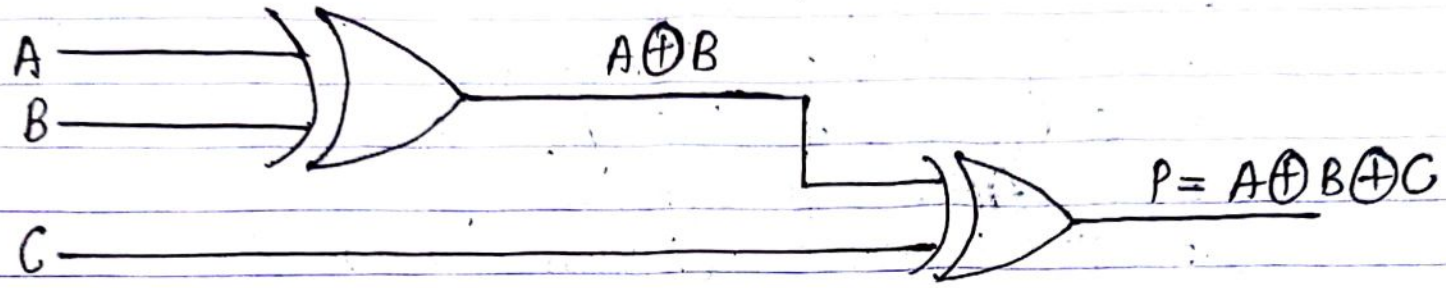


Fig: Logic diagram of even parity generator

(2) Odd parity generator:

Let us consider that the 3-bit data is to be transmitted with an odd parity bit. The three inputs are A, B and C and P is the output parity bit. The total number of 1 must be odd in odd parity generator.

3 bit message			Odd parity bit (P)
A	B	C	P
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1

The K-map of above table is

A \ BC	B'C'	B'C	BC	BC'
A'	1	0	1	0
A	0	1	0	1

$$P = A'B'C' + A'BC + AB'C + ABC'$$
$$= A'B'C' + ABC' + A'BC + AB'C$$
$$= C'(A'B' + AB) + C(A'B + AB')$$
$$= C'\overline{(A \oplus B)} + C(A \oplus B)$$
$$= C'Y' + CY \quad (\text{Assume } A \oplus B = Y)$$
$$= C \odot Y$$
$$= C \odot A \oplus B$$
$$= A \oplus B \odot C$$

$\therefore P = A \oplus B$ EX-NOR C

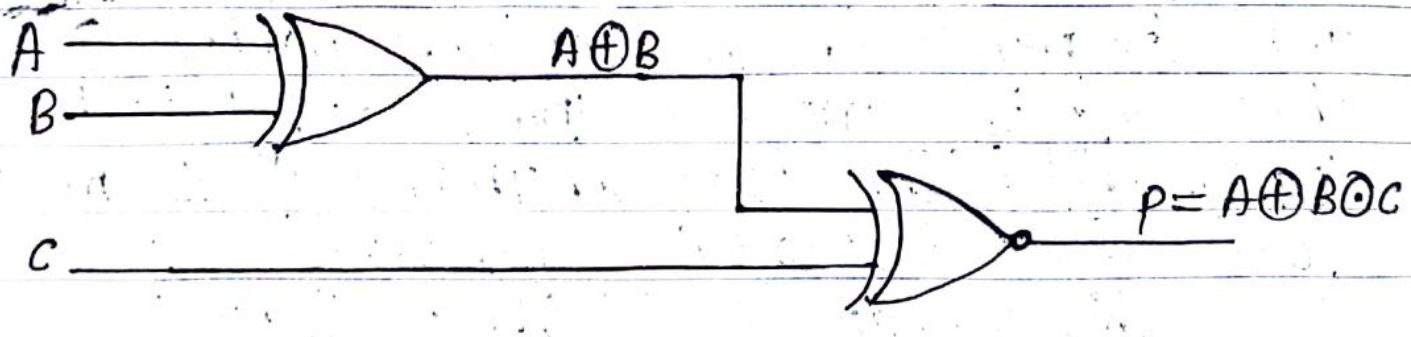


Fig: Logic diagram of odd parity generato

Parity check or parity checker:

Parity check is a logic circuit that checks for possible errors in the transmission. This circuit can be an even parity checker or odd parity checker depending on the type of parity generated at the transmission and when this circuit is used as even parity checker, the number of 1 must be even. When used as odd parity checker, the number of 1 must be odd.

There are two types of parity checker:-

(1) Even parity checker
(2) odd parity checker

(1) Even parity checker:

Consider that three bit input message along with even parity bit is generated at the transmitting end. These 4 bits are applied as input to the parity checker circuit which checks the possibility of error on the data. Since, the data is transmitted with even parity, four bits received at circuit must have an even number of 1's. If any error occurs, the received message. Consider of odd number of 1s. The output of the parity checker is denoted by PEC (Parity Error Check).

The table below shows the truth table for the even parity checker in which PEC = 1 if the error occurs and PEC = 0 if no error occurs.

4-bit received message				Parity error check
A	B	C	P	PEC
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

The truth table can be simplified using k-map as:-

AB \ CP	C'P'	C'P	CP	CP'
A'B'	0	1	0	1
A'B	1	0	1	0
AB	0	1	0	1
AB'	1	0	1	0

$$PEC = A'B'C'P + A'B'CP' + A'BC'P' + A'BCP + ABC'P + ABCP' + AB'C'P' + AB'CP$$

$$= A'B'(C'P + CP') + A'B(C'P' + CP) + AB(C'P + CP') + AB'(C'P' + CP)$$

$$= A'B'(C \oplus P) + A'B(\overline{C \oplus P}) + AB(C \oplus P) + AB'(\overline{C \oplus P})$$

$$= C \oplus P(A'B' + AB) + (\overline{C \oplus P})(A'B + AB')$$

$$= (C \oplus P)(\overline{A \oplus B}) + (\overline{C \oplus P})(A \oplus B)$$

$$= X \cdot \overline{Y} + \overline{X} \cdot Y \quad (\text{Assume, } C \oplus P = X,\ A \oplus B = Y)$$

$$= X \oplus Y$$

$$= C \oplus P \oplus A \oplus B$$

$$= A \oplus B \oplus C \oplus P$$

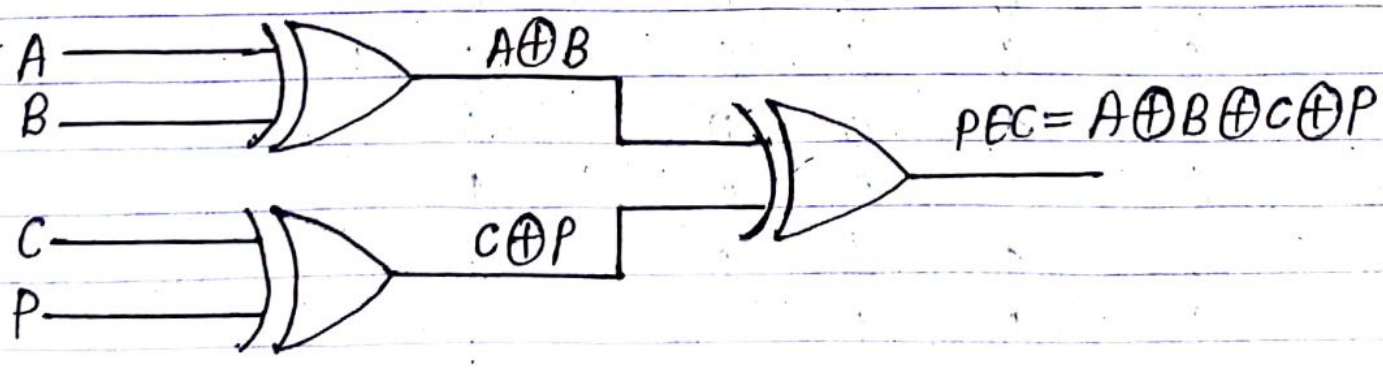


Fig: Logic diagram of even parity checker

(2) Odd parity checker:

Consider that a three bit message along with odd parity bit is transmitted at the transmitting end. Odd parity checker circuit receives these 4bits and checks whether any error are present in the data.

If the total number of 1s in the data is odd, then it indicates no error, whereas if the total number of 1s is even then it indicates the error. Since, the data is transmitted with odd parity at transmitting end.

The figure shows the truth table for odd parity checker in which PEC=1 if error occured and PEC=0 if no error occurs.

A	B	C	P	PEC
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

(2) Odd parity checker:

Consider that a three bit message along with odd parity bit is transmitted at the transmitting end. Odd parity checker circuit receives these 4 bits and checks whether any error are present in the data.

If the total number of 1s in the data is odd, then it indicates no error, whereas if the total number of 1s is even then it indicates the error. Since, the data is transmitted with odd parity at transmitting end.

The figure shows the truth table for odd parity checker in which PEC=1 if error occured and PEC=0 if no error occurs.

A	B	C	P	PEC
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

Using K-map simplification, we have

AB \ CP	C'P'	C'P	CP	CP'
A'B'	1	0	1	0
A'B	0	1	0	1
AB	1	0	1	0
AB'	0	1	0	1

$$PEC = A'B'C'P' + A'B'CP + A'BC'P + A'BCP' + ABC'P' + ABCP + AB'C'P + AB'CP'$$

$$= A'B'(C'P' + CP) + A'B(C'P + CP') + AB(C'P' + CP) + AB'(C'P + CP')$$

$$= A'B'\overline{(C \oplus P)} + A'B(C \oplus P) + AB\overline{(C \oplus P)} + AB'(C \oplus P)$$

$$= \overline{(C \oplus P)}(A'B' + AB) + (C \oplus P)(A'B + AB')$$

$$= \overline{(C \oplus P)}\,\overline{(A \oplus B)} + (C \oplus P)(A \oplus B)$$

Assume, $C \oplus P = X$, $A \oplus B = Y$

Then,

$$PEC = X'Y' + XY$$
$$= X \odot Y$$
$$= X \text{ EX-NOR } Y$$
$$= C \oplus P \odot A \oplus B$$
$$= A \oplus B \odot C \oplus P$$

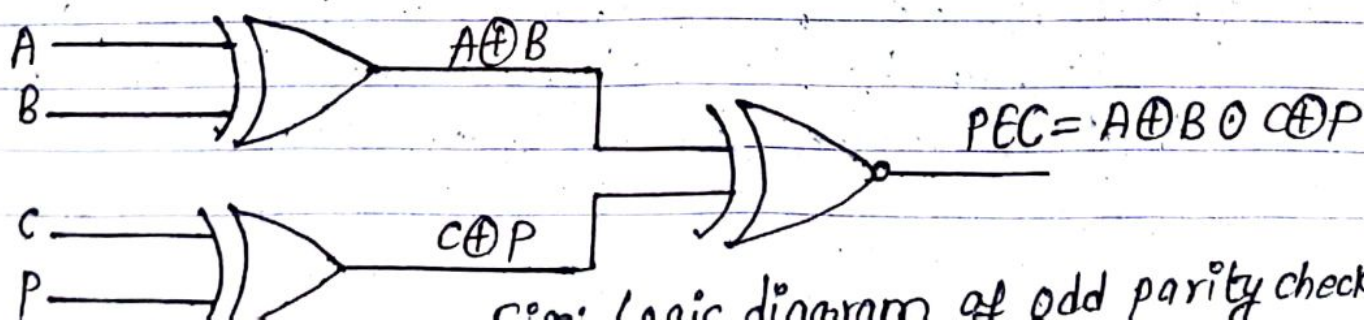


Fig: Logic diagram of odd parity checker