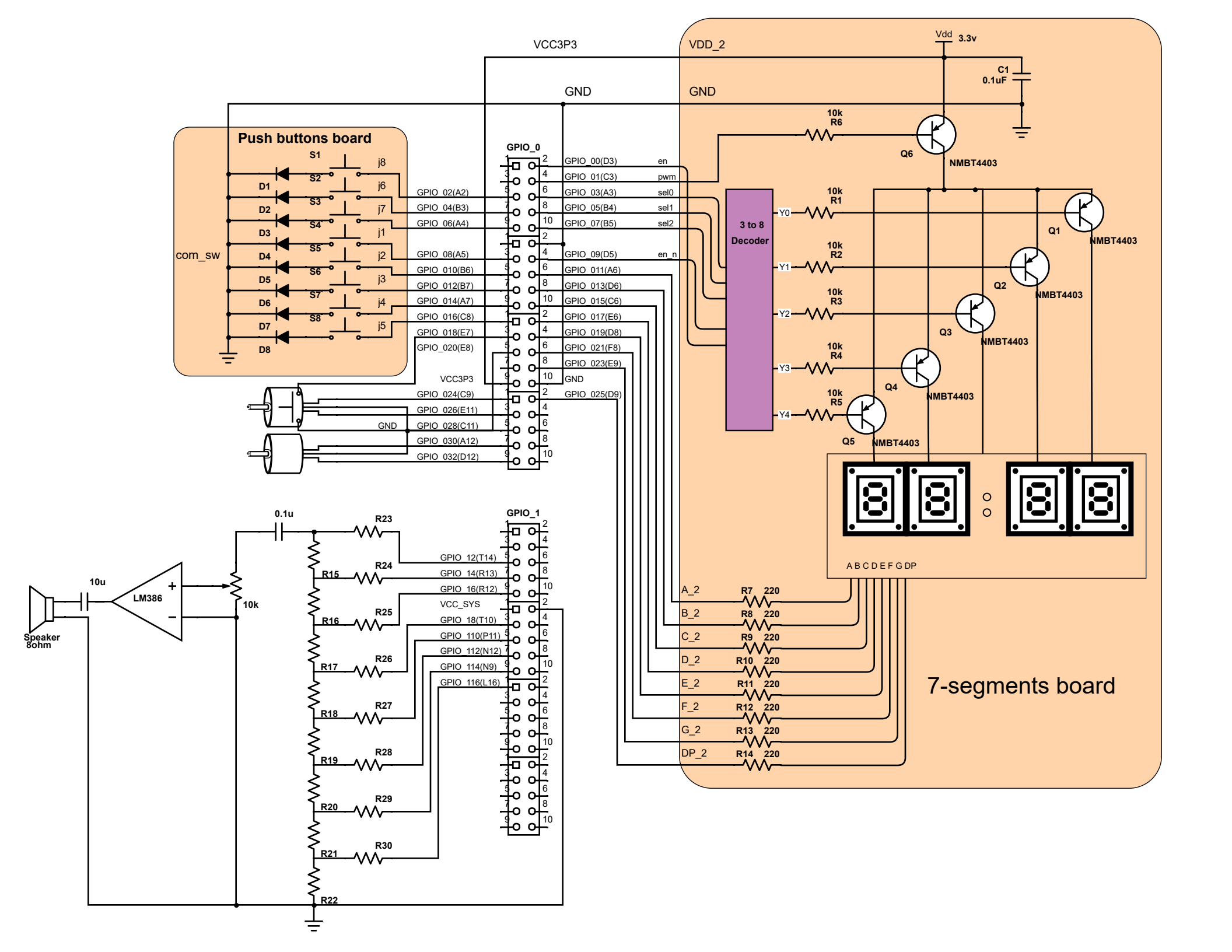
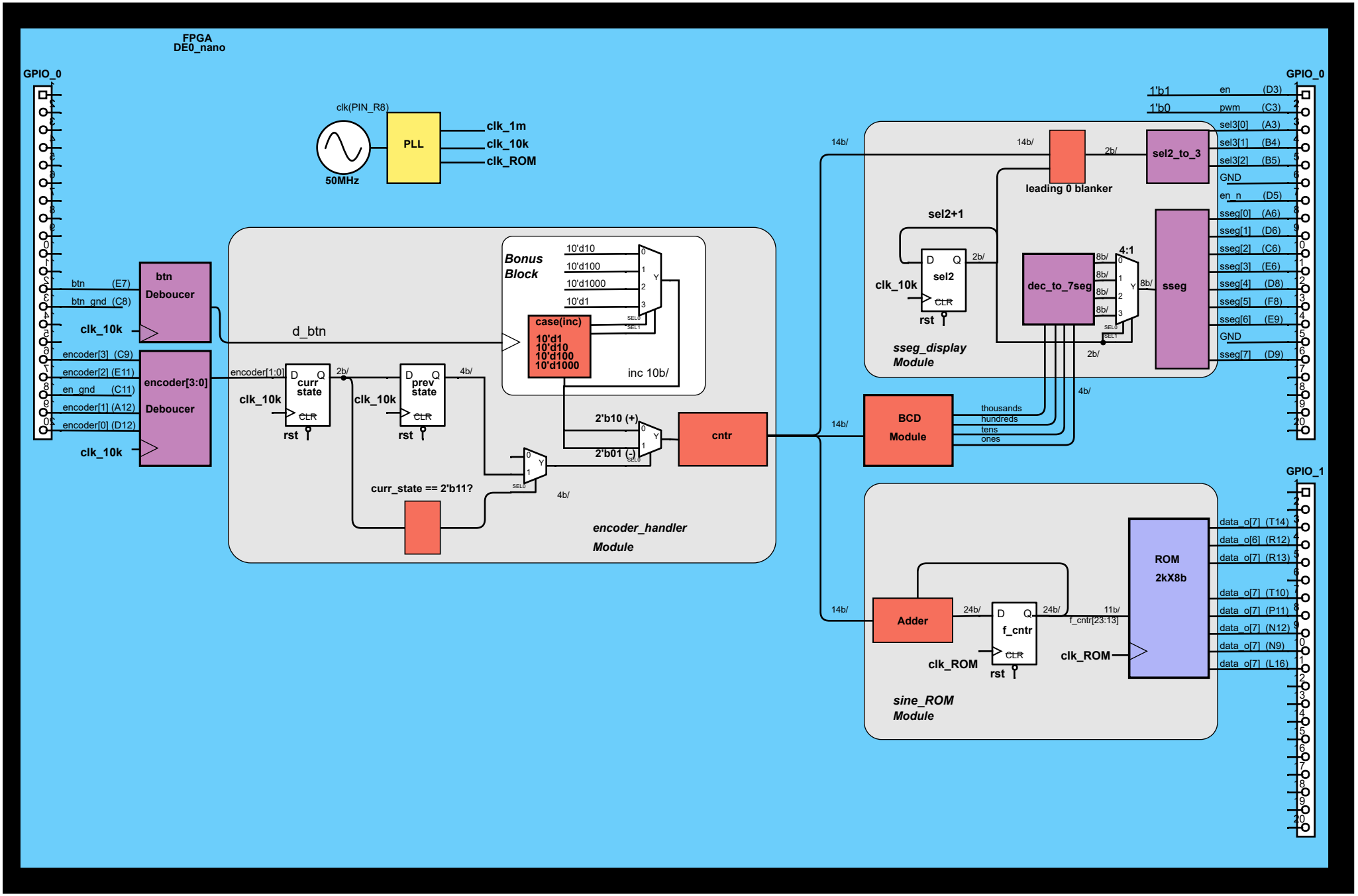

VCC3P3
GND
VDD_2
GND
Vdd 3.3v
C1
0.1uF
Push buttons board
com_sw
S1
S2
S3
S4
S5
S6
S7
S8
D1
D2
D3
D4
D5
D6
D7
D8
j8
j6
j7
j1
j2
j3
j4
j5
GPIO_0
GPIO_02(A2)
GPIO_04(B3)
GPIO_06(A4)
GPIO_08(A5)
GPIO_010(B6)
GPIO_012(B7)
GPIO_014(A7)
GPIO_016(C8)
GPIO_018(E7)
GPIO_020(E8)
VCC3P3
GND
GPIO_024(C9)
GPIO_026(E11)
GPIO_028(C11)
GPIO_030(A12)
GPIO_032(D12)
GPIO_00(D3)
GPIO_01(C3)
GPIO_03(A3)
GPIO_05(B4)
GPIO_07(B5)
GPIO_09(D5)
GPIO_011(A6)
GPIO_013(D6)
GPIO_015(C6)
GPIO_017(E6)
GPIO_019(D8)
GPIO_021(F8)
GPIO_023(E9)
GND
GPIO_025(D9)
en
pwm
sel0
sel1
sel2
en_n
3 to 8
Decoder
Y0
Y1
Y2
Y3
Y4
10k
R6
10k
R1
10k
R2
10k
R3
10k
R4
10k
R5
Q6
NMBT4403
Q1
NMBT4403
Q2
NMBT4403
Q3
NMBT4403
Q4
NMBT4403
Q5
NMBT4403
A B C D E F G DP
A_2
B_2
C_2
D_2
E_2
F_2
G_2
DP_2
R7 220
R8 220
R9 220
R10 220
R11 220
R12 220
R13 220
R14 220
7-segments board
0.1u
10u
LM386
10k
Speaker
8ohm
GPIO_1
R23
R24
R25
R26
R27
R28
R29
R30
R15
R16
R17
R18
R19
R20
R21
R22
GPIO_12(T14)
GPIO_14(R13)
GPIO_16(R12)
VCC_SYS
GPIO_18(T10)
GPIO_110(P11)
GPIO_112(N12)
GPIO_114(N9)
GPIO_116(L16)


FPGA
DE0_nano
GPIO_0
GPIO_1
clk(PIN_R8)
50MHz
PLL
clk_1m
clk_10k
clk_ROM
btn (E7)
btn_gnd (C8)
btn Deboucer
encoder[3] (C9)
encoder[2] (E11)
en_gnd (C11)
encoder[1] (A12)
encoder[0] (D12)
encoder[3:0] Deboucer
d_btn
encoder[1:0]
curr state
prev state
rst
Bonus Block
10'd10
10'd100
10'd1000
10'd1
case(inc)
10'd1
10'd10
10'd100
10'd1000
inc 10b/
2'b10 (+)
2'b01 (-)
cntr
curr_state == 2'b11?
encoder_handler Module
14b/
2b/
4b/
BCD Module
thousands
hundreds
tens
ones
leading 0 blanker
sel2_to_3
sel2+1
sel2
dec_to_7seg
4:1
8b/
sseg
sseg_display Module
1'b1
1'b0
en (D3)
pwm (C3)
sel3[0] (A3)
sel3[1] (B4)
sel3[2] (B5)
GND
en_n (D5)
sseg[0] (A6)
sseg[1] (D6)
sseg[2] (C6)
sseg[3] (E6)
sseg[4] (D8)
sseg[5] (F8)
sseg[6] (E9)
GND
sseg[7] (D9)
Adder
24b/
f_cntr
11b/
f_cntr[23:13]
ROM 2kX8b
data_o[7] (T14)
data_o[6] (R12)
data_o[7] (R13)
data_o[7] (T10)
data_o[7] (P11)
data_o[7] (N12)
data_o[7] (N9)
data_o[7] (L16)
sine_ROM Module