Mid-term project
ECE 471

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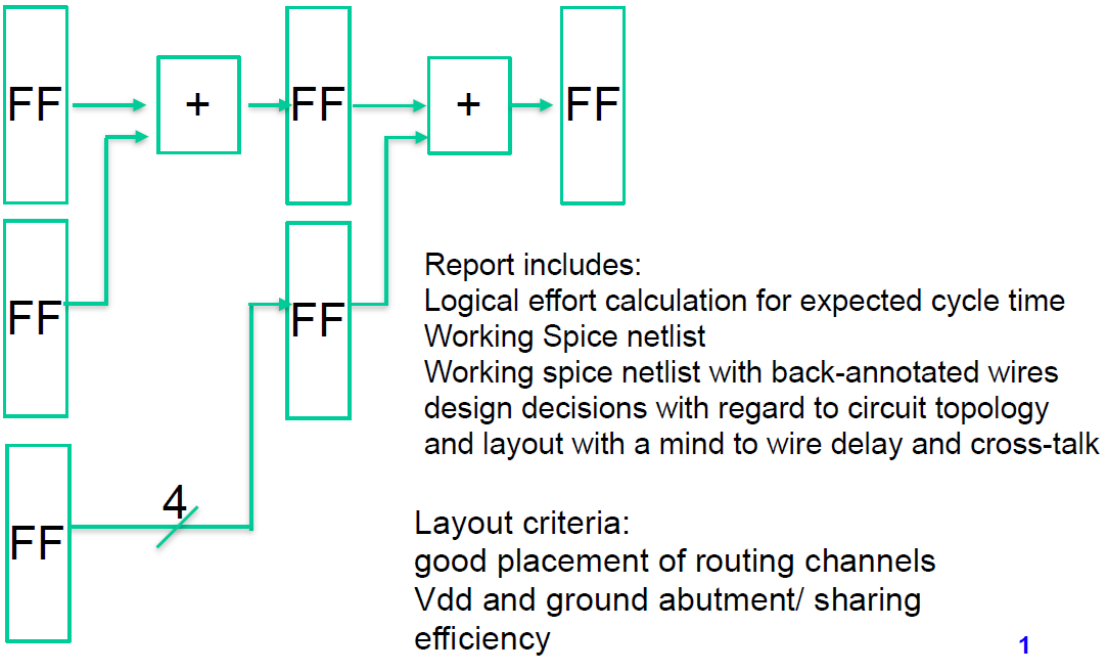
LVS and DRC correct 4 bit adder design



1. Logical effort and expected maximum clock rate:
   According to my assignment, Beta should be 2.5, total layout W/L ratio is about 1. Therefore Width of my PMOS is 20 λ and NMOS is 20 λ. L is set to 0.08um, 2*λ. Since we are using 90nm process and the gate has 10nm overlapping, λ = 40nm. Thus PMOS sizes 25*40nm, NMOS sizes 20*40nm. **Total NAND gate size** is

$$25 * 40nm + 20 * 40\ nm = 1800\ nm.$$

   Longest logical path in my design is from the first bit inputs to carry out at the highest bit.

My NAND2 gate individual Logical effort, according to the sizing equation, is

$$\frac{\text{beta}+2}{\text{beta}+1}=\frac{2.5+2}{2.5+1}=\frac{9}{7}$$

Total Logical effort (L)

3+2+2+2+2 = 11 NAND2 gates

$$(\frac{9}{7})^{11}$$

Branching effort (B) = 2 * 2 = 4 two branching happened at two XOR gate in full-adder.

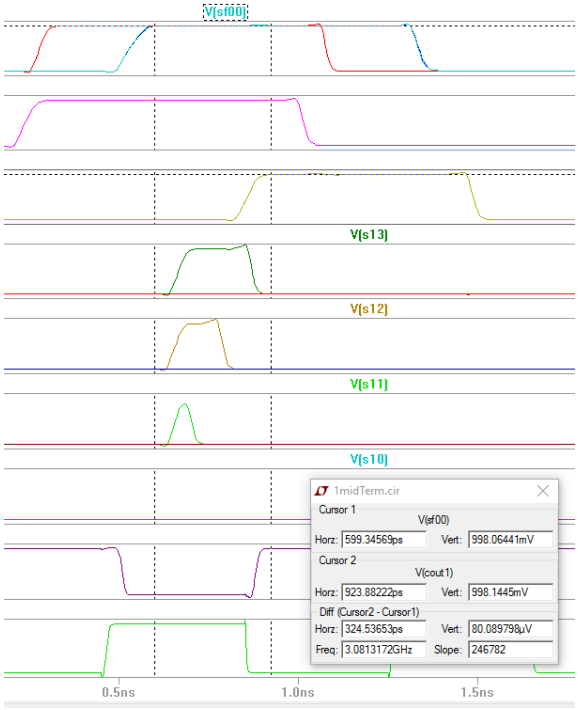
Electrical effort (E) = 1, since input and output are two identical Flip-flops.

Total path effort = L*B*E = 15.87 * 4 * 1 = 63.48

Intrinsic Delay ≈ D_{inc} = 12ps, from LTspice fanout vs. delay measurement

Path Delay = $\left(11 * \sqrt[11]{63.48}+2*11\right) * 12\text{ps} = (16.04 + 22) * 12\text{ps} = 456.5\text{ps}$

Path delay measured from LTspice is showed in the following picture.



Left cursor is located at first adder flip-flop output reach to 1. Second cursor is located at second adder carry out reach the final output 1. The difference from those two is 324.5ps which is less than our expected path delay by 28.9%.

The expected maximum clock rate is limited by one adder path delay plus one D-FlipFlop. The adder path delay is calculated above is 456.5ps, the D-FlipFlop is

Total Path Effort = LE * BE * EE = $(\frac{9}{7})^4$ * 2 * 1 = 5.47

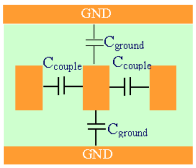
Delay = $\left(4 * \sqrt[4]{5.47}+2*4\right) * 12ps = 169.4ps$

Thus the minimum clock period is (456.5ps + 169.4ps) * 2= 1251.78ps

The expected maximum clock rate is 800MHz.

The LTspice simulation found the D-FlipFlop delay as 99.5ps. The clock maximum rate is calculated as 1.18GHz. The test result shows the maximum clock is the 1.25GHz.

CrossTalk:
The longest wire in the layout is the clock from the pin input to the most far D-FF is 69.2um in length.
W is 10 * 40nm = 0.400um
S is 4 * 40nm = 0.160um
The rest value keep defaults



Dimensions	RLC	RLC (/mm)
W = 0.400 um s = 0.160 um l = 69.2 um t = 0.20 um h = 0.20 um K = 2.2	R = 19.029 Ohm L = 0.082 nH M12 = 0.062 nH M13 = 0.053 nH M14 = 0.047 nH (k12 = 0.756 k13 = 0.646 k14 = 0.573) Cground = 3.6774956 fF Ccouple = 2.1544728 fF Ctotal = 11.6639368 fF	R = 274.985549132948 Ohm/mm L = 1.1849710982659 nH/mm Cg = 53.143 fF/mm Cc = 31.134 fF/mm Ctotal = 168.554 fF/mm

- **Resistance (R)**

$$R = \frac{\rho \cdot l}{w \cdot t}$$. For Cu: resistivity rou = 2.2 uohm-cm; For Al: resistivity rou=3.3 uohm-cm.

- **Inductance (L)**

$$L_s = \frac{\mu_0 \cdot l}{2\pi}\left[\ln\left(\frac{2l}{w+t}\right) + \frac{1}{2} + \frac{0.22(w+t)}{l}\right], \quad M = \frac{\mu_0 \cdot l}{2\pi}\left[\ln\left(\frac{2l}{d}\right) - 1 + \frac{d}{l}\right],$$

mu0 = 4 Pi x 10^{-7} H/m; mu0/Pi = 0.4nH/mm; d is the center-to-center distance between two wires.

- **Capacitance (C)**

[Shyh-Chyi Wong, Winbond TSM, Feb2000]

C_{total}: total capacitance of wire

$C_t = 2C_g + 2C_c$

C_g : area and fringe flux to the underlying plane

$$C_g = \varepsilon\left[\frac{w}{h} + 2.04\left(\frac{s}{s+0.54h}\right)^{1.77} \cdot \left(\frac{t}{t+4.53h}\right)^{0.07}\right]$$

C_c: coupling capacitance

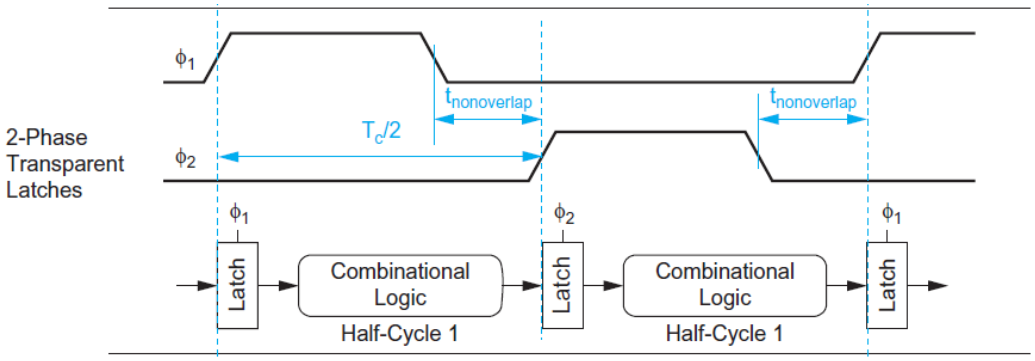
$$C_c = \varepsilon\left[1.41\frac{t}{s}e^{-\frac{4s}{s+8.01h}} + 2.37\left(\frac{w}{w+0.31s}\right)^{0.28} \cdot \left(\frac{h}{h+8.96s}\right)^{0.76} \cdot e^{-\frac{2s}{s+6h}}\right]$$

2. Design decisions:
   Using NAND2 gate for all of the other logic gates. One bit adder contains 9 NAND2 gates. 1-bit D-type flip-flop contains 4 NAND2 gates.

   My design implemented with NAND2 gate mostly. Reasons for doing so are varied. One is the NAND2 gate is cheapest among all the gates and easy to acquire from most of companies. Another reason is because the size of the PMOS and NMOS in NAND2 are the same after sizing according to their different strengths to source voltage. Same 4 transistors NOR gate will be larger than NAND gate on CMOS. And the logic effort of a NOR gate is larger than NAND gate as well. The other reason is those NAND2 gates are able to stack easily horizontally to make the layout design neat and clean, possibly reducing power consummation by saving wire length.

   I use this D-type flip-flop instead of latches in the following graph.

   Clock cycle implementation:



   My clock source split into two clocks, clk and _clk. Clk in charge of turning on first and third D-FF, _clk in charge of turning on second D-FF. For my design, t nonoverlap ~= 0. In this design, one set of data can be load and calculated between 1 full period of clock cycle and be presented at the third D-FF when the second clock cycle kicks in. The minimum interval for each set of data will be half cycle of clk period. We can maximum the performance by reducing the clock period to have _clk rising edge right after when cout, the longest logic path in adder, is calculated.

3. Directions and notes for navigating your <adder>.jelib and spice nettles file
   Electric:
   3sum is the top level layout without clk handler. It calls the cell instance of 1 bit adder and 1 bit D-FlipFlop from other groups.
   Total layout size is

$$926 * 40nm * 944 * 40\ nm = 1398.6um^2.$$

$$The\frac{W}{L}ratio = 1.0194$$

   Layout error rate is 1.9% which is under 5% requirements.