UNIVERSITY OF SOUTHERN CALIFORNIA
USC VITERBI SCHOOL OF ENGINEERING
MING HSIEH DEPARTMENT OF ELECTRICAL ENGINEERING

EE 348: FINAL EXAMINATION #3 (OPEN NOTES, HOMEWORK) — **MAY 08, 2007 11:00-TO-1:00**

PROBLEM #1: *(45%)*

Except for possible differences in gate aspect ratios, all transistors in the two-stage differential amplifier of Figure (E1) are identical. All transistors are biased in saturation, have infinitely large channel resistances, and boast negligible bulk-induced threshold voltage modulation. The capacitances, C and C_p, are sufficiently large to enable them to function as respective short circuits for the signal frequencies of interest.

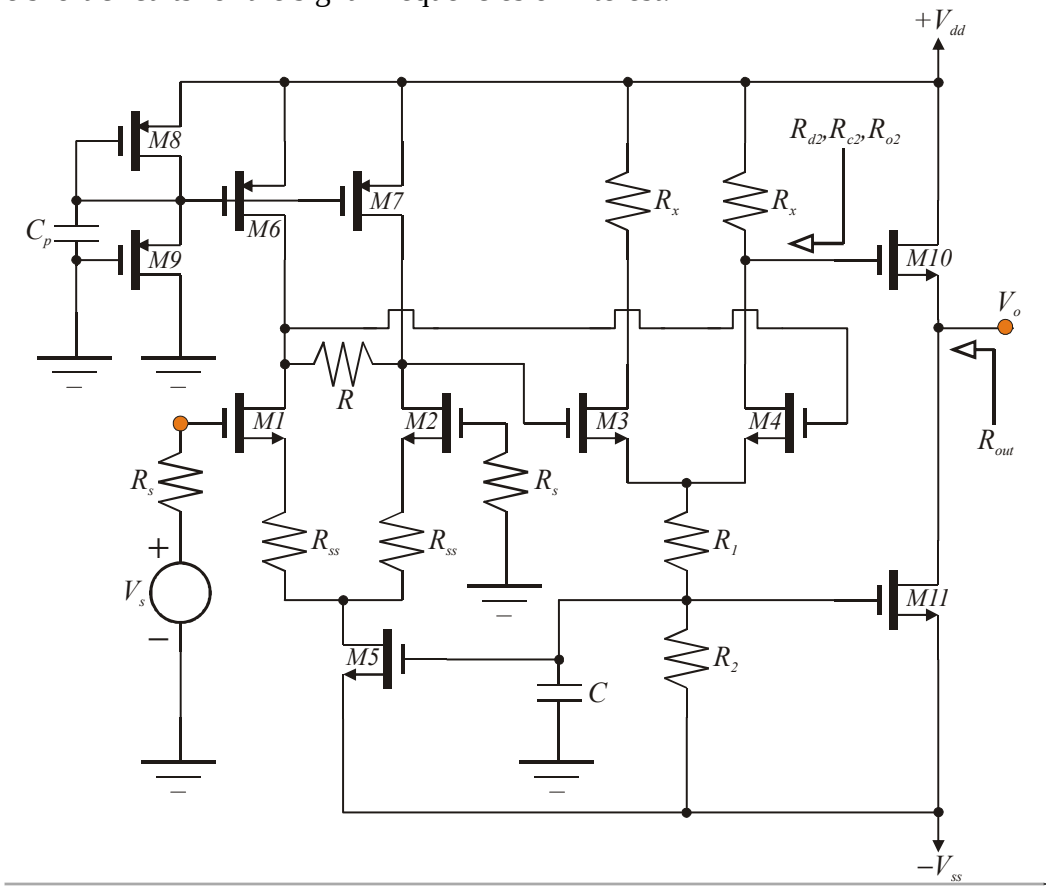

Fig. (E1)

(a). Respond to the following queries as briefly and as clearly as you can.

(a1). Under small signal operating conditions, what fundamental purpose is served by the current sink formed of transistor *M5* and its associated biasing?

Transistor *M5* establishes ideally infinitely large impedance from the junction of the two source degeneration resistances, R_{ss}, to signal ground. This infinitely large impedance ensures a common mode voltage gain in the first differential stage of zero and therefore an infinitely large common mode rejection ratio in the first differential stage. ← ANS. #1a1

(a2). Note that the second differential stage comprised of transistors *M3* and *M4* does not use active current sinking at the source terminal interconnection of these devices. Why might active current sinking here be construed as unnecessary?

Since the common mode gain of the first differential stage is reduced to zero because of the current sinking action of transistor *M5*, the common mode input signal applied to the second differential stage is necessarily zero. As a result, the common mode output signal of the second differential stage is clamped to zero, thereby disavowing the necessity of designing this second stage for high common mode rejection ratio. A current source that supplants the resistances, R_1 and R_2, therefore amounts to engineering overkill. **ANS. #1a2**

(a3). What purpose is served by the indicated interconnection of transistors *M8* and *M9*?

Transistors *M8* and *M9*, which are respectively connected as diodes, comprise a voltage divider off of the positive supply voltage, V_{dd}. This divider establishes the appropriate static voltage to bias transistors *M6* and *M7* in their saturation domains. **ANS. #1a3**

(a4). What purposes are served by capacitances *C* and C_p?

Both of these capacitors are selected to ensure that they respectively emulate short circuits over all signal frequencies of immediate interest. As such, they null any signal voltages that might appear at the gates of transistors *M5*, *M6*, and *M7*, which in turn assures strictly constant, signal invariant, drain currents in these three transistors. **ANS. #1a4**

(a5). Is the circuit a balanced architecture? If it is not balanced, what electrical connection must be severed to establish balance?

The circuit **is not** a balanced architecture. In order to restore balance, the gate connection of transistor *M10* to the drain of transistor *M4* must be severed. Strictly speaking, the gate connection of transistor *M11* to the gate of transistor *M5* must likewise be severed. However, the latter point is moot since the decoupling of *M10* forces *M11* into a zero drain current conduction state. **ANS. #1a5**

(b). Under balanced conditions and in terms of input voltage signal V_s and appropriate transistor and circuit parameters, determine the differential signal voltage, say V_{di2}, established from the gate of transistor *M3* to the gate of transistor *M4*.

Noting that the differential input signal, say V_{di1}, applied to the first differential stage is simply the indicated signal voltage, V_s, the differential mode half circuit schematic diagram of the first stage is the structure appearing in Figure (E1a). The indicated model exploits the fact that the constant current sources established by transistors *M6* and *M7* are open circuits to small signal input excitation, while the junction of the two source degeneration resistances is a short circuit under differential analytical conditions. Moreover, the midpoint of resistance *R* is a virtual ground. By inspection of the diagram,

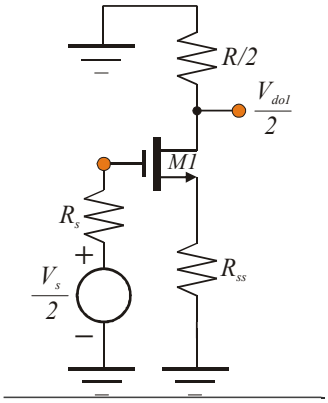

Fig. (E1a)

$$V_{do1} = -\left[\frac{g_{m1}(R/2)}{1+g_{m1}R_{ss}}\right]V_s \ . \qquad (1\text{-}1)$$

It should be noted that this differential voltage appears from the drain of transistor *M1* to the drain of transistor *M2*. On the other hand, the differential input voltage, V_{di2}, applied to the second balanced stage from the gate of transistor *M3* to the gate of *M4* is extracted from the drain of transistor *M2* to the drain of transistor *M1*; that is, the polarity of V_{di2} is the opposite of the voltage polarity implicit to V_{do1} in (1-1). Accordingly,

$$V_{di2} = -V_{do1} = \left[\frac{g_{m1}(R/2)}{1+g_{m1}R_{ss}}\right]V_s \ .$$

← **ANS. #1b**

(c). Under balanced conditions and in terms of input voltage signal V_s and appropriate transistor and circuit parameters, determine the common mode signal voltage, say V_{ci2}, established with respect to signal ground at the individual gates of transistors *M3* and *M4*.

Since the current sink formed of transistor *M5* and its associated biasing forges infinitely large common mode rejection ratio in the first differential stage, the common mode output signal voltages established at the drains of transistors *M1* and *M2* are zero. These drains interface directly with the gates of transistors *M3* and *M4*. Therefore, the common mode input signals, V_{ci2}, observed at the gate terminal input ports of the second stage are zero; that is, $V_{ci2} = 0$. ← **ANS. #1c**

(d). Give expressions for the differential mode, the common mode, and actual output resistances, R_{d2}, R_{c2}, and R_{o2}, respectively, "seen" by the gate of transistor *M10*.

Once again by inspection, the differential output resistance of the second differential amplifier is

$$R_{d2} = 2R_x \ .$$

← **ANS. #1d**

On the other hand, the common mode output resistance is

$$R_{c2} = R_x \ .$$

← **ANS. #1d**

Since $R_{d2} = 2R_{c2}$, the resistance R_{x2} strapping together the two drains of transistors *M3* and *M4* is infinitely large. It therefore follows that the output resistance, R_{o2}, which effectively is the Thévenin resistance associated with the signal source driving the gate terminal of transistor *M10* is

$$R_{o2} \equiv R_{c2} = R_x \ .$$

← **ANS. #1d**

(e). Give an expression for the small signal voltage gain, $A_v = V_{os}/V_s$.

One need worry only about the differential response of the *M3-M4* pair in that the common mode signal applied to this pair is zero by virtue of the infinitely large common mode rejection ratio of the first differential pair. Recalling that the differential signal applied from the gate of *M3* to the gate of *M4* is V_{di2}, as defined by the answer to part (b) of this problem, the differential mode half circuit model of the second stage is the structure provided in Figure (E1b).

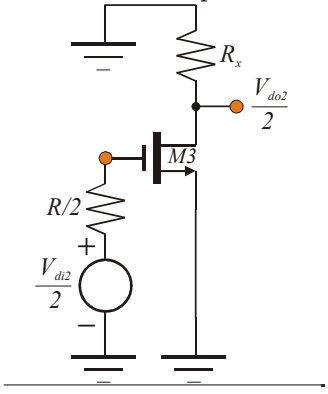

Fig. (E1b)

The subject diagram implies straightforwardly that

$$\frac{V_{do2}}{2} = -(g_{m3}R_x)\frac{V_{di2}}{2} = -(g_{m3}R_x)\left[\frac{g_{m1}(R/4)}{1+g_{m1}R_{ss}}\right]V_s \ . \qquad (1\text{-}2)$$

The corresponding signal voltage established at the drain of transistor *M4*, which is connected directly to the gate of transistor *M10*, is the negative of the signal given in the preceding expression. In view of the fact that *M10* is a source follower terminated at its output port in a current sink, *M11*, which features ideally infinitely large terminal impedance, the signal voltage, V_{os}, established at the output port of the entire amplifier is identical to the signal featured at the gate terminal of *M10*. Accordingly,

$$A_v = \frac{V_{os}}{V_s} = +(g_{m3}R_x)\left[\frac{g_{m1}(R/4)}{1+g_{m1}R_{ss}}\right].$$

← ANS. #1e

(f). What is the output resistance, R_{out}?

Since the output port of the amplifier is the source terminal of transistor *M10*, which functions as a classic source follower, the output resistance, R_{out}, is

$$R_{out} = 1/g_{m10} \ .$$

← ANS. #1f

PROBLEM #2: (40%)

In the current amplifier shown in Figure (E2), the input signal is the signal component, I_s, to the net input current, $I_Q + I_s$, while the output response to the signal input is taken as the signal component, I_{Ls}, to the indicated current, $I_{LQ} + I_{Ls}$. Of course, I_{LQ} and I_Q are quiescent biasing currents. Transistors *M1* and *M2* are identical, save for the fact that the gate aspect ratio of transistor *M1* is *k-times* smaller than the gate aspect ratios of transistors *M2* and *M3*. All transistors are biased in saturation, have infinitely large channel resistances, and have negligibly small bulk-induced threshold modulation.

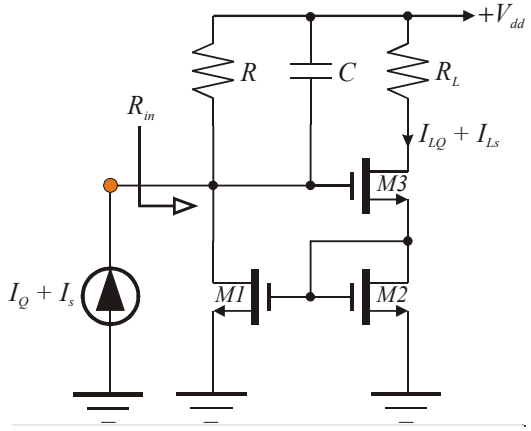

Fig. (E2)

(a). Under quiescent operating conditions, express in terms of the aspect ratio parameter, *k*, the relationship among the device transconductances, g_{m1}, g_{m2}, and g_{m3}.

Observe from the circuit schematic diagram, that the drain current, I_{LQ}, conducted by transistor *M3* also flows through transistor *M2*. Since *M2* and *M3* have identical gate aspect ratios

$$\left.\begin{aligned} g_{m2} &= \sqrt{2K_n(W_2/L_2)I_{LQ}} \\ g_{m3} &= \sqrt{2K_n(W_3/L_3)I_{LQ}} = \sqrt{2K_n(W_2/L_2)I_{LQ}} = g_{m2} \end{aligned}\right\} . \qquad (2\text{-}1)$$

Given that the gate-source voltages of transistors *M1* and *M2* are identical, and given further that

the gate aspect ratio of *M1* is *k-times* smaller than that of transistor *M1*, the static current conducted by the drain of *M1* is I_{LQ}/k. Thus

$$g_{m1} = \sqrt{2K_n\left(W_1/L_1\right)\frac{I_{LQ}}{k}} = \sqrt{2K_n\frac{\left(W_2/L_2\right)}{k}\frac{I_{LQ}}{k}} = \frac{g_{m2}}{k}\,. \tag{2-2}$$

In short,

$$\boxed{g_{m3} = g_{m2} = kg_{m1}\,.}$$

ANS. #2a

(b). Draw the low frequency, small signal equivalent circuit of the network.

The requisite small signal model of the amplifier appears in Figure (E2a). In this model, $g_{m3} = g_{m2} = kg_{m1}$.

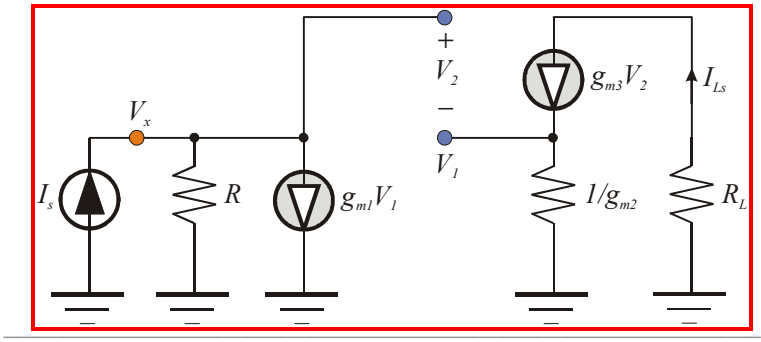

Fig. (E2a)

ANS. #2b

(c). Derive an expression for the small signal, low frequency input resistance, R_{in}. Express your result in terms of appropriate circuit parameters and device transconductances.

An inspection of the equivalent circuit reveals that

$$R_{in} = \frac{V_x}{I_s} = R\left\|\frac{V_x}{g_{m1}V_1}\right.\,. \tag{2-3}$$

Now,

$$V_1 = \frac{g_{m3}V_2}{g_{m2}}\,, \tag{2-4}$$

while

$$V_x = V_2 + V_1 = V_1\left(1 + \frac{V_2}{V_1}\right) = V_1\left(1 + \frac{g_{m2}}{g_{m3}}\right)\,. \tag{2-5}$$

Accordingly,

$$\frac{V_x}{g_{m1}V_1} = \frac{V_x\left(1 + \dfrac{g_{m2}}{g_{m3}}\right)}{g_{m1}V_x} = \frac{2}{g_{m1}}\,. \tag{2-6}$$

The insertion of this result into (2-3) yields

$$\boxed{R_{in} = \frac{V_x}{I_s} = R\left\|\frac{V_x}{g_{m1}V_1}\right. = \frac{R}{1 + g_{m1}R/2}\,.}$$

ANS. #2c

(d). Derive an expression for the low frequency, small signal current gain, $A_i = I_{Ls}/I_s$. Simplify your result for the case of very large R and express the result in terms of parameter k.

It is obvious that $I_{Ls} = g_{m3}V_2$, while the result to part (c) implies

$$V_x = \frac{RI_s}{1 + g_{m1}R/2}\,. \tag{2-7}$$

From (2-5),

$$V_2 = \frac{V_x}{1 + \dfrac{g_{m3}}{g_{m2}}} . \tag{2-8}$$

It follows that

$$I_{Ls} = g_{m3}V_2 = \frac{g_{m3}V_x}{1 + \dfrac{g_{m3}}{g_{m2}}} = \left(\frac{g_{m3}}{1 + (g_{m3}/g_{m2})}\right)\left(\frac{R}{1 + g_{m1}R/2}\right)I_s , \tag{2-9}$$

from which

$$A_i = \frac{I_{Ls}}{I_s} = \left(\frac{g_{m3}}{1 + (g_{m3}/g_{m2})}\right)\left(\frac{R}{1 + g_{m1}R/2}\right) = \left(\frac{g_{m3}R/2}{1 + g_{m1}R/2}\right) . \tag{2-10}$$

For large R,

$$A_i = \left(\frac{g_{m3}}{1 + (g_{m3}/g_{m2})}\right)\left(\frac{R}{1 + g_{m1}R/2}\right) = \left(\frac{g_{m3}R/2}{1 + g_{m1}R/2}\right) \approx \frac{g_{m3}}{g_{m1}} = k .$$

← **ANS. #2d**

(e). Derive an expression for the *3-dB* bandwidth, B, of this current gain. Assume that all capacitances indigenous to the three transistors are negligibly small.

The *3-dB* bandwidth, B, is

$$B = \frac{1}{R_{in}C} = \frac{1 + g_{m1}R/2}{RC} .$$

← **ANS. #2e**

(f). If the resistances, R and R_L, satisfy the inequality, $R > kR_L$, briefly discuss any problems encountered with respect to sustaining the operation of transistor *M3* in saturation.

The quiescent gate-source voltage, V_{gs2}, of transistor *M2* is identical to the gate-source voltage of transistor *M3* since *M2* and *M3* are identical devices conducting identical quiescent currents. Accordingly, the drain-source voltage, V_{ds3}, developed across *M3* is $(V_{dd} - R_L I_{LQ} - V_{gs3})$, and this voltage must be at least as large as the *M3* saturation voltage, $(V_{gs3} - V_h)$, where V_h signifies the threshold potential. But since *M1*, and thus resistance R, conducts I_{LQ}/k,

$$V_{dd} = R_L\left(\frac{I_{LQ}}{k}\right) + 2V_{gs3} , \tag{2-11}$$

which can certainly be solved for voltage V_{gs3}. Thus, since

$$V_{dd} - R_L I_{LQ} - V_{gs3} \geq V_{gs3} - V_h , \tag{2-12}$$

for saturation to prevail in transistor *M3*, the combination of (2-11) with this expression leads to the requirement,

$$\frac{I_{LQ}}{k}(R - kR_L) \geq -V_h , \tag{2-13}$$

which is certainly satisfied if $R > kR_L$. As long as $R > kR_L$, **there are no issues** pertinent to sustaining *M3* operation in saturation.

← **ANS. #2f**

PROBLEM #3: (15%)

Return to the circuit in Figure (E1).

(a). Let transistors *M8* and *M9* be identical, inclusive of gate aspect ratios. If transistors *M6* and *M7* are biased so that their respective source to drain quiescent voltages are one P-channel threshold voltage above their source-drain saturation voltage, what quiescent volt-

age is established with respect to ground at the drains of transistors *M1* and *M2*?

If transistors *M8* and *M9* are identical, the static voltage developed at the gate of transistor *M6* is $V_{dd}/2$, which means that the source-gate voltage on transistor *M6* is $V_{dd} - V_{dd}/2 = V_{dd}/2$. In turn, the saturation voltage for *M6* follows as $V_{dd}/2 - V_{hp}$, where V_{hp} is the threshold voltage of the P-channel transistors. If the source-drain voltage of *M6* is one threshold above saturation level, $V_{sd6} = V_{sd7} = V_{dd}/2 - V_{hp} + V_{hp} = V_{dd}/2$. Accordingly, the static voltage developed at the drains of transistors *M1* and *M2* is $V_{dd} - V_{dd}/2 = V_{dd}/2$. ← **ANS. #3a**

(b). Let the quiescent voltage developed with respect to ground at the drain of transistor *M5* be V_Q and let this same static voltage prevail at the source interconnection of transistors *M3* and *M4*. Will transistor *M5* operate in saturation for any values of resistances R_1 and R_2?

The gate-source voltage developed on transistor *M5* is obviously something smaller than V_Q, while the drain-source voltage on *M5* is larger than V_Q by an amount equal to V_{ss}. Since saturation of *M5* mandates $V_{ds5} \geq V_{gs5} - V_{hn}$, any values of R_1 and R_2 sustain *M5* saturation. ← **ANS. #3b**

(c). What detrimental impact on the small signal performance of the amplifier is likely to be observed if transistor *M5* operates in its triode domain?

If transistor *M5* enters its triode regime of operation, its channel resistance becomes necessarily finite and in general, far smaller than the channel resistance evidenced in saturation. As a result, the common mode rejection ratio of the first stage degrades substantively, and this degradation most assuredly reduces the overall gain of the amplifier. ← **ANS. #3c**

(d). How much power is dissipated by resistance *R* under quiescent operating conditions?

Since the drain terminal voltages of transistors *M1* and *M2* sustain identical voltages under static operational circumstances, no static power is dissipated in resistance R . ← **ANS. #3d**

(e). For differential mode small signal operation, how must capacitance *C* be chosen so that *C* emulates a short circuit for all signal frequencies above ω_L?

The resistance facing capacitance *C* is the shunt combination of resistances R_1 and R_2, since the sources of *M3* and *M4* lie at virtual ground for differential input signals. Consequently,

$$\omega_L \left(R_1 \| R_2\right) C >> 1 \ .$$

← **ANS. #3e**

(f). For differential mode small signal operation, how must capacitance C_p be chosen so that C_p emulates a short circuit for all signal frequencies above ω_L?

The resistance facing capacitance C_p is the shunt combination of the small signal resistances associated with the diode connected P-channel devices, *M8* and *M9*. Consequently,

$$\omega_L \left(\frac{1}{g_{m8}} \Bigg\| \frac{1}{g_{m9}} \right) C_p >> 1 \ .$$

← **ANS. #3f**