UNIVERSITY OF SOUTHERN CALIFORNIA
USC VITERBI SCHOOL OF ENGINEERING
MING HSIEH DEPARTMENT OF ELECTRICAL ENGINEERING

EE 348: FINAL EXAMINATION #3 (OPEN NOTES, HOMEWORK) — **MAY 08, 2007 11:00-TO-1:00**

PROBLEM #1: *(45%)*

Except for possible differences in gate aspect ratios, all transistors in the two-stage differential amplifier of Figure (E1) are identical. All transistors are biased in saturation, have infinitely large channel resistances, and boast negligible bulk-induced threshold voltage modulation. The capacitances, C and C_p, are sufficiently large to enable them to function as respective short circuits for the signal frequencies of interest.

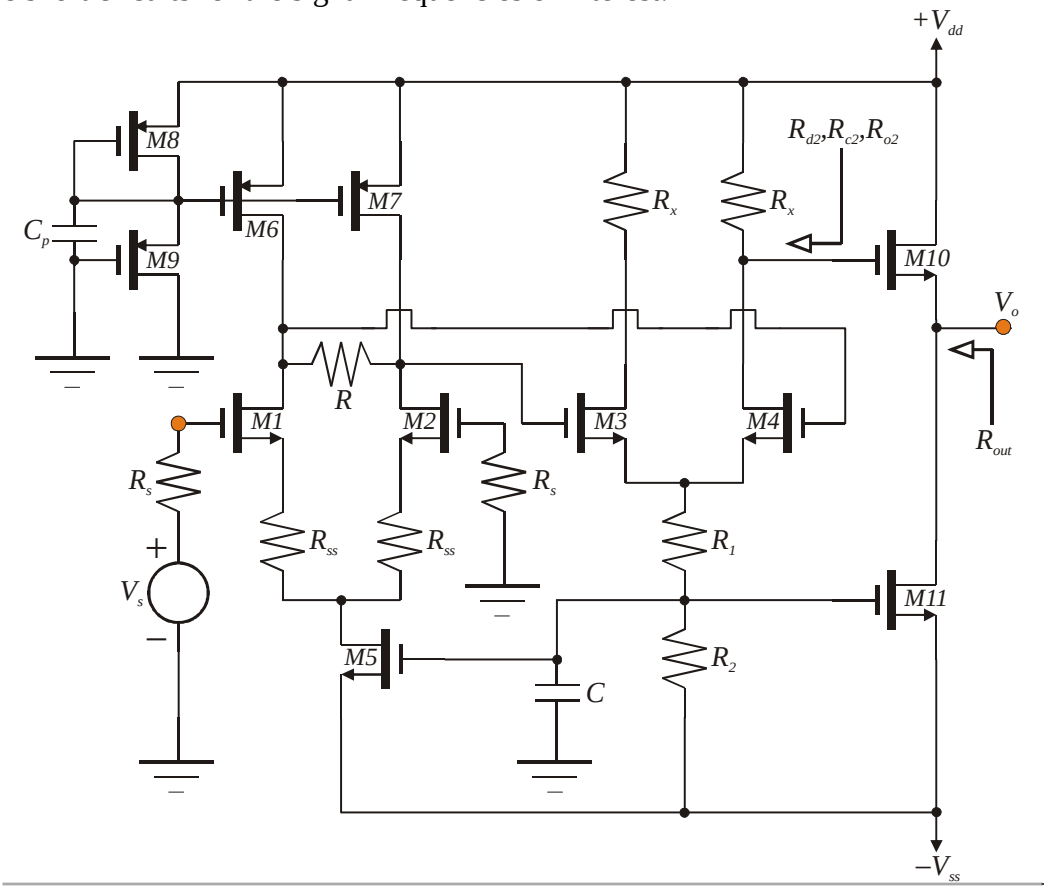

Fig. (E1)

(a). Respond to the following queries as briefly and as clearly as you can.

(a1). Under small signal operating conditions, what fundamental purpose is served by the current sink formed of transistor *M5* and its associated biasing?

(a2). Note that the second differential stage comprised of transistors *M3* and *M4* does not use active current sinking at the source terminal interconnection of these devices. Why might active current sinking here be construed as unnecessary?

(a3). What purpose is served by the indicated interconnection of transistors *M8* and *M9*?

(a4). What purposes are served by capacitances C and C_p?

(a5). Is the circuit a balanced architecture? If it is not balanced, what electrical connection must be severed to establish balance?

(b). Under balanced conditions and in terms of input voltage signal V_s and appropriate transistor and circuit parameters, determine the differential signal voltage, say V_{di2}, established from the gate of transistor *M3* to the gate of transistor *M4*.

(c). Under balanced conditions and in terms of input voltage signal V_s and appropriate transistor and circuit parameters, determine the common mode signal voltage, say V_{ci2}, established with respect to signal ground at the individual gates of transistors *M3* and *M4*.

(d). Give expressions for the differential mode, the common mode, and actual output resistances, R_{d2}, R_{c2}, and R_{o2}, respectively, "seen" by the gate of transistor *M10*.

(e). Give an expression for the small signal voltage gain, $A_v = V_{os}/V_s$.

(f). What is the output resistance, R_{out}?

PROBLEM #2: (40%)

In the current amplifier shown in Figure (E2), the input signal is the signal component, I_s, to the net input current, $I_Q + I_s$, while the output response to the signal input is taken as the signal component, I_{Ls}, to the indicated current, $I_{LQ} + I_{Ls}$. Of course, I_{LQ} and I_Q are quiescent biasing currents. Transistors *M1* and *M2* are identical, save for the fact that the gate aspect ratio of transistor *M1* is *k-times* smaller than the gate aspect ratios of transistors *M2* and *M3*. All transistors are biased in saturation, have infinitely large channel resistances, and have negligibly small bulk-induced threshold modulation.

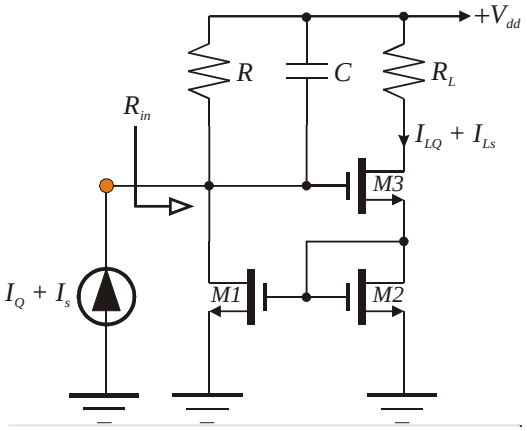

Fig. (E2)

(a). Under quiescent operating conditions, express in terms of the aspect ratio parameter, k, the relationship among the device transconductances, g_{m1}, g_{m2}, and g_{m3}.

(b). Draw the low frequency, small signal equivalent circuit of the network.

(c). Derive an expression for the small signal, low frequency input resistance, R_{in}. Express your result in terms of appropriate circuit parameters and device transconductances.

(d). Derive an expression for the low frequency, small signal current gain, $A_i = I_{Ls}/I_s$. Simplify your result for the case of very large R and express the result in terms of parameter k.

(e). Derive an expression for the *3-dB* bandwidth, B, of this current gain. Assume that all capacitances indigenous to the three transistors are negligibly small.

(f). If the resistances, R and R_L, satisfy the inequality, $R > kR_L$, briefly discuss any problems encountered with respect to sustaining the operation of transistor *M3* in saturation.

PROBLEM #3: (15%)

Return to the circuit in Figure (E1).

(a). Let transistors *M8* and *M9* be identical, inclusive of gate aspect ratios. If transistors *M6* and *M7* are biased so that their respective source to drain quiescent voltages are one P-channel threshold voltage above their source-drain saturation voltage, what quiescent voltage is established with respect to ground at the drains of transistors *M1* and *M2*?

(b). Let the quiescent voltage developed with respect to ground at the drain of transistor *M5* be V_Q and let this same static voltage prevail at the source interconnection of transistors *M3* and *M4*. Will transistor *M5* operate in saturation for any values of resistances R_1 and R_2?

(c). What detrimental impact on the small signal performance of the amplifier is likely to be observed if transistor *M5* operates in its triode domain?

(d). How much power is dissipated by resistance *R* under quiescent operating conditions?

(e). For differential mode small signal operation, how must capacitance *C* be chosen so that *C* emulates a short circuit for all signal frequencies above ω_L?

(f). For differential mode small signal operation, how must capacitance C_p be chosen so that C_p emulates a short circuit for all signal frequencies above ω_L?