University of Southern California
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EE 348: Homework Assignment #08 (Due 04/19/2007) — **Spring, 2007** — **Choma**

Problem #29:

The transistors in the balanced differential amplifier of Fig. (P29) have negligible bulk-induced threshold modulation and small signal channel resistances that are sufficiently large to justify their tacit neglect. The substrate terminals of all transistors are appropriately connected; that is, the substrate terminals of all N-channel devices are connected to the $-V_{ss}$ supply, while the substrate terminals of the P-channel transistors are incident with the $+V_{dd}$ supply. All biasing sources, V_{b1}, V_{b2}, V_{b3}, and V_{b4}, can be taken as ideal constant voltage sources. In general, the forward transconductance of transistor *Mi* and *Mia* can be denoted as g_{mi}. The capacitances symbolized as C in the network can be presumed to emulate AC short circuits over the signal frequency passband of interest.

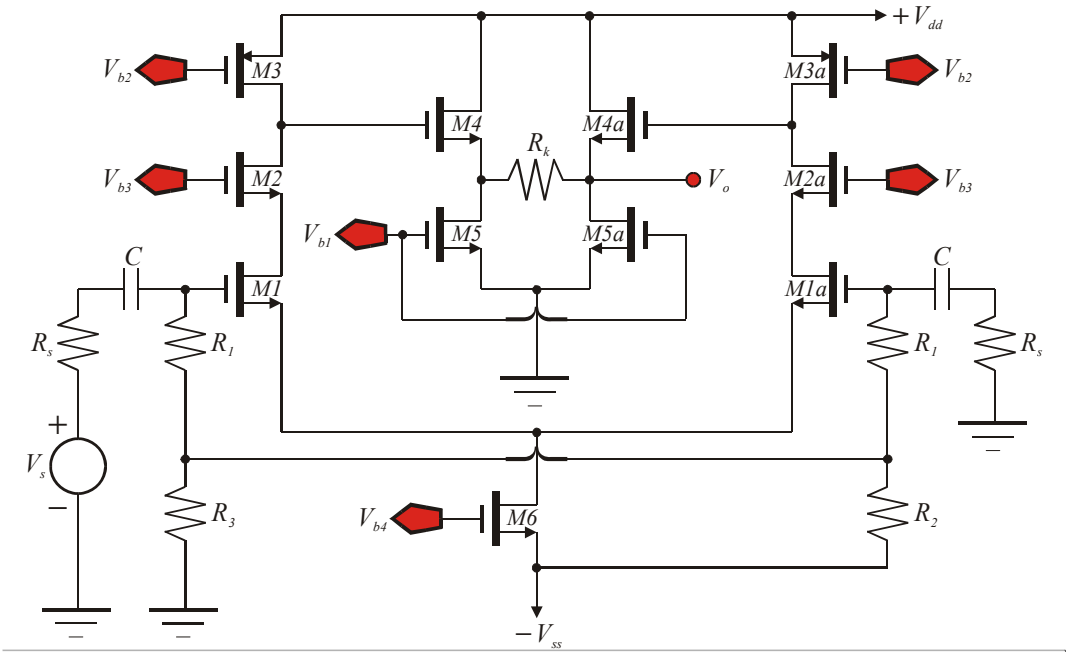

Figure (P29)

(a). Draw the differential mode and common mode equivalent half circuit schematic diagrams.

Before plunging into this problem, several noteworthy observations can be made. First, transistors *M3* and *M3a* function as constant current sources since their respective source-gate voltages are $(V_{dd} - V_{b2})$, which are time invariant constants. Second, transistors *M5* and *M5a* operate as constant current sinks owing to the constant voltage, V_{b1}, impressed across their gate-source terminals. Third, transistors *M2* and *M2a* function as common gate cascode architectures that, owing to the device modeling assumptions invoked herewith, feature unity current gains. On the other hand, *M4* and *M4a* are source followers having less than unity voltage gains, while *M1* and *M1a* are common source transistors. Fourth, the drain of transistor *M6* is a virtual ground for exclusively differential mode input excitation. Fifth, resistors R_2 and R_3 form a voltage divider off of the $-V_{ss}$ supply to

bias properly the gate terminals of transistors *M1* and *M1a*. The node at which resistors R_1 (on the right) and R_2, are connected, which is the same as the connection node for resistors R_1 (on the left) and R_3, is a virtual ground for differential mode excitation. Sixth, the center of resistance R_k is a virtual ground for differential mode inputs. Finally, capacitance C is a short circuit over the signal frequency range of interest for both differential mode and common mode inputs. Armed with these declarations and the fact that the differential mode input voltage, V_{di}, is

$$V_{di} = \frac{V_s - 0}{2} = \frac{V_s}{2} , \tag{29-1}$$

while the common mode input voltage, V_{ci}, is

$$V_{ci} = \frac{V_s + 0}{2} = \frac{V_s}{2} = V_{di} , \tag{29-2}$$

the differential mode and common mode half circuit schematics are as depicted in Figure (P29a).

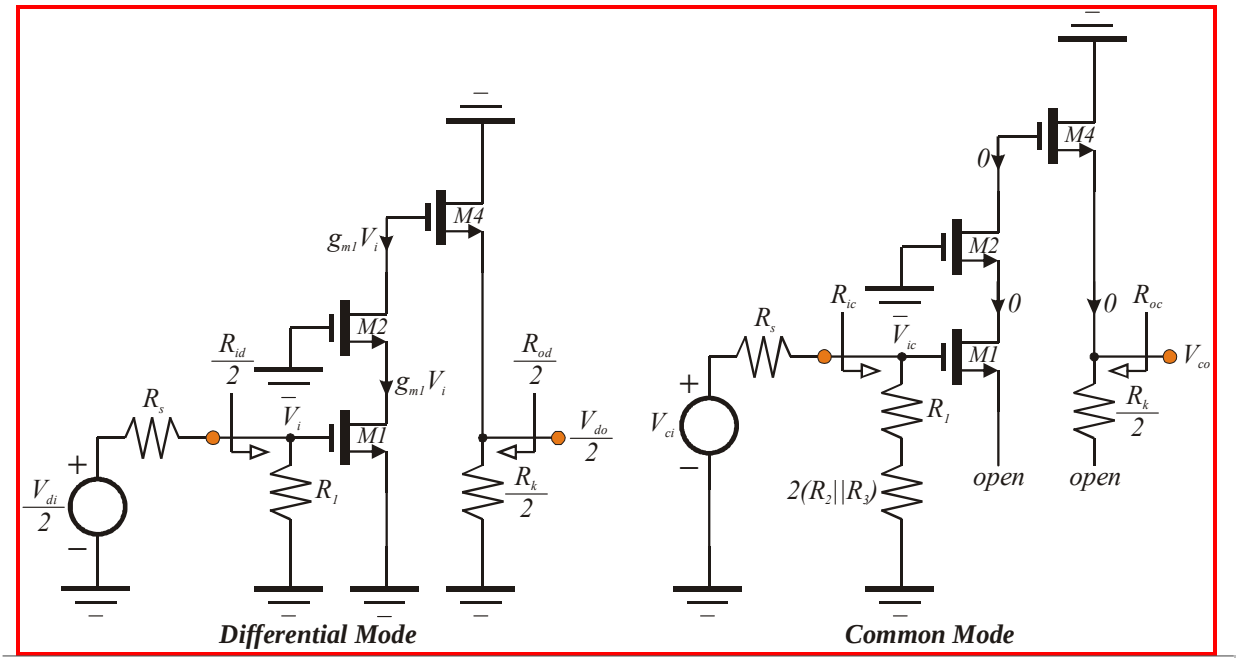

Figure (P29a)

(b). Derive an expression for the differential mode voltage gain, A_{vd}.

The signal voltage, V_i, developed from the gate to ground of transistor *M1* in the differential mode half circuit is

$$V_i = \left(\frac{R_1}{R_1 + Rs}\right)\frac{V_{di}}{2} , \tag{29-3}$$

which means that the signal current, I_{ds}, flowing in the drain of *M1*, and hence in the drain of *M2*, is

$$I_{ds} = g_m V_i = \left(\frac{R_1}{R_1 + Rs}\right)\frac{V_{di}}{2} . \tag{29-4}$$

But since this signal current must flow through the *M4* gate, which cannot conduct current, V_{di} is forced to be zero. Note that if the channel resistance, r_{o3}, of transistor *M3* is not ignored, the voltage established at the gate of *M4* would be $-g_{m1}r_{o3}V_i$, which would establish a negative voltage at the output port where $V_{do}/2$ is the extracted signal in Figure (P29a). Thus, since $V_{di} = 0$, the differential gain, A_{vd}, of the amplifier is $\boxed{A_{vd} = -\infty}$.

(c). Derive an expression for the common mode voltage gain, A_{vc}.

Under common mode operating conditions, the source of *M1* is terminated to ground in a resistance

of $2r_{o6}$, where r_{o6} is the channel resistance of transistor *M6*. Since r_{o6} is infinitely large, the *M1* source is left open circuited, thereby precluding any signal current flow through the drains of *M1* and *M2*. Accordingly, no signal voltage can be established at the gate of *M4* and resultantly, no signal voltage appears at the source of *M4*. These voltage conditions prevail even if the channel resistance of *M3* is not taken to be infinity. It follows that the common mode voltage gain, A_{vc}, of the amplifier at hand is $\boxed{A_{vc} = 0}$.

(d). Derive an expression for the overall voltage gain, $A_v = V_o/V_s$.

The output response at the source of *M4* is $V_{co} + (V_{do}/2)$, while at the source of *M4a*,

$$V_{os} = V_{co} - \frac{V_{do}}{2} = A_{vc}V_{ci} - \frac{A_{vd}V_{di}}{2} \tag{29-6}$$

and since $V_{ci} = V_{di} = V_s/2$, $A_{vc} = 0$, and $A_{vd} = -\infty$, the overall voltage gain, $A_v = V_{os}/V_s$, is $\boxed{A_v = +\infty}$.

(e). Derive expressions for the differential mode input resistance, R_{id}, the common mode input resistance, R_{ic}, and the net input resistance, R_{in}, seen by the input signal source.

By inspection of the diagrams in Figure (P29a),

$$\left.\begin{aligned} \frac{R_{id}}{2} &= R_1 \quad \Rightarrow \quad R_{id} = 2R_1 \\ R_{ic} &= R_1 + 2\left(R_2 \| R_3\right) \end{aligned}\right\rangle . \tag{29-7}$$

The input resistance model pertinent to the computation of the input resistance, R_{in}, is depicted in Figure (P29b), where

$$R_{ix} = \frac{2R_{id}R_{ic}}{2R_{ic} - R_{id}} = \left(2 + \frac{R_1}{\left(R_2 \| R_3\right)}\right)R_1 . \tag{29-8}$$

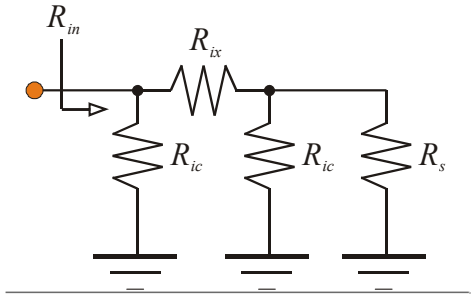

Figure (P29b)

The input resistance follows as

$$\boxed{R_{in} = R_{ic} \left\| \left[R_{ix} + \left(R_{ic} \| R_s\right)\right] ,} \tag{29-9}$$

where R_{ic} in (29-7) and R_{ix} in (29-8) can be substituted into this relationship.

(f). Derive expressions for the differential mode output resistance, R_{od}, the common mode output resistance, R_{oc}, and the net output resistance, R_{out}, seen at the indicated output terminal.

By inspection of the diagrams in Figure (P29a),

$$\left.\begin{aligned} \frac{R_{od}}{2} &= \frac{R_k}{2} \left\| \frac{1}{g_{m4}} \right. \quad \Rightarrow \quad R_{od} = \frac{R_k}{1 + \left(g_{m4}R_k/2\right)} \\ R_{oc} &= \frac{1}{g_{m4}} \end{aligned}\right\rangle . \tag{29-10}$$

The output resistance model pertinent to the computation of the output resistance, R_{out}, is depicted in Figure (P29c), where

$$R_{ox} \;=\; \frac{2R_{od}R_{oc}}{2R_{oc} - R_{od}} \;=\; R_k \;. \tag{29-11}$$

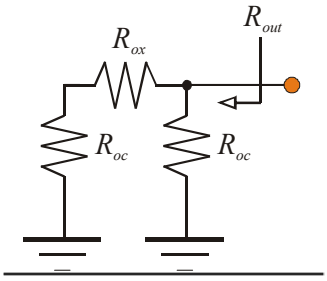

Figure (P29c)

The output resistance follows as

$$R_{out} \;=\; R_{oc}\left\|\left(R_{ox} + R_{oc}\right) \;=\; \left(\frac{1 + g_{m4}R_k}{2 + g_{m4}R_k}\right)\frac{1}{g_{m4}} \;. \right. \tag{29-12}$$

(g). Give a strategy for selecting capacitance C if this capacitance is to approximate a signal short circuit for all frequencies above ω_l in the differential voltage gain response.

Capacitance C must be selected so that the magnitude of its impedance at frequency ω_l is significantly smaller than the resistance faced by the capacitor. Thus,

$$\frac{1}{\omega_l C} \;<<\; R_s + R_{in} \;\;\Rightarrow\;\; \omega_l\left(R_s + R_{in}\right)C \;>>\; 1 \;. \tag{29-13}$$

When capacitances are selected to emulate short circuits above a stipulated lower frequency, it generally suffices to interpret "much, much greater" as a number no smaller than the square root of ten.

PROBLEM #30:

In the so-called telescopic amplifier diagrammed in Figure (P30), the drain-source channel resistances of all transistors, except transistor *M9*, can be taken to be infinitely large. Moreover, bulk-induced modulation of all threshold voltages can be ignored. The output response is the indicated differential voltage, V_o, while the input is the signal voltage, V_s.

(a). Draw the differential mode and common mode small signal half circuit models.

As in the preceding exercise, it is worthwhile digesting the circuit architecture prior to drawing the requested small signal models. Note that the source terminals of transistors *M7* and *M8* are connected to a constant voltage source, $+V_{dd}$, and similarly, the gates of these two active devices are connected to a constant voltage of V_{bias4}. It follows that transistors *M7* and *M8* conduct only constant drain currents. Since *M5* is in series with *M7*, *M6* is in series with *M8*, *M3* is connected in series with *M5*, and *M4* is in series with *M6*, which in turn is in series with *M8*, transistors *M3*, *M4*, *M5*, and *M6* conduct the same constant current that flows through the drains of transistors *M7* and *M8*. Assuming transistors *M3* and *M4* are matched, as they must be to preserve balanced operation, the drains of transistors *M1* and *M2* are each terminated to ground in a resistance of $1/g_{m3}$. As far as the inputs are concerned, there is only one signal, V_s, applied to the circuit, which implies that the differential input signal, V_{di}, is V_s, while the common mode component, V_{ci}, of the applied signal excitation is $V_s/2$.

It is convenient to view the resistance, R, as the series interconnection of two resistances of value $R/2$. Likewise, capacitance C may be viewed as the series interconnection of two capacitances, each of value $2C$. For differential excitation, the center taps of these two split components are virtual short circuits. The center tap of the source terminal connection of transistors *M1* and *M2* is

also a virtual ground for differential mode operation of the circuit. Under common mode circumstances, this center tap is terminated to signal ground in a resistance of $2r_{o9}$, where r_{o9} is understood to be the drain-source channel resistance of transistor *M9*, which serves as a current sink for transistors *M1* and *M2*.

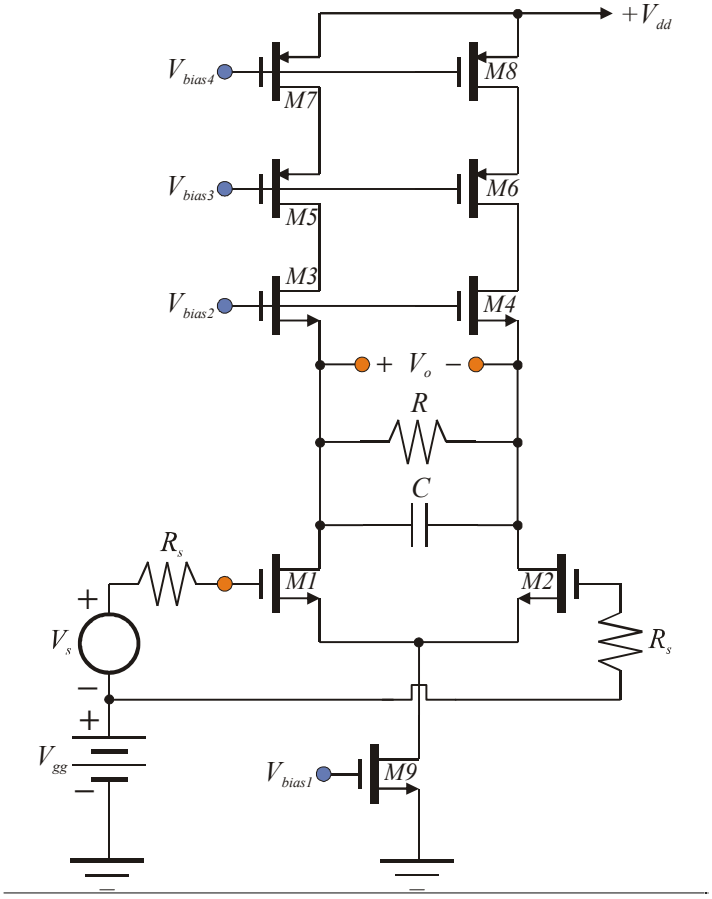

Figure (P30)

The immediate ramifications of the foregoing observations are the half circuit models propounded in Figure (P30a).

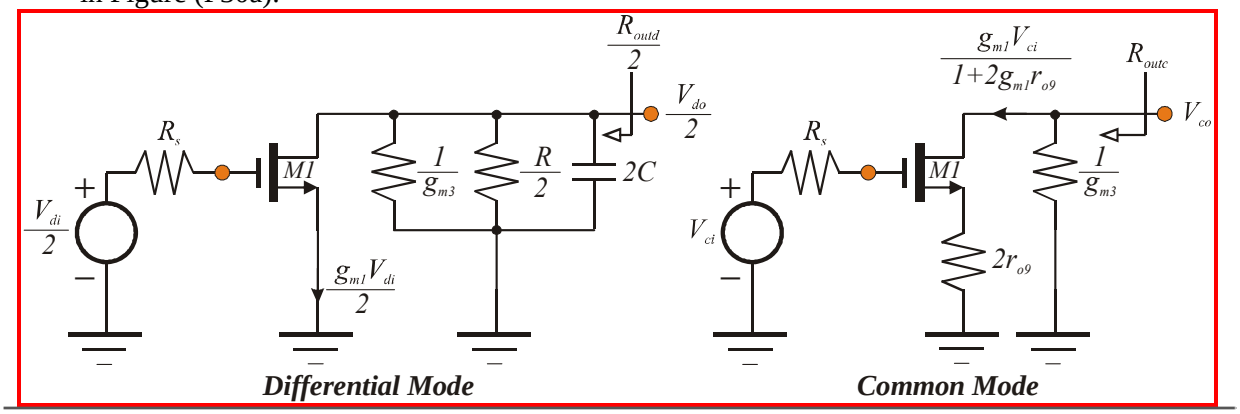

Figure (P30a)

(b). Give expressions for the low frequency differential voltage gain, A_{vd}, the low frequency common mode voltage gain, A_{vc}, and the common mode rejection ratio, ρ.

At low signal frequencies, the capacitance, *2C*, in each of the equivalent circuits of Figure (P30a) behave as open circuits. Thus, the differential mode circuit yields

$$\frac{V_{do}}{2} = -\frac{g_{m1}V_{di}}{2}\left(\frac{R/2}{1+g_{m3}R/2}\right), \tag{30-1}$$

whence a differential mode voltage gain, A_{vd}, of

$$A_{vd} = \frac{V_{do}/2}{V_{di}/2} = -\frac{g_{m1}R/2}{1+g_{m3}R/2}. \tag{30-2}$$

On the other hand, the common mode equivalent half circuit gives

$$V_{co} = -\frac{g_{m1}V_{ci}/g_{m3}}{1+2g_{m1}r_{o9}}, \tag{30-3}$$

which implies a common mode voltage gain, A_{vc}, of

$$A_{vc} = \frac{V_{co}}{V_{ci}} = -\frac{g_{m1}/g_{m3}}{1+2g_{m1}r_{o9}}. \tag{30-4}$$

The common mode rejection ratio, ρ, follows as

$$\rho = \frac{A_{vd}}{A_{vc}} = \left(1+2g_{m1}r_{o9}\right)\left(\frac{g_{m3}R/2}{1+g_{m3}R/2}\right). \tag{30-5}$$

(c). Derive expressions for the differential mode and common mode output resistances, R_{outd} and R_{outc}, respectively, seen at the output terminals.

By inspection of the diagrams in Figure (P30a), the differential output resistance, R_{outd}, is

$$R_{outd} = \frac{R}{1+g_{m3}R/2}. \tag{30-6}$$

On the other hand, the common mode output resistance, R_{outc}, is simply

$$R_{outc} = \frac{1}{g_{m3}}. \tag{30-7}$$

Care must be exercised when evaluating the differential output resistance in that the output resistance indicated in the differential mode half circuit of Figure (30a) is $R_{outd}/2$, not simply R_{outd}.

(d). Give an expression for the *3-dB* bandwidth, *B*, of the differential mode voltage gain response.

From Figure (P30a), the time constant associated with the capacitance, *2C*, is $2C(R_{outd})$. Therefore, the *3-dB* bandwidth, *B*, for differential mode operation is

$$B = \frac{1}{2CR_{outd}} = \frac{1+g_{m3}R/2}{2RC}. \tag{30-8}$$

PROBLEM #31:

Channel length modulation and bulk-induced threshold voltage modulation can be tacitly ignored in all MOSFETs embedded in the amplifier of Figure (P31). The transistor pairs, *M1–M2, M3–M4, M5–M6,* and *M7–M8*, are matched and biased identically. Transistors *M9, M10, M11,* and *M12* are biased to yield respectively identical small signal parameters. The capacitance of capacitor *C* is very large and therefore behaves as a short circuit over the signal frequencies of interest.

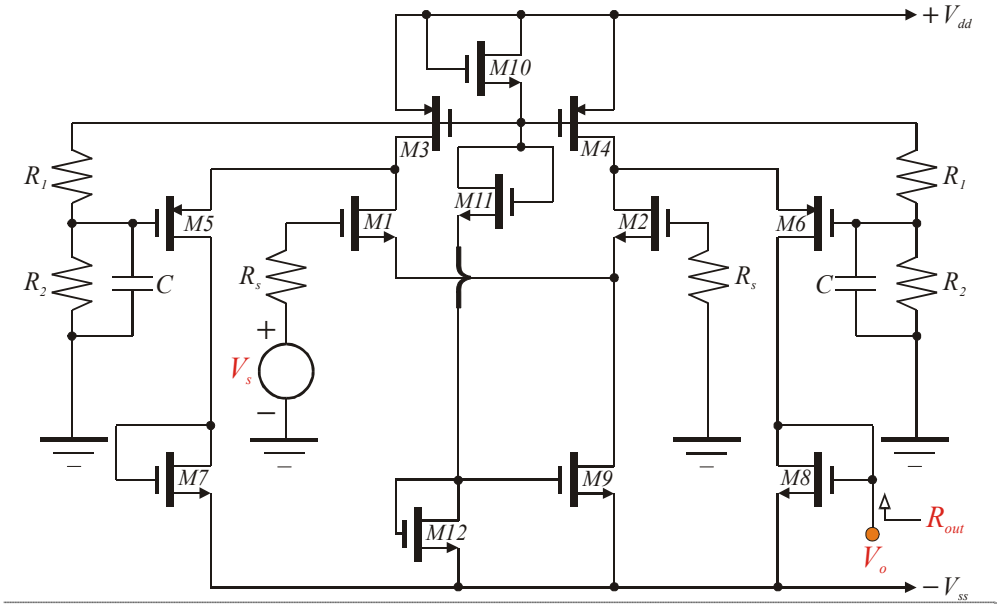

Figure (P31)

(a). Draw the differential mode, half circuit schematic diagram.

Because of the power supply voltage divider formed by the diode-connected transistors, *M10*, *M11*, and *M12*, transistors *M3* and *M4* act as constant current source loads for the drains of transistors *M1* and *M2*. For differential mode operation, the source terminals of *M1* and *M2* are grounded, while for common mode circumstances, these source terminals are left open circuited because of the presumption that the channel resistance of *M9* (and of all other transistors) is infinitely large. The gates of transistors *M5* and *M6* are grounded for small signal operation in that capacitance *C* is selected large enough to behave as a short circuit for all signal frequencies of interest. Transistors *M7* and *M8* are diode-connected devices that establish active loads at a resistance of $1/g_{m7}$. There is only one signal, V_s, applied to the circuit, which implies that the differential input signal, V_{di}, is V_s, while the common mode component, V_{ci}, of the applied input signal is $V_s/2$. The requested half circuit diagrams appear in Figure (P31a).

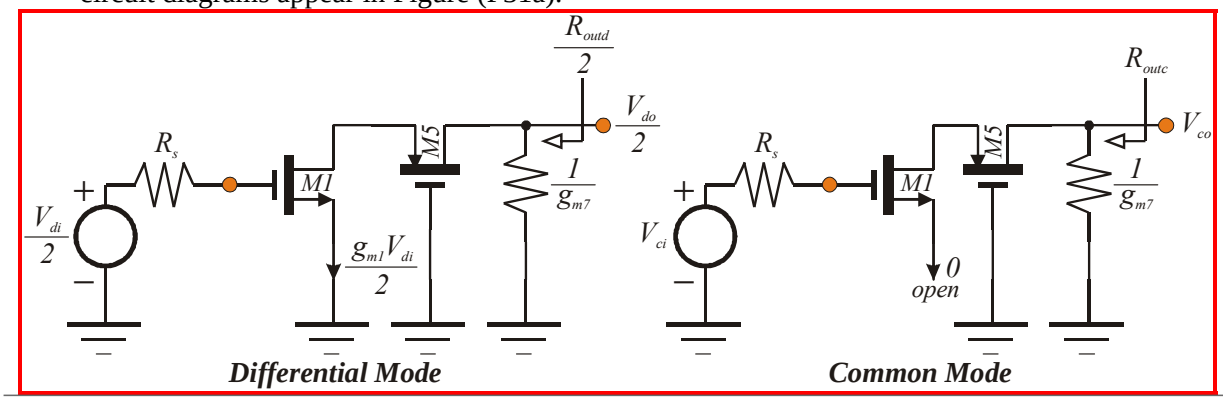

Figure (P31a)

(b). What is the common mode rejection ratio, ρ, of the amplifier? Briefly rationalize your answer without explicitly solving for this metric.

By inspection of the equivalent half circuits in Figure (P31a), the differential voltage gain, A_{vd}, is

$$A_{vd} = \frac{V_{do}/2}{V_{di}/2} = -\frac{g_{m1}}{g_{m7}}, \qquad (31\text{-}1)$$

while the common mode gain, A_{vc}, is zero because zero signal current flows through the $1/g_{m7}$ load

resistance. Thus, the common mode rejection ratio, ρ, is

$$\rho = \frac{A_{vd}}{A_{vc}} = \infty . \tag{31-2}$$

Of course, this metric is rendered infinitely large only because the presumption of infinitely large channel resistance in *M9* precludes the flow of common mode signal current in the load resistance, which leads to null common mode gain. For future reference, note that the differential and common mode output resistances, R_{outd} and R_{outc}, respectively, are

$$\left.\begin{aligned} R_{outd} &= \frac{2}{g_{m7}} \\ R_{outc} &= \frac{1}{g_{m7}} \end{aligned}\right\} . \tag{31-3}$$

(c). Derive an expression for the small signal voltage gain, $A_v = V_{os}/V_s$, of the amplifier.

The signal component, V_{os}, of the indicated output voltage, V_o, is

$$V_{os} = V_{co} - \frac{V_{do}}{2} = A_{vc}V_{ci} - \frac{A_{vd}V_{di}}{2} , \tag{31-4}$$

and since $A_{vc} = 0$,

$$V_{os} = -\frac{A_{vd}V_{di}}{2} = -\frac{A_{vd}V_s}{2} . \tag{31-5}$$

It follows that, the overall voltage gain, A_v, of the balanced configuration is

$$A_v = \frac{V_{os}}{V_s} = -\frac{A_{vd}}{2} = \frac{g_{m1}}{2g_{m7}} . \tag{31-6}$$

Note the absence of phase inversion in this transfer characteristic. If the output were to be extracted at the drain of transistor *M7*, the same gain magnitude would prevail, but with *180°* phase inversion.

(d). Give an expression for the small signal output resistance, R_{out}.

In general, the model pertinent to the computation of output resistance in a balanced differential amplifier is the structure depicted in Figure (P31b), where

$$R_{ox} = \frac{2R_{outc}R_{outd}}{2R_{outc} - R_{outd}} . \tag{31-7}$$

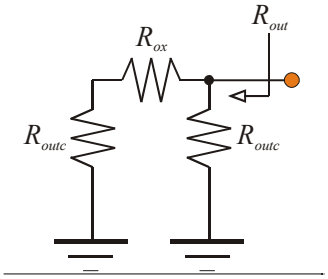

Figure (P31b)

Recalling (31-3), $R_{outd} = 2R_{outc}$, thereby making R_{ox} infinitely large. Accordingly, the output resistance, R_{out}, is simply

$$R_{out} = R_{outc} = \frac{1}{g_{m7}} . \tag{31-8}$$

(e). Under differential mode operating conditions, what is the time constant, τ, associated with capacitance C?

In view of the fact that the gates of transistors *M3* and *M4* lie at signal ground under differential operating conditions, the time constant, τ, associated with capacitance C is

$$\tau = (R_1 \| R_2) C \ . \tag{31-9}$$

(f). Is the circuit best suited for voltage, transimpedance, or transconductance amplification?

The input resistance is obviously extremely large because the gate terminals of *M1* and *M2* conduct no signal current. The output resistance, which is $1/g_{m7}$, is substantively smaller, especially if transistors *M7* and *M8* conduct large drain currents and/or are implemented with large gate aspect ratios. Therefore, the amplifier is best suited for voltage amplification.

(g). Assuming differential operating conditions and that the source resistance, R_s, is the traditional *50* Ω, is stray capacitance appearing at the input port, the output port, the gate node of transistor *M5*, or the drain node of transistor *M2* likely to establish the dominant amplifier pole?

This one is difficult to call. It is unlikely that the input port forges the dominant amplifier pole since R_s is only *50* Ω and transistor *M5*, which acts as a common gate cascode, mitigates Miller multiplication of the gate-drain capacitance of transistor *M1*. The gate node of *M5* is also an unlikely candidate in that the resistance established at this node is of the order of $1/g_{m5}$. This resistance is small because the gate aspect ratio of cascode devices is generally chosen to be reasonably large. The output node is the likely source of pole dominance. To be sure, the resistance at this output node is only $1/g_{m7}$, but g_{m7} is likely to be kept small in the interest of maintaining reasonable voltage gain.

(h). Assuming that the output port drives a balanced, purely capacitive load of capacitance C_L, and that no other circuit or device capacitances are significant, what is the amplifier *3-dB* bandwidth?

The bandwidth, B, is

$$B = \frac{1}{R_{out} C_L} = \frac{g_{m7}}{C_L} \ . \tag{31-10}$$

(i). Comment as to the dependence of the overall amplifier voltage gain on quiescent device currents. Specifically, what would you advocate to reduce the voltage gain dependence on bias current?

If the circuit is implemented to ensure that transistors *M7* and *M8* conduct the same quiescent currents as do transistors *M1* and *M2*, the voltage gain given by (31-6) is independent of biasing currents.

PROBLEM #32:

In the balanced differential amplifier shown in Figure (P32), all transistors are biased in their saturation regimes. All transistors have negligible channel length modulation and negligible bulk-induced threshold modulation. The capacitances, C_1 and C_2, are chosen to ensure that they emulate signal short circuits for all radial signal frequencies above a specified minimum value, say ω_L. The circuit resistance, R, is chosen to be equal to the signal source resistance, R_s. Output responses can be extracted as either voltage V_{o1} or voltage V_{o2}.

(a). Draw the small signal, differential mode, half circuit schematic diagram of the differential pair.

Using arguments that are similar to those invoked on preceding problems, the differential mode half circuit schematic diagram is the structure offered on the left in Figure (P32a).

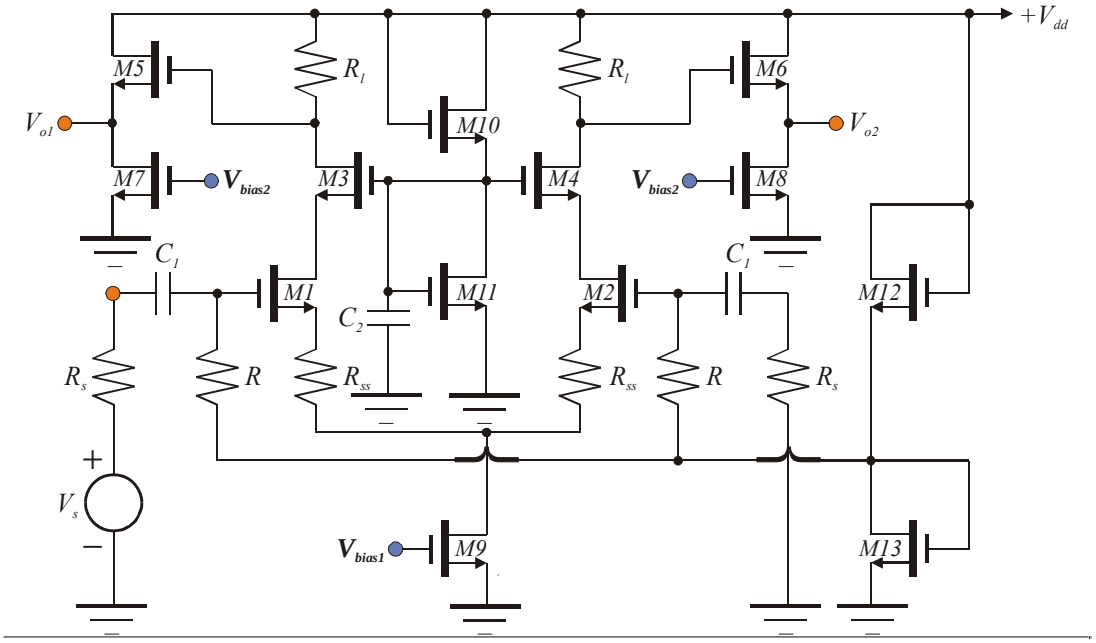

Figure (P32)

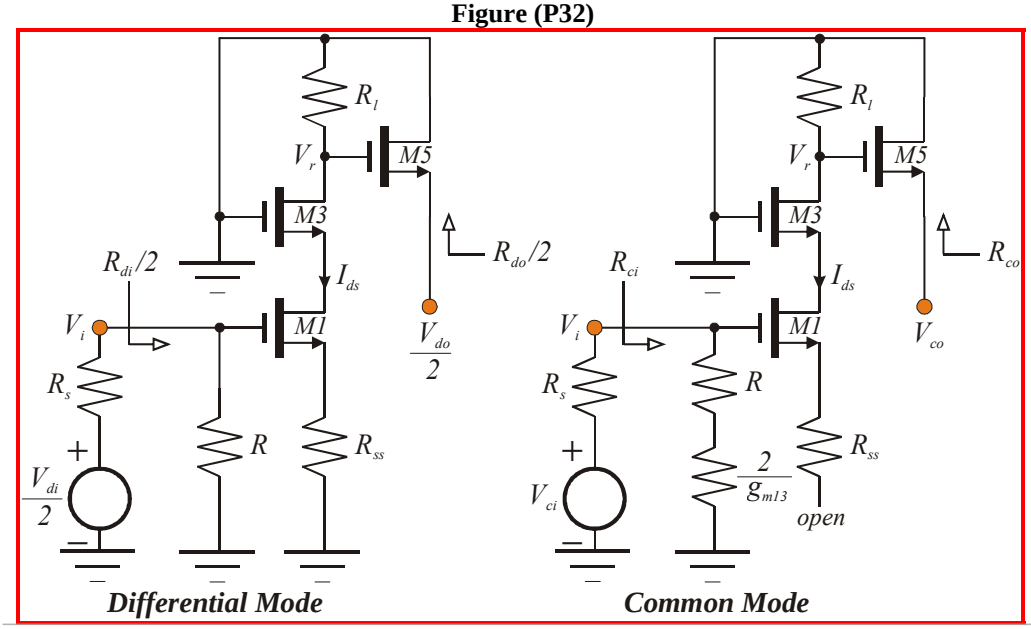

Figure (P32a)

(b). Draw the small signal, common mode, half circuit schematic diagram of the differential pair.

Figure (P32b) also depicts the common mode equivalent half circuit schematic diagram.

(c). Give, preferably by inspection, the common mode voltage gain, say A_c, of the differential amplifier.

In the common mode half circuit, the signal current, I_{ds}, must be zero since the source degeneration resistance, R_{ss}, is not returned to ground. With $I_{ds} = 0$, voltage V_r is necessarily zero, whence the common mode output response, V_{co}, is forced to zero. Accordingly, the common mode gain, A_c, is $A_c = 0$, which is the idealized goal of any balanced network.

(d). Give, preferably by inspection, the differential mode voltage gain, say A_d, of the differen-

tial amplifier.

The signal voltage, V_i, established at the gate of transistor *M1* is

$$V_i = \left(\frac{R}{R+R_s}\right)\frac{V_{di}}{2} = \frac{V_s}{4}, \tag{32-1}$$

where use is made of the fact that $R = R_s$. The resultant signal current response, I_{ds}, to this gate signal voltage is

$$I_{ds} = \frac{g_{m1}V_i}{1+g_{m1}R_{ss}} = \frac{g_{m1}V_s}{4(1+g_{m1}R_{ss})}. \tag{32-2}$$

This current flows through resistance R_l, with the result that

$$V_r = -I_{ds}R_l = -\frac{g_{m1}R_lV_{di}}{4(1+g_{m1}R_{ss})}. \tag{32-3}$$

Since the source follower, *M5*, drives an open circuited load, the half circuit output response, $V_{do}/2$, is identical to voltage V_r. It follows that the differential voltage gain, A_d, of the amplifier is

$$A_d = \frac{V_{do}/2}{V_{di}/2} = -\frac{g_{m1}R_l}{2(1+g_{m1}R_{ss})}. \tag{32-4}$$

(e). Give, preferably by inspection, the voltage gain, say $A_v = V_{o2s}/V_s$, of the differential amplifier, where V_{o2s} is the small signal component of the net output voltage, V_{o2}.

Given a null common mode gain, the voltage response at the output of the *M6* source follower is $V_{o2s} = -A_dV_{di}/2 = -A_dV_s/2$, whence

$$A_v = \frac{V_{o2s}}{V_s} = \frac{g_{m1}R_l}{4(1+g_{m1}R_{ss})}. \tag{32-5}$$

(f). What design criterion must be satisfied by the capacitance C_l is to emulate a signal short circuit for differential mode excitation?

An inspection of Figure (P32a) reveals differential and common mode input resistances of

$$\left.\begin{aligned} R_{di} &= 2R \\ R_{ci} &= R + \frac{2}{g_{m13}} \end{aligned}\right\rangle. \tag{32-6}$$

The input resistance model is the circuit of Figure (P32b), where

$$R_{ix} = \frac{2R_{ci}R_{di}}{2R_{ci}-R_{di}} = (2+g_{m13}R)R. \tag{32-7}$$

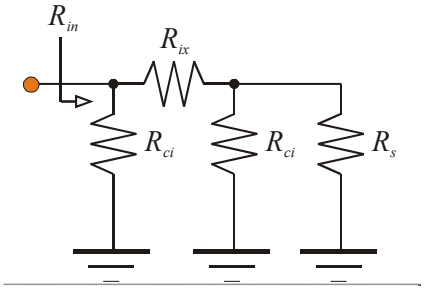

Figure (P32b)

Clearly, the input resistance, R_{in}, is

$$R_{in} = R_{ci}\left\|\left[R_{ix}+\left(R_{ci}\|R_s\right)\right] = R_{ci}\right\|\left[(2+g_{m13}R)R+\left(R_{ci}\|R_s\right)\right]. \tag{32-8}$$

If ω_l designates the lowest radial signal frequency of interest, capacitance C_l must be selected in accord with

$$\omega_l \left(R_s + R_{in} \right) C_l \; >> \; 1 \; , \tag{32-9}$$

where R_{in} is given by (32-8).

PROBLEM #33:

In the circuit of Figure (P33), all N-channel transistors have their bulk terminals incident with the negative supply bus, are biased in saturation, have infinitely large drain-source channel resistances, and have negligible bulk transconductances; that is, all $\lambda_b = 0$. Additionally, all transistors are identical, save for possibly different gate aspect ratios. The capacitance, C, which is obviously an open circuit at low signal frequencies, is inserted between ground and the indicated node to establish a predictable *3-dB* bandwidth for the amplifier. The gate aspect relationships that are relevant to this problem are itemized herewith.

The gate aspect ratio of ***M1*** is *identical* to that of ***M1a***.
The gate aspect ratio of ***M2*** is *identical* to that of ***M2a***.
The gate aspect ratio of ***M3*** is *identical* to that of ***M3a***.
The gate aspect ratio of ***M4*** is *identical* to that of ***M4a***.
The gate aspect ratio of ***M5*** is *4-times greater* than that of ***M7***.
The gate aspect ratio of ***M1*** is *100-times greater* than that of ***M2***.
The gate aspect ratio of ***M5*** is *9-times greater* than that of ***M6***.

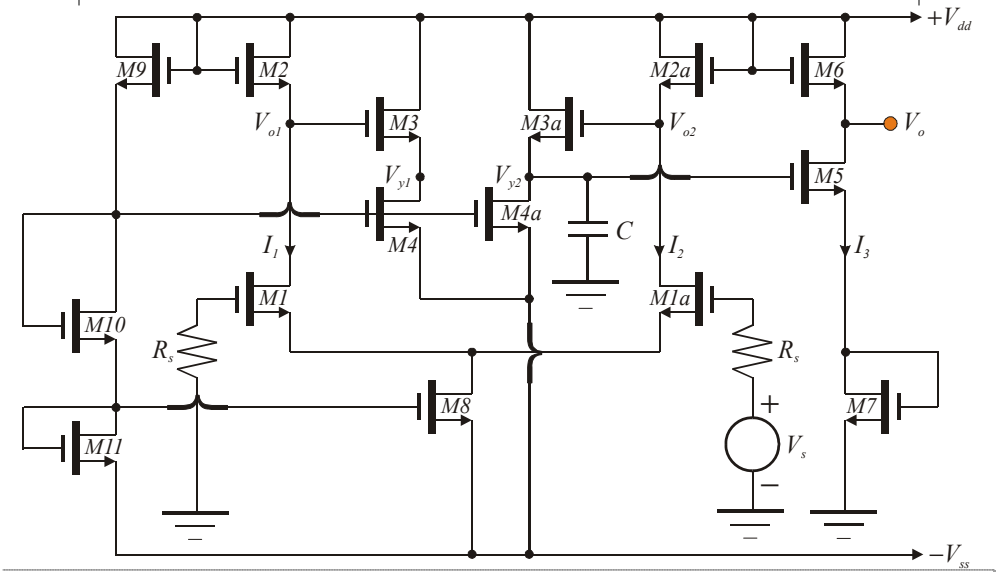

Figure (P33)

(a). The amplifier in Figure (P33) is technically unbalanced. What transistor gate terminal must be disconnected to render the configuration balanced at low signal frequencies?

The amplifier is rendered balanced by open circuiting the gate of transistor *M5*. This means that at low signal frequencies, where capacitance C can be supplanted by an open circuit, the signal voltage response, V_{y2}, is effectively a Thévenin equivalent output response of the resultantly balanced pair. Note that the gate of transistor *M6* need not be open circuited because by disconnecting the gate of transistor *M5*, no signal current can be conducted by transistor *M6*.

(b). For the balanced subcircuit gleaned from the disconnection addressed in Part (a), what are the differential mode, low frequency, small signal components of currents I_1 and I_2? Express these currents in terms of the forward transconductance, g_{m1}, of transistor *M1* and the indicated signal voltage, V_s.

For the resultantly balanced circuit, the differential input signal voltage, V_{di}, is $V_{di} = V_{s1} - V_{s2} = -$

V_s, while the common mode input signal, V_{ci}, is $V_{ci} = (V_{s1} + V_{s2})/2 = V_s/2$. Under differential signal conditions,

$$I_{1s} = g_{m1}\frac{V_{di}}{2} = -g_{m1}\frac{V_s}{2}$$
$$I_{2s} = -g_{m1}\frac{V_{di}}{2} = g_{m1}\frac{V_s}{2}. \quad (33\text{-}1)$$

(c). Using the results of Part (b), give the differential mode, low frequency, small signal components of the voltages, V_{o1}, V_{o2}, V_{y1}, and V_{y2}. By exploiting the aforementioned gate aspect relationships for the transistors, your individual answers can be expressed as a simple numerical constant multiplied by the signal voltage, V_s. The numerical constants obtained may be positive or negative numbers.

Transistor *M2* functions as a resistance, $1/g_{m2}$, as does the identical transistor, *M2a*. The gate aspect ratio of *M1* is *100-times* larger than that of *M2*, whence $g_{m1}/g_{m2} = 10$ owing to the square root dependence of transconductance on gate aspect ratio. Note further that *M3* and *M3a*, which are terminated at their source terminals in current sinks formed of transistors *M4* and *M4a*, respectively, operate as source followers having, within the context of the invoked approximations, unity voltage gain. Thus,

$$\left.\begin{aligned} V_{o1s} &= \frac{V_{do}}{2} = -\frac{I_{1s}}{g_{m2}} = \left(\frac{g_{m1}}{g_{m2}}\right)\frac{V_s}{2} = 5V_s \\ V_{o2s} &= -\frac{V_{do}}{2} = -\frac{I_{2s}}{g_{m2}} = -\left(\frac{g_{m1}}{g_{m2}}\right)\frac{V_s}{2} = -5V_s \\ V_{y1s} &= V_{o1s} = 5V_s \\ V_{y2s} &= V_{o2s} = -5V_s \end{aligned}\right\}. \quad (33\text{-}2)$$

(d). What are the common mode, low frequency, small signal components of the voltages, V_{o1}, V_{o2}, V_{y1}, and V_{y2}?

Since transistor *M8* emulates an ideal constant current sink that carries zero signal current, the common mode components of all four voltages found in the preceding part of this problem solution are zero.

(e). Using the results of Parts (c) and (d), give a simple expression for the small signal, low frequency current, I_3, conducted by the source terminal of transistor *M5*. Express your answer as a function of the forward transconductance, g_{m5}, of *M5* and the signal voltage, V_s.

The gate aspect ratio of transistor *M5* is *4-times* larger than that of transistor *M7*, which means that $g_{m5}/g_{m7} = 2$. Since *M5* operates as a common source amplifier having a source degeneration resistance of $1/g_{m7}$, the signal component, I_{3s}, to the indicated current, I_3 is

$$I_{3s} = \frac{g_{m5}V_{y2s}}{1 + g_{m5}/g_{m7}} = -\frac{5}{3}(g_{m5}V_s). \quad (33\text{-}3)$$

(f). Using the result of Part (e), give a simple expression for the small signal, low frequency voltage gain, V_o/V_s. Using previously stipulated gate aspect ratio relationships, your answer is either a positive or a negative numerical value.

The gate aspect ratio of transistor *M5* is *9-times* larger than that of transistor *M6*, which means that $g_{m5}/g_{m6} = 3$. Since *M5* operates as a common source amplifier having an effective load resistance of $1/g_{m6}$, the small signal output voltage response is

$$V_{os} = -I_{3s}/g_{m6} = \frac{g_{m5}(5V_s)}{3g_{m6}} = 5V_s\ ;$$
$$\frac{V_{os}}{V_s} = 5. \qquad (33\text{-}4)$$

(g). Give an expression for the *3-dB* bandwidth, B, of the amplifier.

Capacitance C faces an effective resistance of $1/g_{m3}$. Accordingly, the radial *3-dB* bandwidth, B, is

$$B = g_{m3}/C. \qquad (33\text{-}5)$$

PROBLEM #34:

Bipolar biasing circuits commonly utilize a subcircuit known as a "V_{be} multiplier," which is diagrammed in Fig. (P34).

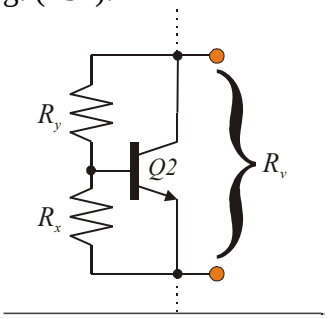

Figure (P34)

(a). Assuming that the transistor is biased in its linear regime by additional circuitry not shown in the subject figure, determine the small signal resistance, R_v, across the terminals of the V_{be} multiplier. Assume that the small signal Early resistance, r_o, of the transistor is sufficiently large to warrant its tacit neglect.

The small signal model of the V_{be} multiplier is given in Figure (P34a), in which pertinent branch currents are indicated. In this model, r_b is the intrinsic base resistance, r_π is the small signal base-emitter junction resistance, and β is the small signal short circuit current gain of the transistor. The desired resistance, R_v, in this model is simply the ratio, V_x/I_x.

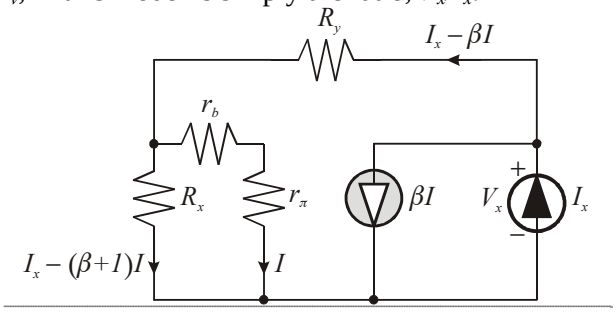

Figure (P34a)

The current, $[I_x-(\beta+1)I]$, conducted by the resistance, R_x, relates to the current, I, flowing through resistance r_π as

$$I_x - (\beta+1)I = \frac{(r_b + r_\pi)I}{R_x}\ , \qquad (34\text{-}1)$$

from which I_x is seen to relate to I in accordance with

$$I_x = I\left(\beta + 1 + \frac{r_b + r_\pi}{R_x}\right). \tag{34-2}$$

By KVL,

$$V_x = R_y\left(I_x - \beta I\right) + \left(r_b + r_\pi\right) I\ . \tag{34-3}$$

The elimination of current I in this relationship through the substitution of (34-2) into (34-3), followed by the obligatory algebra, leads to

$$R_v = \frac{V_x}{I_x} = \left[\frac{r_b + r_\pi + R_x}{r_b + r_\pi + \left(\beta+1\right)R_x}\right] R_y + R_x \left\| \left(\frac{r_b + r_\pi}{\beta+1}\right)\right. . \tag{34-4}$$

(b). Does the expression for R_v collapse to anticipated results for the special case of $R_y = 0$ and $R_x = \infty$? What do you expect this special case to reflect?

With $R_x = 0$ and $R_y = \infty$, the configuration in Figure (P34) becomes a simple diode-connected bipolar junction transistor. The expression in (34-4), reduces to

$$R_v\Big|_{\substack{R_y=0\\R_x=\infty}} = \frac{r_b + r_\pi}{\beta+1}\ , \tag{34-5}$$

which is precisely the resistance seen looking into the emitter of a bipolar junction transistor under the approximation of infinitely large Early resistance. It is interesting to note that for very large β, which is tantamount to near zero transistor base current (just like the gate of a MOSFET conducts zero current), (34-5) can be rewritten as

$$R_v\Big|_{\substack{R_y=0\\R_x=\infty}} = \frac{r_b + r_\pi}{\beta+1} \approx \frac{r_b}{\beta} + \frac{r_\pi}{\beta} \approx \frac{1}{g_m}\ , \tag{34-6}$$

which is reminiscent of the resistance seen looking into the source of a MOSFET. In arriving at (44-6), use is made of the fact that $\beta = g_m r_\pi$, where g_m is the forward, small signal transconductance of a bipolar junction transistor.

(c). If the transistor conducts a nonzero collector current in its linear regime, what is the voltage dropped from collector to emitter in the indicated subcircuit? Express this result in terms of the base-emitter voltage, V_{be}, and the two circuit resistances, R_x and R_y. Furthermore, assume that the static current gain, h_{FE}, of the transistor is sufficiently large to justify the tacit neglect of the transistor base current.

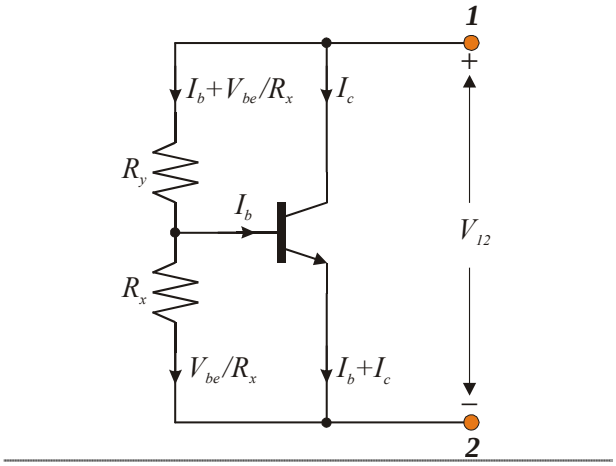

Figure (P34b)

In the diagram of Figure (P34b), the static base current, I_b, relates to the static collector current, I_c, as $I_b = I_c/h_{FE}$. If h_{FE} is suitably large, this base current can be ignored, which means that the volt-

age, say V_{12}, dropped from the collector to the emitter is

$$V_{12} \approx R_y\left(\frac{V_{be}}{R_x}\right) + V_{be} = \left(1 + \frac{R_y}{R_x}\right)V_{be} \ . \tag{34-7}$$

Observe that the static collector-emitter voltage is directly proportional to the base-emitter static voltage, V_{be}, with the multiplicative proportionality being $(1 + R_y/R_x)$.