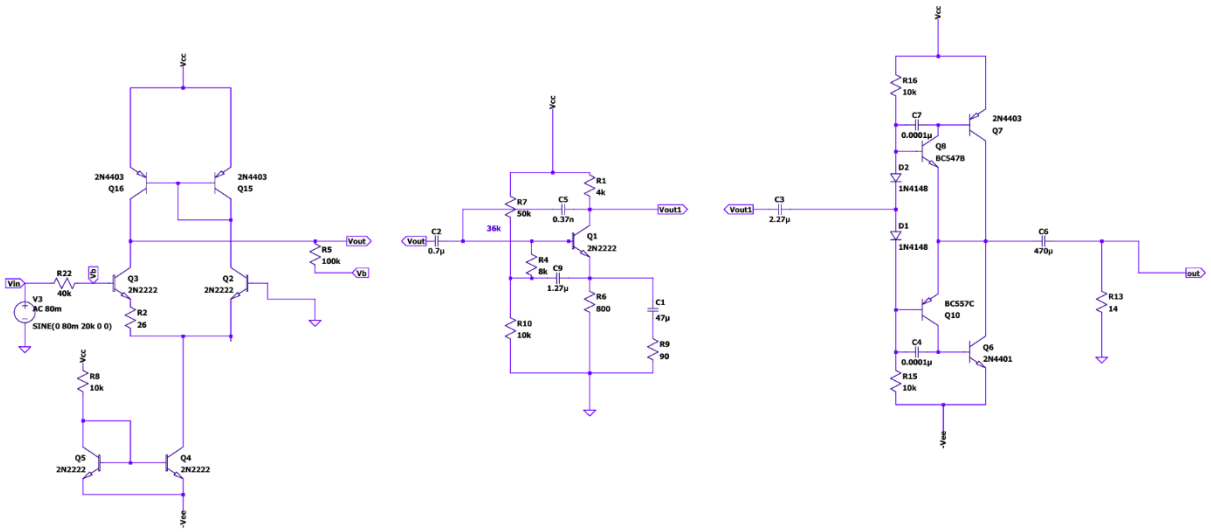
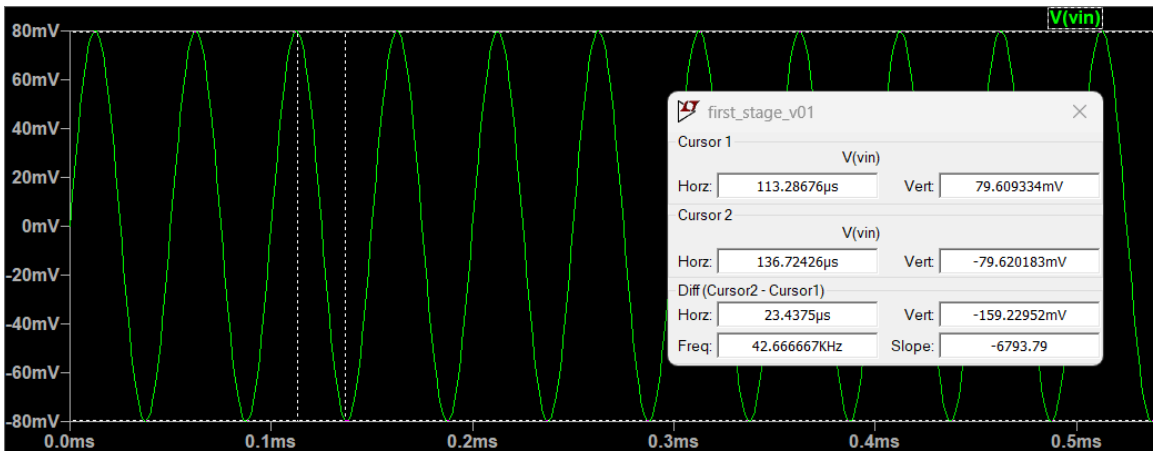
Audio Amplifier

A comprehensive design project which involves designing a 3-stage amplifier aimed for proper amplification of audio signals i.e ..., 20Hz – 20kHz. This document discusses the design of every stage and collective performance grading of the amplifier with data of necessary analysis outcomes.

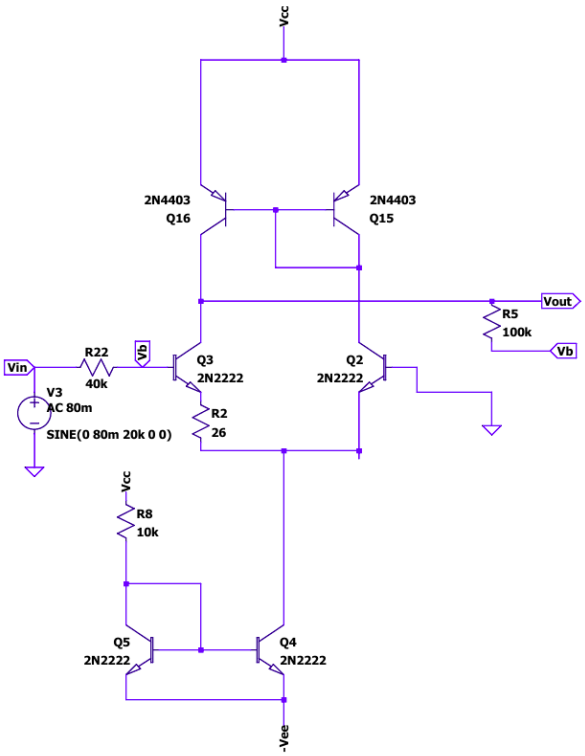
Contents:



This figure below is the signal input for the amplifier which is a **20khz 160mV peak-peak** signal.



Stage 1 – Differential Input stage:



This differential input stage is intended for input noise suppression.

Because, of the constant current source used as the tail it provides very high noise suppression. This can be shown by the following expression.

$$\boldsymbol{Ac = \beta * Rc/(ri + 2 * \beta * Re)}$$

[since, Re = ∞ (constant current source). We have, $Ac = 0$]

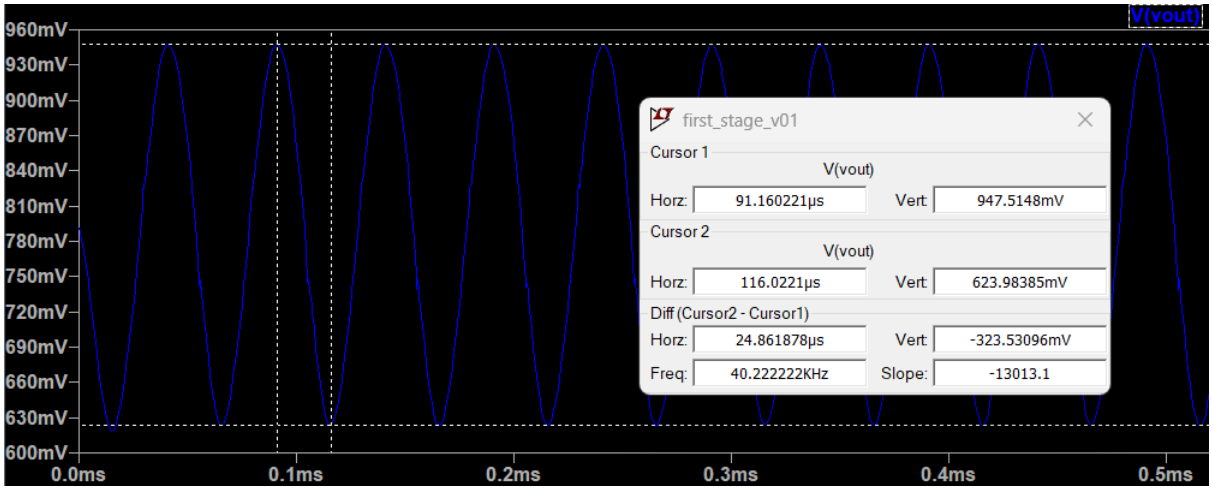
The 26 ohms resistor is used to enforce symmetry in the positive and negative half cycles during amplification. (Done during simulation)

$$Itail = \frac{Vcc - (-Vee) - Vbe}{R8} = \frac{12 - (-12) - 0.7}{10k} = 2.33mA$$

The use of the current mirror makes the gain insanely high, to control the gain negative feedback is provided. As per the closed loop gain expression.

$$Av = \frac{-Rf}{Re} = \frac{-100k}{40k} = -2.5$$

The signal output from the differential amplifier is as shown in the fig below,



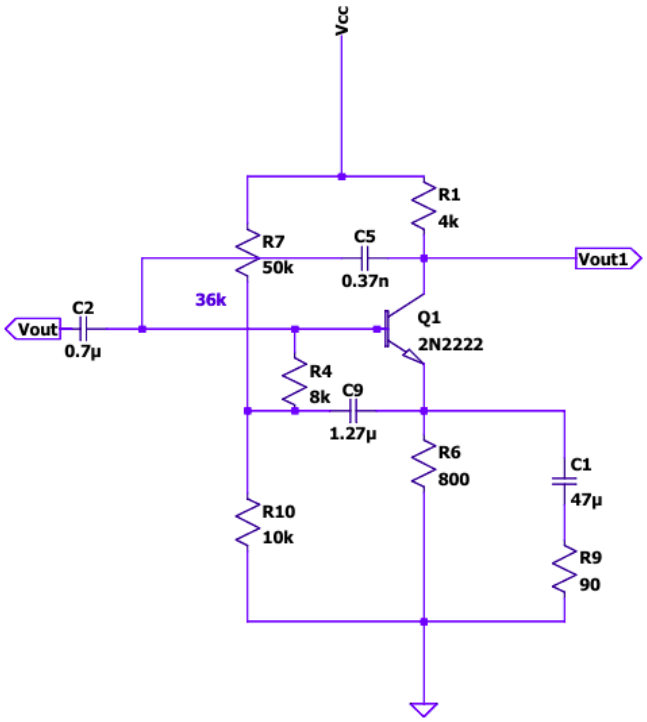
Now as per the simulation results the gain is as follows:

$$Av = -323.53mV/160mV = -2.02$$

Summary: The differential input stage along with the feedback provides excellent noise suppression.

Improvements: A FET input stage can be used to better increase the input impedance if incase the signal source has a high source impedance.

Stage 2 – Gain Stage:



Operating point:

V_{cc} = 12V; V_c = 6V ; V_e = 1.2V ; V_{th} = V_b = 1.9V;

Q-Point: (V_{ce} , I_c) = (4.2V, 1.5mA);

h_{fe} = 150 (for 2N2222)

I_b = 10uA;

This stage is mainly concerned with providing necessary voltage amplification.

- This stage is featured with a **bootstrap configuration** to ensure high enough input impedance so that this stage does not load the previous stage.

Design for DC bias:

1. The Design for DC Bias is simple once the operating voltages are known, the values of the resistors required can be obtained by using following equations.
2. Input Loop:

$$Vth - Vb - I\boldsymbol{b}Rb - IcRe = 0 \text{ ..... loop(1)}$$

3. Output loop:

$$Vcc - IcRc - Vce - IcRe = 0 \quad \text{..... loop(2)}$$

4. Substituting the Voltages and currents from the operating section and solving for the unknowns gives the required resistor values for DC Bias.

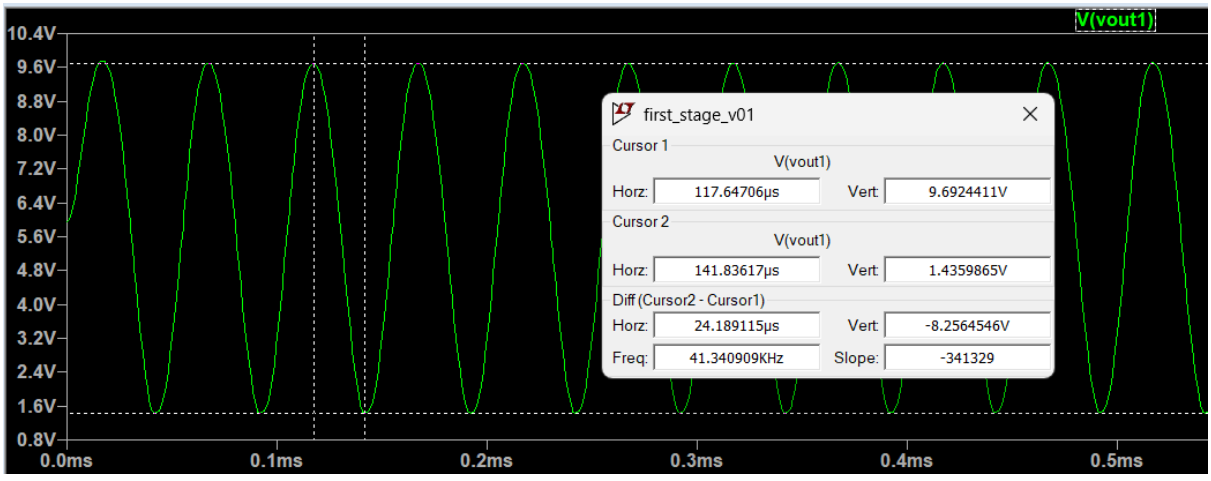
Bootstrap design:

1. We choose the resistors R4, R10, R7 to meet the requirements for V_b and I_b and R_{th} (Equivalent Thevenin's resistance).
2. At signal frequencies R4 acts as a open circuit as the voltage difference between this resistance becomes zero.
3. Looking into the capacitor C9 the resistance seen is the parallel combination between R7 and R10. Thus to allow signal frequencies to pass through the C9. We choose,

$$C9 = \frac{1}{2\pi \times R \times f} = \frac{1}{2\pi \times 8.33k \times 15Hz} = 1.27\mu F$$

Note: *The use of the C5 = 0.37nF called as* ***Miller's compensation capacitor****, is to cause gain roll off at higher frequencies without which the higher harmonics of the signal may cause instability in the circuit.*

$C5 = \frac{1}{2\pi \times 16k \times 22{,}000Hz} = 0.37nF$. where, Zin = 16k => Impedance looking into the base of transistor.



This figure shows the output waveform of the 2nd stage of the amplifier.

Gain of the amplifier:

1. **Theoretical Gain:**

$$Av = -Rc||Zin(next)/Ze = -\frac{4k||Zin(nxt)}{90 + re} = -\frac{4k||10k}{(90 + 17.33)}$$
$$= \frac{-2.85k}{(90 + 17.33)} = -26.55$$

$Z_{in(nxt)}$ = 20k||20k, as seen from the input of the power amplifier stage.

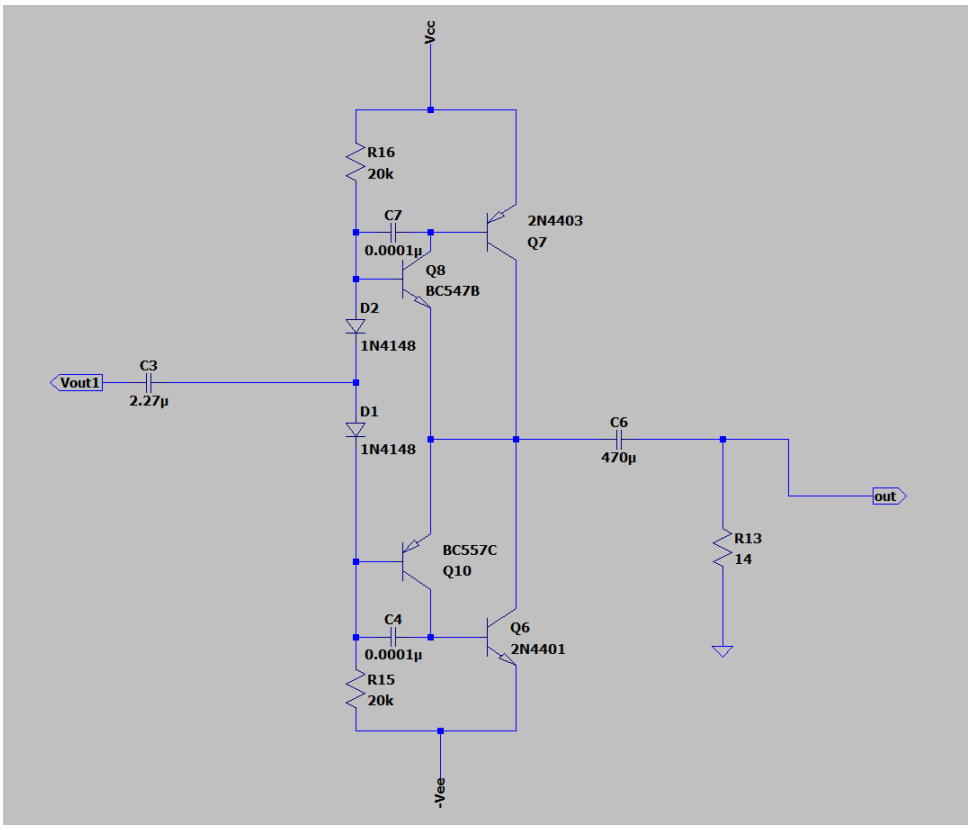
2. **Gain as per simulations:**

$$Av = -8.25V/323.5mV = -25.50$$

Summary: This is the gain stage made with the CE amplifier configuration, along with bootstrap for increased input impedance and a Miller compensation capacitor for gain roll off of high frequency transients that may introduce non-linearities and hence compromise the stability of the amplifier.

Improvements: This stage can be further improved by introducing another complimenting transistor amplifier in parallel with the existing one so that one amplifier works for each cycle this will effectively double the output signal swing and hence, providing room for higher gain.

Stage 3 – Power Amplifier:



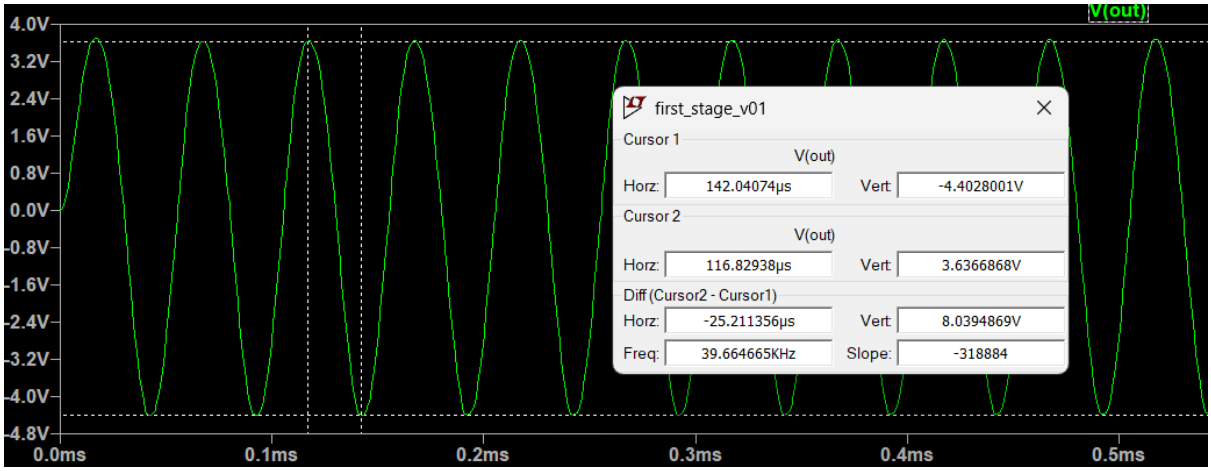
This is the final stage which gives the necessary current gain to drive low impedance loads, like the speaker in this case.

- This configuration or type of power amplifiers are called Class – AB amplifiers.
- This type of amplifier provide better efficiencies than the Class – A amplifiers and better linearity than Class – B amplifiers.
- The Diode's used in the bias network provide the bias to the transistors to keep it just above cut-off region.
- The one used in this case features a Sziklai Pair [made by pnp feeding into npn] these are also called as complimentary feedback pair that effectively square the total gain of the transistor [$\beta 1 \times \beta 2$] but maintaining only diode drop across them.

Design:

1. The output node of the Power Amp before the C6 capacitor referenced at 7.5V and so is the input node at the voltage divider network.

2. The load used is 14 ohms load connected in series with a coupling capacitor that doubles as a current drive assisting device smoothening any spikes by providing current.
3. The voltage divider bias that consists a combination of resistors and diodes provides the necessary bias for keeping the transistors out of cut – off region.
4. The capacitors C7 & C4 are used to roll off (suppress) the transients generated by these transistors when operated such high currents.



This figure shows the output waveform of the 3rd stage of the amplifier.

Summary: This is the last and important stage that is the main driver of the load this is also sometimes called as pre – amp stage. This stage provides very high current gain without which its is impossible to drive low impedance loads.

Improvements: This stage can be further improved by using a Vbe Multiplier instead of the voltage divider bias that provides better temperature stability than the one used here, however the design of the Vbe multiplier is complex. Also the diodes can be replaced with matched transistors for better temp matching so that there wont be thermal run off.

Performance Parameters:

1. **Efficiency**:

DC Power = V_{cc}*(I_c*2/\pi) = 12V*0.17A = 2.14W

AC Power = $V_{rms(out)}$*$I_{c(rms)}$ = (4V*285mA)/2 = .57W

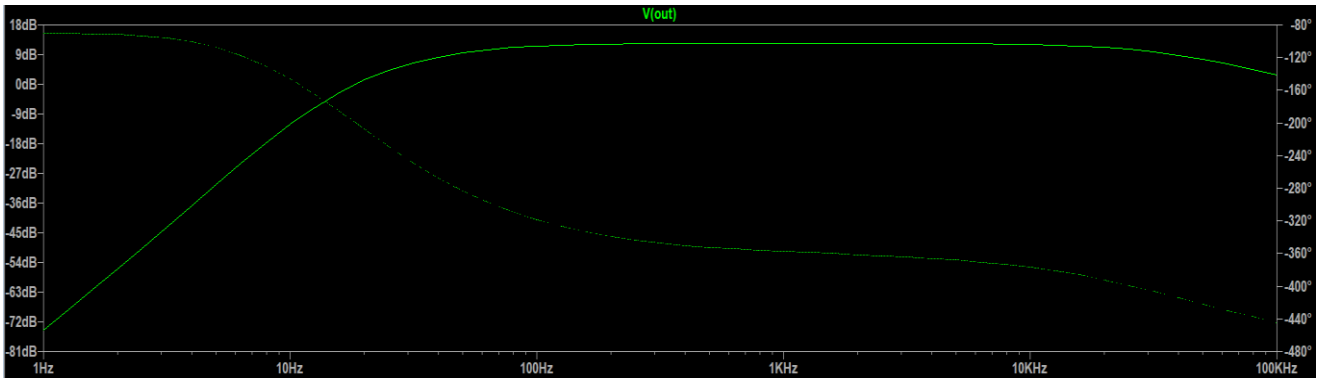
$$Efficiency = AC\frac{Power}{DC}Power$$

$$= \left(\frac{.57}{2.14}\right) * 100$$

$$Efficiency = 26.6\%$$

2. Stability and frequency response:

These parameters can be analyzed using bode plot.

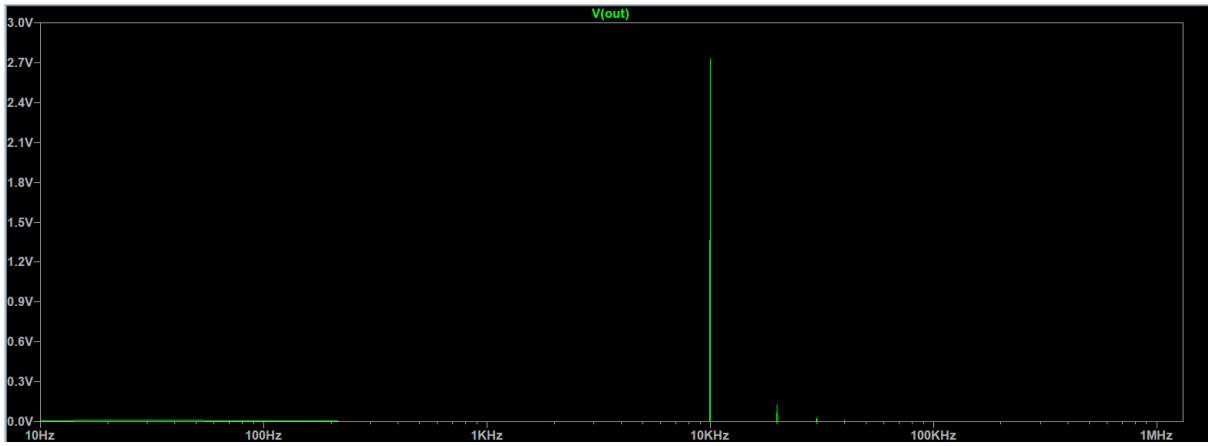


This figure shows the frequency response of the amplifier.

Bode plot data:	**Stability data from Bode plot of the amplifier:**
Lower cut-off Freq: 15.424186Hz	**Gain Margin**: -3.63 dB
Gain: -2.9833089dB	**Phase Margin**: -20 degrees
Phase: -183.49755°	

3. Total Harmonic distortion (THD):

This is measured and computed by performing the FFT of the output signal to check for harmonics the test



This figure shows the FFT of the amplifier output

THD in percentage:

$$\text{THD} = \frac{\sqrt{V_{2(rms)}^2 + V_{3(rms)}^2 + \ldots . + V_{n(rms)}^2}}{V_{1(rms)}} \times 100 = \frac{\sqrt{0.088^2 + 0.025^2 + \ldots . + V_{n(rms)}^2}}{1.97} \times 100$$

$$\text{THD} = \frac{\sqrt{0.088^2 + 0.025^2}}{1.97} \times 100 = 4.64\%$$