Lab9 : Geofence

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Speaker: Justin

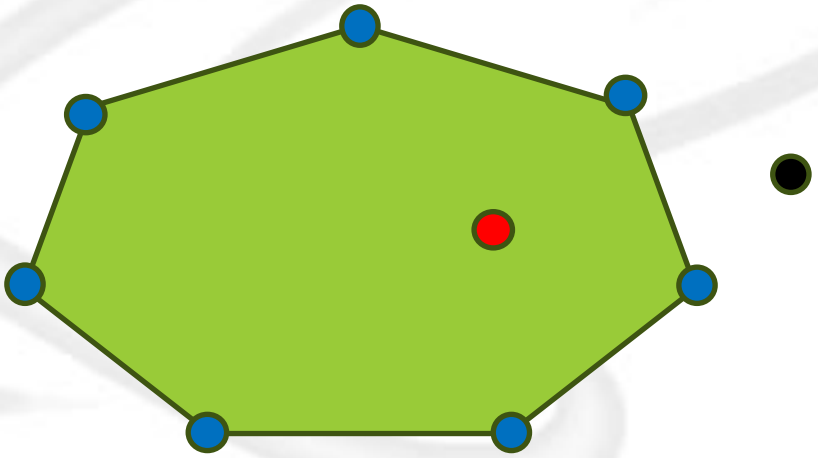
Date: 2024/05/16

Outline

- Introduce to Geofence
- Hardware description
  - Block diagram
  - I/O Information
  - Reference flow for Lab9
- SDC file & testfixture.sv
- Criteria
  - Grading policy
  - Requirement & file format

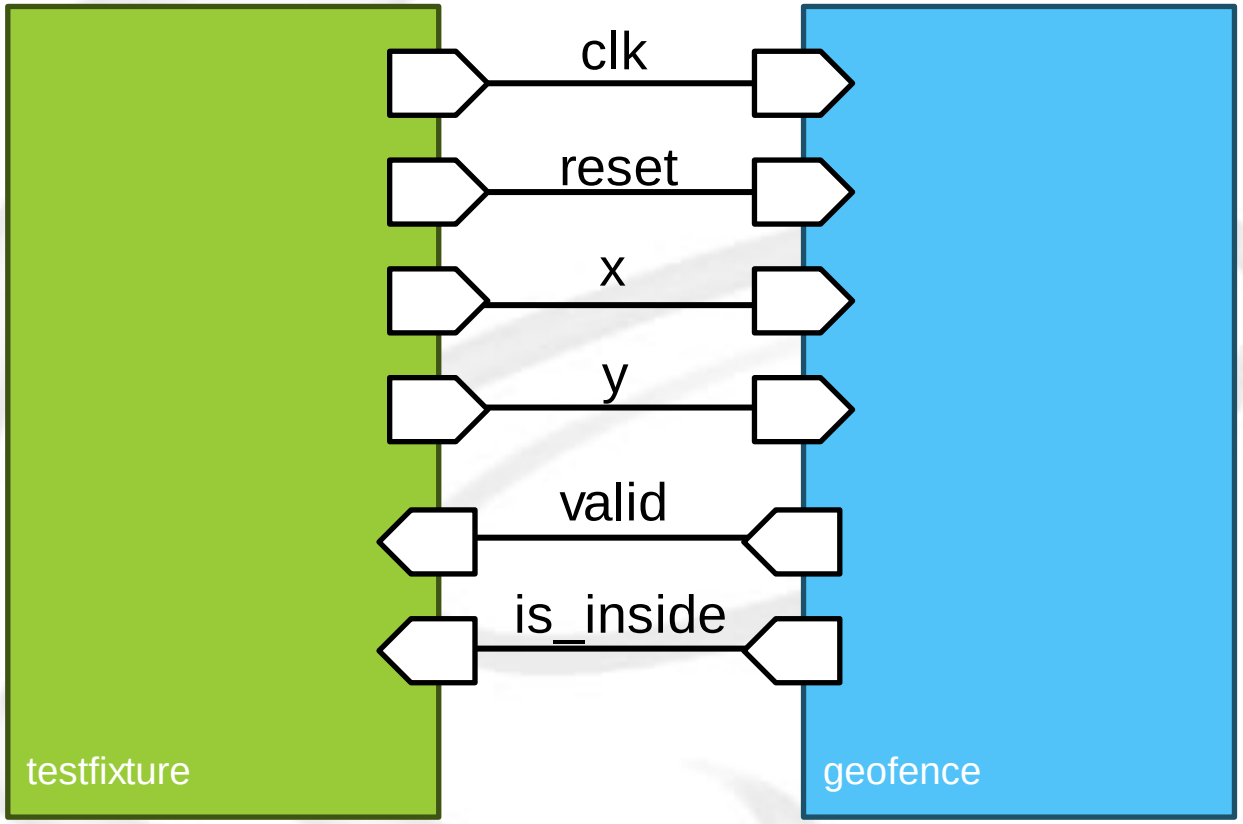
Introduce to Geofence

- This system employs **7 receivers** to construct a virtual convex heptagon on a plane
- Geofence system analyzes whether the object under test is inside or outside based on the coordinates of the **receivers** and the **object** under test



Hardware description

- Block Diagram



Hardware description

I/O Information

Signal	I/O	length	Desc.
clk	I	1	positive-edged triggered
reset	I	1	asynchronous positive-edged triggered
x	I	10	receivers and the object under test coordinate X
y	I	10	receivers and the object under test coordinate Y
valid	O	1	is_inside signal valid, active high
is_inside	O	1	object under test inside or not? 1 for inside, 0 for outside

Hardware description

- I/O Information
  - univ.txt (golden file)
    - 50 objects
    - pattern is_inside
    - object under test coordinate X,Y
    - 7 receivers coordinate X,Y

```
object 1 1
567 975
585 1005
940 758
1005 489
783 68
585 17
95 227
17 614
```

is_inside

object X,Y

receivers X,Y

Hardware description

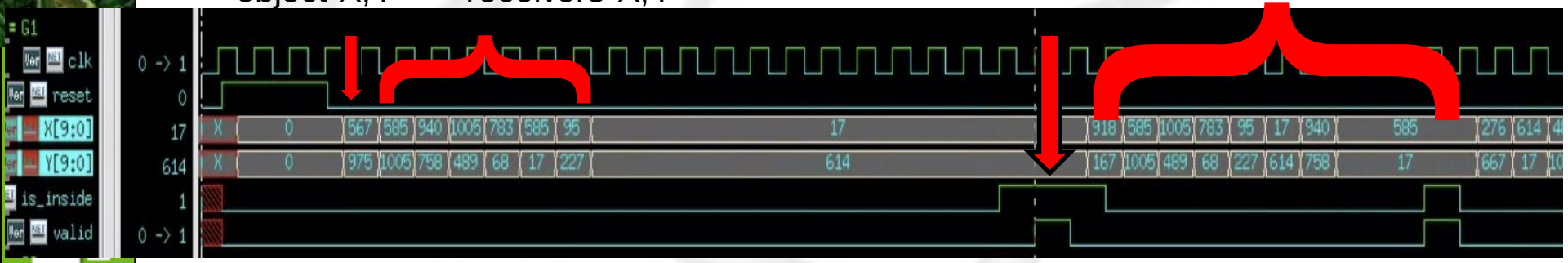
- I/O Information
  - Waveform

```
object 1 1
567 975
585 1005
940 758
1005 489
783 68
585 17
95 227
17 614
```

is_inside

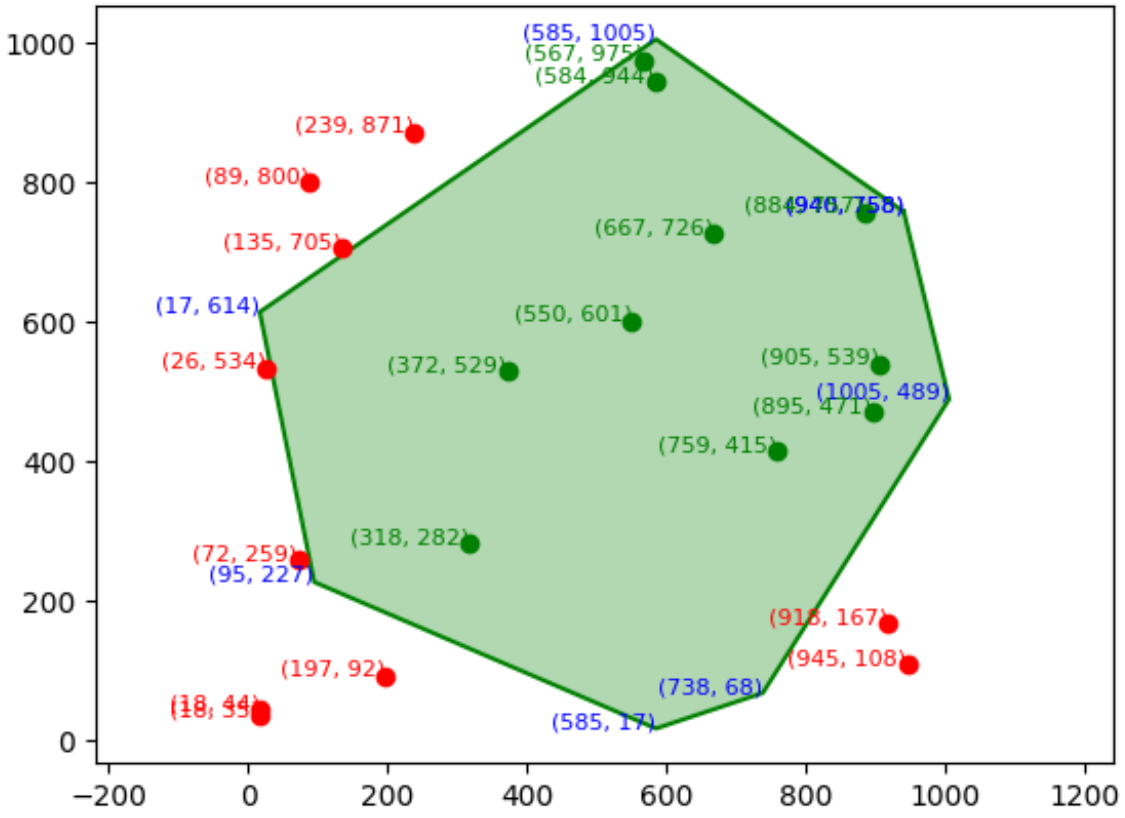
object X,Y

receivers X,Y



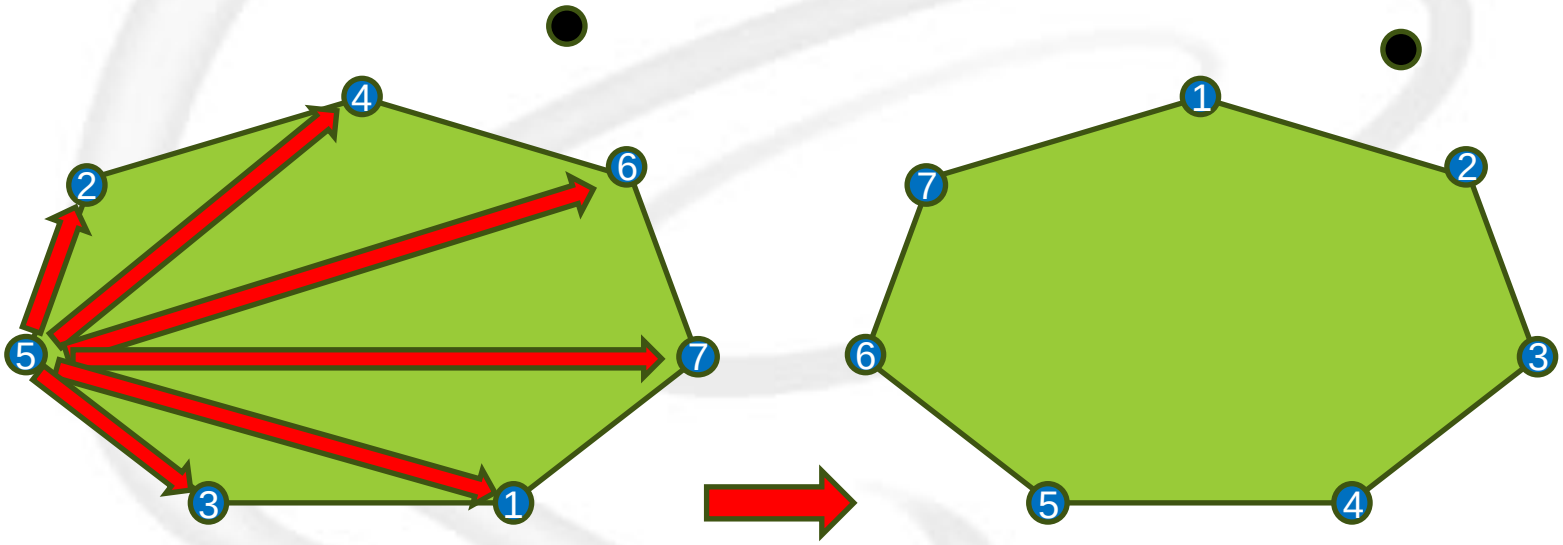
Hardware description

- I/O Information
  - Golden pattern
  - Receivers' order will generate randomly
  - Order may not necessarily be assigned CW or CCW



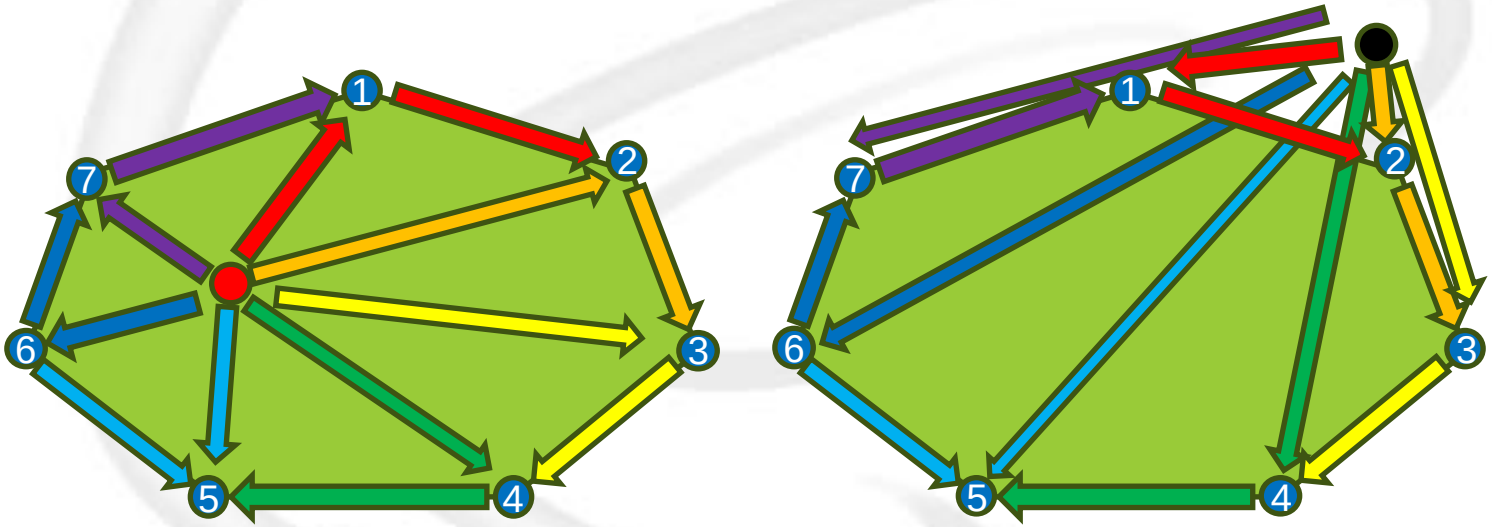
Reference flow for Lab9

- You can reference this algorithm or create a better one by yourself
  - Step 1 sorting receivers to clockwise or counterclockwise
    - ✓ Choose the leftmost point
    - ✓ Calculate the slope with every other receivers
    - ✓ Rearrange the receivers' order



Reference flow for Lab9

- You can reference this algorithm or create a better one by yourself
  - Step 2 Check if the cross products are always positive
    - ✓ Doing cross products sequence in order
    - ✓ If cross products are always positive, object is inside
    - ✓ If some are positive, some are negative, object is not inside



SDC file & testfixture.sv

- Testbench
- You can only modify those red box in testbench
- Simulation screenshot should set check = 0 (if not -10%)

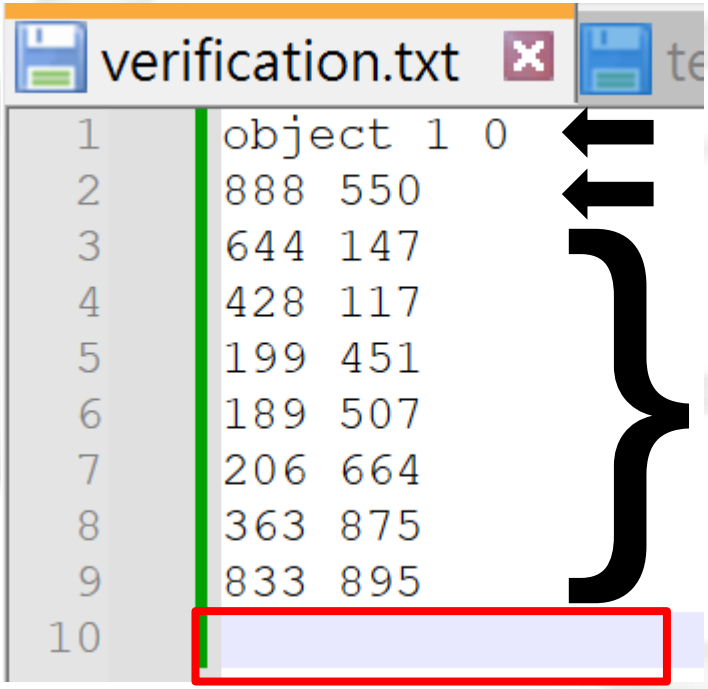
```
`timescale 1ns/10ps
`define CYCLE       16.2
`define End_CYCLE   1000000
//`define PAT         "../../univ.txt"          //Quartus
`define PAT         "../../verification.txt"    //Quartus

//`define PAT         "./univ.txt"              //modelsim
//`define PAT         "./verification.txt"      //modelsim
module testfixture();
integer fd;
integer objnum;
integer obj_isin;
integer charcount;
integer pass=0;
integer fail=0;
string line;
reg [5:0] npoint;
reg [9:0] X;
reg [9:0] Y;

reg check = 0;                          //  0 => no print  1 => print pattern
reg clk = 0;
wire valid;
reg reset =0;
wire is_inside;
```

Choose the pattern you want to test

```
reg check = 1;
reg clk = 0;
wire valid;
```

SDC file & testfixture.sv

- Verification.txt
- Generate your own pattern base on following format
- Please give an explanation in your report
- Generate reasonable & meaningful pattern (corner case of your design), not redundant patterns



SDC file & testfixture.sv

- geofence.sdc
- You can only modify this red box in geofence.sdc
- Do not set this clock period more than 25(ns)
- The “CYCLE” in your TB must be set to match the “clk_period” in your sdc file

```
# operating conditions and boundary conditions #
set clk_period 16.2          //you can only modify this line

#Don't touch the basic environment setting as below

set input_max   [expr { double($clk_period * 0.5) }]
set input_min   [expr { double($clk_period * 0.1) }]
set output_max  [expr { double($clk_period * 0.5) }]
set output_min  [expr { double($clk_period * 0.1) }]

#================================================================
# Setting Clock Constraints
#================================================================
create_clock -name clk  -period $clk_period   [get_ports clk]

set_clock_uncertainty -rise_from [get_clocks clk] -rise_to [get_clocks clk] 0.02
set_clock_uncertainty -rise_from [get_clocks clk] -fall_to [get_clocks clk] 0.02
set_clock_uncertainty -fall_from [get_clocks clk] -rise_to [get_clocks clk] 0.02
set_clock_uncertainty -fall_from [get_clocks clk] -fall_to [get_clocks clk] 0.02

#================================================================
# Setting Design Environment
#================================================================
set_input_delay  -clock clk  -max $input_max  [remove_from_collection [all_inputs] [get_ports clk]]
set_input_delay  -clock clk  -min $input_min  [remove_from_collection [all_inputs] [get_ports clk]]

set_output_delay -clock clk  -max $output_max [all_outputs]
set_output_delay -clock clk  -min $output_min [all_outputs]
```

```
`timescale 1ns/10ps
`define CYCLE      16.2
`define End_CYCLE  1000000
```

Criteria

- Grading policy(100%)
  - Score – simulation with univ.txt pattern (50%)
    - Class S (50 points)
      - Pass == 50/50 (Gate level & RTL)
      - Area <= 1500
    - Class A (40 points)
      - Pass == 50/50 (Gate level & RTL)
      - Area <= 2500
    - Class B (35 points)
      - Pass == 50/50 (Gate level & RTL)
      - Area <= 3000
    - Class C (30 points)
      - Pass == 50/50 (Gate level & RTL)
      - Area > 3000
    - Class D (25 points)
      - Pass == 50/50 (RTL)
    - Class E (15 points)
      - Pass == (45~50)/50 (RTL)
    - Class F (5 points)
      - Pass < 44/50 (RTL)
  - PA(Simulation time * Area) – univ.txt pattern (25%)
  - Report (25%)

Criteria

- Grading policy - Performance & Area (25%)
  - Performance : Simulation time in Gate-Level Simulation
  - Area : Total logic elements + 1000 * embedded Multipliers
  - This 25 points need Gate-Level all pass to attend the PA Ranking
  - Top 10% got 25 points, Top 10%~20% got 22.5 points….

```
# Loading instances from geofence_7_1200mv_85c_v_slow.sdo
# Loading altera_ver.PRIM_GDFF_LOW
# Loading timing data from geofence_7_1200mv_85c_v_slow.sdo
# ** Note: (vsim-3587) SDF Backannotation Successfully Completed.
#    Time: 0 ps  Iteration: 0  Instance: /testfixture File: C:/Users/justi/Documents/NCKU/HDL/geofence/2021_univ_cell/testfixture.sv
#
# add wave *
# view structure
# .main_pane.structure.interior.cs.body.struct
# view signals
# .main_pane.objects.interior.cs.body.tree
# run -all
# ---------------------
# -- Simulation Start --
# ---------------------
# -----------------------------------------------
# --    Simulation finish,  ALL PASS           --
# -----------------------------------------------
# ** Note: $finish    : C:/Users/justi/Documents/NCKU/HDL/geofence/2021_univ_cell/testfixture.sv(144)
#    Time: 15762600 ps  Iteration: 1  Instance: /testfixture
```

You should prove this scream shot is Gate-Level simulation & run in the same cell library case

"Check" in TB should = 0

Simulation time : 15762600(ps)

Flow Summary

<<Filter>>

Flow Status	Successful - Wed May 15 11:50:05 2024
Quartus Prime Version	17.1.0 Build 590 10...017 SJ Lite Edition
Revision Name	geofence
Top-level Entity Name	geofence
Family	Cyclone IV E
Device	EP4CE115F29C7
Timing Models	Final
Total logic elements	665 / 114,480 (< 1 %)
Total registers	261
Total pins	24 / 529 (5 %)
Total virtual pins	0
Total memory bits	0 / 3,981,312 (0 %)
Embedded Multiplier 9-bit elements	2 / 532 (< 1 %)
Total PLLs	0 / 4 (0 %)

Area = 665 + 1000 *2 = 2665

Criteria

- Grading policy - Performance & Area (25%)
- Please update your PA every time you upload your code!!!
- No upload, no PA credit
  - Report can submit individually after submitting your code.

Lab9 geofence - PA google form

  - You can check your PA from the excel link on Moodle

Lab 9 geofence - PA excel report

A	B	C	D	E	F	G
時間戳記	電子郵件地址	Student ID	Score	Gate level simulation time (ps)	Area (Total elements + 1000*embedded 9 bit mul)	Performance * Area
2024/5/15 下午 2:22:51	justin4638@gmail.com	TA test	Class B	15762600	2665	42007329000

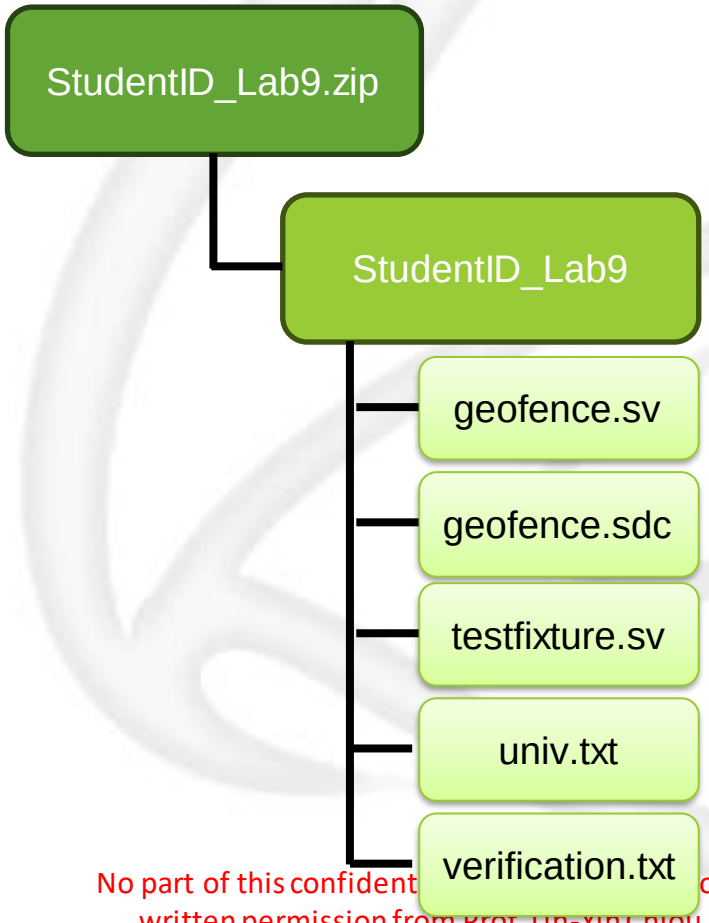
Criteria

- Grading policy – Report (25%)
  - Your Report should include those components
    - Performance & Area table
    - Architecture Diagram (10%)
    - Explain algorithm & how your design works? (25%)
    - RTL & Gate-level simulation result on the terminal. (5%)
    - Screenshot form Quartus (10%, 2% each)
      - ✓ Schematic view of the design netlist
      - ✓ Finite State Machine view
      - ✓ Fmax summery
      - ✓ worst-case timing paths
      - ✓ flow summery
    - Verification (create new pattern in verification.txt) (40%)
      - ✓ Explain the pattern you generate to test your design
      - ✓ Simulation result
    - lesson learned (10%)

Requirement & file format

- File format
- Deadline:2024/05/23 8:59:59

Midterm project code



Midterm project report

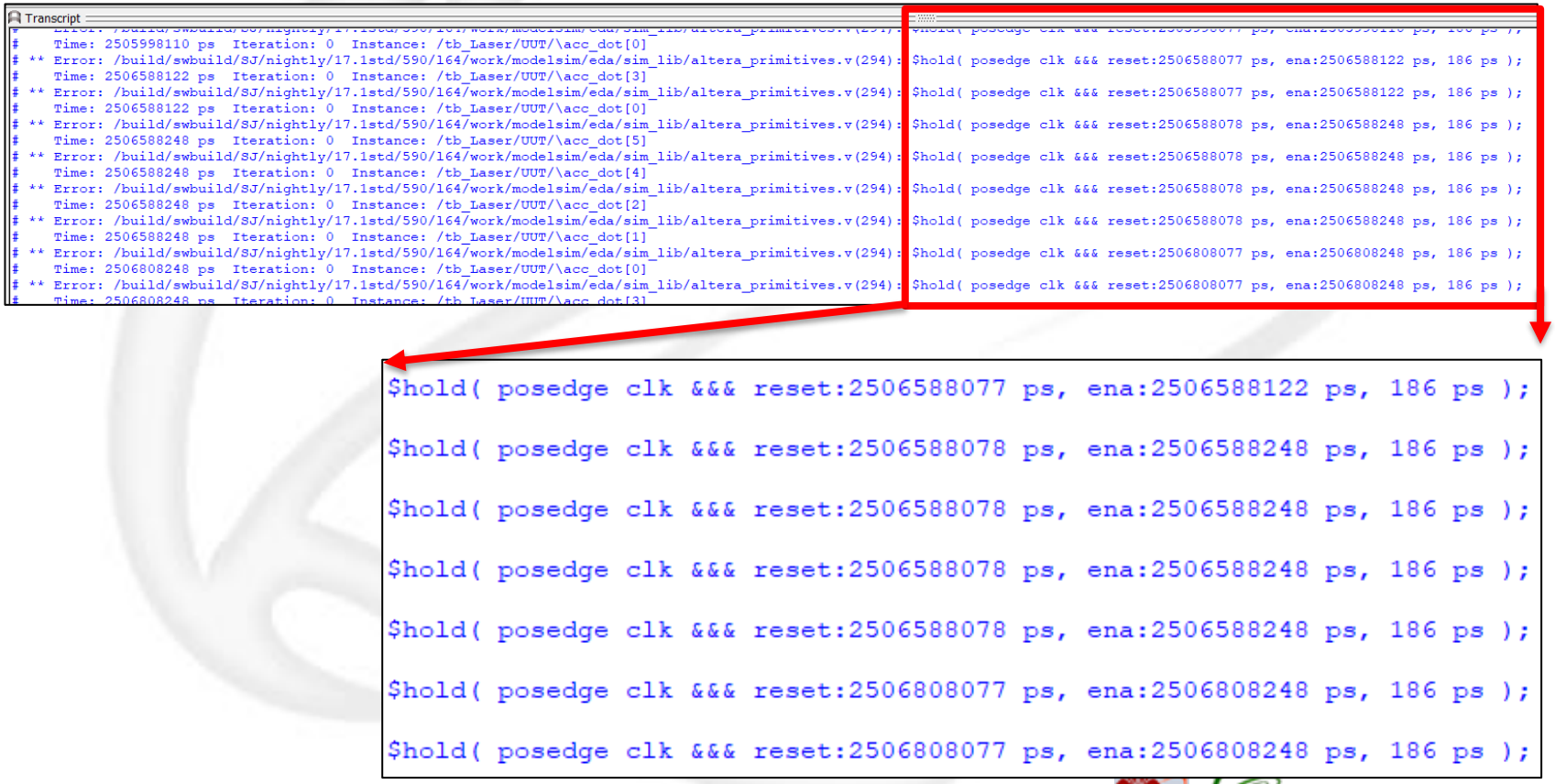
Requirement & file format

Friendly reminder

- Please complete the assignment by your own, discussion with peers is recommended, but do not cheat.
- Warning! Any dishonesty found will result in zero grade.
- Warning! Designing responses tailored to the golden files will result in zero grade.
- Warning! Any late submission will also receive zero.
- Warning! Please make sure that your code can be compiled in Modelsim & Quartus, any dead body that we cannot compile will also receive zero.
- Warning! Please submit your work according to the specified file format, making sure not to include any unnecessary files. Any unnecessary file found, will lead to 10% deduction from the overall score.
- Please start this project As Soon As Possible, Quartus synthesize & Gate Level simulation will take you a lot of time.
- A bad coding style may cause your Gate Level simulation unsuccessful!!!
- **There should be no setup time/hold time violation in your gate-level simulation.**

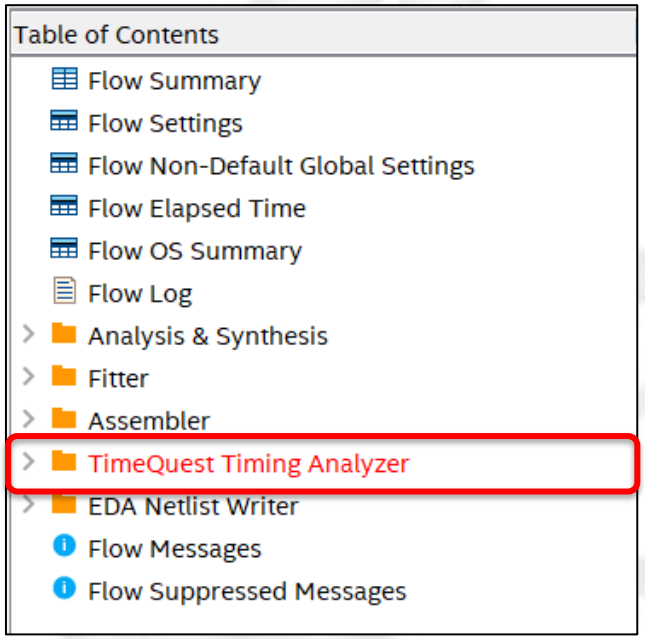
Criteria

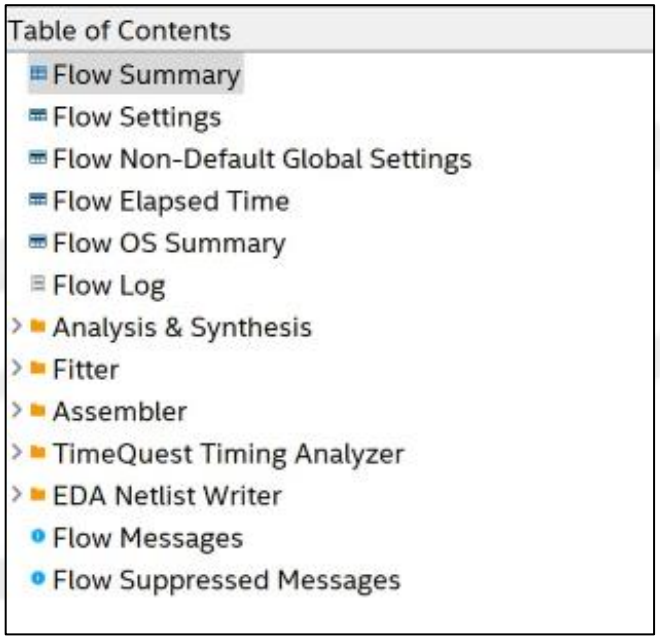
- Simulation result
  - Failed
    - There should be no setup time/hold time violation in your gate-level simulation, as shown in the figure below.



Requirement & file format

- Friendly reminder
  - Table of contents should not have any red symbol.





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Thanks for listening