HDL Digital Design (Graduate Level)
Spring 2024

HOMEWORK
REPORT

Must do self-checking before submission:

☐ Compress all files described in the problem into one zip file.
☐ All files can be compiled under ModelSim environment.
☐ All port declarations comply with I/O port specifications.
☐ Organize files according to File Hierarchy Requirement
☐ No waveform files or project file in deliverables

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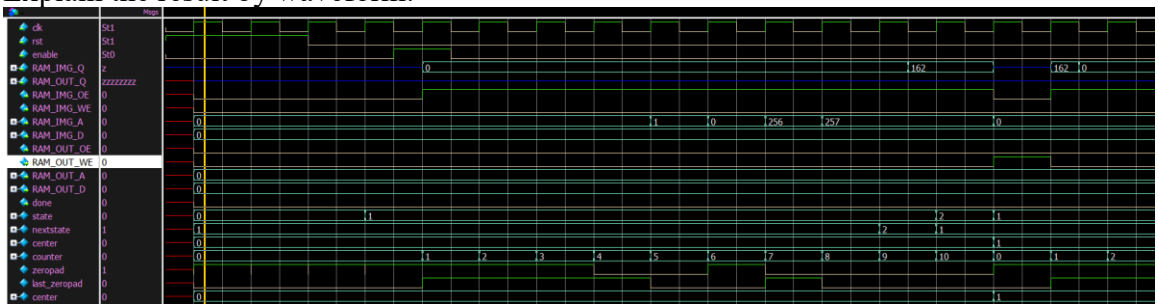
1. Your simulation result on the terminal (Transcript) .

```
#
#
#  ****************************
#  **                        **       |\__||
#  **  Congratulations !!    **      / O.O  |
#  **                        **    /_____   |
#  **  Simulation PASS!!     **   /^ ^ ^ \  |
#  **                        **  |^ ^ ^ ^ |w|
#  ****************************   \m___m__|_|
#
#
# ** Note: $finish    : D:/00_second_under/StudentID_Lab5/tb_median_fliter.sv(163)
#    Time: 7209015 ns  Iteration: 1  Instance: /tb_median_fliter
# 1
# Break in Module tb_median_fliter at D:/00_second_under/StudentID_Lab5/tb_median_fliter.sv line 163
```

2. Explain the result by waveform.



利用 counter 來記數，依序讀取 local window 裡的 9 個 pixel。Center 為圖片的最左上角，直到移動到最右下角的 pixel 就代表結束整過流程。

```
always @(*) begin
  case (counter)
    4'd0: begin
      if(center[15:8]==0 | center[7:0]==0) zeropad = 1;
      else zeropad = 0;
    end
    4'd1: begin
      if(center[15:8]==0) zeropad = 1;
      else zeropad = 0;
    end
    4'd2: begin
      if(center[15:8]==0 | center[7:0]==255) zeropad = 1;
      else zeropad = 0;
    end
    4'd3: begin
      if(center[7:0]==0) zeropad = 1;
      else zeropad = 0;
    end
    4'd4: begin
      zeropad = 0;
    end
    4'd5: begin
      if(center[7:0]==255) zeropad = 1;
      else zeropad = 0;
    end
    4'd6: begin
      if(center[15:8]==255 | center[7:0]==0) zeropad = 1;
      else zeropad = 0;
    end
    4'd7: begin
      if(center[15:8]==255) zeropad = 1;
      else zeropad = 0;
    end
    4'd8: begin
      if(center[15:8]==255 | center[7:0]==255) zeropad = 1;
      else zeropad = 0;
    end
    default: zeropad = zeropad;
  endcase
end

always @(*) begin
  if(~zeropad) begin
    case (counter)
      0,1,2: RAM_IMG_A[15:8] = center[15:8] - 8'd1;
      3,4,5: RAM_IMG_A[15:8] = center[15:8];
      6,7,8: RAM_IMG_A[15:8] = center[15:8] + 8'd1;
    endcase

    case (counter)
      0,3,6: RAM_IMG_A[7:0] = center[7:0] - 8'd1;
      1,4,7: RAM_IMG_A[7:0] = center[7:0];
      2,5,8: RAM_IMG_A[7:0] = center[7:0] + 8'd1;
    endcase
  end
  else RAM_IMG_A = 0;
end
```

利用這兩個 always block 來判斷是否需要 zero padding，並輸出 required address。

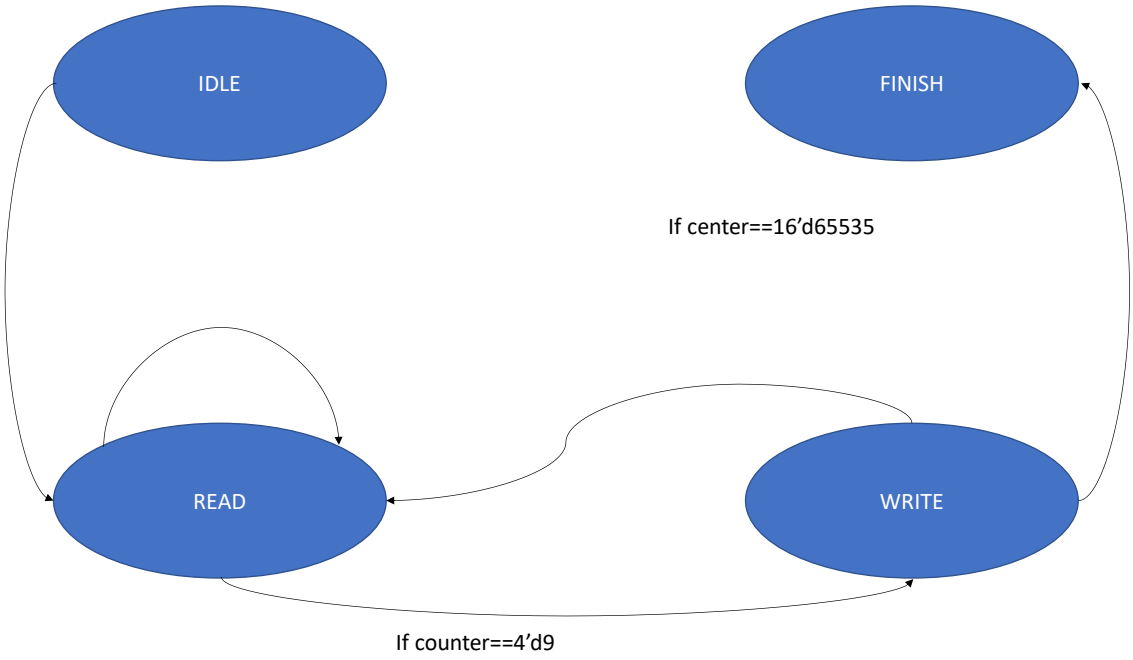
```
READ: begin
  counter <= counter + 1;
  RAM_IMG_OE <= 1;
  RAM_OUT_WE <= 0;
  last_zeropad <= zeropad;

  if(counter>0) begin
    case (counter)
      4'd1: sortNum1_i <= (~last_zeropad)? RAM_IMG_Q : 0;
      4'd2: sortNum2_i <= (~last_zeropad)? RAM_IMG_Q : 0;
      4'd3: sortNum3_i <= (~last_zeropad)? RAM_IMG_Q : 0;
      4'd4: sortNum4_i <= (~last_zeropad)? RAM_IMG_Q : 0;
      4'd5: sortNum5_i <= (~last_zeropad)? RAM_IMG_Q : 0;
      4'd6: sortNum6_i <= (~last_zeropad)? RAM_IMG_Q : 0;
      4'd7: sortNum7_i <= (~last_zeropad)? RAM_IMG_Q : 0;
      4'd8: sortNum8_i <= (~last_zeropad)? RAM_IMG_Q : 0;
      4'd9: sortNum9_i <= (~last_zeropad)? RAM_IMG_Q : 0;
    endcase
  end
end
```

這裡就是把剛剛判斷 zero pad flag 當作條件，判斷放進 reg sort 的值是 0 還是 RAM_IMG_Q。

```
WRITE: begin
  RAM_IMG_OE <= 0;
  counter <= 0;
  RAM_OUT_WE <= 1;
  RAM_OUT_A <= center;
  RAM_OUT_D <= med61;
  center <= center + 1;
end
FINISH: done <= 1;
```

排序的部分就利用 Lab2 的方式，接著就把找到的 median 寫出去，並 center = center + 1，移動到下一個新 pixel，然後就依序反覆上述操作直到結束。

3. Draw the flowchart for your Finite State Machine (FSM).



4. At last, please write the lesson you learned from Lab5.
   更精確的控制 FSM 以及 zero padding。