Lab8: Laser

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Date: 2024/05/02

Outline

- Problem description for Lab8
- Hardware description
  - Block diagram
  - I/O Information
  - Recommend flow in Lab8
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  - Grading policy
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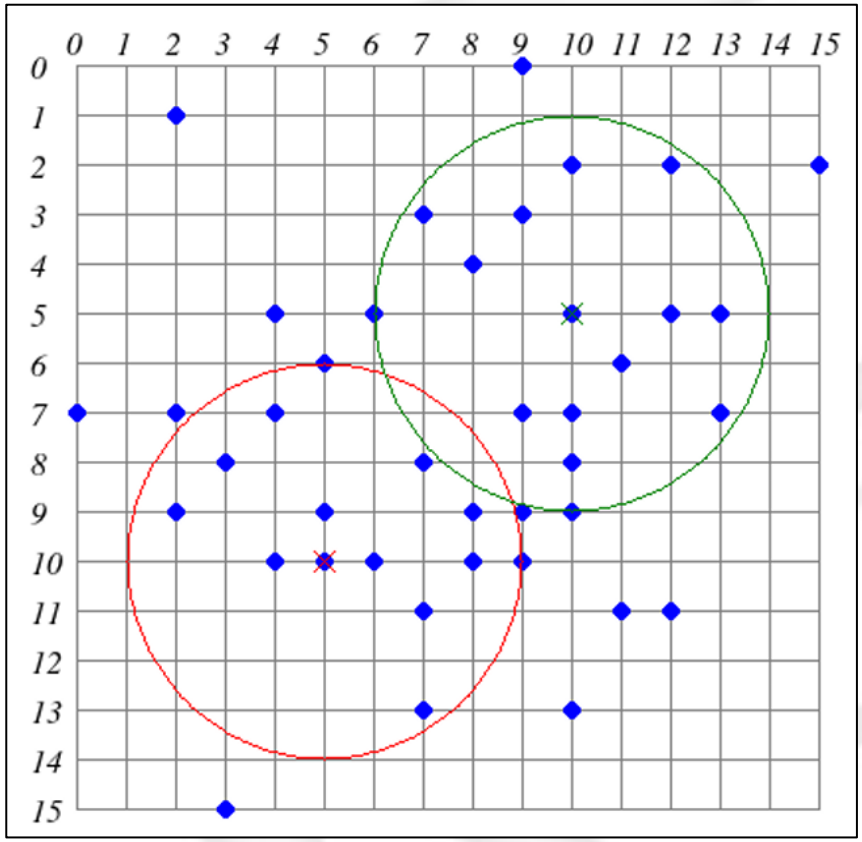
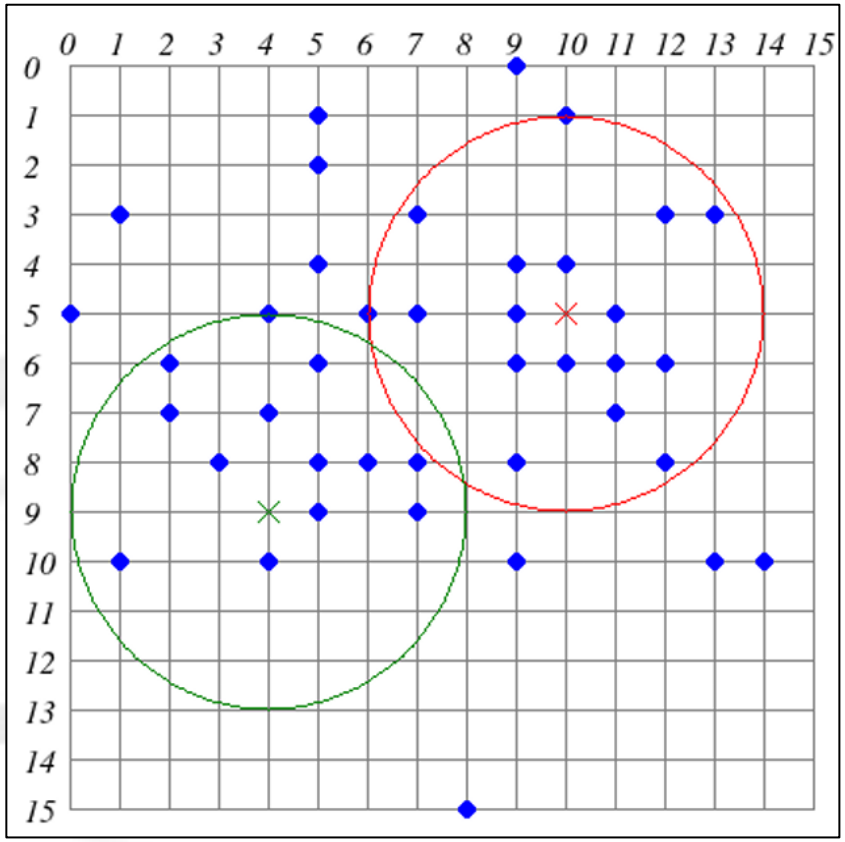
Problem description for Lab8

- It is assumed that are **40 targets** within a fixed area of 16x16 units.
- Only two laser shots are allowed in this area, and the lasers are circular with a **radius of 4 units**.
- The objective is to find the positions of the centers of these two circles to achieve **the maximum coverage** of targets by the circles.
- There are 6 sets of patterns, and when the completion signal (DONE) is received, the next set of patterns will be generated.

Problem description for Lab8

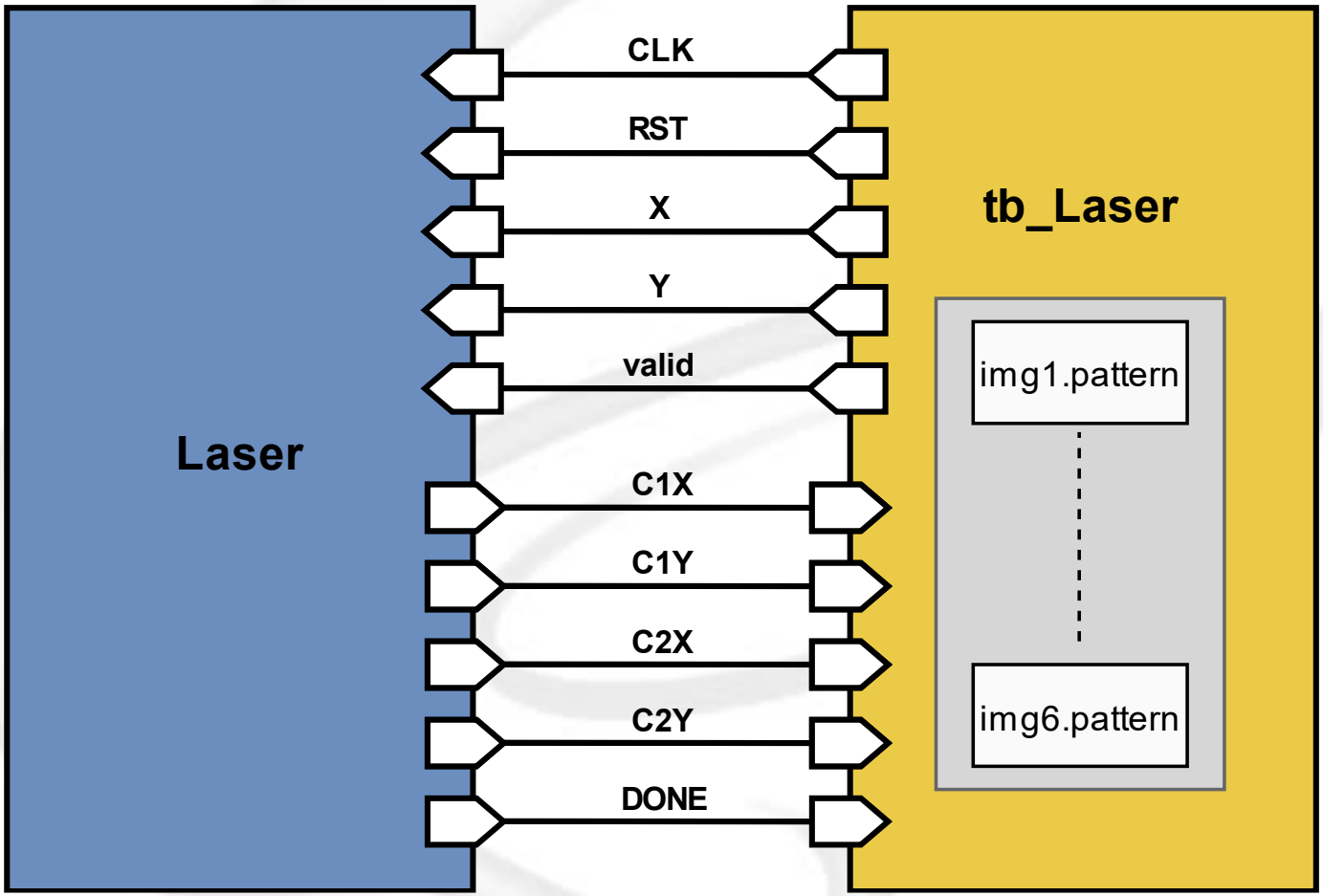
- Ex:





Hardware description

- Block Diagram



Hardware description

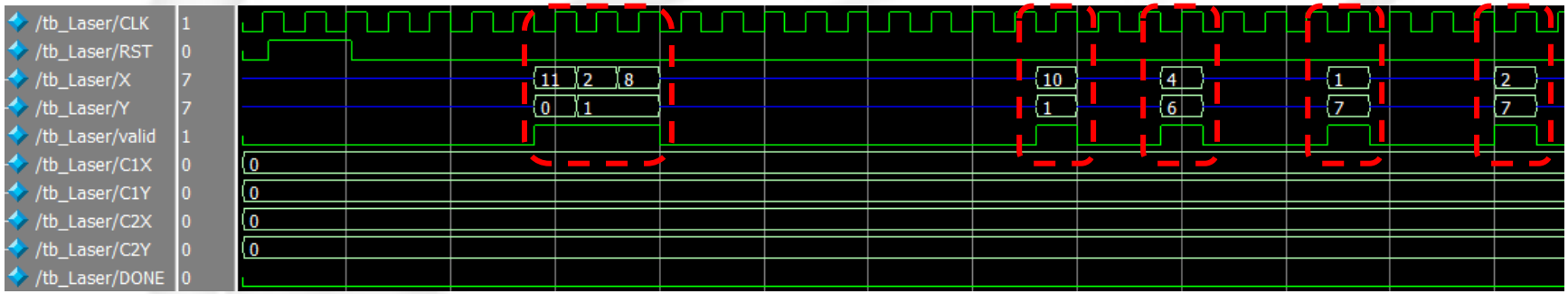
I/O Information

Signal	I/O	width	Desc.
CLK	I	1	positive-edged triggered
RST	I	1	asynchronous positive-edged triggered
valid	I	1	Valid signal of input data
X	I	4	The X-coordinate of the target
Y	I	4	The Y-coordinate of the target
C1X	O	4	X-coordinate of the first point
C1Y	O	4	Y-coordinate of the first point
C2X	O	4	X-coordinate of the second point
C2Y	O	4	Y-coordinate of the second point
DONE	O	1	Finish signal

Unsigned 4-bit integer

Recommend flow in Lab8 (1/3)

- Get input data
  - The X and Y coordinates of the targets in this problem are inputted from ports X and Y.
  - The values of X and Y are considered valid when the 'valid' signal is HIGH.
  - You need to record these 40 sets of coordinates for subsequent calculations.



Recommend flow in Lab8 (2/3)

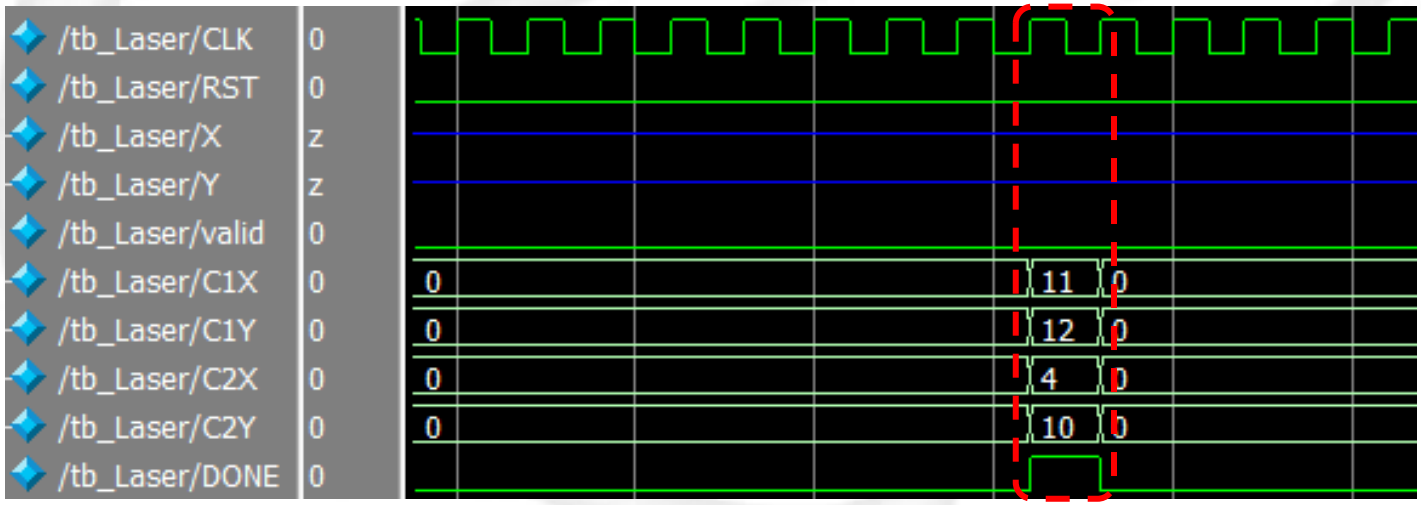
- Calculate the positions of two circles
  - Listing out all possible positions for the two circles takes too much time, but we can work through the problem iteratively.
    - Step1: Find Circle One: Find the center position of the circle that maximizes coverage when there is only one circle.
    - Step2: Fix the position of Circle One and determine the position of Circle Two to maximize coverage.
    - Step3: Keep the position of Circle Two fixed and readjust the position of Circle One to maximize coverage.
    - Step4: Repeat steps 2 and 3 until the results converge.
  - If the distance is exactly equal to 4, it is considered inside the circle. If two circles cover the same target, only one object is counted.

Recommend flow in Lab8 (2/3)

- Notice
  - During steps 2 and 3, when selecting the center position of a circle, there may be multiple choices available. Different selection strategies will affect the convergence speed.
  - The issue with iterative solutions is that they may fall into local stable points, leading to the inability to find the optimal solution.
    - This problem has been excluded in this Lab.
  - For the same set of patterns, there may be multiple combinations where the coverage can reach its maximum value, and any one of these combinations is considered the optimal solution.

Recommend flow in Lab8 (3/3)

- Output the coordinates of two circles
  - The calculation result is sent through ports C1X, C1Y, C2X, C2Y, while simultaneously raising the DONE signal.
  - When the testbench receives the DONE signal, it will start calculating the number of covered targets.



SDC file

- You can only modify this red box in “Laser.sdc”

Laser.sdc | tb_Laser.sv | Laser.sv | Compilation Report - Laser

```
1  # operating conditions and boundary conditions #
2
3  set clk_period 12.33
4
5
6  #Don't touch the basic environment setting as below
7
8  set input_max   [expr { double($clk_period * 0.5) }]
9  set input_min   [expr { double($clk_period * 0.1) }]
10 set output_max  [expr { double($clk_period * 0.5) }]
11 set output_min  [expr { double($clk_period * 0.1) }]
12
13 #================================================================
14 # Setting Clock Constraints
15 #================================================================
16 create_clock -name CLK  -period $clk_period   [get_ports CLK]
17
18 set_clock_uncertainty -rise_from [get_clocks CLK] -rise_to [get_clocks CLK] 0.02
19 set_clock_uncertainty -rise_from [get_clocks CLK] -fall_to [get_clocks CLK] 0.02
20 set_clock_uncertainty -fall_from [get_clocks CLK] -rise_to [get_clocks CLK] 0.02
21 set_clock_uncertainty -fall_from [get_clocks CLK] -fall_to [get_clocks CLK] 0.02
22
23 #================================================================
24 # Setting Design Environment
25 #================================================================
26 set_input_delay  -clock CLK  -max $input_max  [remove_from_collection [all_inputs] [get_ports CLK]]
27 set_input_delay  -clock CLK  -min $input_min  [remove_from_collection [all_inputs] [get_ports CLK]]
28
29 set_output_delay -clock CLK  -max $output_max [all_outputs]
30 set_output_delay -clock CLK  -min $output_min [all_outputs]
```

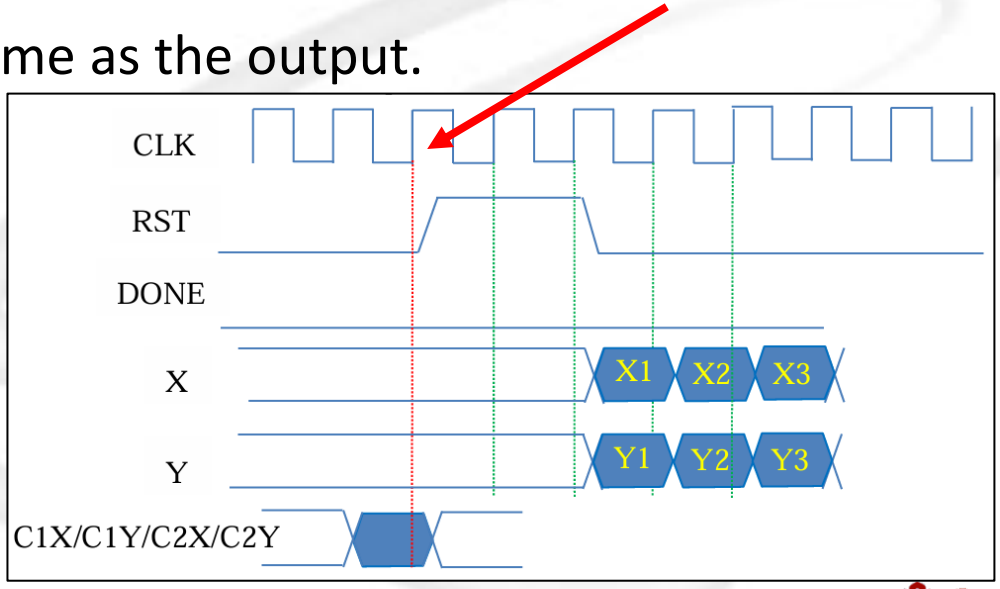
tb_Laser.sv

- You can only modify those red boxes in “tb_Laser.sv”

```
1   `timescale 1ns/10ps
2
3   `define CYCLE 12.33 // Modify your clock period here !!
4
5   `define MAX_CYCLE_PER_PATTERN 50000
6
7   //`define PatternPATH "../../pattern/"  // Open in Quartus
8
9   `define PatternPATH "./pattern/"      // Open in Modelsim
10
11  `define printMap 0 // You can set it to 1 to print out the map
```

Criteria

- Output within a specified time limit
  - The maximum number of calculation cycles for each test pattern is 50,000 cycles.
  - If the DONE signal is not raised within this time, the testbench will automatically capture the content of C1X, C1Y, C2X, C2Y at that time as the output.



Criteria

Simulation result

➔ Pass -> Cover total = 170 (Summation of cover number in pattern1~6)

```
VSIM 59> run -all
# ********************************
# **      Simulation Start      **
# ********************************
# ======================== PATTERN img1.pattern ========================
# ---- Used Cycle:        4554 ----
# ---- Get Return: C1( 4,10),C2(11,12) ----
# ---- cover =  30, optimum =  30
# ======================== PATTERN img2.pattern ========================
# ---- Used Cycle:        6605 ----
# ---- Get Return: C1( 5,11),C2(11, 6) ----
# ---- cover =  28, optimum =  28
# ======================== PATTERN img3.pattern ========================
# ---- Used Cycle:        6605 ----
# ---- Get Return: C1( 5,10),C2(10, 5) ----
# ---- cover =  29, optimum =  29
# ======================== PATTERN img4.pattern ========================
# ---- Used Cycle:        6605 ----
# ---- Get Return: C1( 4, 9),C2(10, 5) ----
# ---- cover =  30, optimum =  30
# ======================== PATTERN img5.pattern ========================
# ---- Used Cycle:        6605 ----
# ---- Get Return: C1(10,11),C2( 2,11) ----
# ---- cover =  23, optimum =  23
# ======================== PATTERN img6.pattern ========================
# ---- Used Cycle:        4554 ----
# ---- Get Return: C1( 9, 9),C2(13, 2) ----
# ---- cover =  30, optimum =  30
#
# Your clock period: 12.33 ns
# ********************************
# **    Finish Simulation       **
# **    RUN CYCLE =   36685     **
# **    RUN TIME  =   452326 ns **
# **    Cover total = 170/170   **
# ********************************
```

Every cover number in pattern 1~6 will be printed on the transcript

!!!!!!! The “CYCLE” in your tb_Laser.sv file must be set to match the “clk_period” in your Laser.sdc file !!!!!!!

Criteria

- Simulation result
  - ➔ Failed -> Cover total < 170

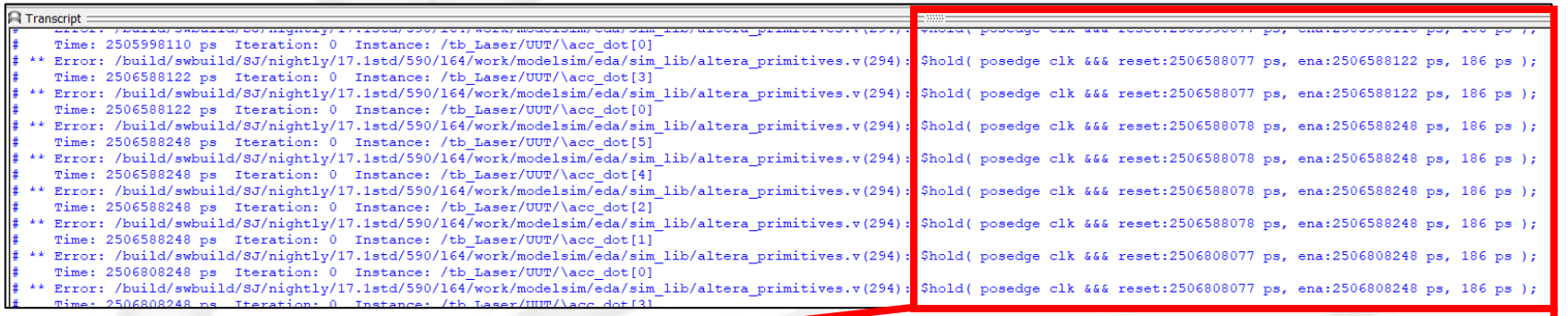
```
# ==== PATTERN img6.pattern ====
# ---- Used Cycle:        5441 ----
# ---- Get Return: C1( 9, 6),C2(14, 1) ----
# ---- cover =  29, optimum =  30
#     0 1 2 3 4 5 6 7 8 9 a b c d e f
#   0 - - + - - - - - - - - - - x - x
#   1 - - - - - - - - - - - x - - x * -
#   2 - - - - - - - - - - x - - - - - x
#   3 - - + - - - - - - - - x - - - - x
#   4 - - - - + - - x - - x - x x - - -
#   5 - - - - - - - - - - x - - x - - -
#   6 - - - - - - - - x x X x - - - - -
#   7 - + - - - - - - - x - x x - - - +
#   8 - - - - - - - - x - - x - - - - -
#   9 - - - - - - - - x x x x x - - - -
#   a - - - - - - - - - + x - - - - + -
#   b - - - - - - - - - - - + - - - - -
#   c - - - - - - - + - - - - - - - - -
#   d - - - - - - - - - - - - - + - - -
#   e - + - - - - - - - - - - - - - - -
#   f - - - - - - - - - - - - - - - - -
#
#
# ********************************
# **    Finish Simulation       **
# **    RUN CYCLE =  33803      **
# **    Cover total = 156/170   **
# ********************************
# ** Note: $finish    : E:/HDL_course_prepare/Lab8_Laser/tb_Laser.sv(236)
#    Time: 270420 ns  Iteration: 1  Instance: /tb_Laser
```

```
1   `timescale 1ns/10ps
2
3   `define CYCLE 12.33 // Modify your clock period here !!
4
5   `define MAX_CYCLE_PER_PATTERN 50000
6
7   `define PatternPATH "../../pattern/"  // Open in Quartus
8
9   //`define PatternPATH "./pattern/"      // Open in Modelsim
10
11  `define printMap 0 // You can set it to 1 to print out the map
12
13  module tb_Laser;
14
15  parameter pat_number = 6;
16
17  integer fd;
18  string  line;
19
20  logic        CLK;
21  logic        RST;
22  logic [3:0]    x;
```

symbol	Desc.
-	No target
+	Target uncovered
x	Target covered
X	Center position coincides with target
*	Center position does not coincide with target

Criteria

- Simulation result
  - Failed
    - There should be no setup time/hold time violation in your gate-level simulation, as shown in the figure below.




```
$hold( posedge clk &&& reset:2506588077 ps, ena:2506588122 ps, 186 ps );
$hold( posedge clk &&& reset:2506588078 ps, ena:2506588248 ps, 186 ps );
$hold( posedge clk &&& reset:2506588078 ps, ena:2506588248 ps, 186 ps );
$hold( posedge clk &&& reset:2506588078 ps, ena:2506588248 ps, 186 ps );
$hold( posedge clk &&& reset:2506588078 ps, ena:2506588248 ps, 186 ps );
$hold( posedge clk &&& reset:2506808077 ps, ena:2506808248 ps, 186 ps );
$hold( posedge clk &&& reset:2506808077 ps, ena:2506808248 ps, 186 ps );
```

Criteria

Score – Part1(65%)

➔ Your designs will be categorized into seven levels, namely Class A ~ Class G.

- Class A (65 points)
  - Cover total **= 170/170** (RTL & Gate-level simulation)
  - RUN CYCLE **< 50,000**
- Class B (55 points)
  - Cover total **= 170/170** (RTL & Gate-level simulation)
  - RUN CYCLE **: 50,000 ~ 100,000**
- Class C (45 points)
  - Cover total **= 170/170** (RTL & Gate-level simulation)
  - RUN CYCLE **: 100,000 ~ 150,000**
- Class D (35 points)
  - Cover total **= 170/170** (RTL & Gate-level simulation)
  - RUN CYCLE **: 150,000 ~ 200,000**
- Class E (25 points)
  - Cover total **= 170/170** (RTL & Gate-level simulation)
  - RUN CYCLE **> 200,000**
- Class F (15 points)
  - Cover total **: (160 ~ 169)/170** (RTL & Gate-level simulation)
- Class G (5 points)
  - Cover total **: (< 160)/170** (RTL & Gate-level simulation)

```
# ********************************
# **    Finish Simulation       **
# **    RUN CYCLE =   36685     **
# **    RUN TIME  =   452326 ns **
# **    Cover total = 170/170   **
# ********************************
# ** Note: $finish    : E:/HDL_cou
#    Time: 452686730 ps  Iteration
```

Criteria

Score – Part2(25%)

- PA (Performance & Area) Ranking.
- This 25 points need Gate-Level all pass (Cover total = 170) to attend the PA Ranking.
- We will multiply "RUN TIME" by "Total logic elements" as the sorting index. The top 1st to 4th will receive 25 points, the 5th to 8th will receive 24 points, and so on (**The score will decrease by one point for every four people**). From the 96th to the 99th, only 1 point will be awarded, while those ranked 100th or later will receive **0** points.

```
# ********************************
# **    Finish Simulation       **
# **    RUN CYCLE =   36685     **
# **    RUN TIME  =   452326 ns **
# **    Cover total = 170/170   **
# ********************************
# ** Note: $finish    : E:/HDL_cou
#    Time: 452686730 ps  Iteration
```

Flow Status	Successful - Sat Apr 27 23:46:45 2024
Quartus Prime Version	17.1.0 Build 590 10/25/2017 SJ Lite Edition
Revision Name	Laser
Top-level Entity Name	Laser
Family	Cyclone IV E
Device	EP4CE115F29C7
Timing Models	Final
Total logic elements	678 / 114,480 (< 1 %)
Total registers	417
Total pins	28 / 529 (5 %)
Total virtual pins	0
Total memory bits	0 / 3,981,312 (0 %)
Embedded Multiplier 9-bit elements	0 / 532 (0 %)
Total PLLs	0 / 4 (0 %)

Criteria

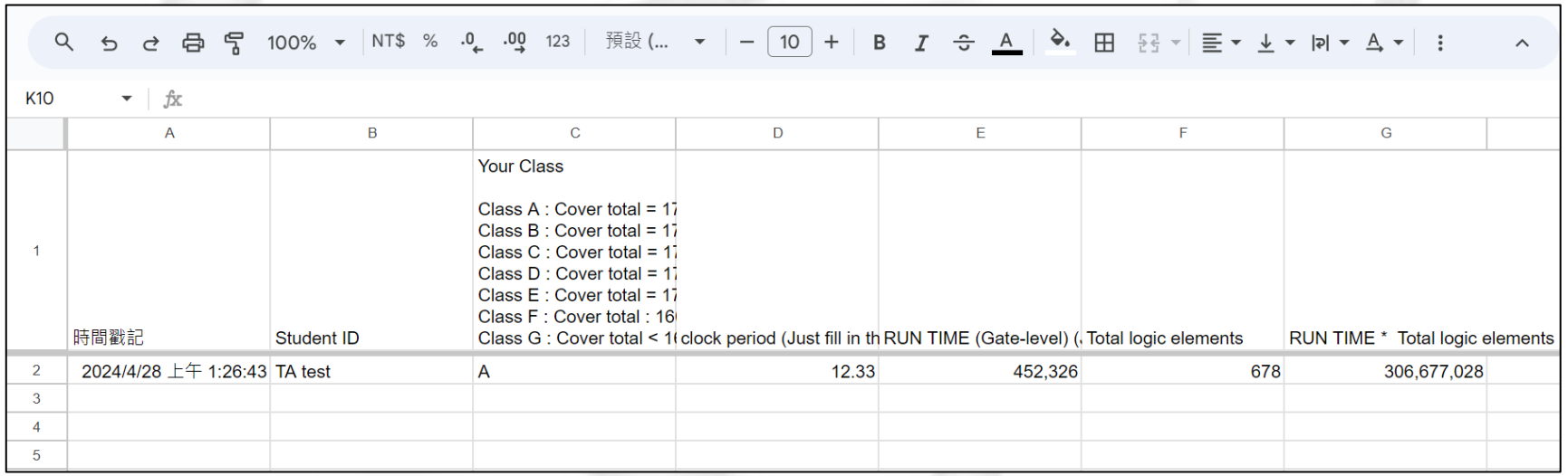
Score – Part2(25%)

- Please update your PA every time you upload your code!!!

Lab8 (Laser) Performance & Area google form link

- You can check your PA from the excel link

Lab8 (Laser) Performance & Area excel report link



K10

	A	B	C	D	E	F	G
1	時間戳記	Student ID	Your Class Class A : Cover total = 17 Class B : Cover total = 17 Class C : Cover total = 17 Class D : Cover total = 17 Class E : Cover total = 17 Class F : Cover total : 16 Class G : Cover total < 1(	clock period (Just fill in th	RUN TIME (Gate-level) (.	Total logic elements	RUN TIME * Total logic elements
2	2024/4/28 上午 1:26:43	TA test	A	12.33	452,326	678	306,677,028
3							
4							
5							

Criteria

Score – Part3(10%)

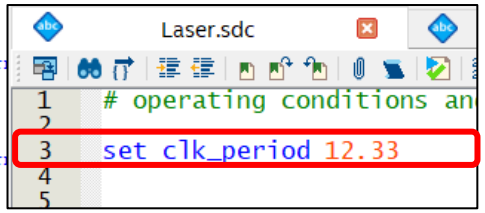
Report

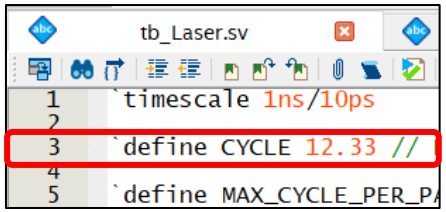
- Performance & Area table (1%)
- RTL & Gate-level simulation result on the terminal. (1%)
- Draw the flowchart for your Finite State Machine (FSM). (1%)
- Explain how your design works? (1%)
- What is your strategy to get a batter Performance? (1%)
- Screenshot from Quartus
  - flow summery (1%)
  - worst-case timing paths (1%)
  - Schematic view of the design netlist (1%)
  - Fmax summary (1%)
- Lesson learned from this Lab. (1%)

Criteria

```
# Loading instances from Laser_7_1200mv_85c_v_slow.sdo
# Loading altera_ver.PRIM_GDFF_LOW
# Loading timing data from Laser_7_1200mv_85c_v_slow.sdo
# ** Note: (vsim-3587) SDF Backannotation Successfully Completed.
#    Time: 0 ps  Iteration: 0  Instance: /tb_Laser File: E:/HDL_course_prepare/Lab8_Laser_QuartusProj/tb_Laser.sv
#
# add wave *
# view structure
# .main_pane.structure.interior.cs.body.struct
# view signals
# .main_pane.objects.interior.cs.body.tree
# run -all
# ********************************
# **      Simulation Start      **
# ********************************
# ======================== PATTERN img1.pattern ========================
# ---- Used Cycle:       4554 ----
# ---- Get Return: C1( 4,10),C2(11,12) ----
# ---- cover =  30, optimum =  30
# ======================== PATTERN img2.pattern ========================
# ---- Used Cycle:       6605 ----
# ---- Get Return: C1( 5,11),C2(11, 6) ----
# ---- cover =  28, optimum =  28
# ======================== PATTERN img3.pattern ========================
# ---- Used Cycle:       6605 ----
# ---- Get Return: C1( 5,10),C2(10, 5) ----
# ---- cover =  29, optimum =  29
# ======================== PATTERN img4.pattern ========================
# ---- Used Cycle:       6605 ----
# ---- Get Return: C1( 4, 9),C2(10, 5) ----
# ---- cover =  30, optimum =  30
# ======================== PATTERN img5.patter
# ---- Used Cycle:       6605 ----
# ---- Get Return: C1(10,11),C2( 2,11) ----
# ---- cover =  23, optimum =  23
# ======================== PATTERN img6.patter
# ---- Used Cycle:       4554 ----
# ---- Get Return: C1( 9, 9),C2(13, 2) ----
# ---- cover =  30, optimum =  30
#
# Your clock period: 12.33 ns
# ********************************
# **    Finish Simulation       **
# **    RUN CYCLE =  36685      **
# **    RUN TIME  =  452326 ns  **
# **    Cover total = 170/170   **
# ********************************
```

You should prove this screenshot is
Gate-Level simulation & run in the same corner case





!!!!!!! The “CYCLE” in your tb_Laser.sv file must be set to match the “clk_period” in your Laser.sdc file !!!!!!!

Lab8 Requirement & file format

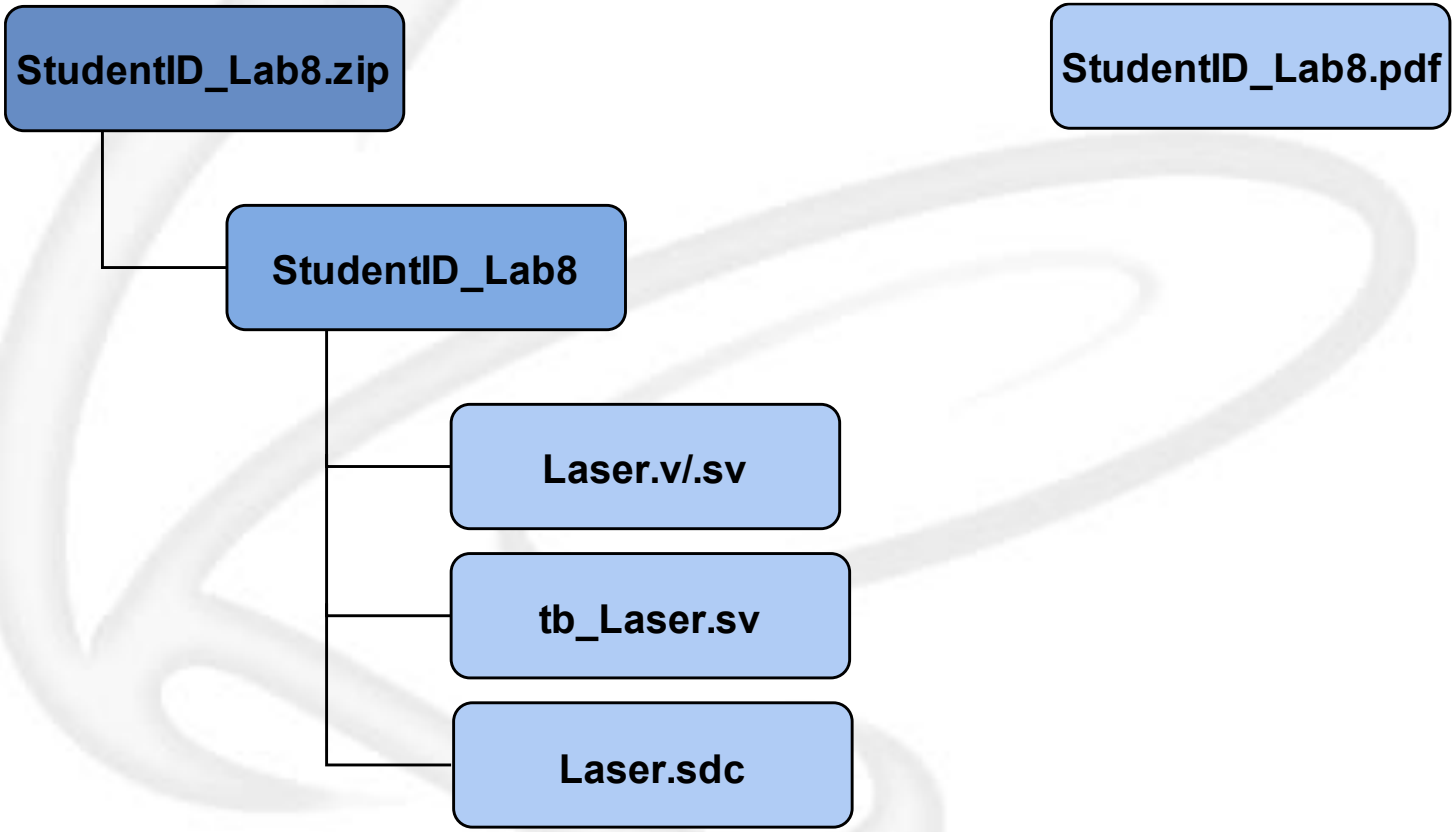
- You must finish Laser.v/.sv and pass all patterns
- For Lab8, you need to submit
  - Laser.v / Laser.sv
  - Laser.sdc
  - tb_Laser.sv
  - StudentID_Lab8.pdf
- Deadline:2024/05/09 08:59 a.m. (No late submission)

Lab8 Requirement & file format

File format

project code

project report

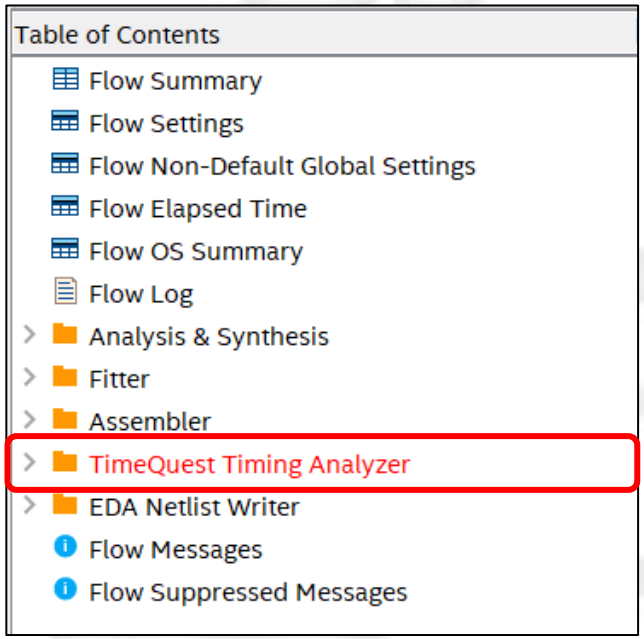


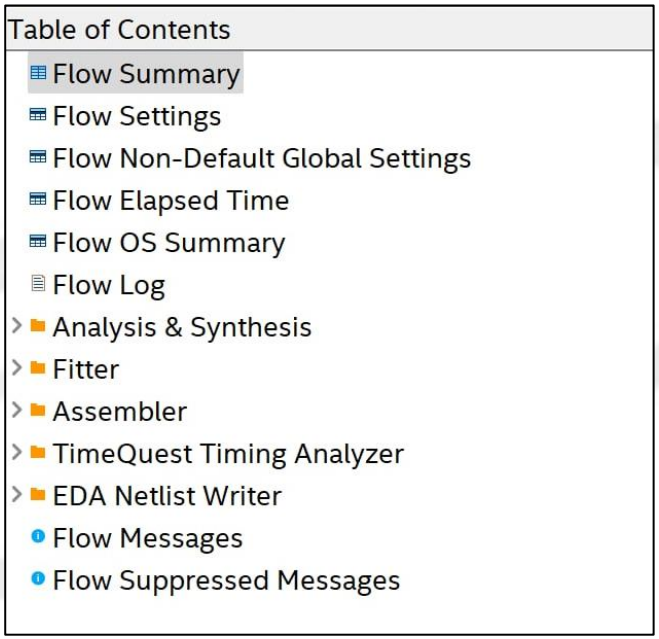
Requirement & file format

- Friendly reminder
  - Please complete the assignment by your own, discussion with peers is recommended, but do not cheat.
  - Warning! Any dishonesty found will result in zero grade.
  - Warning! Designing responses tailored to the golden files will result in zero grade.
  - Warning! Any late submission will also receive zero.
  - Warning! Please make sure that your code can be compiled in Modelsim & Quartus, any dead body that we cannot compile will also receive zero.
  - Warning! Please submit your work according to the specified file format, making sure not to include any unnecessary files. Any unnecessary file found, will lead to 10% deduction from the overall score.
  - Please start this project As Soon As Possible, Quartus synthesize & Gate Level simulation will take you a lot of time.
  - A bad coding style may cause your Gate Level simulation unsuccessful!!!
  - **There should be no setup time/hold time violation in your gate-level simulation.**

Requirement & file format

- Friendly reminder
  - Table of contents should not have any red symbol.





Thanks for listening