CSD23203W 8 V P-Channel NexFET™ Power MOSFET

1 Features

- Ultra-Low Q_g and Q_{gd}
- Low $R_{DS(on)}$
- Small Footprint
- Low Profile 0.62 mm Height
- Pb Free
- RoHS Compliant
- Halogen Free
- CSP 1 × 1.5 mm Wafer Level Package

2 Applications

- Battery Management
- Load Switch
- Battery Protection

3 Description

This 16.2 mΩ, –8 V, P-Channel device is designed to deliver the lowest on-resistance and gate charge in a small 1.0 × 1.5 mm outline with excellent thermal characteristics in an ultra-low profile.

Product Summary

T_A = 25°C		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	–8		V
Q_g	Gate Charge Total (–4.5 V)	4.9		nC
Q_{gd}	Gate Charge Gate-to-Drain	0.6		nC
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = –1.8 V	35.0	mΩ
		V_{GS} = –2.5 V	22.0	mΩ
		V_{GS} = –4.5 V	16.2	mΩ
$V_{GS(th)}$	Voltage Threshold	–0.8		V

Ordering Information(1)

Device	Qty	Media	Package	Ship
CSD23203W	3000	7-Inch Reel	1.0 mm × 1.5 mm Wafer Level Package	Tape and Reel
CSD23203WT	250	7-Inch Reel		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

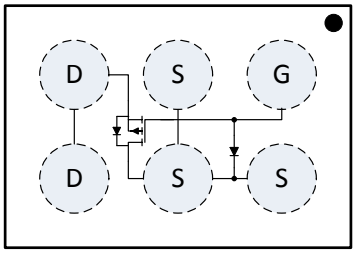
Absolute Maximum Ratings

T_A = 25°C		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	–8	V
V_{GS}	Gate-to-Source Voltage	–6	V
I_D	Continuous Drain Current(1)	–3.0	A
I_{DM}	Pulsed Drain Current(2)	–54	A
P_D	Power Dissipation	0.75	W
T_J, T_{stg}	Operating Junction and Storage Temperature Range	–55 to 150	°C

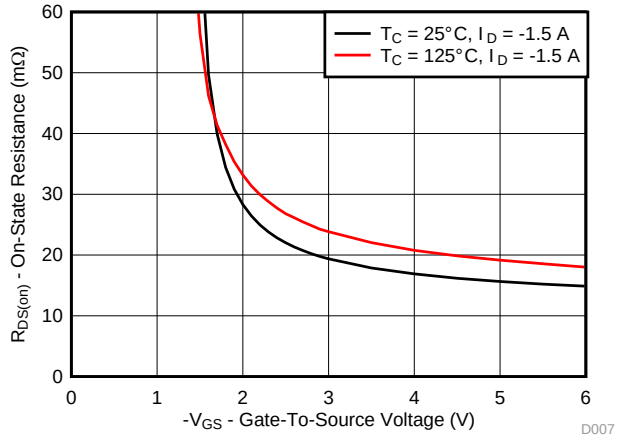
(1) Device operating at a temperature of 105ºC

(2) Typ $R_{\theta JA}$ = 170°C/W, Pulse width ≤100 µs, duty cycle ≤1%

Top View



$R_{DS(on)}$ vs V_{GS}



Gate Charge

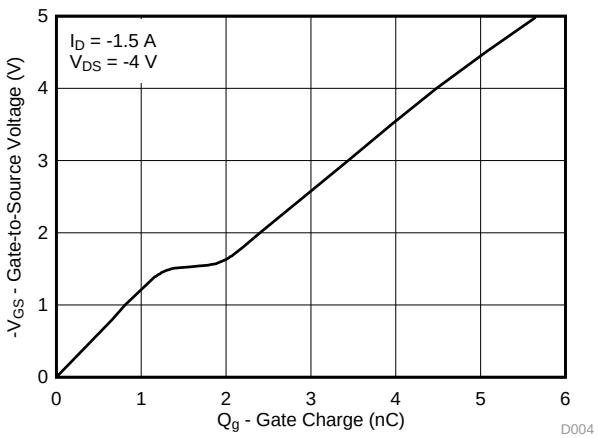


Table of Contents

4 Revision History

DATE	REVISION	NOTES
December 2014	*	Initial release.

5 Specifications

5.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

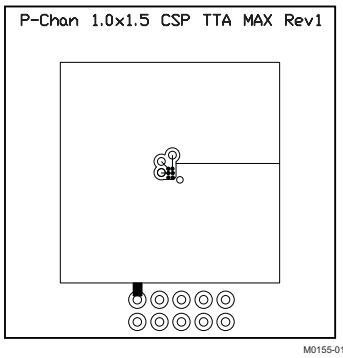
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = –250 µA	–8			V
I_{DSS}	Drain-to-Source Leakage Current	V_{GS} = 0 V, V_{DS} = –6.4 V			–1	µA
I_{GSS}	Gate-to-Source Leakage Current	V_{DS} = 0 V, V_{GS} = –6 V			–100	nA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	V_{DS} = V_{GS}, I_D = –250 µA	-0.6	–0.8	–1.1	V
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = –1.8 V, I_D = –1.5 A		35	53	mΩ
		V_{GS} = –2.5 V, I_D = –1.5 A		22	26.5	mΩ
		V_{GS} = –4.5 V, I_D = –1.5 A		16.2	19.4	mΩ
g_{fs}	Transconductance	V_{DS} = –0.8 V, I_D = –1.5 A		14		S
DYNAMIC CHARACTERISTICS						
C_{ISS}	Input Capacitance	V_{GS} = 0 V, V_{DS} = –4 V, f = 1 MHz		703	914	pF
C_{OSS}	Output Capacitance			391	508	pF
C_{RSS}	Reverse Transfer Capacitance			133	172	pF
Q_g	Gate Charge Total (–4.5 V)	V_{DS} = –4 V, I_D = –1.5 A		4.9	6.3	nC
Q_{gd}	Gate Charge Gate-to-Drain			0.6		nC
Q_{gs}	Gate Charge Gate-to-Source			1.3		nC
$Q_{g(th)}$	Gate Charge at V_{th}			0.6		nC
Q_{OSS}	Output Charge	V_{DS} = –4 V, V_{GS} = 0 V		1.9		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = –4 V, V_{GS} = –4.5 V, I_D = –1.5 A R_G = 10 Ω		14		ns
t_r	Rise Time			12		ns
$t_{d(off)}$	Turn Off Delay Time			58		ns
t_f	Fall Time			27		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode Forward Voltage	I_S = –1.5 A, V_{GS} = 0 V		–0.75	–1	V
Q_{rr}	Reverse Recovery Charge	V_{DS}= –4.7 V, I_F = –1.5 A di/dt = 100 A/µs		6.1		nC
t_{rr}	Reverse Recovery Time			21		ns

5.2 Thermal Information

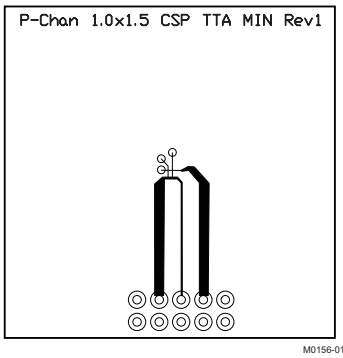
(T_A = 25°C unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance(1)		170		°C/W
	Junction-to-Ambient Thermal Resistance(2)		55		

(1) Device mounted on FR4 material with minimum Cu mounting area.
(2) Device mounted on FR4 material with 1 $inch^2$ (6.45 cm^2), 2 oz. (0.071 mm thick) Cu.



Typ $R_{\theta JA}$ = 55°C/W when mounted on 1 inch^2 of 2 oz. Cu.



Typ $R_{\theta JA}$ = 170°C/W when mounted on minimum pad area of 2 oz. Cu.

5.3 Typical MOSFET Characteristics

(T_A = 25°C unless otherwise stated)

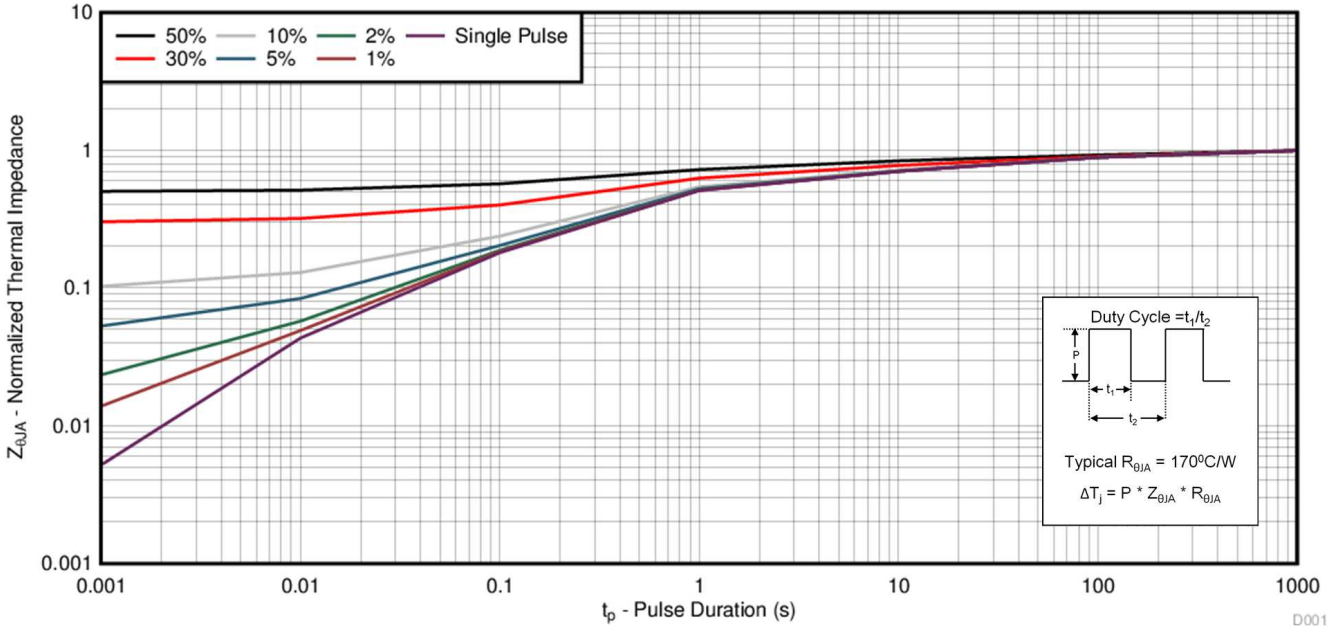


Figure 1. Transient Thermal Impedance

Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

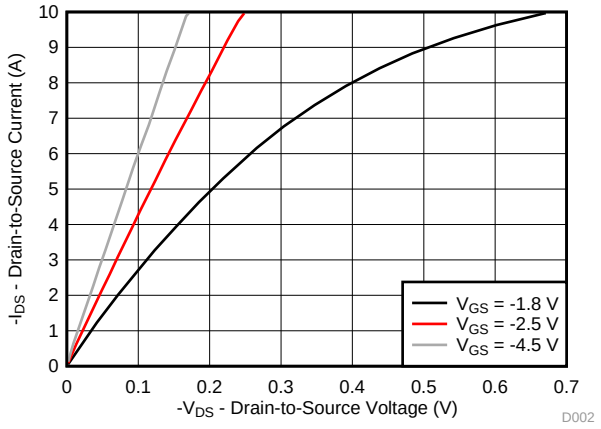
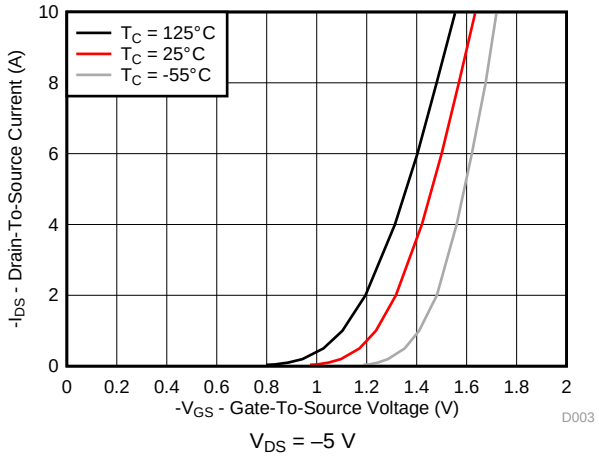
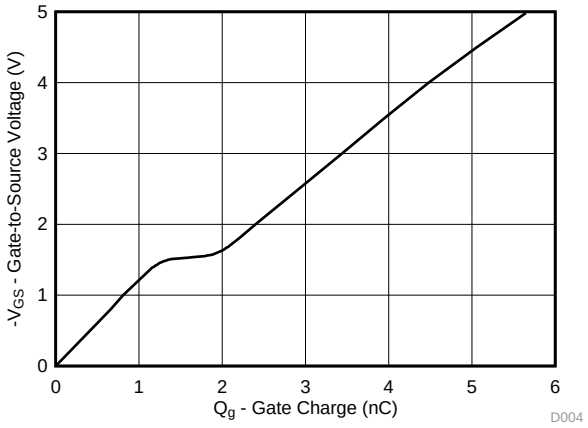


Figure 2. Saturation Characteristics



VDS = –5 V

Figure 3. Transfer Characteristics



ID = –1.5 A VDS = –4 V

Figure 4. Gate Charge

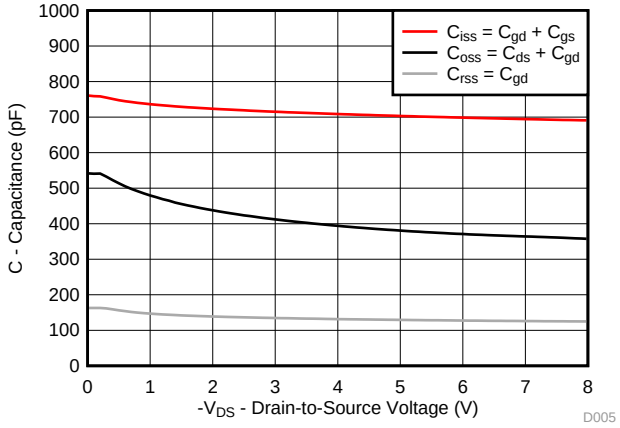
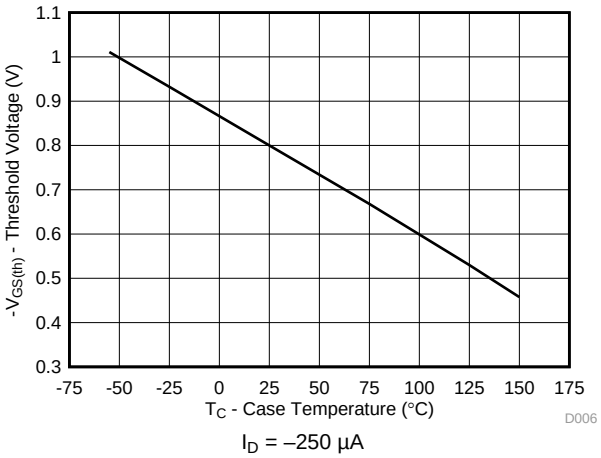


Figure 5. Capacitance



ID = –250 µA

Figure 6. Threshold Voltage vs Temperature

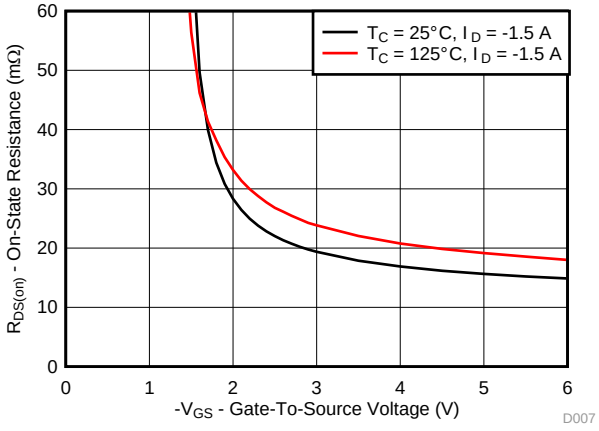
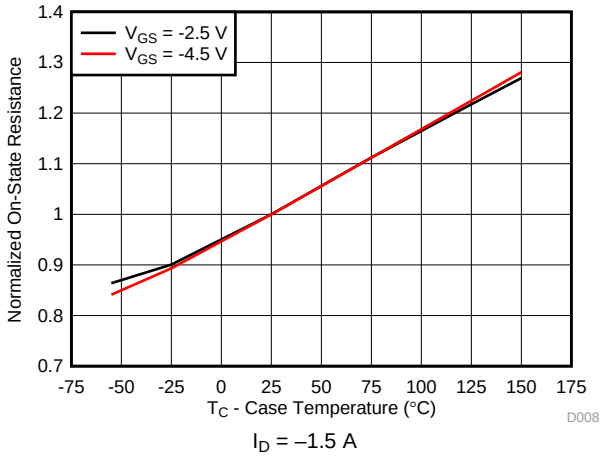


Figure 7. On-State Resistance vs Gate-to-Source Voltage

Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)



I_D = –1.5 A

Figure 8. Normalized On-State Resistance vs Temperature

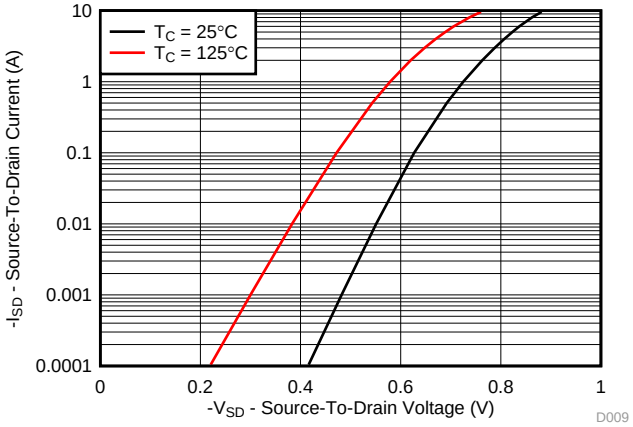
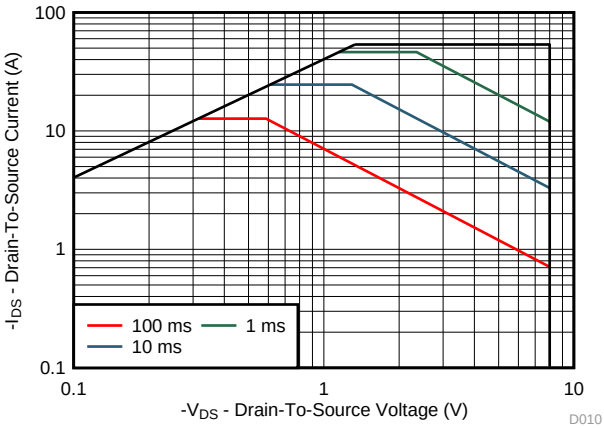


Figure 9. Typical Diode Forward Voltage



Single Pulse, Typical $R_{\theta JA}$ = 170°C/W

Figure 10. Maximum Safe Operating Area

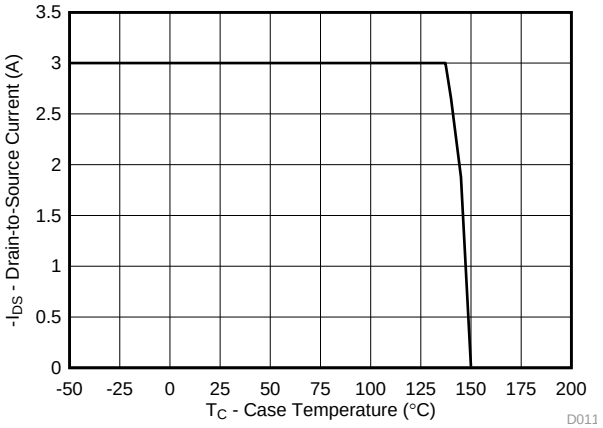


Figure 11. Maximum Drain Current vs Temperature

6 Device and Documentation Support

6.1 Trademarks

NexFET is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

6.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.3 Glossary

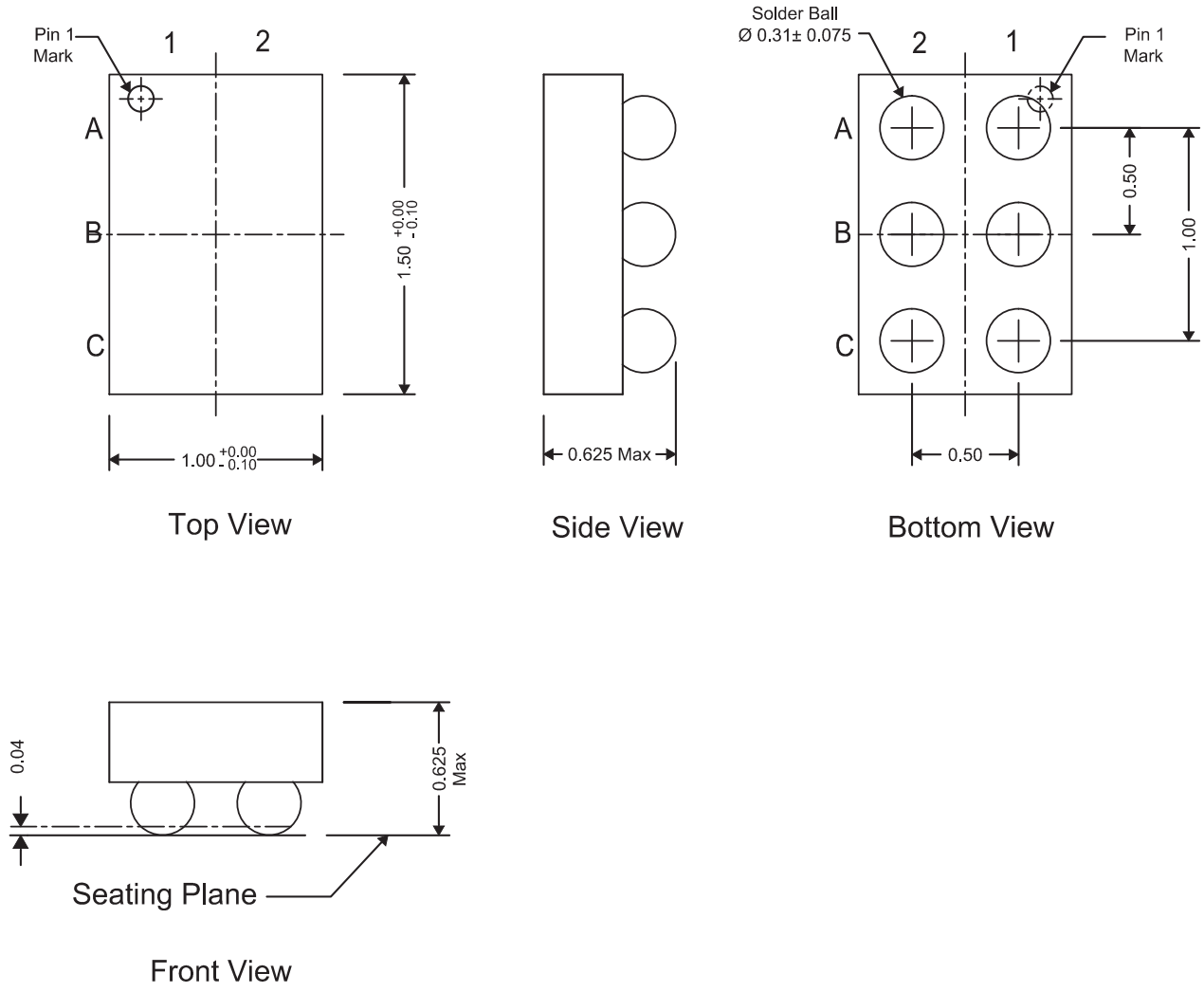
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 CSD23203W Package Dimensions

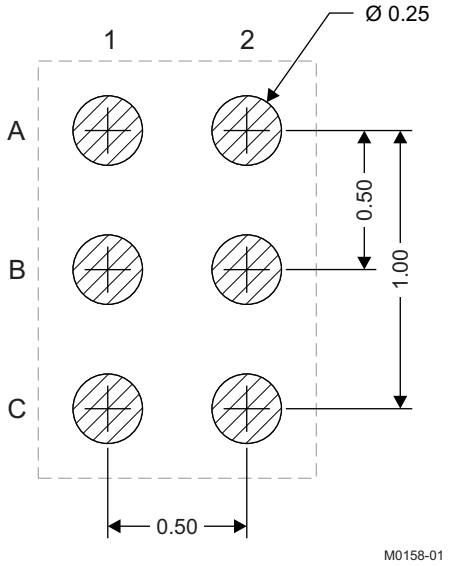


NOTE: All dimensions are in mm (unless otherwise specified).

Pinout

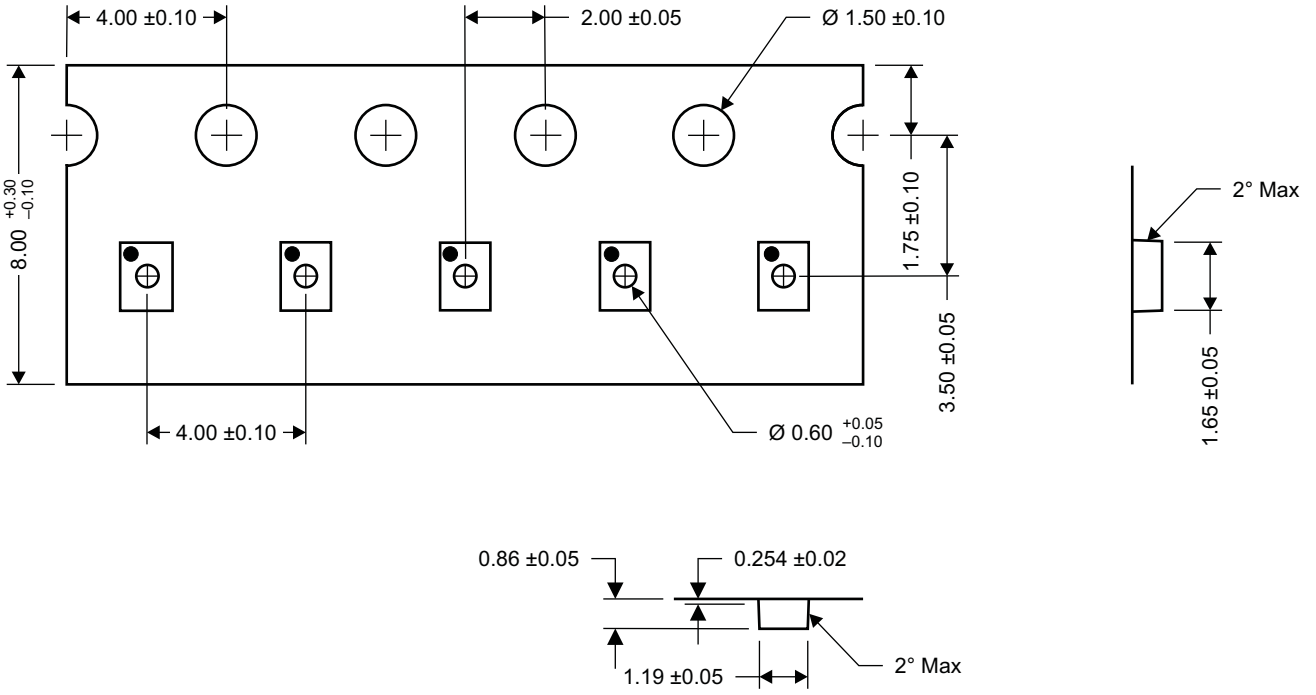
POSITION	DESIGNATION
C1, C2	Drain
A1	Gate
A2, B1, B2	Source

7.2 Land Pattern Recommendation



NOTE: All dimensions are in mm (unless otherwise specified).

7.3 Tape and Reel Information



NOTE: All dimensions are in mm (unless otherwise specified).

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD23203W	ACTIVE	DSBGA	YZC	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		23203	Samples
CSD23203WT	ACTIVE	DSBGA	YZC	6	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		23203	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

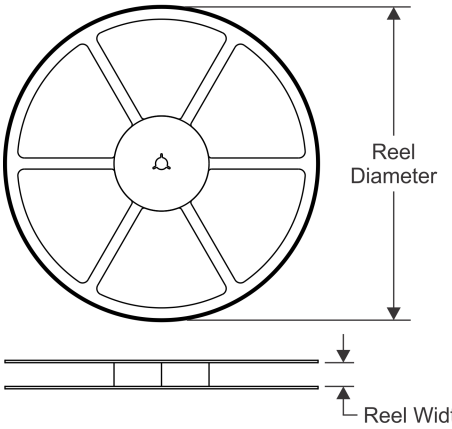
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

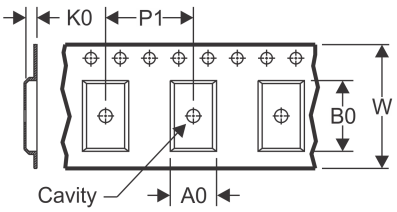
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

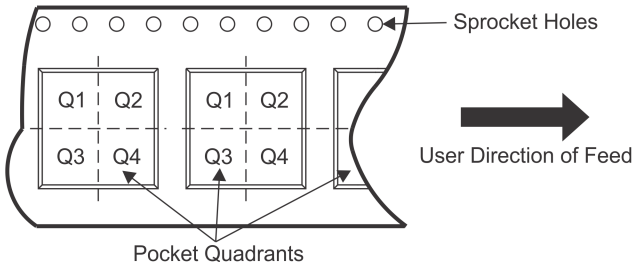


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

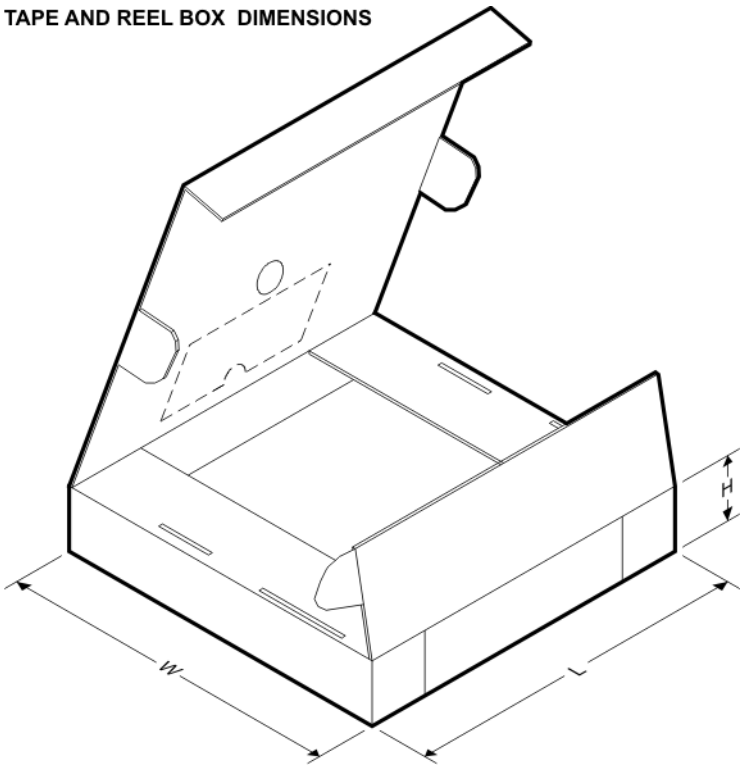
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD23203W	DSBGA	YZC	6	3000	180.0	8.4	1.18	1.68	0.83	4.0	8.0	Q1
CSD23203WT	DSBGA	YZC	6	250	180.0	8.4	1.18	1.68	0.83	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD23203W	DSBGA	YZC	6	3000	182.0	182.0	17.0
CSD23203WT	DSBGA	YZC	6	250	182.0	182.0	17.0

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265