

REV	Description	DATE	BY
A4A	Initial Production Release.	11/19/2012	GC
A5	On the initial production release the processors were to be found incorrect as supplied by TI. Parts while marked AM3359 were actually AM3352. This revision uses the correct parts.	1/2/2013	GC
	1. Deleted R29-R44 from the LCD lines. 2. Added 47pf capacitors C156-C173 to LCD data lines to ground. 3. Changed schematic revision to A5A. 4. Changed a few footprints after PCB update for above changes. 5. Added access point for the battery function of the TPS65217C. 6. Added Ferrite beads in series with LED power and 5V power rail of the USB host connector. Required to pass FCC/CE testing due to noise emissions on that pin. 7. Added power button to enable sleep, wakeup, power down and power up features on the system. 8. Added Modification to add 100K ohm resistor to ground to prevent crosstalk when serial cable is not plugged in.	2/8/2013	GC
A5B	1. Added 100K pulldown on J1 pin 4 to prevent crosstalk when serial cable is not connected into PCB layout.	4/1/2013	

This schematic is \*NOT SUPPORTED\* and DOES NOT constitute a reference design. Only "community" support is allowed via resources at BeagleBoard.org/discuss.

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PAGE NO.	SCHEMATIC PAGE
1	COVER PAGE
2	POWER MANAGEMENT
3	PROCESSOR 1 OF 3, JTAG HEADER
4	PROCESSOR 2 OF 3, USB PORTS
5	PROCESSOR 3 OF 3
6	LED, CONFIGURATION AND BUTTON
7	DDR3 MEMORY
8	eMMC FLASH
9	10/100 ETHERNET
10	HDMI FRAMER
11	EXP CONN, uSD

NOTE: PCB Revision for this board is Rev B4.

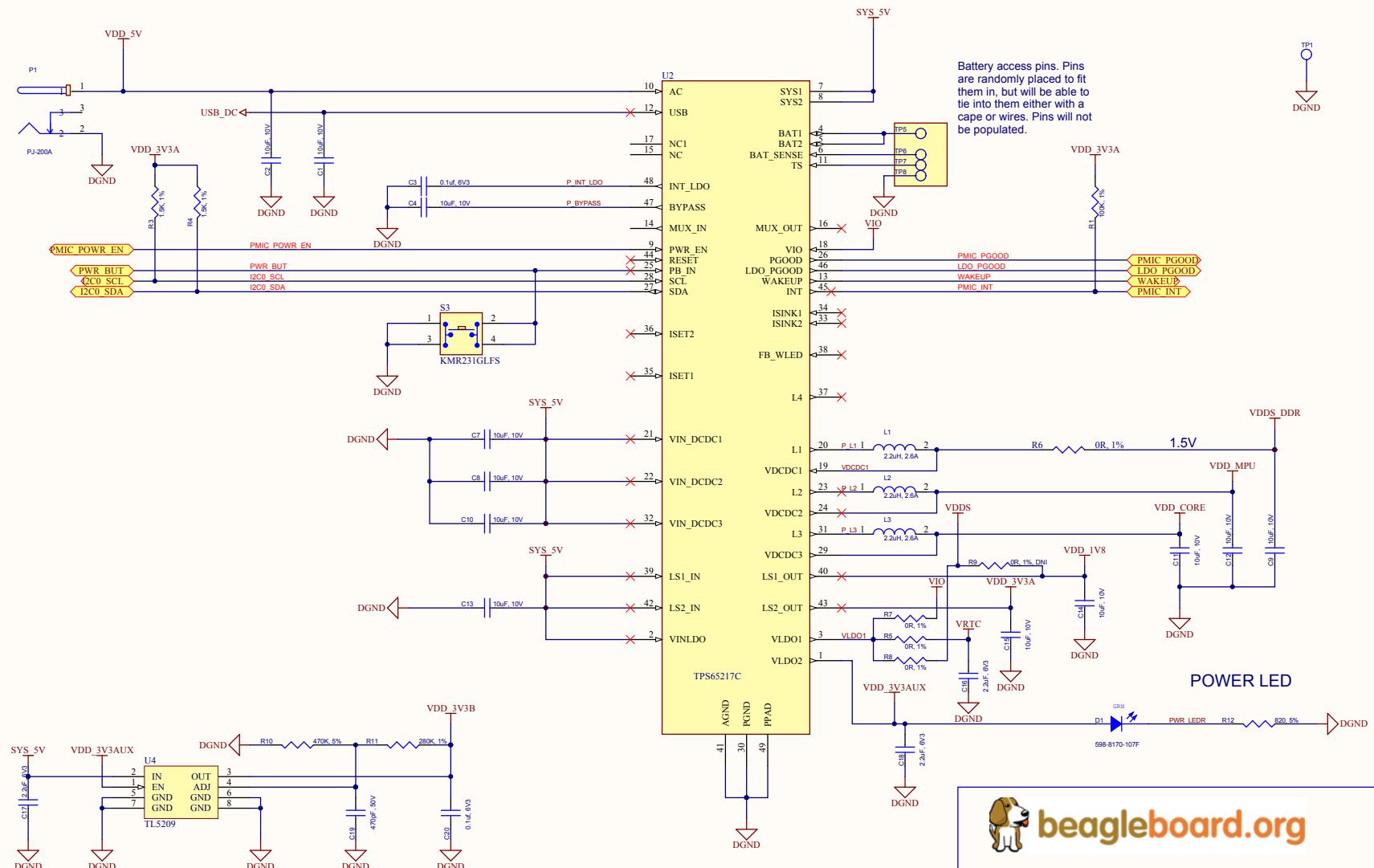


Title  
BeagleBoneBlack Cover Page

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## 5V DC POWER



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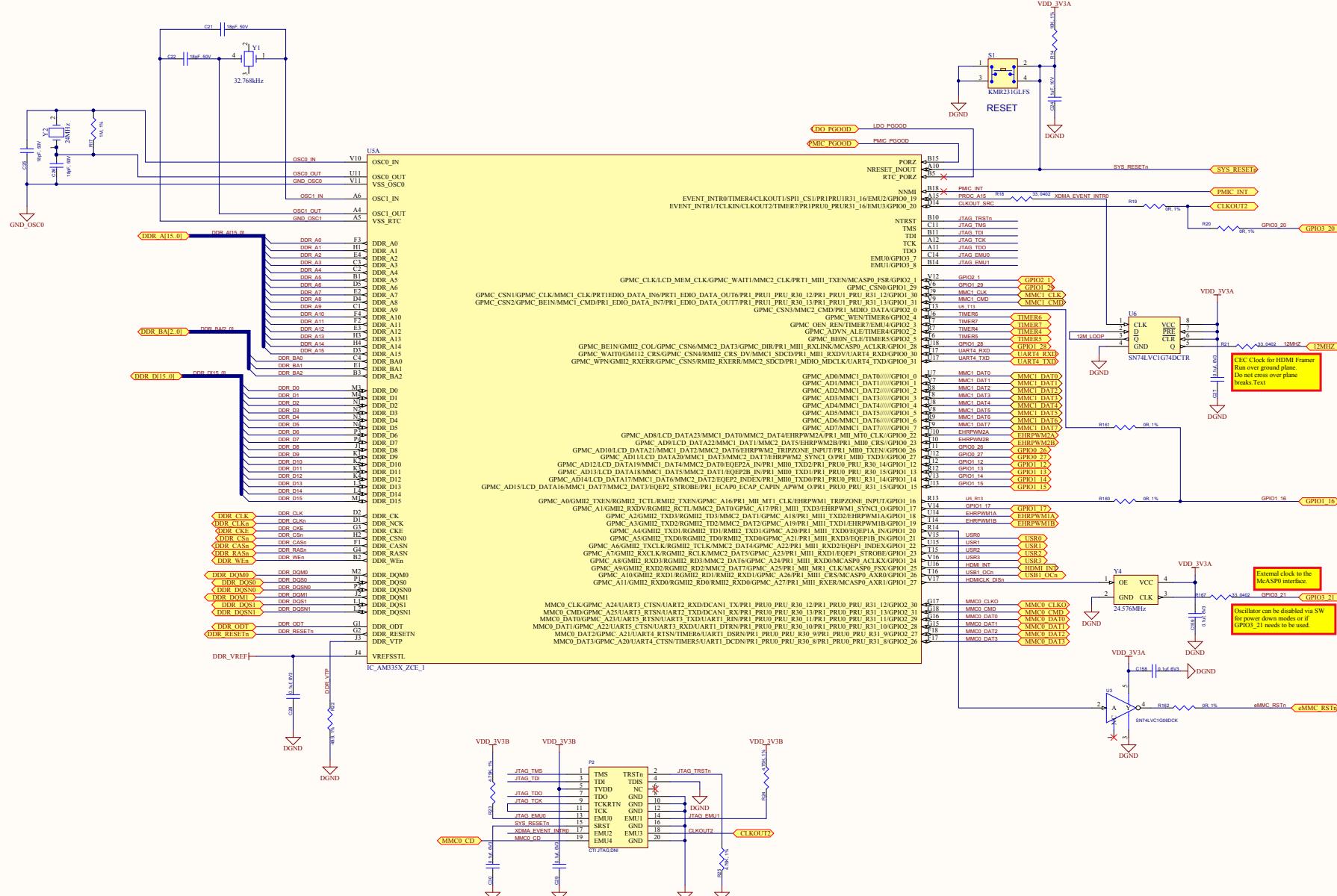
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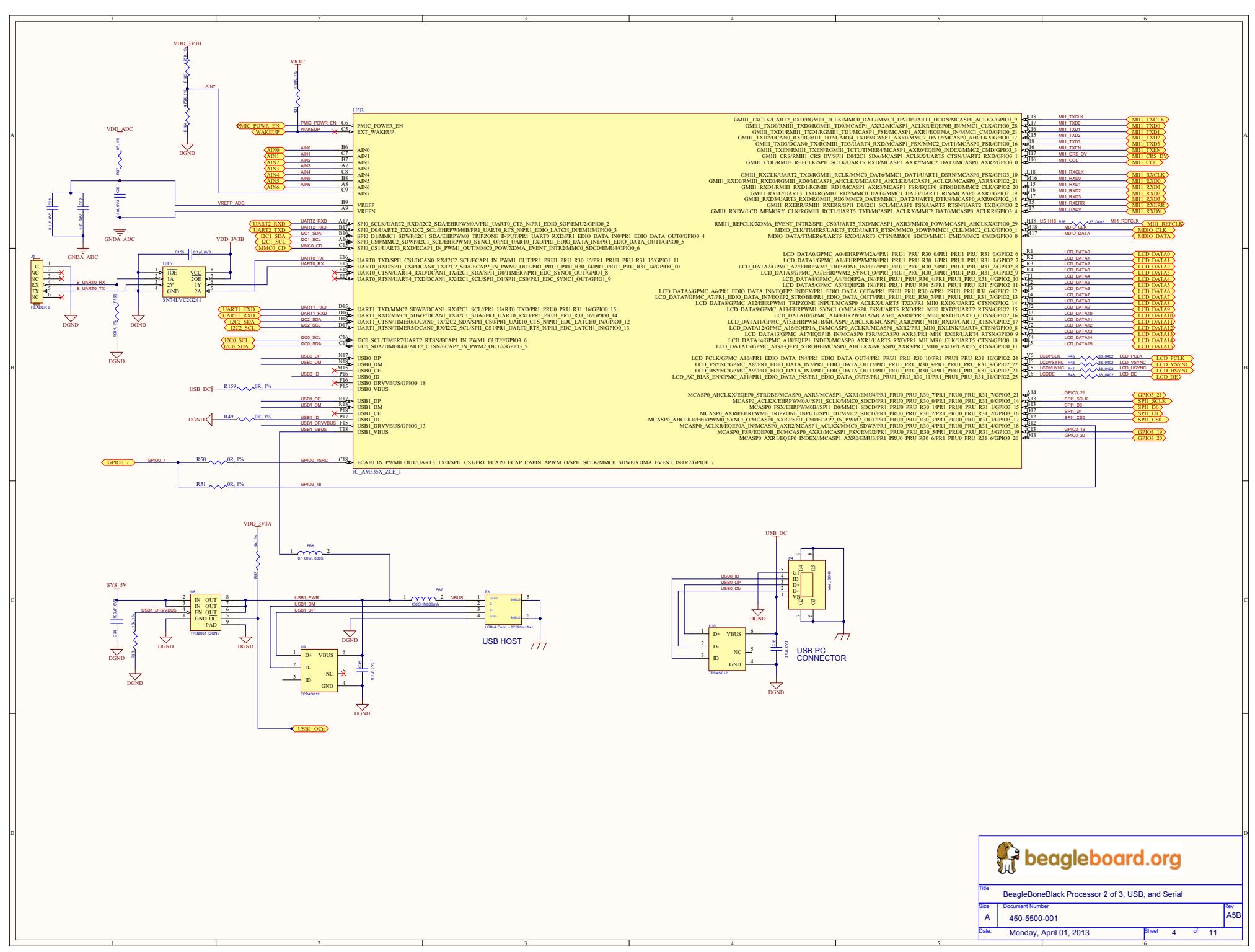
BeagleBoneBlack Processor 1 of 3 and JTAG

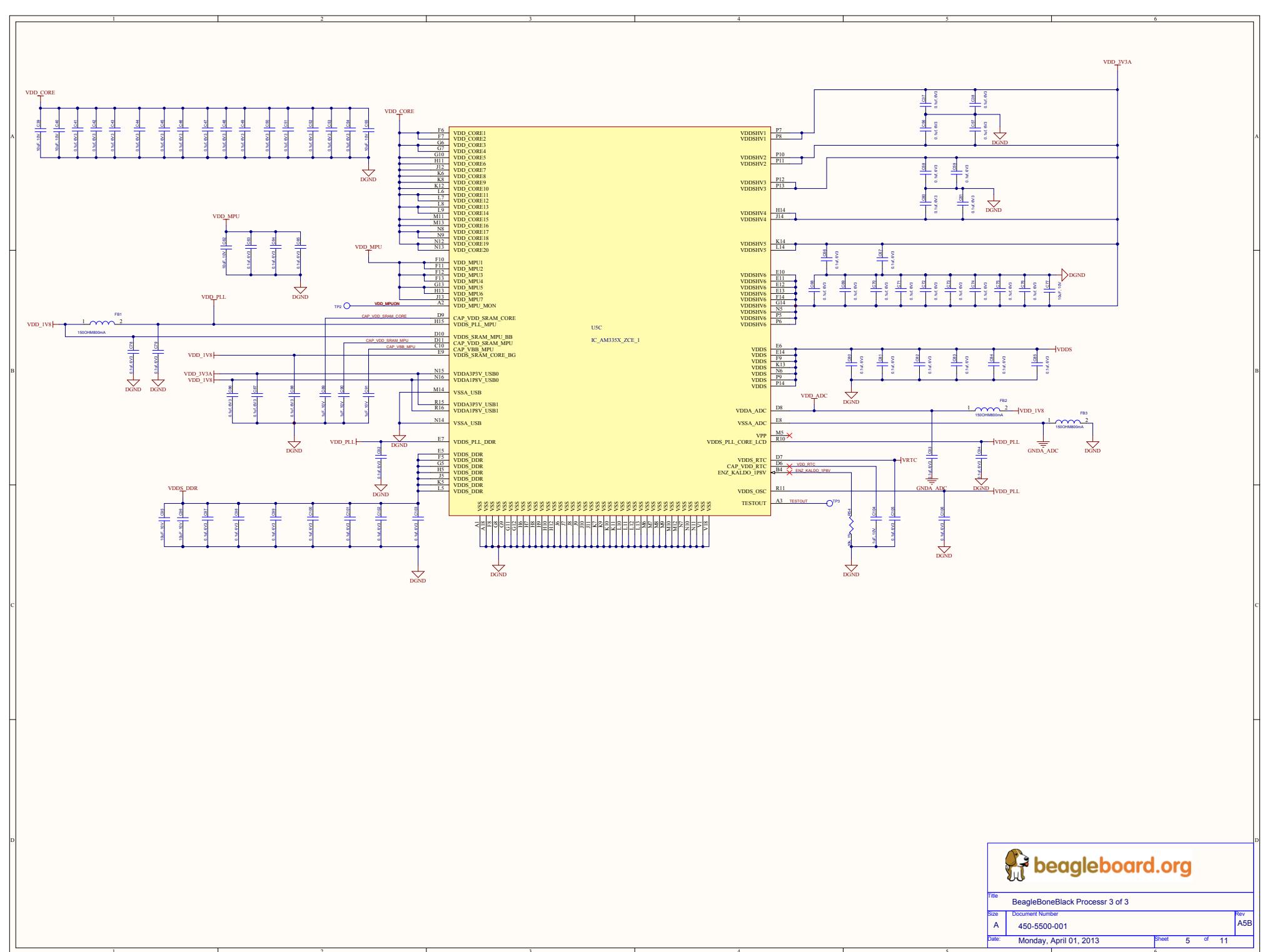
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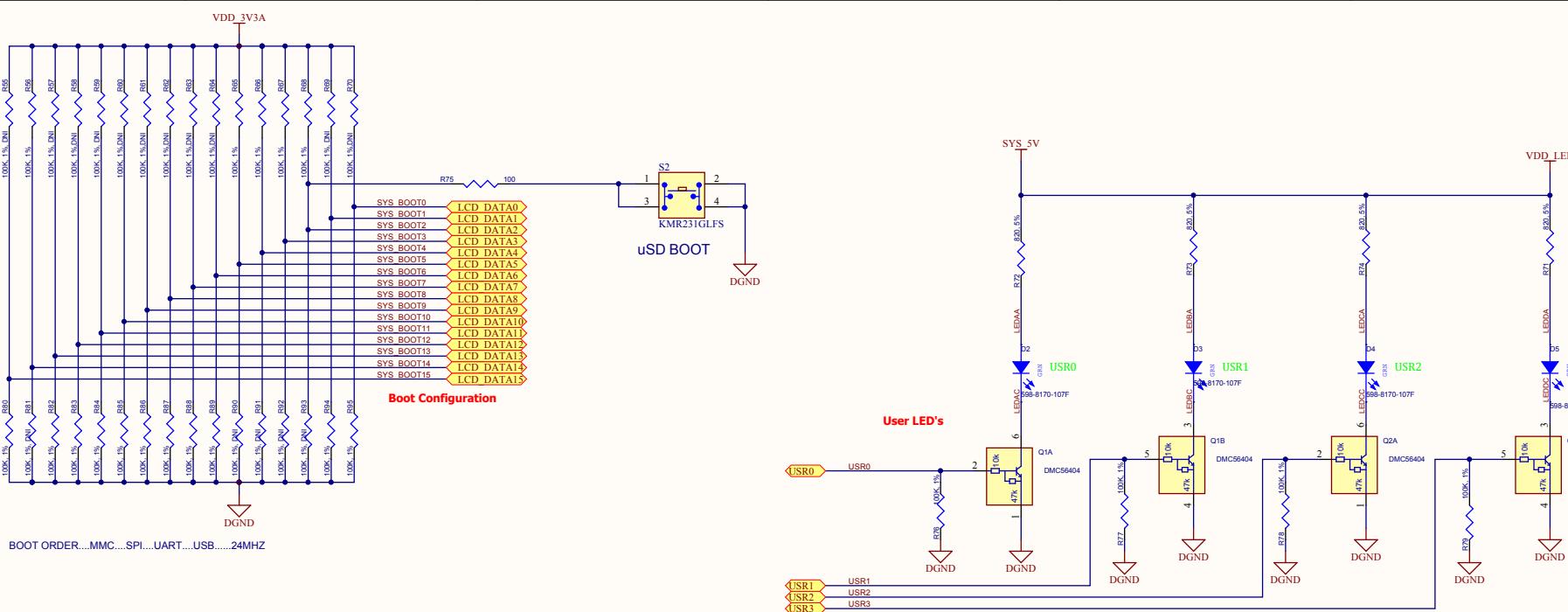
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Boot Sequence													
SYSBOOT[15:14]	SYSBOOT[13:12]	SYSBOOT[11:10]	SYSBOOT[9]	SYSBOOT[8]	SYSBOOT[7:6]	SYSBOOT[5]	SYSBOOT[4:0]						
00b = 19.2MHz 01b = 24MHz 10b = 25MHz 11b = 26MHz	00b (all other values reserved)	Don't care for ROM code	Don't care for ROM code	Don't care for ROM code	0 = CLKOUT1 disabled 1 = CLKOUT1 enabled	11100b	MMC1	MMC0	UART0	USB0[5]			
00b = 19.2MHz 01b = 24MHz 10b = 25MHz 11b = 26MHz	00b (all other values reserved)	Don't care for ROM code	Don't care for ROM code	Don't care for ROM code	0 = CLKOUT1 disabled 1 = CLKOUT1 enabled	11000b	SPI0	MMC0	USB0[5]	UART0			



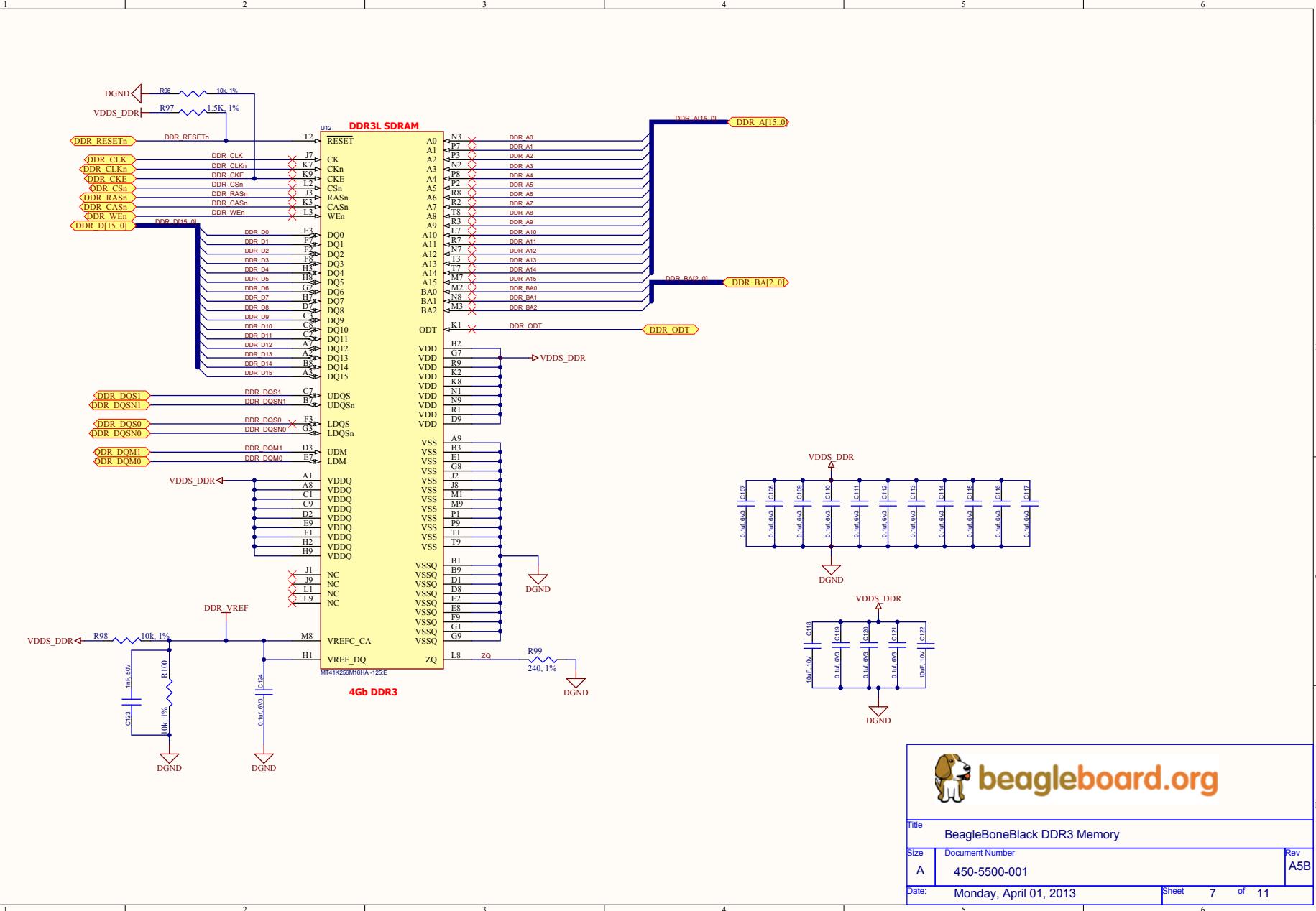
Title: BeagleBoard LED, Configuration, and Reset

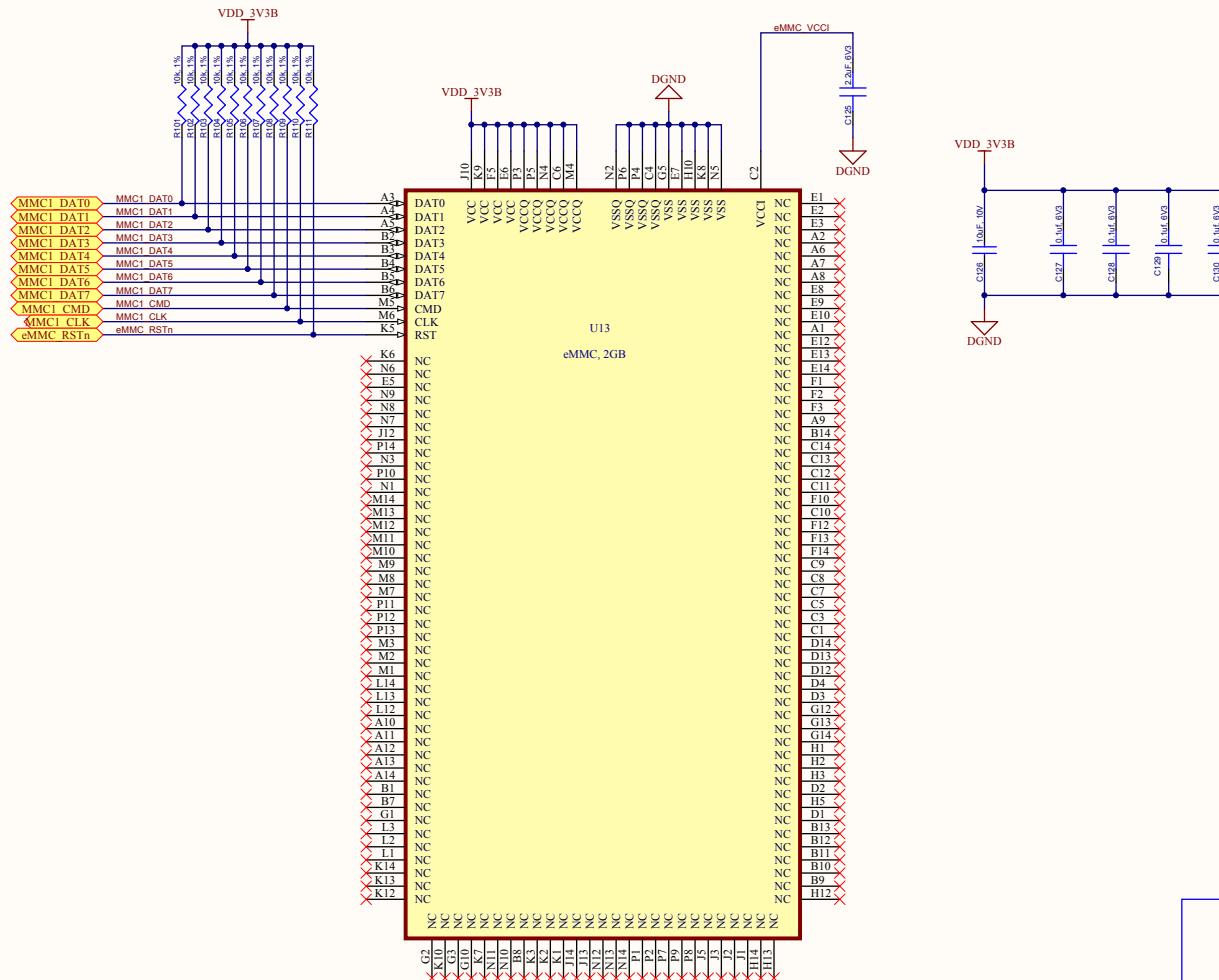
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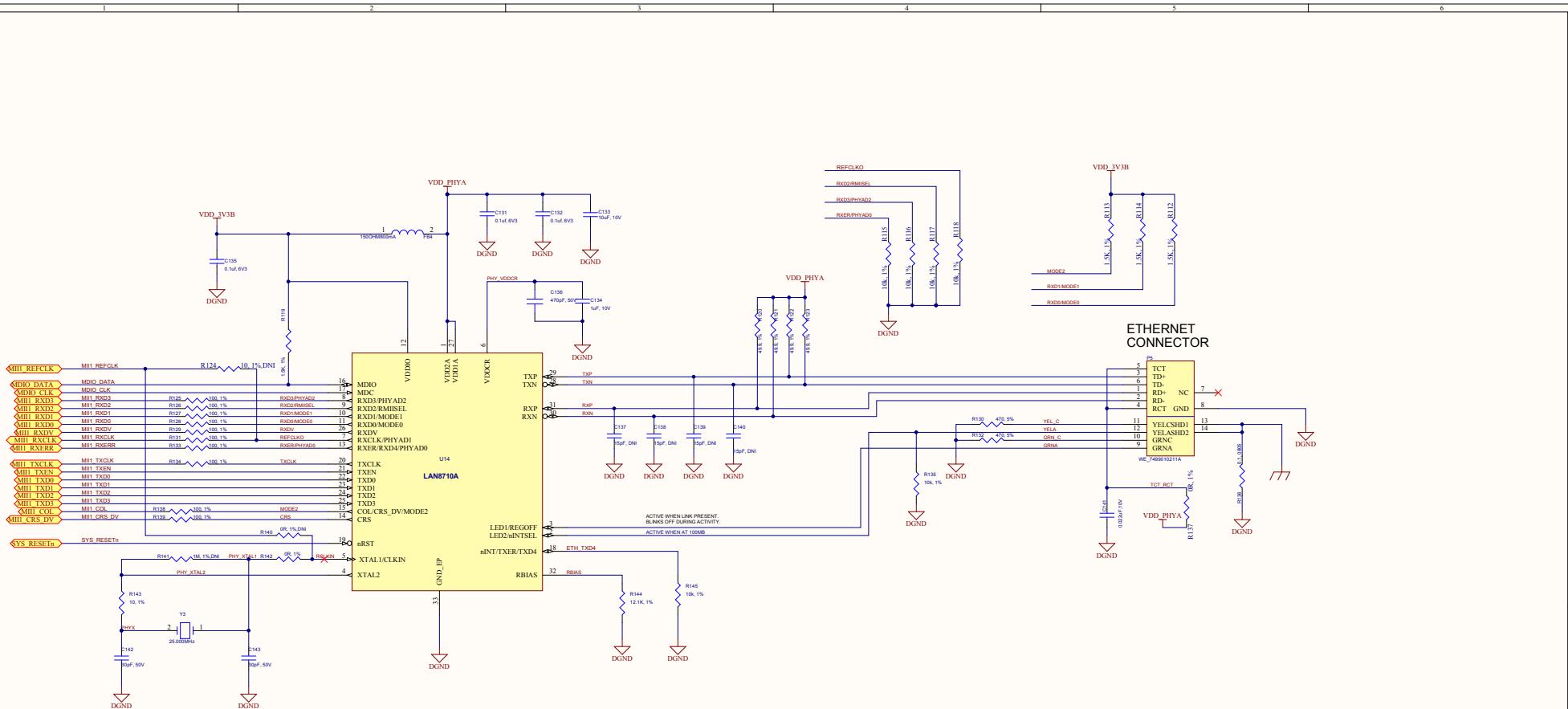
Rev: A5B

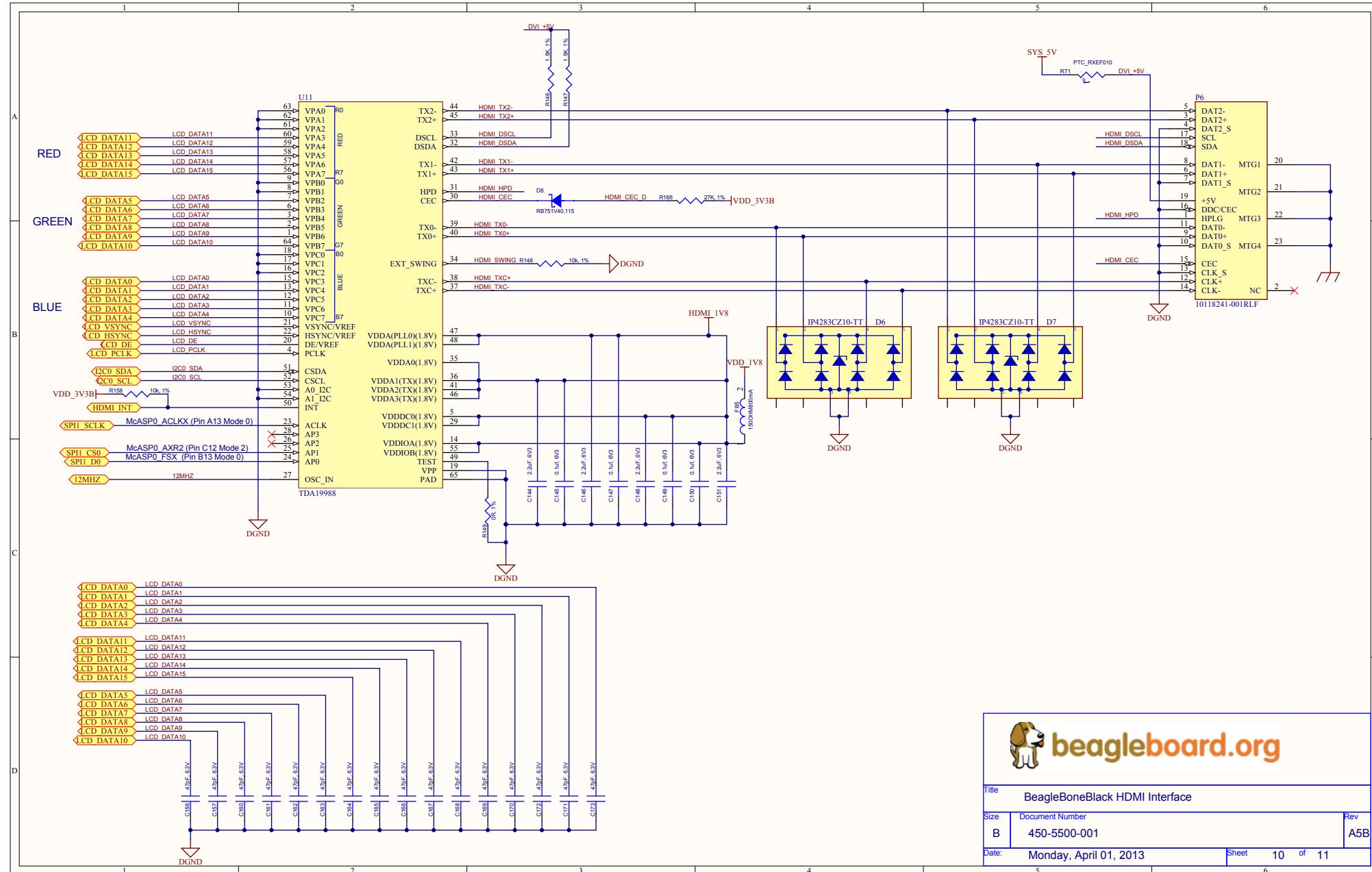
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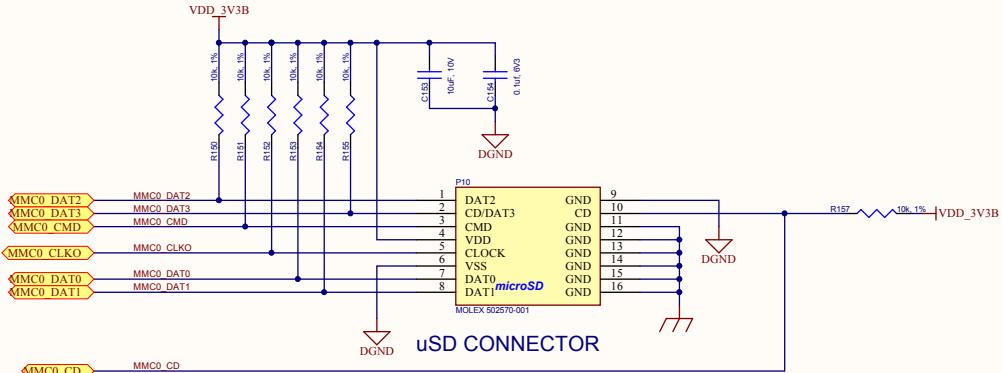
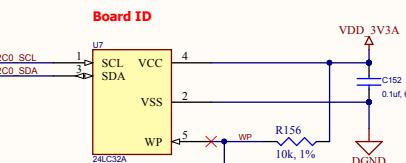
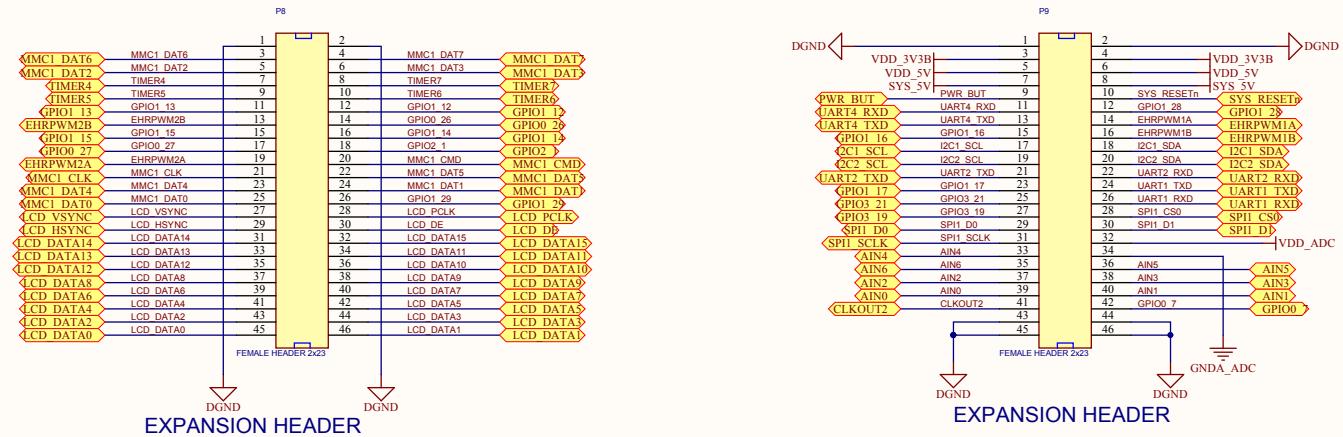
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1 2 3 4 5 6 7 8 9 10 11

**FAB NOTES:**

- ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE NOTED.
- THE PWB SHALL BE FABRICATED TO IPC-6012, CLASS 2 AND WORKMANSHIP SHALL CONFORM TO IPC-A-600, CLASS 2, CURRENT REVISIONS.
- BOARD MATERIAL SHALL BE 180 Tg/350 Td ISOLA FR-370HR OR EQUIVALENT, R/H/S COMPLIANT AND LEAD FREE ASSEMBLY CAPABLE. BOARD MATERIAL SHALL MEET REQUISITES FOR 100% SMT MATERIAL.
- BOARD MATERIAL & CONSTRUCTION TO BE UL APPROVED AND MARKED ON THE FINISHED BOARD.
- MINIMUM COPPER WALL THICKNESS OF PLATED-THRU HOLES TO BE .001 INCH, WITH A MINIMUM ANULAR RING OF .002 INCH.
- OVERALL BOARD THICKNESS TO BE .062 +/- 10% AND APPLIES AFTER ALL LAMINATION AND PLATING PROCESSES, MEASURED FROM COPPER TO COPPER.
- MAX. WARP & TWIST TO BE .0075 INCHES PER INCH.
- BOARD MUST BE ELECTRICALLY TESTED USING SUPPLIED PC-D-356 NETLIST.
- ALL LAYUP TO HAVE SOLDERMASK.

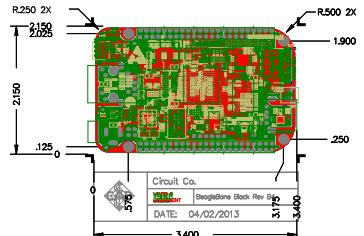
**FINISHED AS SMOOTH WALL BY VENDOR.  
PROCESS NOTES:**

- PLATE ALL EXPOSED AREAS WITH ELECTROLESS IMPERSON GOLD, NO/C: 150 MICRONCHES THK MIN GOLD 5-15 MICRONCHES THK MAX.
- Z-IMPROVE COAT OVER BARE COPPER (SMBC) COLOR: BLACK. SOLDERMASK SHALL CONFORM TO PC-SM-840, CLASS H, CURRENT REV.
- SOLDERMASK ARTWORK HAS ZERO (0) OVERRIDDEN PADS. FABRICATION VENDOR IS ALLOWED TO ADJUST THE COMPONENT SOLDERMASK PADS TO MEET THEIR TOOLING REQUIREMENTS.
- APPLY LPI SULSCREEN OR EQUIVALENT PER THE ARTWORK. COLOR: WHITE.

**LAYER STACK-UP – ALL DIMENSIONS IN INCHES**

LAYER#	COPPER WEIGHT	50mil SINGLE ENDED LINE WIDTH CONTROL +/- 10%		90mil DIFFERENTIAL LINE WIDTH CONTROL +/- 10%		1000mil DIFFERENTIAL LINE WIDTH CONTROL +/- 10%	
		TRACE WIDTH	TRACE WIDTH / SPACE	TRACE WIDTH / SPACE	TRACE WIDTH / SPACE	TRACE WIDTH / SPACE	TRACE WIDTH / SPACE
LAYER 1 – PRIMARY SIDE – SIGNAL	HALF+PLATING	4.75	4.5/6.5	3.75/7.25			
LAYER 2 – GROUND PLANE	1						
LAYER 3 – SIGNAL	1	5.25	5.0/7.0	4.00/8.00			
LAYER 4 – SIGNAL	1	5.25	5.0/7.0	4.00/8.00			
LAYER 5 – SPLIT POWER PLANE	1						
LAYER 6 – SECONDARY SIDE – SIGNAL	HALF+PLATING	4.75	4.5/6.5	3.75/7.25			

DRILL CHART: TOP to BOTTOM			
FIGURE	SIZE	ALL UNITS ARE IN MILS	QTY
+	6.0	+3.0/-3.0	PLATED 27
*	8.0	+3.0/-3.0	PLATED 794
*	12.0	+3.0/-3.0	PLATED 30
*	30.0	+3.0/-3.0	PLATED 96
*	40.0	+3.0/-3.0	PLATED 26
*	63.0	+3.0/-3.0	PLATED 2
◊	125.0	+3.0/-3.0	PLATED 4
○	420.0	+3.0/-3.0	NOT PLATED 2
*	50.0x15.0	+3.0/-3.0	PLATED 2
*	95.0x40.0	+3.0/-3.0	PLATED 2
*	120.0x40.0	+3.0/-3.0	PLATED 1
*	120.0x40.0	+3.0/-3.0	PLATED 1
*	140.0x40.0	+3.0/-3.0	PLATED 1



APPROVED	CHECKED	CIRCUITCO.	
DESIGN ENGR	DRAFTING	CalCed	
PROJECT ENGR		TOLERANCES UNLESS OTHERWISE SPECIFIED	
ENGR MGR		0.001" +0.0005" -0.0005"	
NEXT ASSEMBLY		DO NOT SCALE DRAWINGS	
DATE	04/02/13	SCALE	NONE
DESIGN ENGR		SHEET	1 OF 1
PROJECT ENGR		PCB REV	B4
ENGR MGR		SIZE	D

FABRICATION DRAWING,  
BeagleBone Block

