Progress Report #2

One month ago, I set a few goals with high expectations in mind. They were as follows:

* Completely port over the QM-FIR project and be able to demonstrate its functionality to my mentor and fellow interns
* Write extensive documentation for future users to comprehend and replicate my project design
* Team up with another intern to develop a python-based GUI for analyzing the filter’s outputs and simulate radar application
* Get started on implementing the digital filter through hardware only, and use python scripts to send data over UART

Unfortunately, due to unforeseen circumstances (which will be discussed later in more detail), I was not able to complete everything as intended. However, I was able to make significant progress on multiple projects during the past four weeks.

After hours of debugging the UDP Ethernet implementation of the QM-FIR digital filter core, I finally solved the problem and was able to demonstrate the filter's functionality. The main issue was related to the interface between hardware and software interrupts, which caused the iBoard's inability to transfer data back to a host machine. I had forgotten to initialize the interrupts in software, and thus there was no way for the hardware to respond. ***~~After I got the interrupts working, I noticed that the iBoard Temac Ethernet Tx FIFO had substantial packet loss, which caused even more interrupt trouble. The FIFO was overrun and was not receiving the expected amount of data to generate an interrupt. To reduce packet loss, I slowed down the UDP transmission rate, adding a delay after each individual packet was sent from the host machine to the iBoard. These fixes allowed me to successfully demonstrate a working digital filter core during a short lab presentation, where presented my project to my mentor, my fellow interns, and a few other JPLers.~~***

My technical approach to this project was primarily to start and develop a new project design from scratch, using the existing digital filter core as a model. First, I integrated the old EDK project with the new iBoard configuration. This involved removing or replacing certain components like the Compact Flash and other digital logic cores. The next step was to revise and complete the existing Matlab, C, and Verilog source code because the software controls the overall data flow of the design. The last task was to verify the digital filter's functionality, and I did so using a Matlab GUI and UDP Ethernet communication between an iBoard and a host machine. I have begun to document my work with this core, defining and illustrating the digital filter's functions, modules, parameters, ports, data flows, and overall design.

I have teamed up with fellow intern, Kevin Ortega, to include the QM-FIR digital filter core in the iPanel. The iPanel is a python-based GUI for analyzing the filter’s outputs and simulate radar application. It allows integrated functional testing and validation of ISAAC-based instrument digital electronics systems to fine-tune the overall performance of specific ISAAC configurations. I have provided the custom IP core, and Kevin is currently writing code to plot the received filter output in the iPanel.

Since completing the UDP Ethernet implementation, I have moved on to another implementation of the filter—using UART to facilitate data transfer. The UART implementation is a slightly different filter design than UDP, taking an input signal of 240MHz instead of 60MHz. This means that another decimation is required to turn high-rate samples into data ready to be down-linked for further ground processing. The UART implementation performs packet transfer through the hardware core only, avoiding the software overhead experienced in Ethernet transfer protocols. However, UART is limited in speed because of a relatively slow baud rate. I am currently working on completing this project and demonstrating its functionality through a similar setup using Matlab, ChipScope, ISE, and a Python-based GUI.

There are about six weeks left in the USRP internship program, and I am hoping to achieve many things. First, I want to complete the projects I am currently working on, which include qmfir\_uart and a full-length documentation on these IP cores. Next, I will either move on to another implementation of the filter (using TCP Ethernet or raw Ethernet packet transfer) or I will port over the Binary Floating Point Quantization (BFPQ) core to the new iBoard. I could also experiment with other data acquisition techniques such as using a DAC board to verify the on-board processing with real-time analog data. I also need to make sure I have enough time to complete the USRP technical report and final presentation.

The relationship between me and Yutao continues to excel. He is a pleasure to work with, and is an overall fantastic mentor. In addition to providing useful feedback and guiding my research work, he encourages other “non-work” activities like attending JPL talks and learning Chinese Mandarin (a class at JPL). We still have weekly meetings, except for this week because he is attending a week-long conference in Florida to promote a new ISAAC proposal. He works very hard, and it inspires me everyday.

•Discuss in detail the work you have completed over the past month. (Describe your

experiments, progress on data analysis, etc.) Include exact technical specifications

and quantities and source or method of preparation for work you have done thus far.

You should present the methods in chronological order if possible.

•Discuss the progress of your work so far. What observations have you made? Describe

how your observations are (or are not) in line with what you expected.

•Describe any problems you have encountered. What was the source of the problem,

and how have you worked (or how are you working) on solving the problem(s)?

•What are your research goals for the remainder of the project? Have these goals

changed since you started working on your project?