

Temperature Monitor Diode Version 0.1 Physical Design Integration

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1 Introduction

This document provides recommendations for physical design integration into ASIC designs of temperature monitor diode macro (btmonitor_ssdbh). The intended audience is customers, Customer Design Centers (CDCs), and ASIC Physical Design engineers who work on designs that use these macros. These recommendations are in addition to the standard TI static timing analysis (STA) requirements outlined in the Pyramid documentation.

Temperature monitor macros contain sensitive analog circuitry. Consequently, some level of manual intervention is required to ensure that these macros are given a suitable environment in which to operate. Currently, the rules and recommendations specified in this document are not checked automatically, so vigilance is required to ensure that all guidelines are carefully followed.

2 Integration Strategy

A temperature monitor diode provides an external temperature sensor circuit with differential voltage measurements used to determine the temperature of the diode. The accuracy of the reported temperature will be affected by the process characteristics of the diode on the ASIC, the resistance of the connections between the thermal diode and the sensor circuit, and the magnitude of non-differential noise coupled into the differential traces connecting the diode and sensor (both on and off the ASIC). The goal of this document is to improve temperature monitor performance by providing guidelines to minimize the connection resistance and non-differential coupling noise.

Integration strategy topics addressed:

- PCB Recommendations
- Package and On-ASIC Routing Recommendations
- Placement Recommendations

2.1 PCB

The following recommendations are taken from several vendor Temperature Sensor data sheets outlining best practices for board routing. The customer should always refer to the documentation provided for the particular Temperature Sensor being used for recommendations. Any conflicts should defer to the Sensor documentation.

- Keep traces away from noise sources.
- Differential routing widths and shielding are shown in Figure 1.
- Route between ground planes, or over ground plane if routes are top level of board.

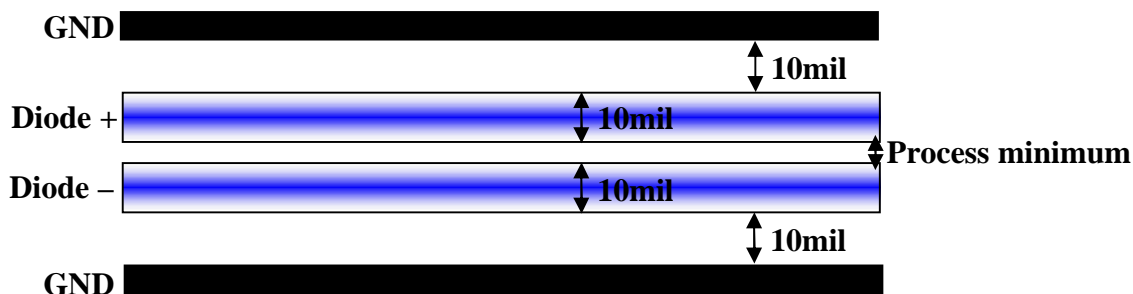


Figure 1. PCB Route Dimensions and Shielding

The temperature sensor generally requires an external capacitor placed very close to the Sensor Chip diode connection pins to mitigate the effect of noise. A typical configuration is shown in Figure2.

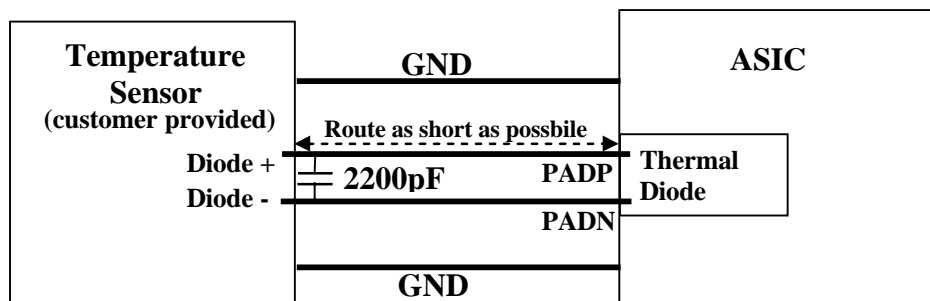


Figure 2. PCB Differential Capacitor

Please refer to the vendor temperature sensor documentation for additional guidelines.

2.2 Package and On-ASIC Routing

Package Routing Recommendations:

- Minimize package trace width and route between non-switching signals where possible.
- Route DIODE+/DIODE- (PADP/PADN on macro) signals differentially and tightly coupled.
- Use 2x spacing or greater to adjacent signals.
- Adjacent bumps preferred for PADN/PADP away from switching bumps and routes.

On-ASIC Routing Recommendations:

- Keep traces away from noise sources.
- Recommended differential routing widths and shielding are shown in Figure 3.
- Avoid routing other nets on adjacent layers immediately above or below and in the same direction as these nets.
- Minimize route lengths to reduce trace resistance.

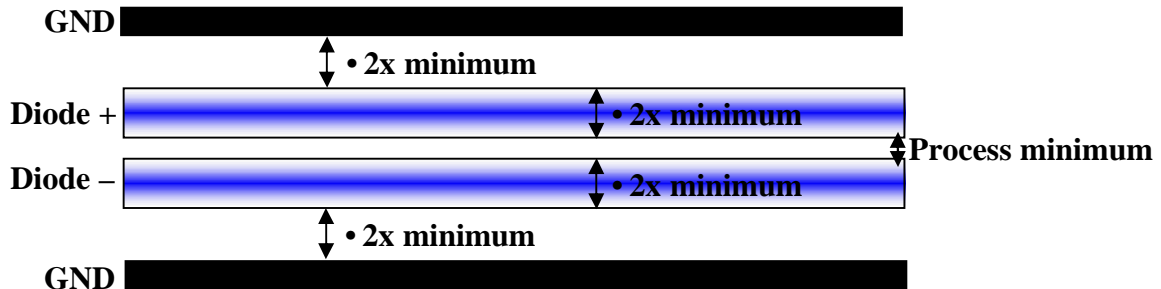


Figure 3. On-ASIC Routing

2.3 Placement

Placement Recommendations:

- Place temperature monitor macro away from switching IOs and logic gates (>100um preferred)
- Do not share VSS/VDDS connections with switching IOs

Appendix A. Related Documentation

Temperature Sensor Reference Datasheets:

Maxim-IC – MAX1617A Data Sheet-

<http://pdfserv.maxim-ic.com/en/ds/MAX1617A.pdf>

Analog Devices - ADM1032 Data Sheet-

http://www.analog.com/UploadedFiles/Data_Sheets/374025792ADM1032_c.pdf

Appendix B. Revision History

Version	Date	Author	Notes
0.1	Dec 15,2009	M Arvind	Initial version