SN74LVC244A
OCTAL BUFFER/DRIVER
WITH 3-STATE OUTPUTS

FEATURES

- **Operates From 1.65 V to 3.6 V**
- **Inputs Accept Voltages to 5.5 V**
- **Specified From –40°C to 85°C and –40°C to 125°C**
- **Max t_{pd} of 5.9 ns at 3.3 V**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
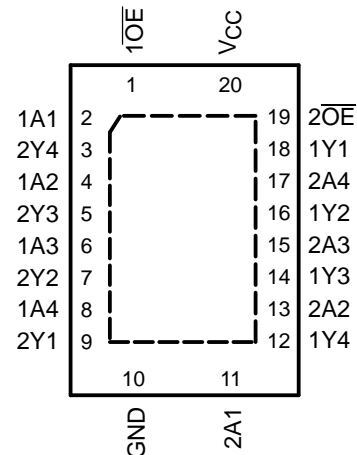 - **1000-V Charged-Device Model (C101)**

DESCRIPTION/ORDERING INFORMATION

This octal buffer/line driver is operational at 1.5-V to 3.6-V V_{CC}, but is designed specifically for 1.65-V to 3.6-V V_{CC} operation.

DB, DGV, DW, N, NS, OR PW PACKAGE
(TOP VIEW)

Pin		Pin
1OE	1	20	VCC
1A1	2	19	2OE
2Y4	3	18	1Y1
1A2	4	17	2A4
2Y3	5	16	1Y2
1A3	6	15	2A3
2Y2	7	14	1Y3
1A4	8	13	2A2
2Y1	9	12	1Y4
GND	10	11	2A1
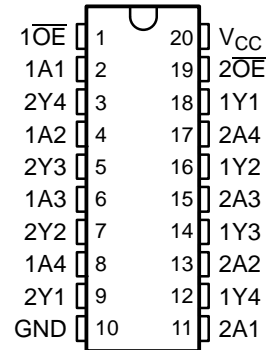
RGY PACKAGE
(TOP VIEW)

ORDERING INFORMATION

T_A	PACKAGE[(1)]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RGY	Reel of 1000	SN74LVC244ARGYR	LC244A
	VFBGA – GQN	Reel of 1000	SN74LVC244AGQNR	LC244A
	VFBGA – ZQN (Pb-Free)		SN74LVC244AZQNR	
–40°C to 125°C	PDIP – N	Tube of 20	SN74LVC244AN	SN74LVC244AN
	SOIC – DW	Tube of 25	SN74LVC244ADW	LVC244A
		Reel of 2000	SN74LVC244ADWR	
	SOP – NS	Reel of 2000	SN74LVC244ANSR	LVC244A
	SSOP – DB	Reel of 2000	SN74LVC244ADBR	LC244A
	TSSOP – PW	Tube of 70	SN74LVC244APW	LC244A
		Reel of 2000	SN74LVC244APWR	
		Reel of 250	SN74LVC244APWT	
	TVSOP – DGV	Reel of 2000	SN74LVC244ADGVR	LC244A

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

⚠ Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SN74LVC244A
OCTAL BUFFER/DRIVER
WITH 3-STATE OUTPUTS

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DESCRIPTION/ORDERING INFORMATION (CONTINUED)

The SN74LVC244A is organized as two 4-bit line drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of this device as a translator in a mixed 3.3-V/5-V system environment.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

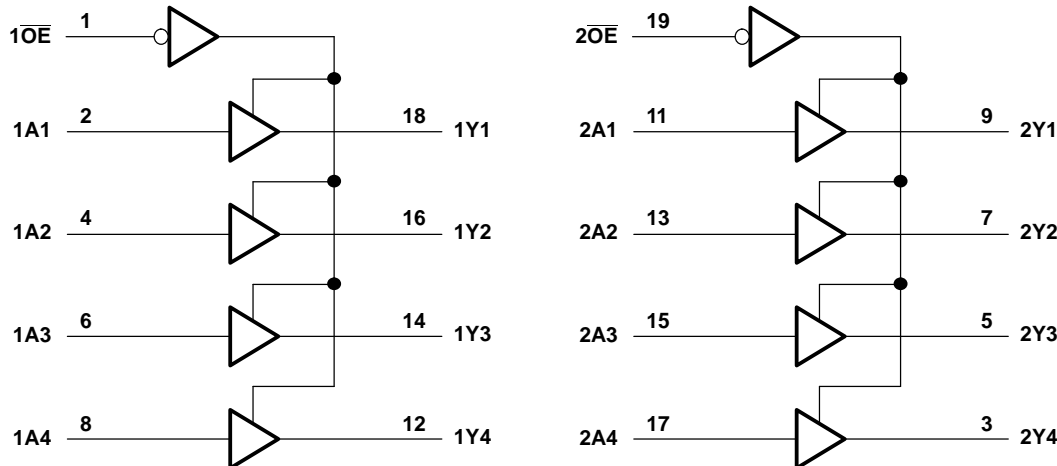**GQN OR ZQN PACKAGE**
(TOP VIEW)
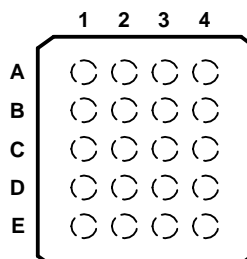
TERMINAL ASSIGNMENTS

	1	2	3	4
A	1A1	1$\overline{OE}$	V_{CC}	2$\overline{OE}$
B	1A2	2A4	2Y4	1Y1
C	1A3	2Y3	2A3	1Y2
D	1A4	2A2	2Y2	1Y3
E	GND	2Y1	2A1	1Y4

FUNCTION TABLE
(EACH BUFFER)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

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LOGIC DIAGRAM (POSITIVE LOGIC)

Pin numbers shown are for the DB, DGV, DW, N, NS, PW, and RGY packages.

Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		−0.5	6.5	V
V_I	Input voltage range[2]		−0.5	6.5	V
V_O	Voltage range applied to any output in the high-impedance or power-off state[2]		−0.5	6.5	V
V_O	Voltage range applied to any output in the high or low state[2][3]		−0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		−50	mA
I_{OK}	Output clamp current	V_O < 0		−50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
θ_{JA}	Package thermal impedance	DB package[4]		70	°C/W
		DGV package[4]		92	
		DW package[4]		58	
		GQN/ZQN package[4]		78	
		N package[4]		69	
		NS package[4]		60	
		PW package[4]		83	
		RGY package[5]		37	
T_{stg}	Storage temperature range		−65	150	°C
P_{tot}	Power dissipation	T_A = −40°C to 125°C[6][7]		500	mW

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of V_{CC} is provided in the recommended operating conditions table.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.
(5) The package thermal impedance is calculated in accordance with JESD 51-5.
(6) For the DW package: above 70°C the value of P_{tot} derates linearly with 8 mW/K.
(7) For the DB, DGV, N, NS, and PW packages: above 60°C the value of P_{tot} derates linearly with 5.5 mW/K.

Recommended Operating Conditions[1]

			$T_A = 25°C$		−40 TO 85°C		−40 TO 125°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	Operating	1.65	3.6	1.65	3.6	1.65	3.6	V
		Data retention only	1.5		1.5		1.5		
V_{IH}	High-level input voltage	V_{CC} = 1.65 V to 1.95 V	$0.65 \times V_{CC}$		$0.65 \times V_{CC}$		$0.65 \times V_{CC}$		V
		V_{CC} = 2.3 V to 2.7 V	1.7		1.7		1.7		
		V_{CC} = 2.7 V to 3.6 V	2		2		2		
V_{IL}	Low-level input voltage	V_{CC} = 1.65 V to 1.95 V		$0.35 \times V_{CC}$		$0.35 \times V_{CC}$		$0.35 \times V_{CC}$	V
		V_{CC} = 2.3 V to 2.7 V		0.7		0.7		0.7	
		V_{CC} = 2.7 V to 3.6 V		0.8		0.8		0.8	
V_I	Input voltage		0	5.5	0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 1.65 V		−4		−4		−4	mA
		V_{CC} = 2.3 V		−8		−8		−8	
		V_{CC} = 2.7 V		−12		−12		−12	
		V_{CC} = 3 V		−24		−24		−24	
I_{OL}	Low-level output current	V_{CC} = 1.65 V		4		4		4	mA
		V_{CC} = 2.3 V		8		8		8	
		V_{CC} = 2.7 V		12		12		12	
		V_{CC} = 3 V		24		24		24	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			−40 TO 85°C		−40 TO 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −100 μA		1.65 V to 3.6 V	V_{CC} − 0.2			V_{CC} − 0.2		V_{CC} − 0.3		V
	I_{OH} = −4 mA		1.65 V	1.29			1.2		1.05		
	I_{OH} = −8 mA		2.3 V	1.9			1.7		1.55		
	I_{OH} = −12 mA		2.7 V	2.2			2.2		2.05		
			3 V	2.4			2.4		2.25		
	I_{OH} = −24 mA		3 V	2.3			2.2		2		
V_{OL}	I_{OL} = 100 μA		1.65 V to 3.6 V			0.1		0.2		0.3	V
	I_{OL} = 4 mA		1.65 V			0.24		0.45		0.6	
	I_{OL} = 8 mA		2.3 V			0.3		0.7		0.75	
	I_{OL} = 12 mA		2.7 V			0.4		0.4		0.6	
	I_{OL} = 24 mA		3 V			0.55		0.55		0.8	
I_I	V_I = 5.5 V or GND		3.6 V			±1		±5		±20	μA
I_{off}	V_I or V_O = 5.5 V		0			±1		±10		±20	μA
I_{OZ}	V_O = 0 to 5.5 V		3.6 V			±1		±10		±20	μA
I_{CC}	V_I = V_{CC} or GND	I_O = 0	3.6 V			1		10		40	μA
	3.6 V ≤ V_I ≤ 5.5 V [1]					1		10		40	
ΔI_{CC}	One input at V_{CC} − 0.6 V, Other inputs at V_{CC} or GND		2.7 V to 3.6 V			500		500		5000	μA
C_i	V_I = V_{CC} or GND		3.3 V		4						pF
C_o	V_O = V_{CC} or GND		3.3 V		5.5						pF

(1) This applies in the disabled state only.

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			−40 TO 85°C		−40 TO 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	1.5 V	1	7	14.4	1	14.9	1	16.4	ns
			1.8 V ± 0.15 V	1	5.9	10.4	1	10.9	1	12.4	
			2.5 V ± 0.2 V	1	4.2	7.4	1	7.9	1	10	
			2.7 V	1	4.2	6.7	1	6.9	1	8.2	
			3.3 V ± 0.3 V	1.5	3.9	5.7	1.5	5.9	1.5	7.2	
t_{en}	$\overline{OE}$	Y	1.5 V	1	8.3	17.8	1	18.3	1	19.8	ns
			1.8 V ± 0.15 V	1	6.4	12.1	1	12.6	1	14.1	
			2.5 V ± 0.2 V	1	4.6	9.1	1	9.6	1	11.7	
			2.7 V	1	5	8.4	1	8.6	1	10.3	
			3.3 V ± 0.3 V	1.5	4.5	7.4	1.5	7.6	1.5	9.4	
t_{dis}	$\overline{OE}$	Y	1.5 V	1	7.2	15.6	1	16.1	1	17.6	ns
			1.8 V ± 0.15 V	1	5.8	11.6	1	12.1	1	13.6	
			2.5 V ± 0.2 V	1	3.7	7.3	1	7.8	1	9.9	
			2.7 V	1	3.8	6.6	1	6.8	1	8.6	
			3.3 V ± 0.3 V	1.5	3.8	6.3	1.5	6.5	1.5	8	
$t_{sk(o)}$			3.3 V ± 0.3 V					1		1.5	ns

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Operating Characteristics

$T_A = 25°C$

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd} Power dissipation capacitance per buffer/driver	Outputs enabled	f = 10 MHz	1.8 V	43	pF
			2.5 V	43	
			3.3 V	44	
	Outputs disabled	f = 10 MHz	1.8 V	1	
			2.5 V	1	
			3.3 V	2	

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PARAMETER MEASUREMENT INFORMATION
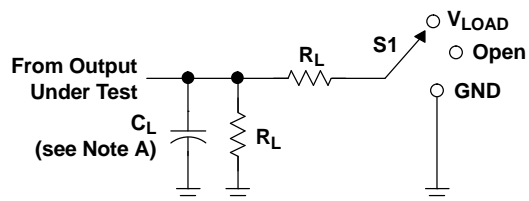
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

| V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.5 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	2 kΩ	0.1 V
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
3.3 V ± 0.3 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
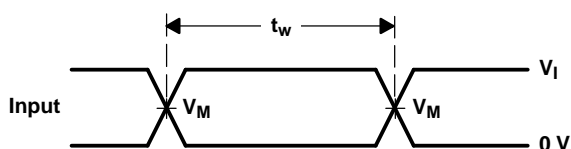
VOLTAGE WAVEFORMS
PULSE DURATION
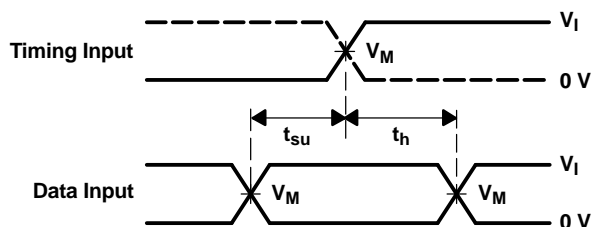
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES
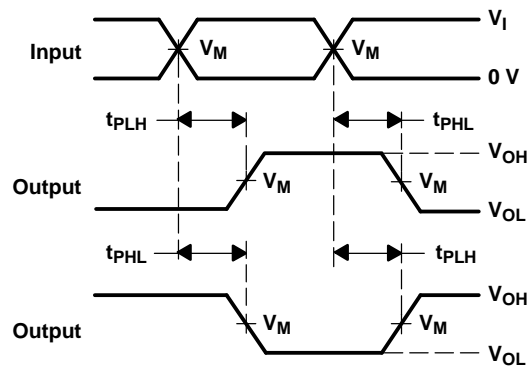
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS
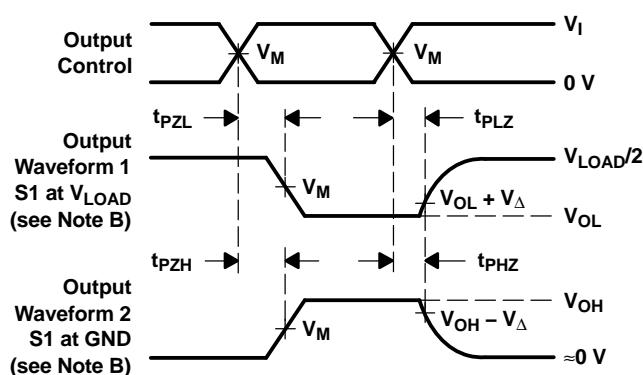
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O = 50$ Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC244ADBLE	OBSOLETE	SSOP	DB	20		TBD	Call TI	Call TI	-40 to 125		
SN74LVC244ADBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC244A	Samples
SN74LVC244ADBRE4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC244A	Samples
SN74LVC244ADBRG4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC244A	Samples
SN74LVC244ADGVR	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC244A	Samples
SN74LVC244ADGVRE4	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC244A	Samples
SN74LVC244ADGVRG4	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC244A	Samples
SN74LVC244ADW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC244A	Samples
SN74LVC244ADWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC244A	Samples
SN74LVC244ADWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC244A	Samples
SN74LVC244ADWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 125	LVC244A	Samples
SN74LVC244ADWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	LVC244A	Samples
SN74LVC244ADWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC244A	Samples
SN74LVC244AGQNR	OBSOLETE	BGA MICROSTAR JUNIOR	GQN	20		TBD	Call TI	Call TI	-40 to 85	LC244A	
SN74LVC244AN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	SN74LVC244AN	Samples
SN74LVC244ANE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	SN74LVC244AN	Samples
SN74LVC244ANSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC244A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC244ANSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC244A	Samples
SN74LVC244ANSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC244A	Samples
SN74LVC244APW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC244A	Samples
SN74LVC244APWE4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC244A	Samples
SN74LVC244APWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC244A	Samples
SN74LVC244APWLE	OBSOLETE	TSSOP	PW	20		TBD	Call TI	Call TI	-40 to 125		
SN74LVC244APWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 125	LC244A	Samples
SN74LVC244APWRE4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC244A	Samples
SN74LVC244APWRG3	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LC244A	Samples
SN74LVC244APWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC244A	Samples
SN74LVC244APWT	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC244A	Samples
SN74LVC244APWTE4	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC244A	Samples
SN74LVC244APWTG4	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC244A	Samples
SN74LVC244ARGYR	ACTIVE	VQFN	RGY	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC244A	Samples
SN74LVC244ARGYRG4	ACTIVE	VQFN	RGY	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC244A	Samples
SN74LVC244AZQNR	ACTIVE	BGA MICROSTAR JUNIOR	ZQN	20	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	LC244A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LVC244A :

● Automotive: SN74LVC244A-Q1

NOTE: Qualified Version Definitions:

    ● Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

![Texas Instruments logo] **PACKAGE MATERIALS INFORMATION**

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC244ADBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74LVC244ADGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC244ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LVC244ANSR	SO	NS	20	2000	330.0	24.4	8.2	13.0	2.5	12.0	24.0	Q1
SN74LVC244APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74LVC244APWRG3	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74LVC244APWT	TSSOP	PW	20	250	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74LVC244ARGYR	VQFN	RGY	20	3000	330.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1
SN74LVC244AZQNR	BGA MICROSTAR JUNIOR	ZQN	20	1000	330.0	12.4	3.3	4.3	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC244ADBR	SSOP	DB	20	2000	367.0	367.0	38.0
SN74LVC244ADGVR	TVSOP	DGV	20	2000	367.0	367.0	35.0
SN74LVC244ADWR	SOIC	DW	20	2000	366.0	364.0	50.0
SN74LVC244ANSR	SO	NS	20	2000	367.0	367.0	45.0
SN74LVC244APWR	TSSOP	PW	20	2000	364.0	364.0	27.0
SN74LVC244APWRG3	TSSOP	PW	20	2000	364.0	364.0	27.0
SN74LVC244APWT	TSSOP	PW	20	250	367.0	367.0	38.0
SN74LVC244ARGYR	VQFN	RGY	20	3000	367.0	367.0	35.0
SN74LVC244AZQNR	BGA MICROSTAR JUNIOR	ZQN	20	1000	338.1	338.1	20.6

GQN (R−PBGA−N20)　　　　PLASTIC BALL GRID ARRAY

1,95

0,65

0,325

3,10 / 2,90

B

A

4,10 / 3,90

2,60

0,65

E

D

C

B

A

1　2　3　4

Ball A1 Corner
Index Area

Ball A1 Identifier

Bottom View

20X Ø 0,45 / 0,35

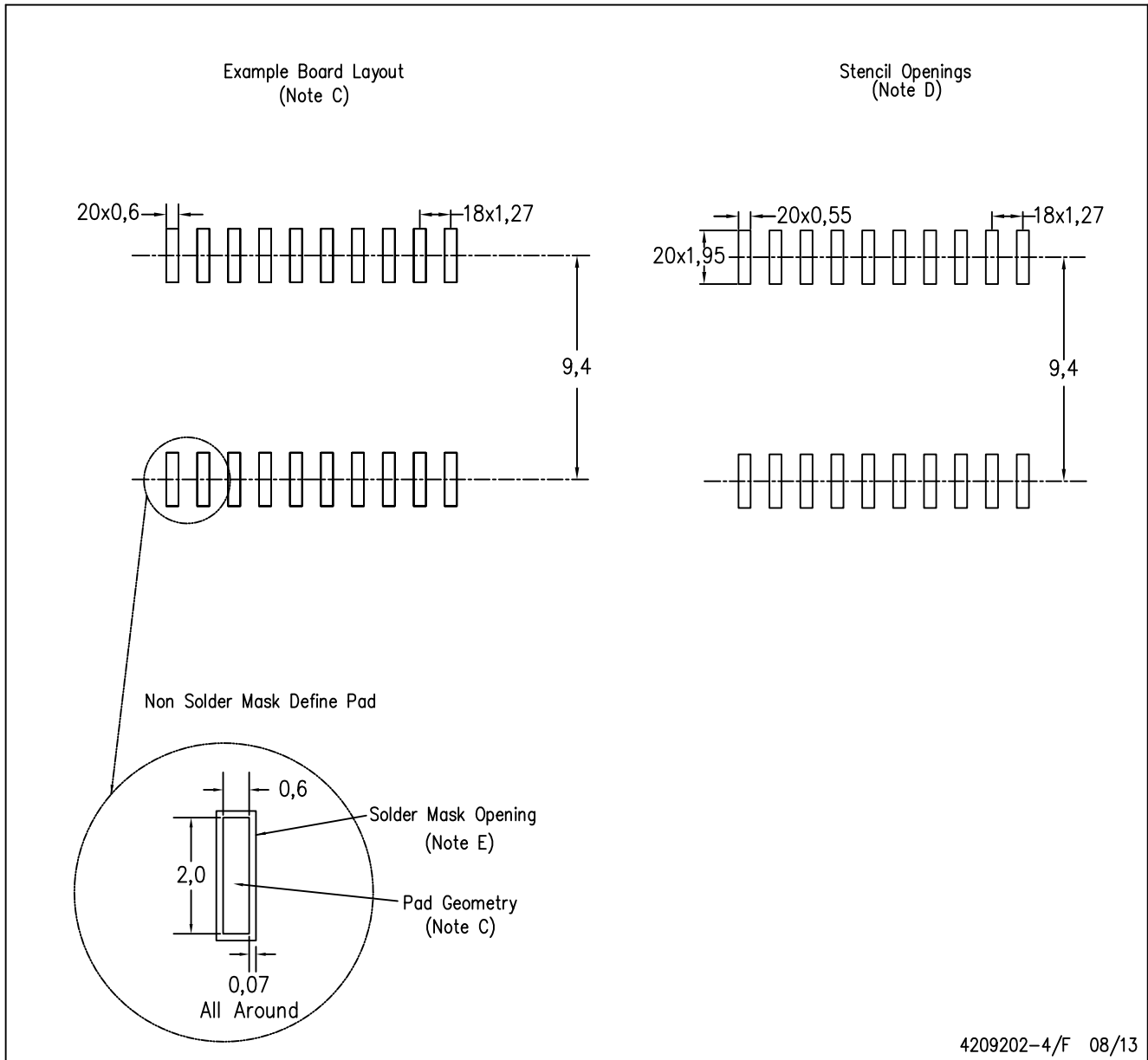| ⊕	Ø 0,15 Ⓜ	C	A	B
	Ø 0,08 Ⓜ	C		

1,00 Max

0,10 C

Seating Plane

0,35 / 0,15

C
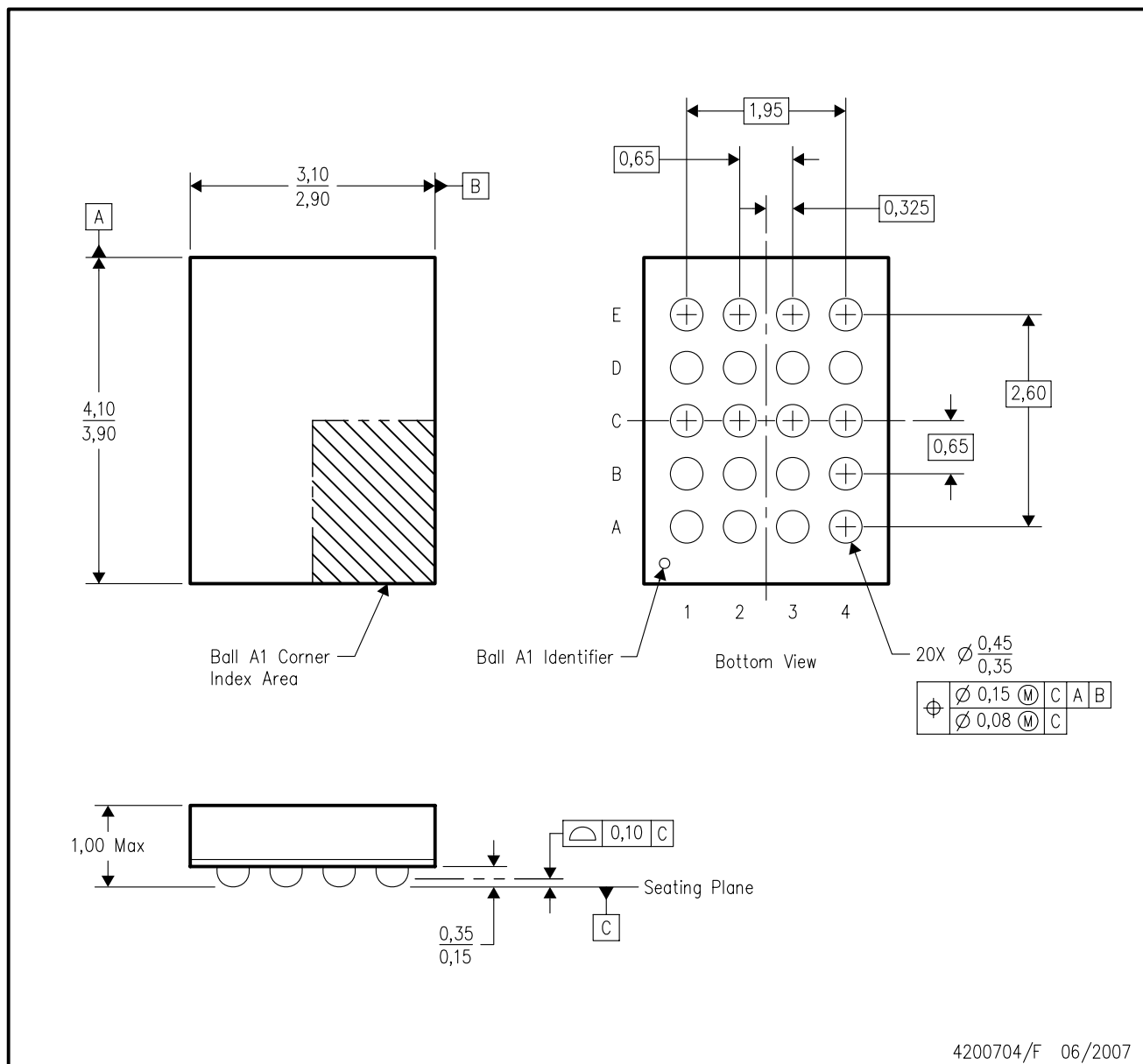
4200704/F　06/2007

NOTES:　A.　All linear dimensions are in millimeters.　Dimensioning and tolerancing per ASME Y14.5M−1994.
　　　　B.　This drawing is subject to change without notice.
　　　　C.　Falls within JEDEC MO−285 variation BC−2.
　　　　D.　This package is tin−lead (SnPb).　Refer to the 20 ZQN package (drawing 4204492) for lead−free.

ZQN (R−PBGA−N20)   PLASTIC BALL GRID ARRAY
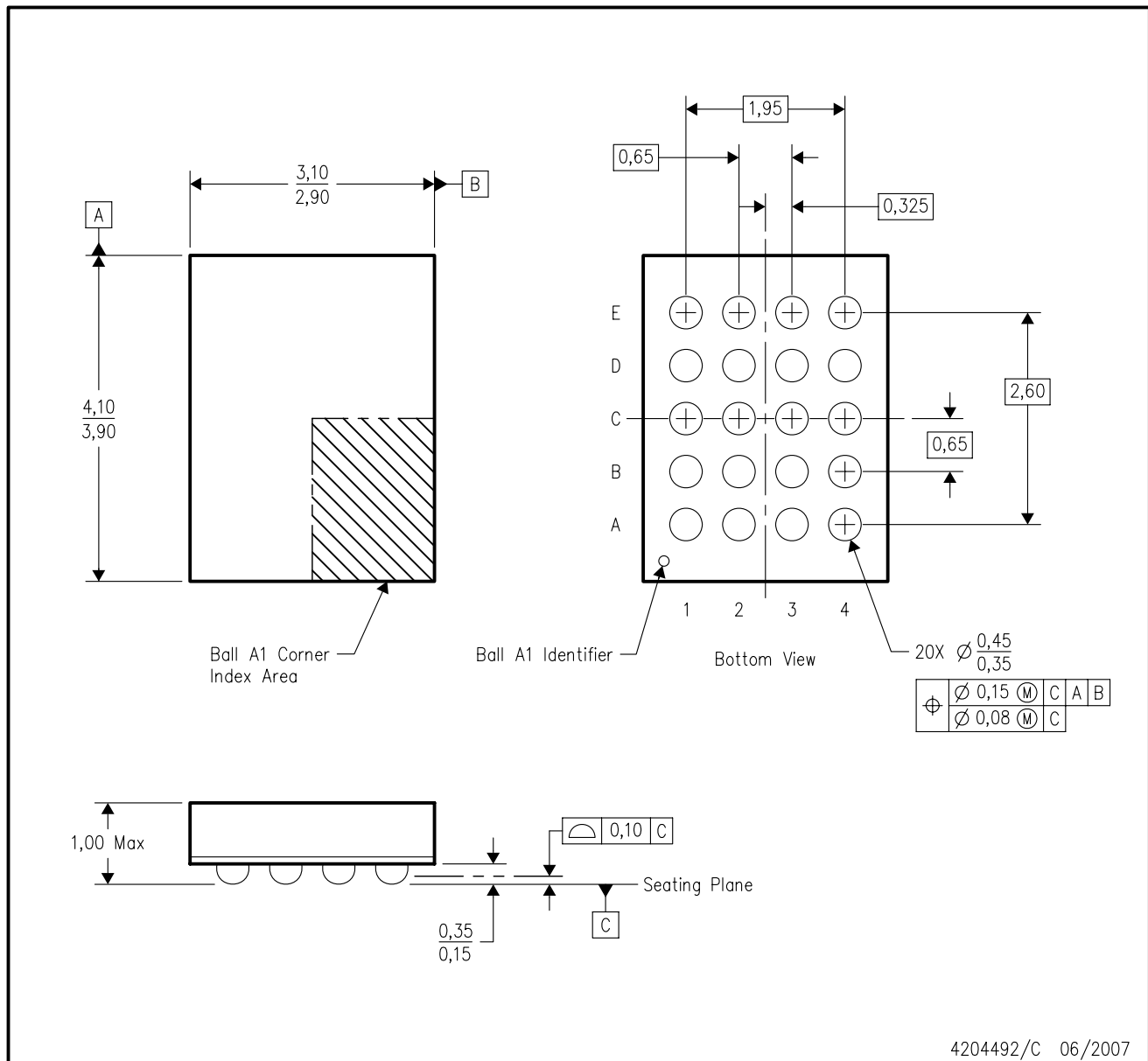
3,10
2,90 B

A

4,10
3,90

Ball A1 Corner
Index Area

1,95

0,65

0,325

E
D
C
B
A

2,60

0,65

1   2   3   4

Ball A1 Identifier

Bottom View

20X ∅ 0,45
         0,35

⊕	∅ 0,15 Ⓜ	C	A	B
	∅ 0,08 Ⓜ	C		

1,00 Max

0,10 C

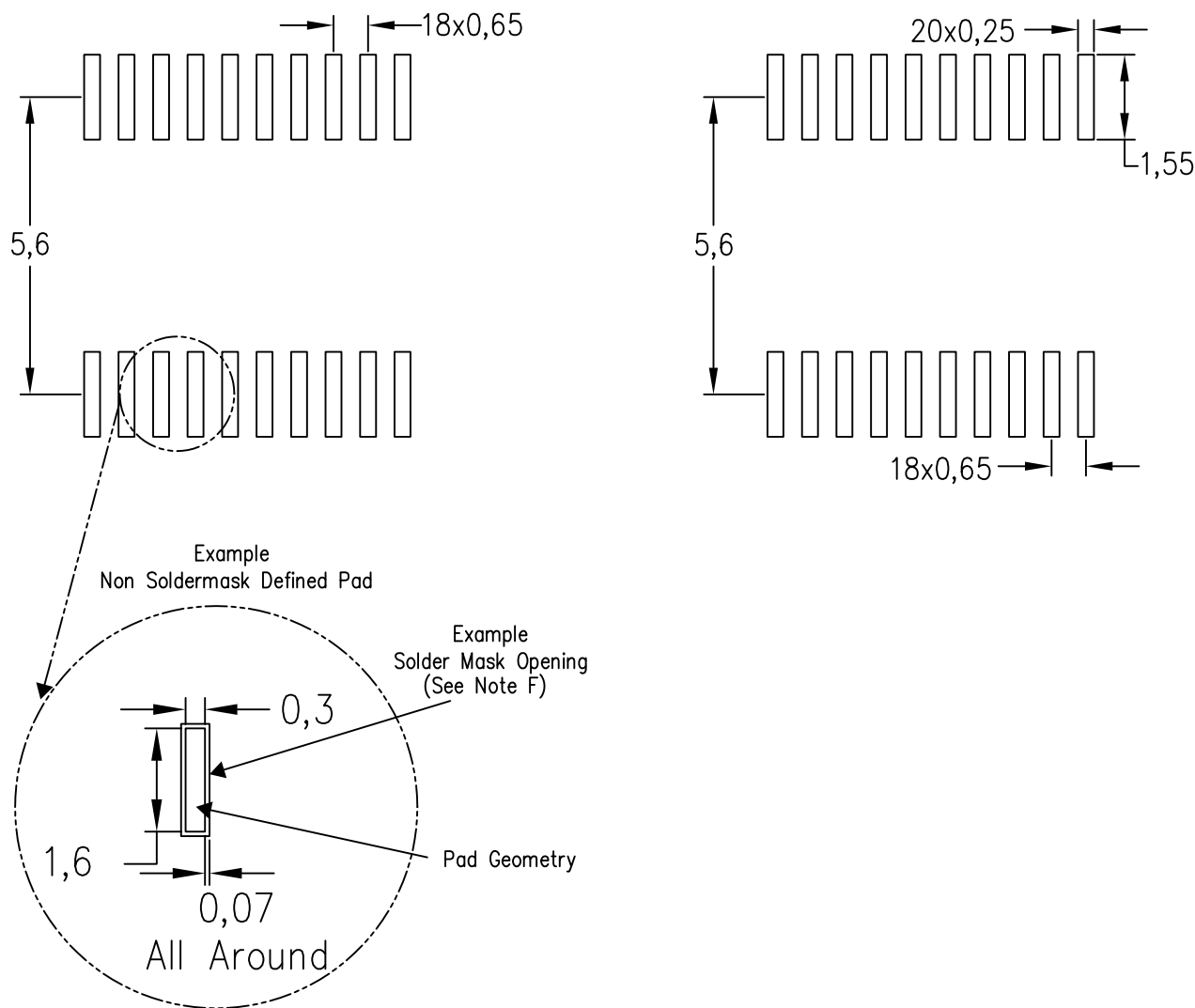Seating Plane

0,35
0,15

C

4204492/C   06/2007

NOTES: A.   All linear dimensions are in millimeters.   Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.   This drawing is subject to change without notice.
         C.   Falls within JEDEC MO−285 variation BC−2.
         D.   This package is lead−free.   Refer to the 20 GQN package (drawing 4200704) for tin−lead (SnPb).

TEXAS INSTRUMENTS
www.ti.com

N (R−PDIP−T**)

PLASTIC DUAL−IN−LINE PACKAGE

16 PINS SHOWN

DIM	PINS **	14	16	18	20
A MAX		0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN		0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION △C		AA	BB	AC	AD

A

16   9

0.260 (6,60)
0.240 (6,10)

1   8

0.070 (1,78)
0.045 (1,14) △D

0.045 (1,14)
0.030 (0,76) △D

0.020 (0,51) MIN

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)

0.200 (5,08) MAX

Gauge Plane

Seating Plane

0.125 (3,18) MIN

0.010 (0,25) NOM

0.100 (2,54)

0.021 (0,53)
0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

0.430 (10,92) MAX
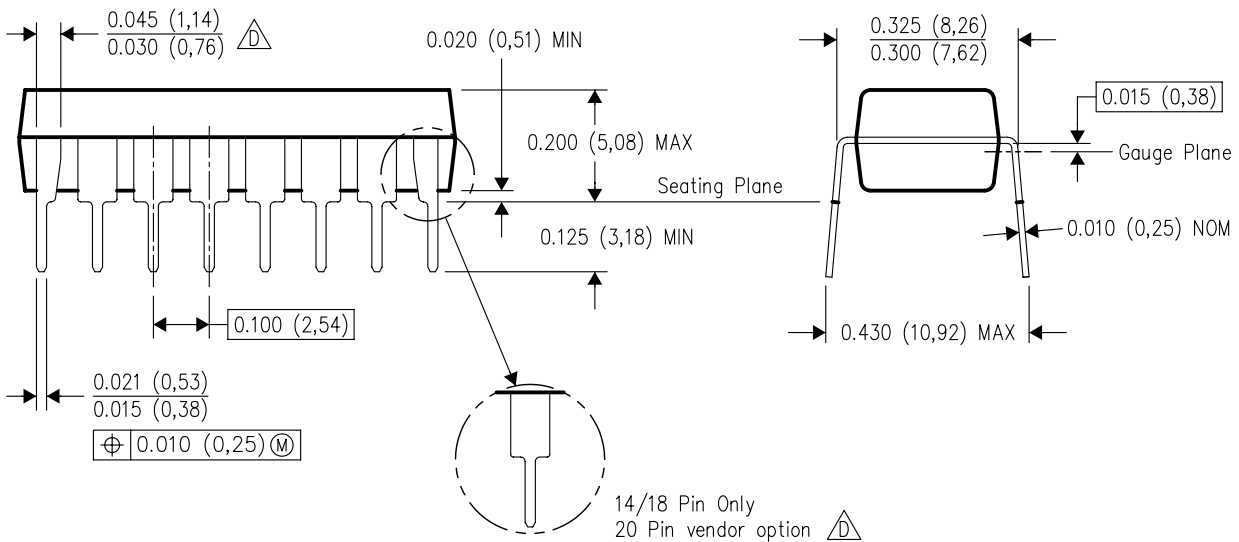
14/18 Pin Only
20 Pin vendor option △D

4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
      △C Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
      △D The 20 pin end lead shoulder width is a vendor option, either half or full width.

DGV (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN

DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

TEXAS INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

DW (R−PDSO−G20)   PLASTIC SMALL OUTLINE

0.512 (13,00)
0.496 (12,60)

20   11

0.419 (10,63)
0.393 (9,97)

0.299 (7,60)
0.291 (7,40)

1   10

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ | 0.010 (0,25) Ⓜ

0.104 (2,65) Max

0.012 (0,30)
0.004 (0,10)

0.013 (0,33)
0.008 (0,20)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)

0°−8°

0.050 (1,27)
0.016 (0,40)
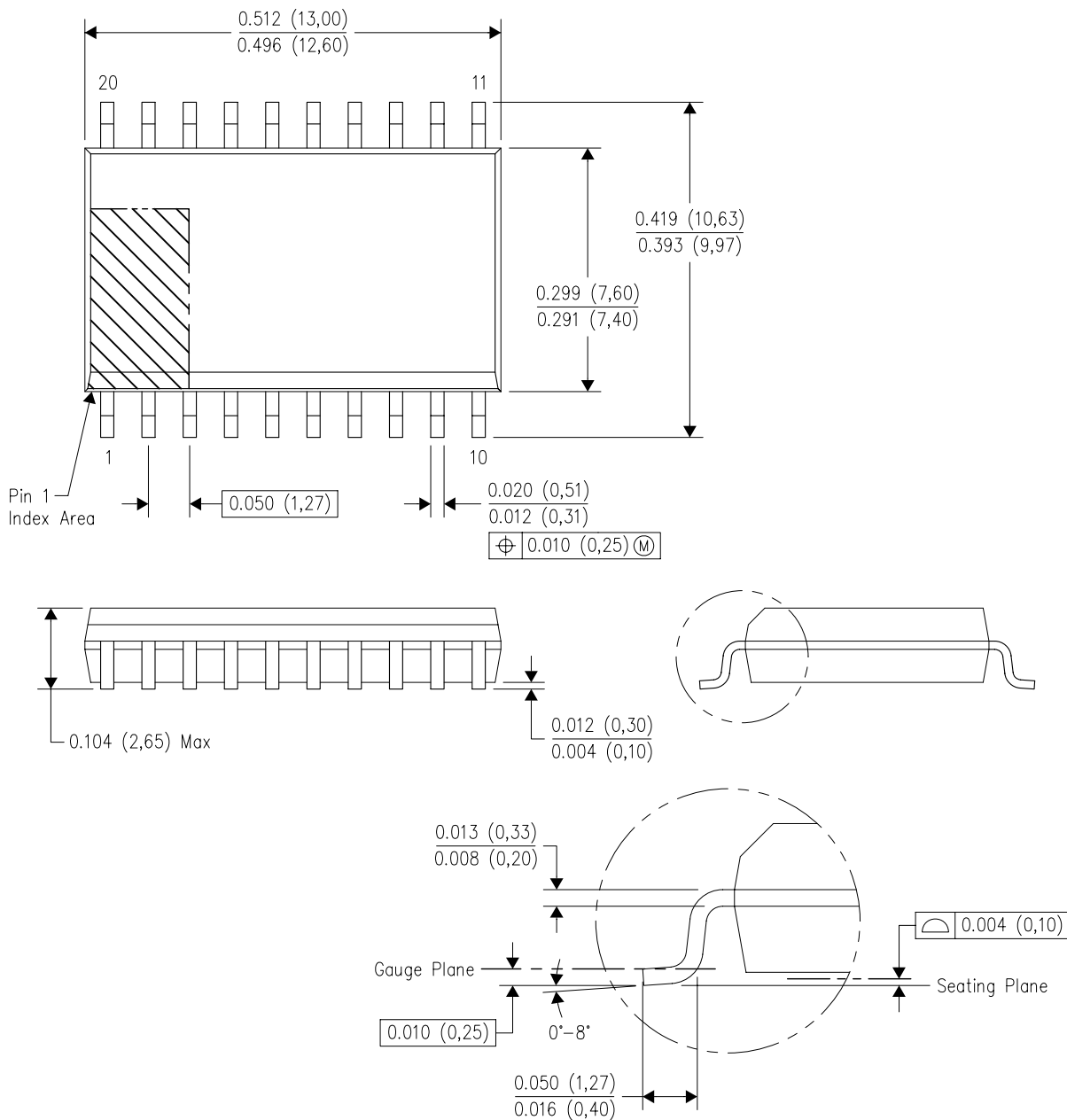
4040000−4/G 01/11

NOTES: A.   All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
         D.   Falls within JEDEC MS−013 variation AC.

DW (R−PDSO−G20)   PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

Stencil Openings
(Note D)

20x0,6

18x1,27

20x0,55

18x1,27

20x1,95

9,4

9,4

Non Solder Mask Define Pad

0,6

Solder Mask Opening
(Note E)

2,0

Pad Geometry
(Note C)

0,07
All Around

4209202−4/F   08/13

NOTES: A.   All linear dimensions are in millimeters.
              B.   This drawing is subject to change without notice.
              C.   Refer to IPC7351 for alternate board design.
              D.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
                   contact their board assembly site for stencil design recommendations. Refer to IPC−7525
              E.   Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

TEXAS INSTRUMENTS
www.ti.com

PW (R−PDSO−G20)   PLASTIC SMALL OUTLINE

4040064−5/G   02/11

NOTES: A.   All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.   This drawing is subject to change without notice.
         C.   Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
         D.   Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
         E.   Falls within JEDEC MO−153

TEXAS INSTRUMENTS
www.ti.com

PW (R−PDSO−G20)   PLASTIC SMALL OUTLINE

Example Board Layout

Based on a stencil thickness
of .127mm (.005inch).

18x0,65

20x0,25

1,55

5,6

5,6

18x0,65

Example
Non Soldermask Defined Pad

Example
Solder Mask Opening
(See Note F)

0,3

Pad Geometry

1,6

0,07
All Around

4211284−5/F   12/12

NOTES: A. All linear dimensions are in millimeters.
         B. This drawing is subject to change without notice.
         C. Publication IPC−7351 is recommended for alternate design.
         D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
             contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
         E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DB (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN

	PINS **	14	16	20	24	28	30	38
DIM								
A MAX		6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN		5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
        D. Falls within JEDEC MO-150

RGY (R−PVQFN−N20)   PLASTIC QUAD FLATPACK NO−LEAD

4,65
4,35 ⬛ A

⬛ B

19   12

20   11

3,65
3,35

1   10

Pin 1 Index Area
Top and Bottom

2   9

⬡ F

0,20 Nominal
Lead Frame

1,00
0,80

Seating Plane

⌓ 0,08 C

0,05
0,00
Seating Height

⬛ C

3,50

0,50

20X 0,50
     0,30

THERMAL PAD

2   9

1   10

1,50

SIZE AND SHAPE
SHOWN ON SEPRATE SHEET

20   11

19   12

20X 0,30
     0,18

+0,10

⊕ | 0,10 Ⓜ | C | A | B |
  | 0,05 Ⓜ | C |

Bottom View
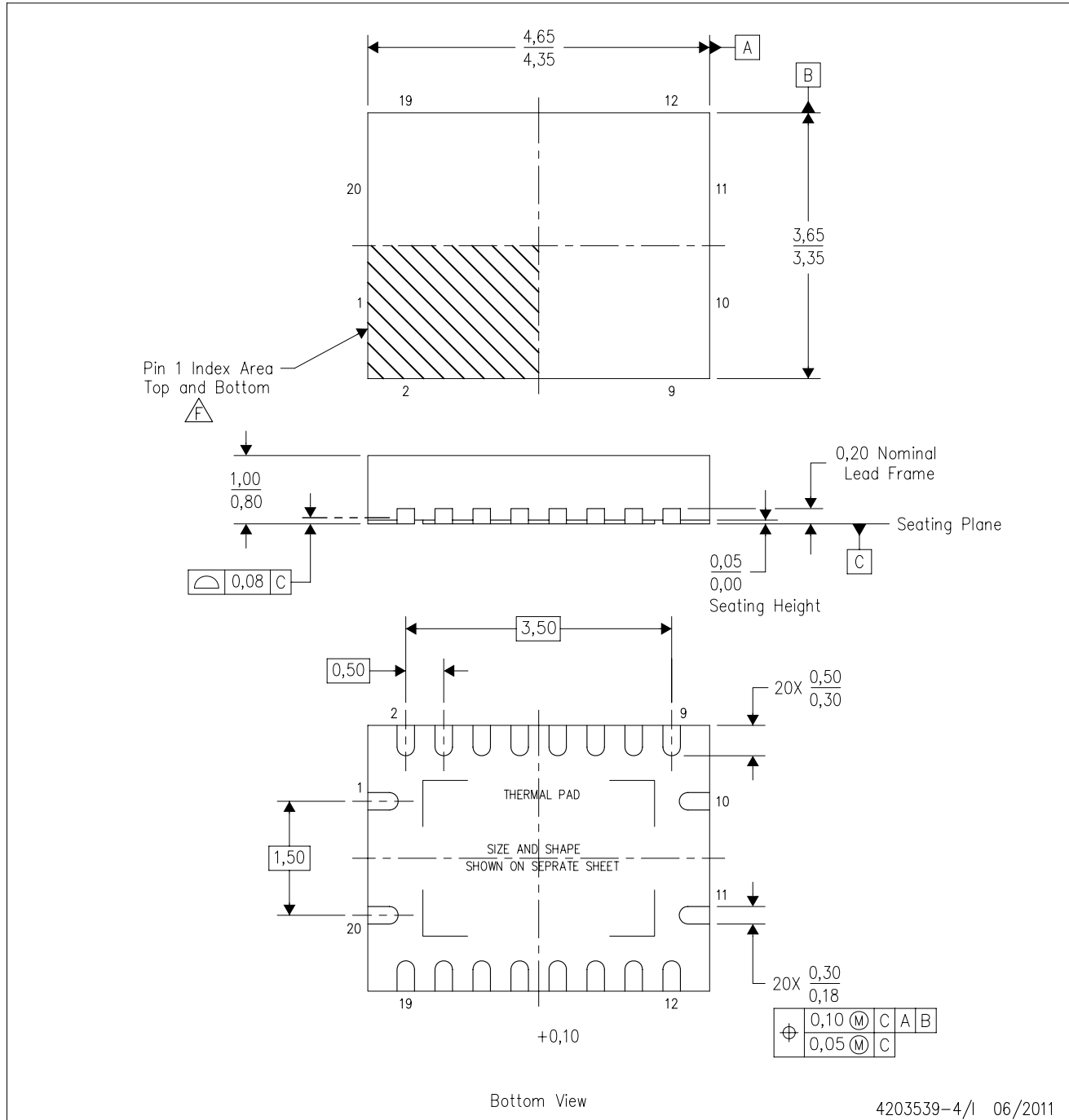
4203539−4/I   06/2011

NOTES: A.   All linear dimensions are in millimeters.   Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.   This drawing is subject to change without notice.
         C.   QFN (Quad Flatpack No−Lead) package configuration.
         D.   The package thermal pad must be soldered to the board for thermal and mechanical performance.
         E.   See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
    ⬡ F   Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated.
         The Pin 1 identifiers are either a molded, marked, or metal feature.
         G.   Package complies to JEDEC MO−241 variation BA.

MECHANICAL DATA

NS (R-PDSO-G)**   PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

IMPORTANT NOTICE

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