Tomasulo 2009 Issue Unit and CDB Controller

USC
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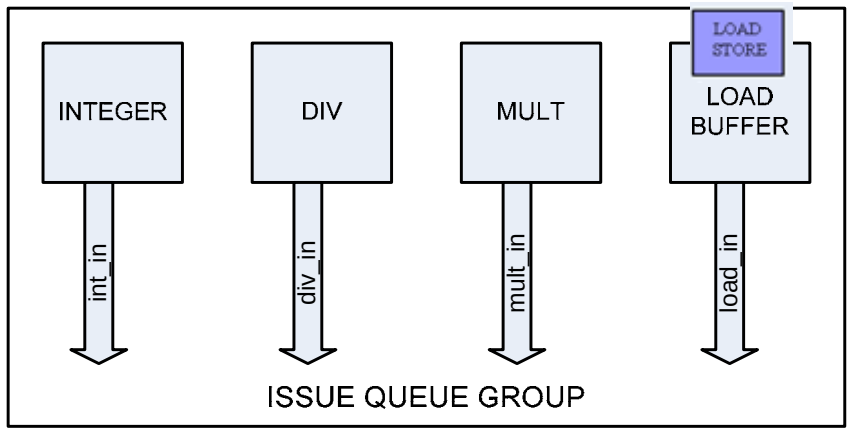
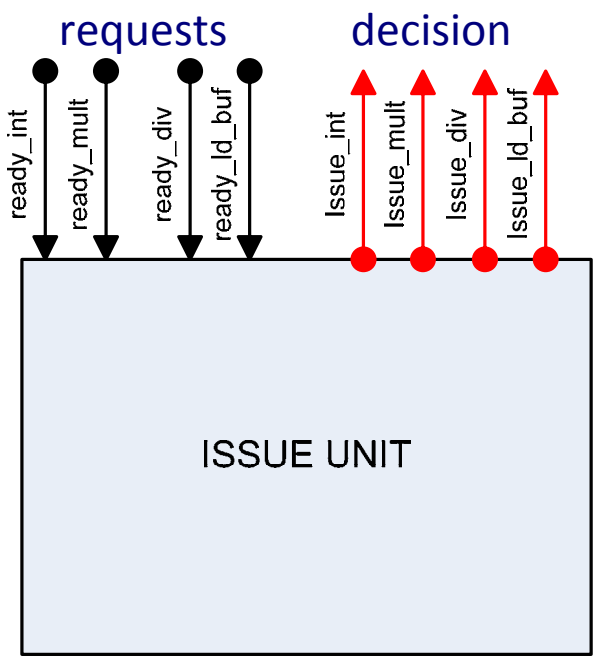
Four Issue Queues send instructions to the Fuctional Units (FUs)

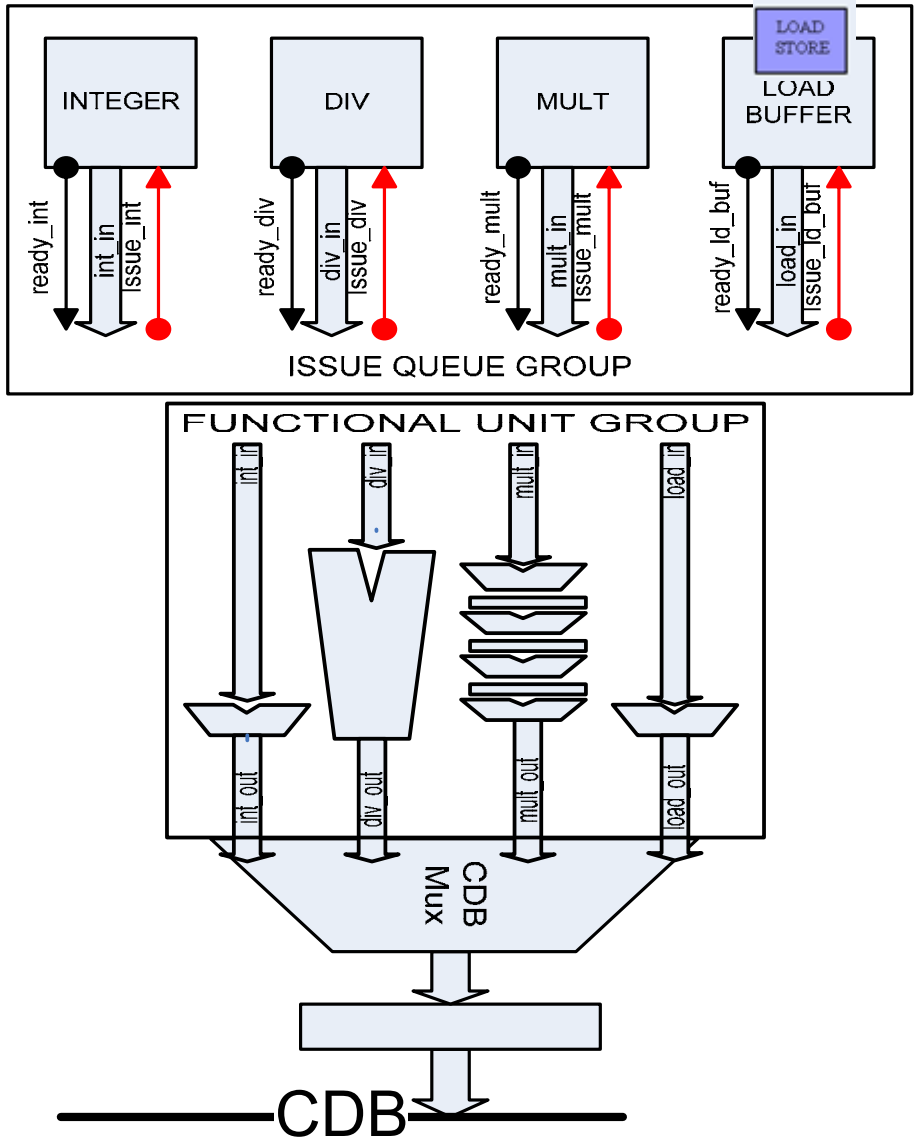


- Integer Issue Queue, Div Issue Queue and Mult Issue Queue are exactly same.
- Lw/Sw Queue is little different because of the memory disambiguation rules resulting in need of Address Buffer and counters.

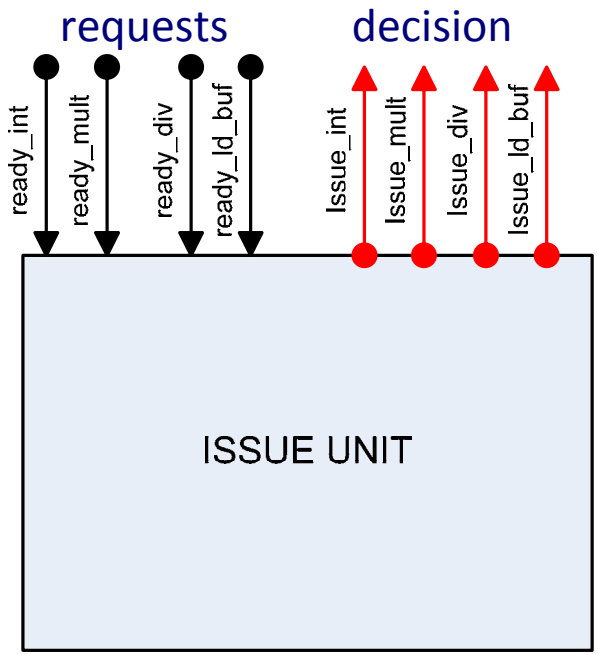
Issue Unit generates the mux-control signals

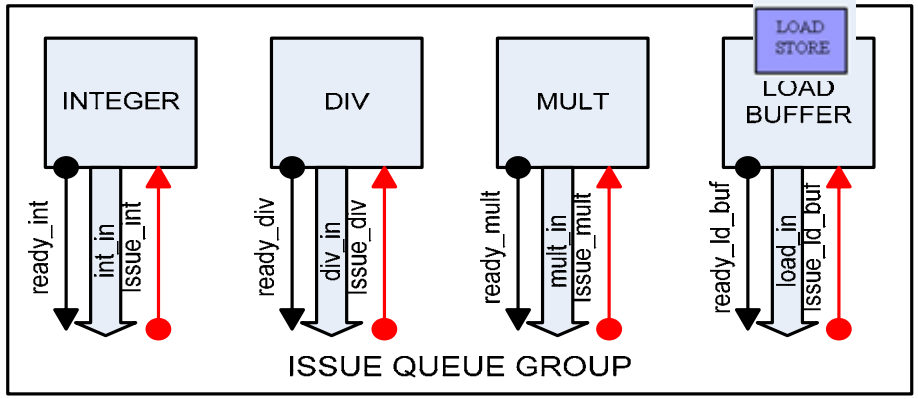
Receive requests from one of the Issue Queues and make Issue Decision

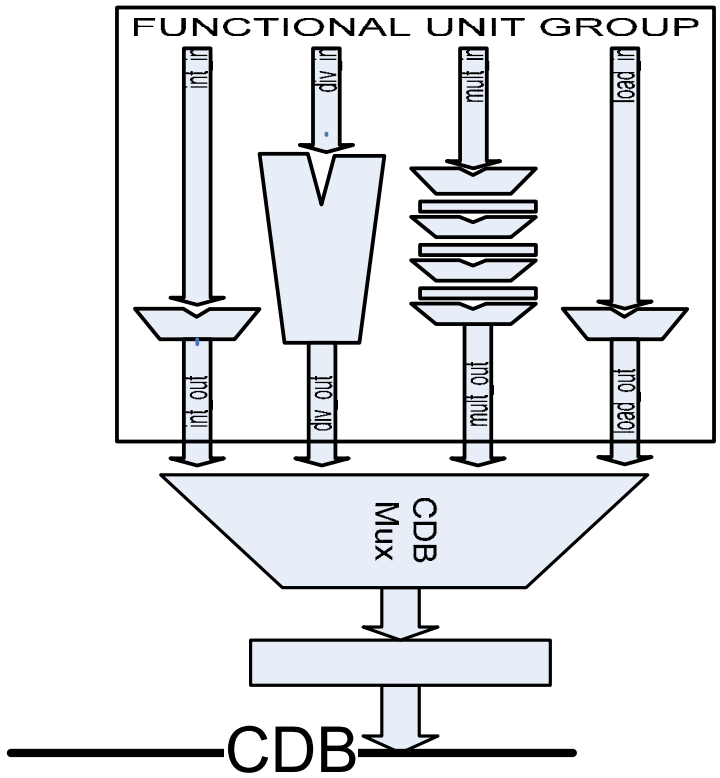




Issue decision goes to the Issue Queue and CDB Mux





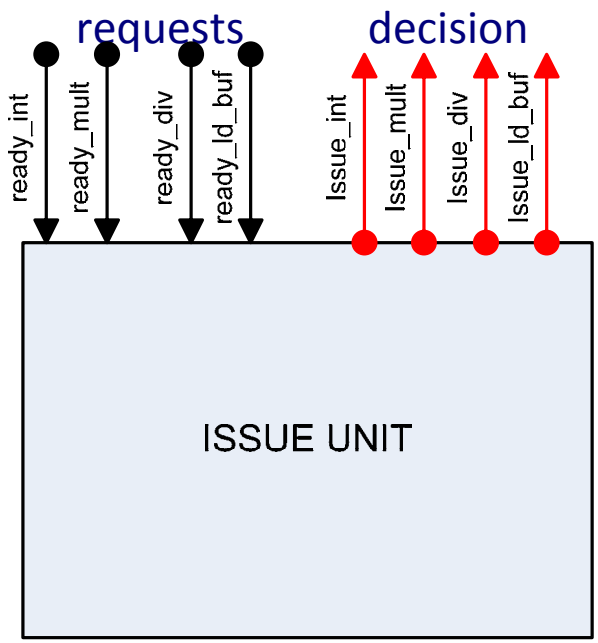


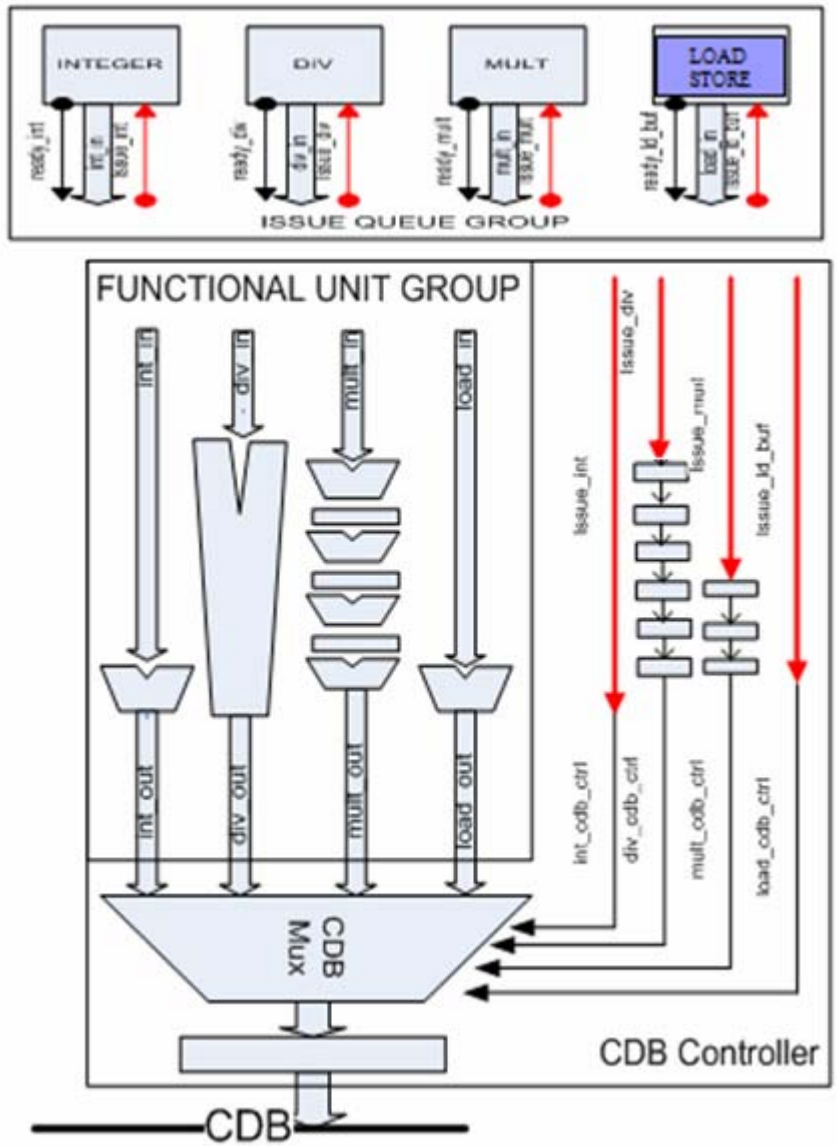
To Issue Queue
- acknowledgement to the Issue request

To CDB Mux
- Mux control signal

Send Mux control signals right away?

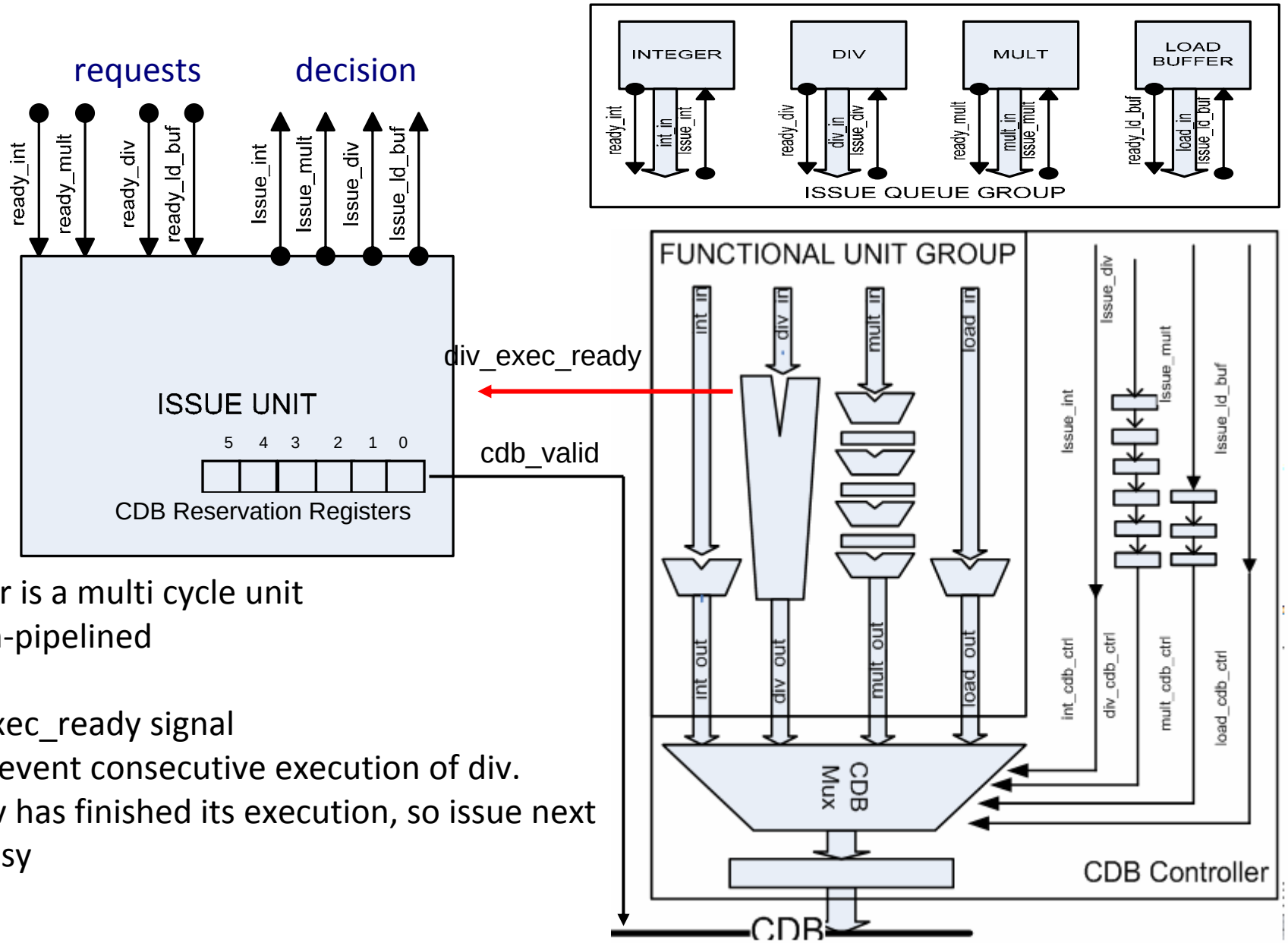
Mux control signals travel through stage registers along with the FU data





Causes BUS contention ?
(or collision of CDB Mux controls ?)

To avoid collision, employ a bus reservation table



divider is a multi cycle unit
- non-pipelined

div_exec_ready signal
to prevent consecutive execution of div.
1: div has finished its execution, so issue next
0: busy

Inside the Issue Unit

Issue Policy
-long-latency instruction first
-LRU for instructions of same later
(decided on by using the rd tag inf

Latencies
-div: 6 clocks + 1 clock
-mult: 3 clocks (pipelined) + 1clock
-int: 1 clock
-ld_buf: 1 clock

LRU_bit
1: int has priority
0: ld_buf has priority

if both requested,
- issue according to the LRU_bit
if one of them requested,
- issue it

Up to 3 instructions enter the CDB
Reservation Register