Common Data Bus

Salient feature –

- Flushing the CDB in case of miss-predicted branch or by Jr flush signal generated by ALU.
- Rob depth of the instruction on CDB is calculated and given to all modules.
- For a branch, jr $31 instruction if mispredicted a flush signal is generated and informed to all the required modules.

- **flush operation:** When CDB_flush signal (mispredicted branch or jr $31) is asserted then using the rob_depth, rob_top and instr_tag identify if the instruction is younger to branch or not. If younger flush it. NOTE: if Its Jr $31 then depending upon ALU_ JR_Flush (result from ALU which is generated continuously by ALU).
- **How to identify a younger instruction:** simple compare the depth of the instruction with depth of branch instruction, if greater depth then the instruction is younger and needs to be flushed.
- Control signals from issue queues properly delayed through shift registers (6 clocks for div and 3 clocks for mult instructions) controls the mux in front of CDB (taken care by issue unit).
- **NOTE:** Remember to do modulo - 32 operation while calculating the depth of each instruction in issue queues.