Characteristic Description

TM1908 is a dedicated circuit with single line three-channel LED constant current drive, which adopts the integrated packaging of lampwick. It is internally integrated with MCU single line digital interface, data latch, LED constant current drive, PWM brightness control, Gamma correction and other circuits. It can be cascaded through two-channel input and output digital interfaces, and the external controller only needs a single line to control the chip. The standby communication port can realize the function that the damage of a chip in the cascade will not affect the normal use of the subsequent stage. The constant current value and PWM brightness value output by each OUT drive port can be set separately by commands. This product has excellent performance and reliable quality.

Functional Features

- Working voltage: 4.0-5.5V
- The current of each channel can be set independently, the output of constant current drive is 2mA-25mA, 128 levels adjustable.
- R/G/B output brightness class: 65536 (GAMA correction)
- Accurate current output value
  Maximum error (channel and channel) : ±3%
  Maximum error (chip and chip) : ±5%
- Single line dual channel serial cascade interface: The chip data interface can be input through command configuration DIN or FDIN pin. In normal mode, the input interfaces switch with each other; in DIN working mode, the data is input by DIN pin; in FDIN working mode, the data is input by FDIN pin. D01 and D02 pin forward the cascaded data. The signal will not affect the normal operation of other chips due to the abnormality of one chip, so as to ensure the reliability.
- DENL port is introduced to ensure normal data communication and greatly reduce the number of wiring and the installation cost of the project when it is applied on the external large screen.
- Oscillation mode: built-in oscillation and clock synchronization according to the signal on the data line. After receiving the data of this unit, it can automatically regenerate the subsequent data and send it to the lower level through the data output terminal. The signal will not be distorted or attenuated as the cascade gets further away.
- Built-in power on reset circuit, which initializes all registers to zero after power-on reset.
- Data transmission rate 1.2MHz
- Application fields: point light source, guardrail tube, soft light belt, indoor and outdoor large screen, etc.
- Packaging form: integrated packaging of lampwick

Internal Structure Block Diagram

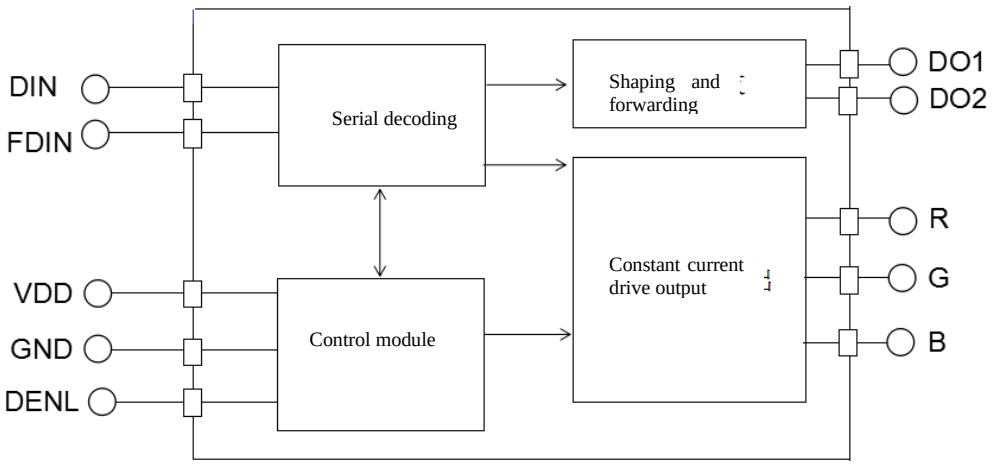


Figure 1

Pin Function

Pin Name	Pin No.	I/O	Function Description
DIN	1	I	Data input
FDIN	2	I	Standby data input
DENL	3	I	Data input enable, active low, built-in 10K pull-down
DO1	4	O	Data cascade forwarding output 1
DO2	5	O	Data cascade forwarding output 2
R	6	O	Red N tube open drain, constant current output
G	7	O	Green N tube open drain, constant current output
B	8	O	Blue N tube open drain, constant current output
GND	9	--	Power ground
VDD	10	--	Positive pole of power supply

Equivalent Circuit of Inputs and Outputs

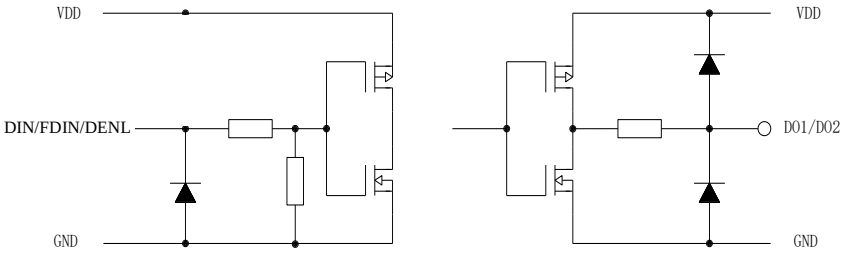


Figure 2

Integrated circuit is an electrostatic sensitive device, which is easy to generate a large number of static electricity when used in dry season or dry environment. Electrostatic discharge may damage integrated circuit. Titan Micro Electronics recommends taking all appropriate preventive measures for integrated circuit. Improper operation and welding may cause ESD damage or performance degradation, and the chip cannot work normally.

Maximum Ratings

Parameter Name	Symbol	Rating	Unit
Logic supply voltage	VDD	-0.4～+7.0	V
DIN, FDIN port voltage	Vin	-0.4～VDD+0.5	V
OUT port voltage	Vout	-0.4～+5.5	V
Operating temperature range	Topr	-40～+85	℃
Storage temperature range	Tstg	-50～+150	℃
Electrostatic ESD	Human Body Model (HBM)	4000	V

(1) For the ratings in the table above, the chip may cause permanent damage to the device and reduce the reliability of the device under long-term use. We do not recommend that the chip work beyond these maximum ratings under any other conditions;
(2) All voltage values are systematically tested relative to each other.

Recommended Operating Conditions

Test at -40 - +85℃, unless otherwise specified			TM1908			Unit
Parameter Name	**Symbol**	**Testing Conditions**	**Min.**	**Typical**	**Max.**	
Power supply voltage	VDD		4.0	5.0	5.5	V
DIN, FDIN port voltage	Vin	VDD=5V, DIN, FDIN concatenation 1KΩ resistance			VDD+0.4	V
DO1, DO2 port voltage	Vdo	VDD=5V, DO1, DO2 concatenation 1KΩ resistance			VDD+0.4	V
OUT port voltage	Vout	OUT＝OFF			5	V

Electrical Characteristics

Test at VDD = 4.0-5.5V and working temperature - 40 - + 85 ℃, unless otherwise specified			TM1908			Unit
Parameter Name	**Symbol**	**Testing Conditions**	**Min.**	**Typical**	**Max.**	
High level output voltage	Voh	Ioh=6mA	VDD-0.5			V
Low level output voltage	Vol	Iol=10mA			0.3	V
High level input voltage	Vih	VDD=5.0V	3.5		VDD	V
Low level input voltage	Vil	VDD=5.0V	0		1	V
High level output current	Ioh	VDD=5.0V, Vdo=4.9V		1.4		mA
Low level output current	Iol	VDD=5.0V, Vdo=0.4V		12		mA
Input current	Iin	DIN, FDINconnect VDD		500		μA
Quiescent current	IDD	VDD=4.0V, GND=0V, other ports are vacant		0.8		mA
OUT output current	Iout	R, G, B=ON, Vout=3.0V	2		25	mA
OUT output leakage current	Iolkg	R, G, B=OFF, Vout=5V			0.3	μA
Constant current error between channels	ΔIolc0	R, G, B=ON, Vout=3.0V			±3	%
Constant current error between chips	ΔIolc1	R, G, B=ON, Vout=3.0V			±5	%

Switching Characteristics

Test at VDD = 4.0-5.5V and working temperature - 40 - + 85 ℃, typical value VDD = 5.0V, TA = + 25 ℃, unless otherwise specified.			TM1908			Unit
Parameter Name	**Symbol**	**Testing Conditions**	**Min.**	**Typical**	**Max.**	
Data rate	Fin			1.2		MHz
OUT PWM output frequency	Fout	R, G, B		2		KHz
Transmission delay time	Tpzl	DIN → DO1, DO2 FDIN → DO1, DO2		150		ns
Input capacitance	Ci				15	pF

Temporal Characteristics

Parameter Name	Symbol	Testing Conditions	Min.	Typical	Max.	Unit
Input 0 code, high level time	T0h		200	240	280	ns
Input 1 code, high level time	T1h		400	480	560	ns

Output 0 code, high level time	T0h’	VDD=5.0V GND=0V	200	240	280	ns
Output 1 code, high level time	T1h’		400	480	560	ns
0 code or 1 code period	T0/T1			830		ns
Reset code, low level time	Treset		80			μs

(1) The chip can work normally when the 0 code or 1 code period is in the range of 830ns (frequency 1.2MHz) to 2.5μs (frequency 400kHz), but the high level time of 0 code and 1 code must conform to the corresponding value range in the table above;

(2) When there is no need to reset, the low level time between bytes shall not exceed 25μs, otherwise the chip may reset, and receive data again after reset, which cannot achieve the correct transmission of data.

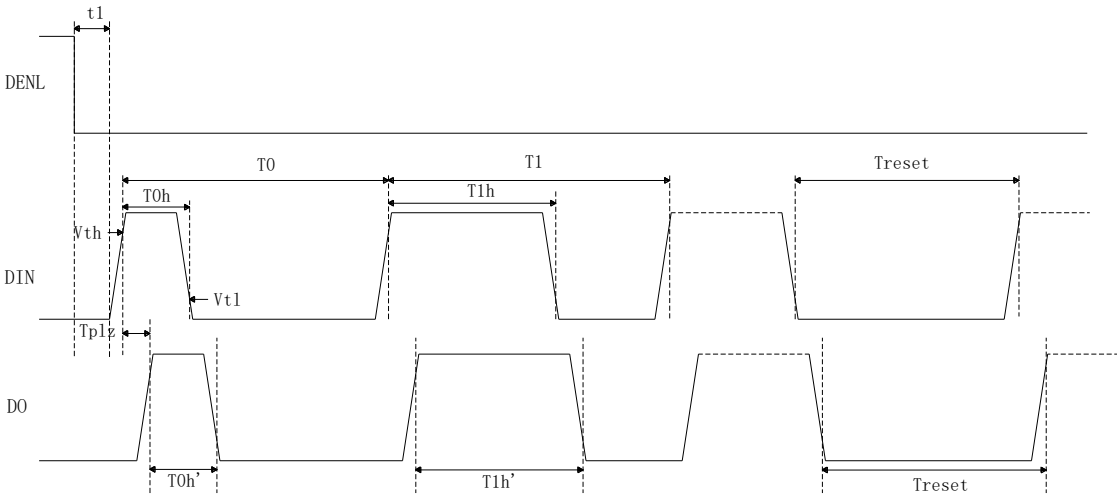


Figure 4

Functional Description

1. Mode Setting

The chip is a single line dual channel communication, using the way of return to zero code to send signals.

Before the chip receives the display data, it needs to configure the correct working mode and select the way to receive the display data. There are a total of 48 bits of mode setting commands, of which the first 24bit is the command code and the last 24bit is the test inverse code. After the chip is reset, it begins to receive data. There are four types of mode setting commands as follows:

(1) 0XFFFFFF_000000 command:

The chip is configured to normal working mode. In this mode, the display data is received by DIN by default for the first time. If the chip detects that there is a signal input to the port, it will keep use the port to receive the display data; if no data is received for more than 160ms, it will switch to FDIN to receive display data; if the chip detects that there is a signal input to the port, it will keep use the port to receive the display data. If no data is received for more than 160ms, it will switch to DIN again to receive the display data. DIN and FDIN switch in turn to receive display data.

(2) 0XFFFFFA_000005 command:

The chip is configured to DIN working mode. In this mode, the chip only receives the display data input from the DIN terminal, and the data from FDIN terminal is invalid.

(3) 0XFFFFF5_00000A command:

The chip is configured to FDIN working mode. In this mode, the chip only receives the display data input from the FDIN terminal, and the data input from DIN terminal is invalid.

(4) 0XFFFFF0_00000F command:

The chip is configured for test mode.

2. Display Data

After the chip is powered on and reset and receives the mode setting command, it starts to receive the constant current value setting command, and then receives the display data. After receiving 24 bits, DO1 and DO2 ports start to forward the data sent continuously from DIN or FDIN to provide the display data for the

next cascade chip. DO1 and DO2 ports are always low level until the data is forwarded. If the reset signal is input at the DIN or FDIN terminal, the OUT port of the chip will output the PWM waveform of corresponding duty ratio according to the 24bit display data received, and the chip waits for receiving new data again. After receiving the first 24bit data, the data will be forwarded through the DO port. Before the chip receives the reset signal, the original output of R, G and B will remain unchanged.

The chip adopts automatic shaping and forwarding technology, and the signal will not be distorted and attenuated. For all the chips cascaded together, the data transmission cycle is the same.

3. One Frame Complete Data Structure

C1	C2	C3	D1	D2	D3	D4	…	Dn	Reset	C1	C2	C3	D1	D2	D3	D4	…	Dn	Reset

C1 and C2 are mode setting commands, each of which contains 24bit data bits. Each chip will receive and forward C1 and C2, of which 0xFFFFFF_000000 is the normal working mode command, 0xFFFFFA_000005 is the DIN working mode command, 0xFFFFF5_00000A is the FDIN working mode command, 0XFFFFF0_00000F is the chip test mode command, C3 is the constant current value setting command, and each chip will receive and forward C1, C2 and C3.

D1, D2, D3, D4, ……, Dn is the PWM setting command of each chip.

Reset indicates reset signal, active low.

4. Data Format of C3

R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0

C3 command contains 8×3bit data bits, high bit first, R7, G7 and B7 are fixed to 0.

R[6:0]: Used to set the constant current value of R output. All 0 code is 2mA, all 1 code is 25mA, 128 levels adjustable.

G[6:0]: Used to set the constant current value of G output. All 0 code is 2mA, all 1 code is 25mA, 128 levels adjustable.

B[6:0]: Used to set the constant current value of B output. All 0 code is 2mA, all 1 code is 25mA, 128 levels adjustable.

5. Data Format of Dn

R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0

Each PWM setting command contains 8×3bit data bits, high bit first.

R[7:0]: Used to set PWM duty ratio of R output. All 0 code is off, all 1 code is maximum duty cycle, 256 levels adjustable.

G[7:0]: Used to set PWM duty ratio of G output. All 0 code is off, all 1 code is maximum duty cycle, 256 levels adjustable.

B[7:0]: Used to set PWM duty ratio of B output. All 0 code is off, all 1 code is maximum duty cycle, 256 levels adjustable.

6. Data Receiving and Forwarding

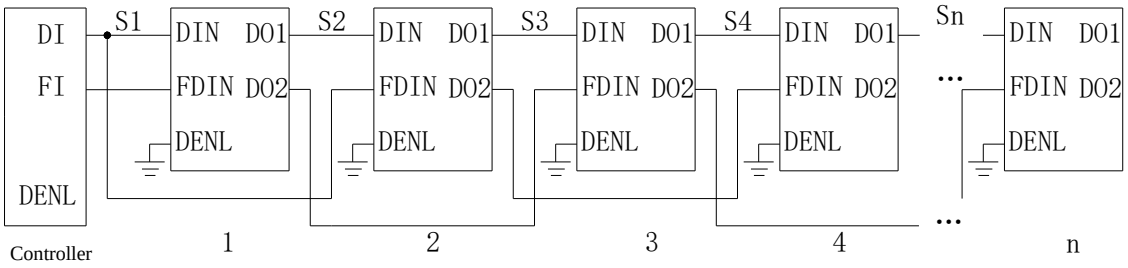


Figure 5

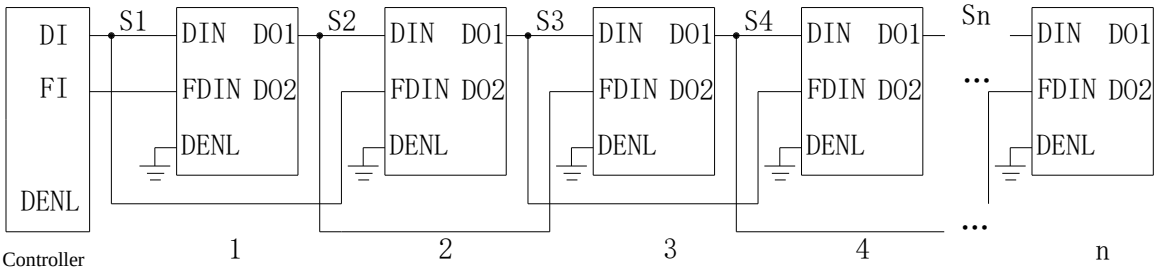


Figure 6

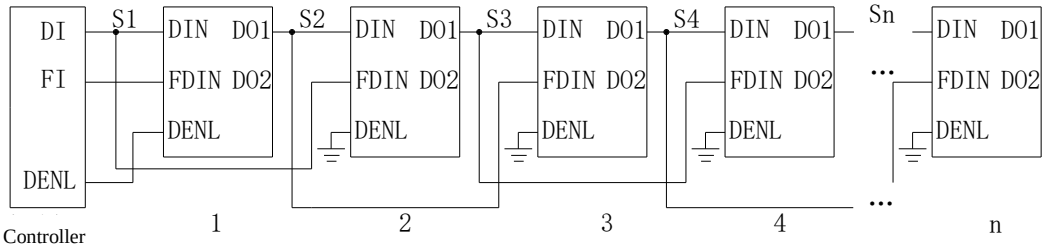


Figure 7

Of which, S1 is the data sent by the Di Port of the controller, S2, S3, S4 and Sn are the data forwarded by the cascade TM1908.

Data structure of controller Di and Fi2 port: C1C2C3D1D2D3D4……Dn;

Data structure of controller Fi port: C1C2C3DxD1D2D3……Dn.

Where, Dx is any 24bit data bit.

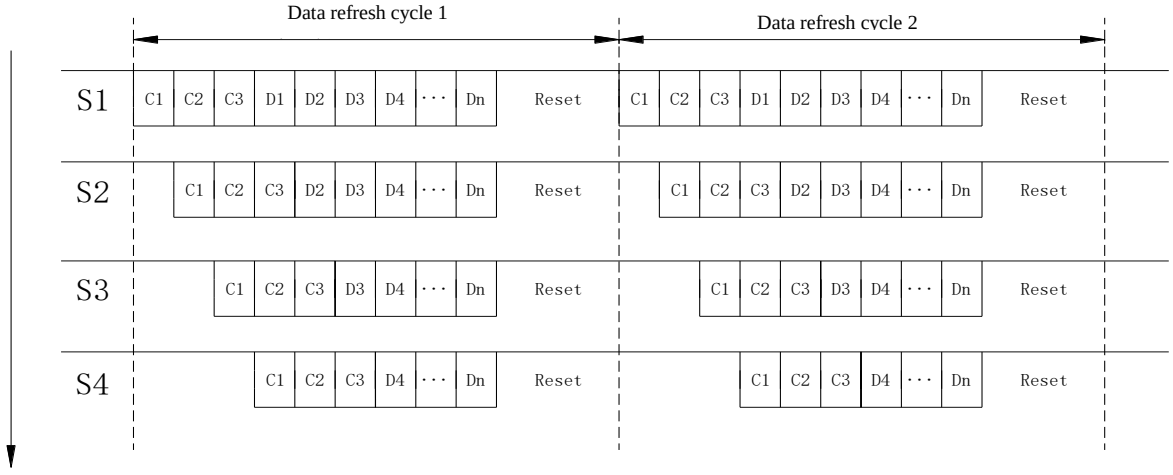


Figure 8

The process of chip cascade and data transmission and forwarding is as follows: the controller sends data S1, and chip 1 receives C1, C2 and C3 for verification. If the command is correct, then it forwards C1, C2 and C3, and absorbs D1 at the same time. If there is no reset signal at this time, chip 1 will constantly forward the data sent by the controller sequentially; the chip 2 also receives C1, C2 and C3 for verification. If the command is correct, it forwards C1, C2 and C3 and absorbs D2 at the same time. If there is no reset signal at this time, chip 2 will constantly forward the data sent by the controller sequentially. And so on, until the controller sends reset signal and completes a data refresh cycle, the chip returns to the receiving ready state. Reset low active, keep low for more than 80 μ s, reset chip.

Application Information

1. Two-wire cascade typical application circuit

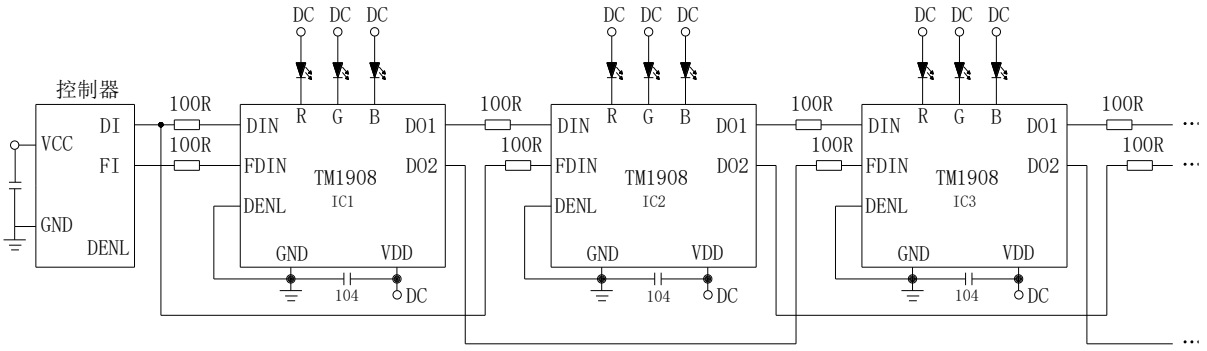


Figure 9

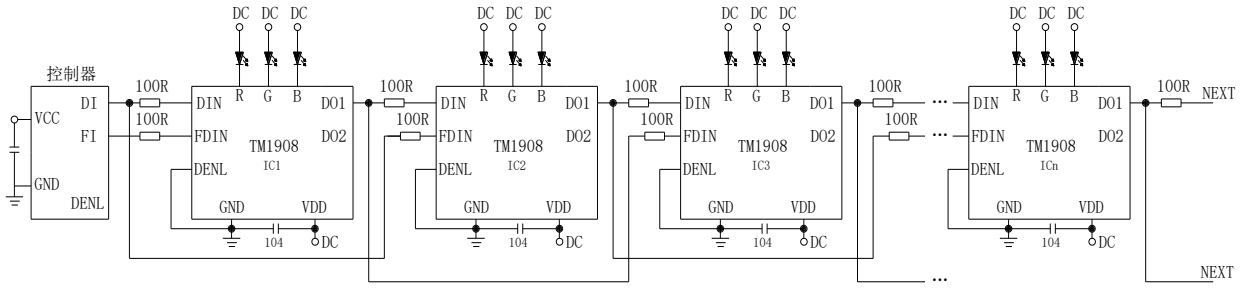


Figure 10

In order to prevent the signal input and output pins of the chip from being damaged due to the instantaneous high voltage generated by the hot plug during the test, 100Ω protective resistance should be connected in series at the signal input and output pins. In addition, the 104 decoupling capacitors of each chip in the figure is indispensable, and the VDD and GND pins connected to the chip should be as short as possible to achieve the best decoupling effect and stabilize the chip operation.

2. Application Circuit Diagram of Communication Control Through DENL Port

Through the DENL port and the DIN port, the matrix wiring is formed to greatly reduce the wiring channels and realize time-sharing control of multiple light strips. The DENL of the first chip of each light strip is controlled by MCU, and the DENL of the subsequent chip is connected to GND. The wiring of each light strip is shown in Figure 7. The application circuit diagram of multiple light strips is as follows:

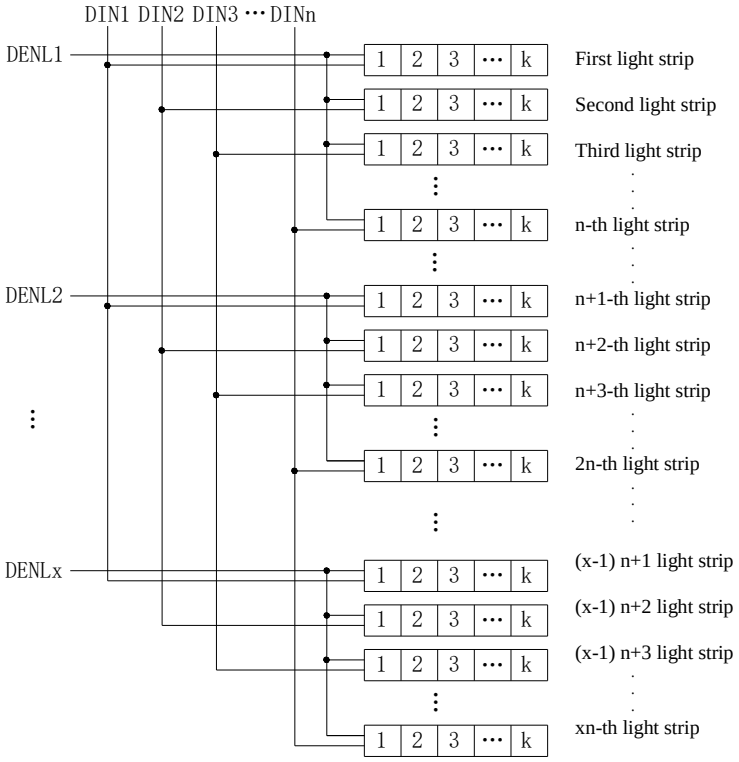


Figure 11

Detailed description of circuit diagram:

The coefficient x represents the number of light strip groups, the coefficient n represents the number of light strips in each group, and the coefficient k represents the number of chips in each light strip.

For example, if x=5, n=10, k=15, it means that there are 5 groups of light strip, 10 light strips in each group, and 15 chips in each light strip.

The control process is as follows:

1. Pull down DEN1L, delay t1, DIN1-DINn data lines of the controller write data to the 1st - nth light strip controlled by DENL1 respectively. After the write data is completed, delay t2.
2. Pull down DENL2, delay t1, DIN1-DINn data lines of the controller write data to the 1st - nth light strip controlled by DENL2 respectively. After the write data is completed, delay t2.
3. Pull down DENL3, delay t1, DIN1-DINn data lines of the controller write data to the 1st - nth light strip controlled by DENL3 respectively. After the write data is completed, delay t2.

……

After writing data to all the light strips by pulling down DENL in turn, send reset code to update data output, delay t3. Pull all DENL up, wait for t4 and enter the next cycle,

Note: After each DENL is enabled, DIN1-DINn will send data. Even if a light strip does not need to update data, it must send the same data as it currently holds.

The sequence diagram of writing data is as follows:

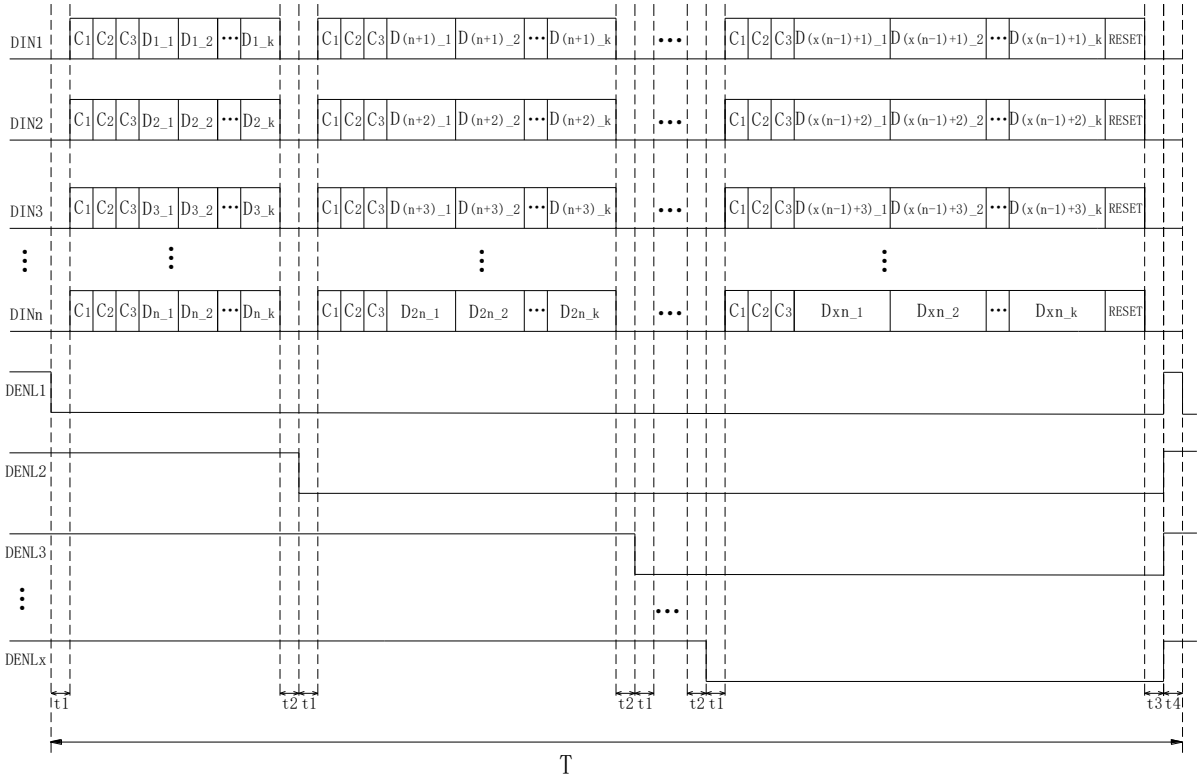


Figure 12

Detailed description of sequence diagram:

Data format: The label on the right of data D indicates sequence number of the chip of the sequence number of the light strip.

For example:

D1_1, D1_2, D1_3 - D1_k represent the data of the 1st, 2nd, 3rd - k chip of the 1st light strip.

D2_1, D2_2, D2_3 - D2_k represent the data of the1st, 2nd, 3rd - k chip of the 2st light strip.

Dn_1, Dn_2, Dn_3 - Dn_k represent the data of the 1st, 2nd, 3rd - k chip of the nth light strip.

Dxn_1, Dxn_2, Dxn_3 - Dxn_k represent the data of the 1st, 2nd, 3rd - k chip of the nx-th light strip. If x=10, n=10, then it represents the 100th light strip.

Remarks:

t1>4us, t2>0us, t1+t2<20us, t3>0us, t4>4us。

3. How to calculate the data refresh rate

The data refresh time is calculated according to the number of cascaded pixels in a system. A group of RGB is usually a pixel (or a segment), and a TM1908 chip can control a group of RGB.

Calculated according to the normal mode:

The period of 1bit data is 830ns (frequency 1.2MHz). One pixel data includes R (8bit), G (8bit) and B (8bit), namely a total of 24bit. The transmission time is 830ns×24≈20μs. If there are a total of 1000 pixels in a system, the time for refreshing all the displays is 20μs×1000=20ms (ignoring C1, C2 and reset signal time), that is, the refresh rate of one second is: 1÷20ms=50Hz.

The following table shows the maximum data refresh rate corresponding to the number of cascade points:

	Normal Mode	
Pixels	**Fastest Data Refresh Time for Once (ms)**	**Maximum data refresh rate (Hz)**
1～500	10	100
1～1000	20	50
1～2000	40	25

Constant Current Curve

When TM1908 is applied to the design of LED products, the current difference between channels and even chips is very small. When the voltage of load terminal changes, the stability of the output current is not affected. The constant current curve is shown as follows:

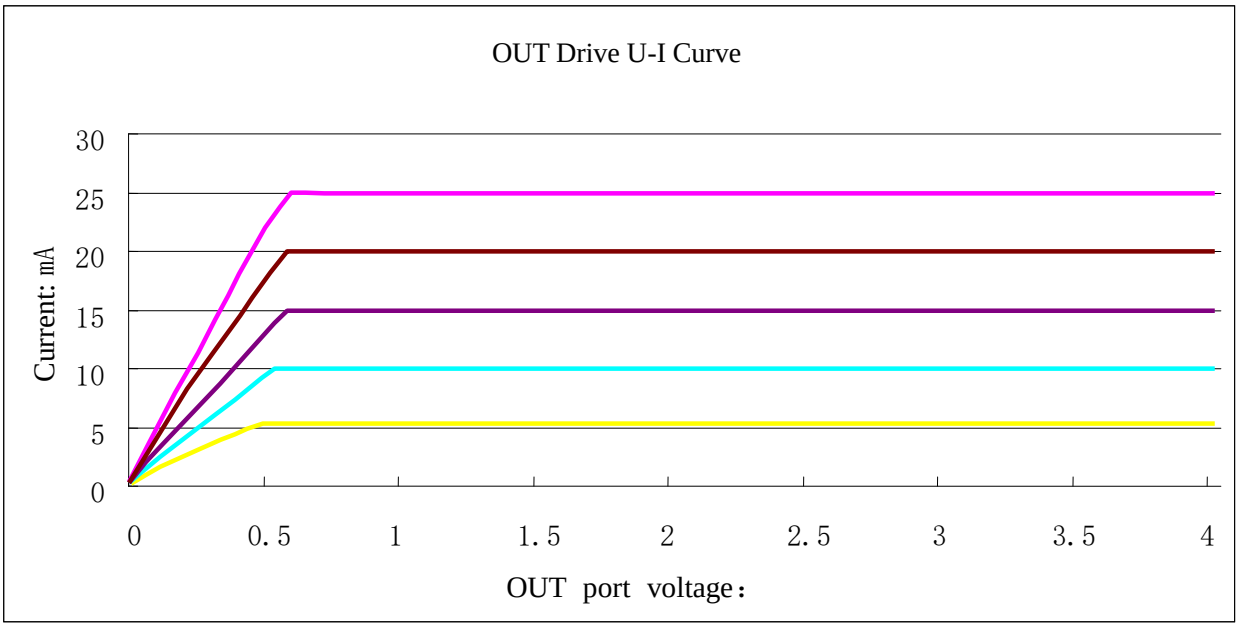
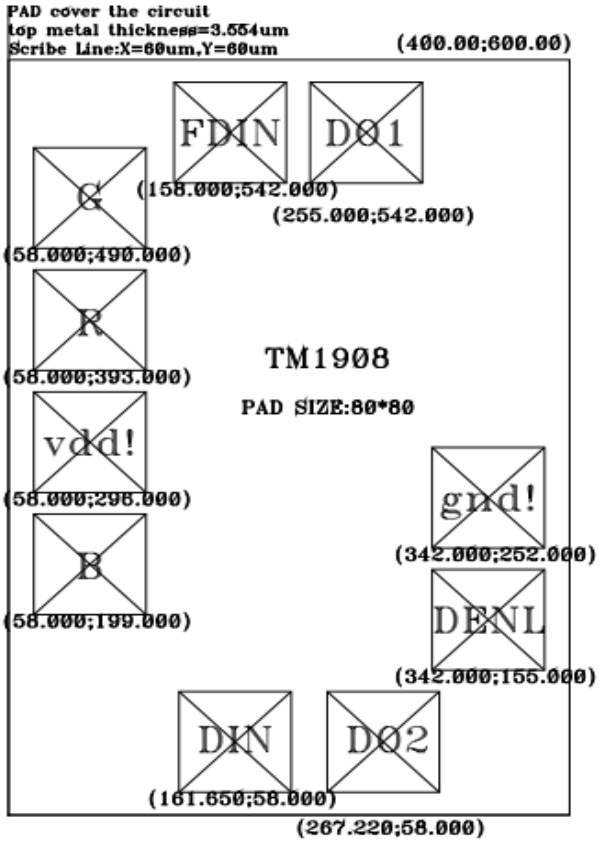


Figure 9

Internal Pin Assignment of Chip



1. Chip size: 400um * 600um
2. The thickness of top aluminum of PAD is 3.554um.
3. Note that the substrate of the chip must be suspended or connected to GND.

PAD Coordinates

S./N.	Pin Name	X(um)	Y（um）	PAD Type	PAD Size
1	G	58	490	Binding PAD	80*80
2	R	58	393	Binding PAD	80*80
3	vdd!	58	296	Binding PAD	80*80
4	B	58	199	Binding PAD	80*80
5	DIN	161.65	58	Binding PAD	80*80
6	DO2	267.22	58	Binding PAD	80*80
7	DENL	342	155	Binding PAD	80*80
8	gnd!	342	252	Binding PAD	80*80
9	DO1	255	542	Binding PAD	80*80
10	FDIN	158	542	Binding PAD	80*80

All specs and applications shown above subject to change without prior notice.