Y.LIN ELECTRONICS CO.,LTD.

Data Sheet

Customer: C3

Part No: YL5050/1R2G3B/XXX/P2/D25I-C

Sample No: YL191216-089

Description: 5050Red/Green/Bule + IC SMD

Item No:

Customer			
Check	Inspection	Approval	Date

Y.LIN			
Drawn	Check	Approval	Date
			2021/5/12

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Y.LIN ELECTRONICS CO.,LTD.

YL5050/1R2G3B/XXX/P2/D25I-C

Characteristic description:

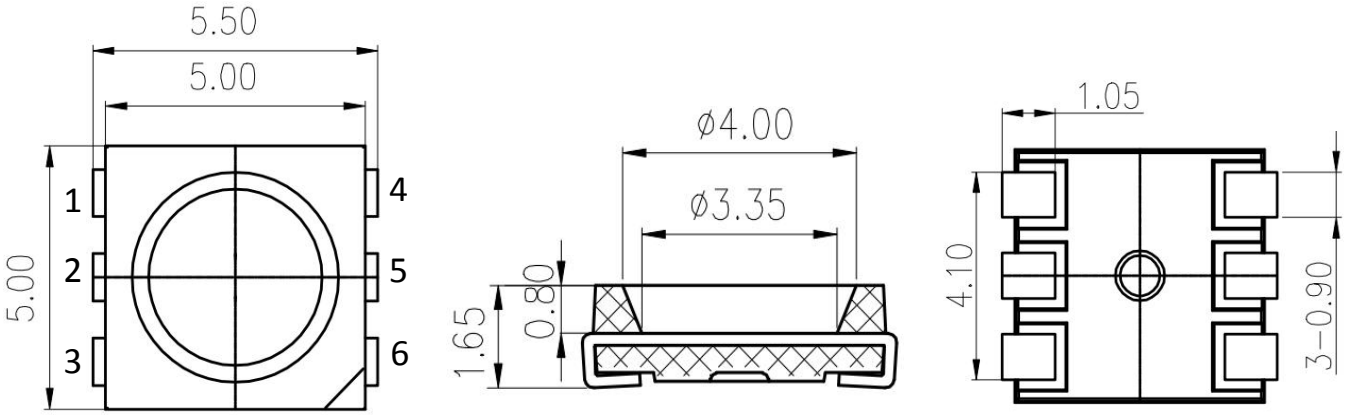
This 5050RGB is a dedicated circuit IC with a single-line three-channel LED constant current driver. It is packaged in a wick, and integrated with MCU single-line digital interface, data latch, LED constant current drive, PWM brightness control, gamma correction and other circuits. Can be cascaded through dual-channel input and output digital interfaces, and the external controller can control the chip with a single wire. Spare communication port, realizes that a chip in the cascade is damaged without affecting the normal use of the subsequent stage. The constant current value and PWM brightness value output by each OUT drive port can be set individually through commands. This product has excellent performance and reliable quality.

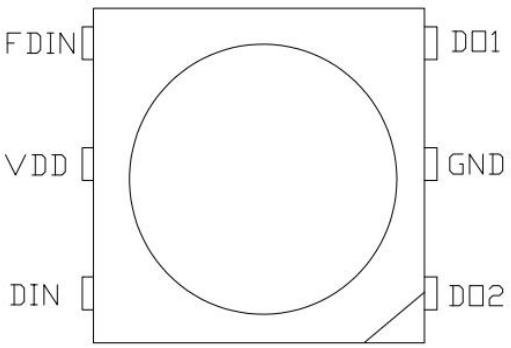
Features:

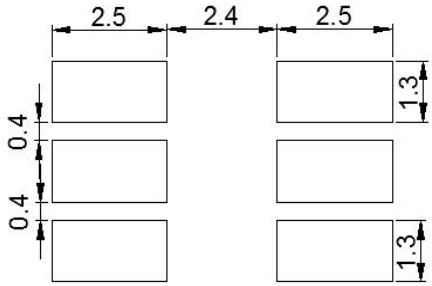
1. Working voltage 4.0 ～ 5.5V
2. Each channel can be independently set current, constant current drive output 2mA ～ 25mA, 128 levels adjustable
3. 256 levels of brightness can be set through the program, with 65536 levels of gamma correction.
4. Accurate current output value
   (Channel and channel) maximum error: ± 3%
   (Chip and chip) maximum error: ± 5%
5. Single-line dual-channel serial cascade interface: The chip data interface can be configured with DIN or FDIN pin input through commands. The input interfaces switch between each other in normal mode. Data is input by DIN pin in DIN mode, and data is input by FDIN pin in FDIN mode. D01 and D02 pins forward the cascaded data, and the signal does not affect the normal operation of other chips due to the abnormality of one chip, ensuring reliability
6. Introduce DENL port, which can ensure the normal communication of data, while greatly reducing the number of wiring and reducing the cost of engineering installation.
7. Oscillation mode: Built-in oscillation and clock synchronization according to the data line signal. After receiving the data of this unit, it can automatically regenerate subsequent data and send it to the lower level through the data output terminal. The signal does not appear distorted or attenuated as the cascade changes
8. Built-in power-on reset circuit, all registers are initialized to zero after power-on reset
9. Data transmission rate: 1.2MHz
10. Application areas: point light source, guardrail tube, flexible light strip, indoor and outdoor large screen, etc.
11. Package: wick integrated package

YL5050/1R2G3B/XXX/P2/D25I-C

Dimensional drawing:







PIN function

NO.	Symbol	Function description
1	FDIN	Alternate data input
2	VDD	Positive power supply
3	DIN	Signal input
4	DO1	Data cascading forwarding output 1
5	GND	Power ground
6	DO2	Data cascading forwarding output 2

Notes:

1.All dimension units are millimeters

2.All dimension tolerance is ±0.2mm unless otherwise noted

Electrical parameter ：

Absolute Maximum Ratings (Ta=25℃,VSS=0V) ：

Symbol	Parameter	Range	Unit
VDD	Logic supply voltage	-0.4-+7.0	V
Vin	DIN, FDIN port voltage	-0.4-VDD+0.5	V
Vout	OUT port voltage	-0.4-+5.5	V
Topr	Working temperature	-40-+85	℃
Tstg	Storage temperature	-50-+150	℃
VESD	ESD pressure	4000	V

Recommended working conditions(Test at -40 ~ +85℃, unless otherwise specified)

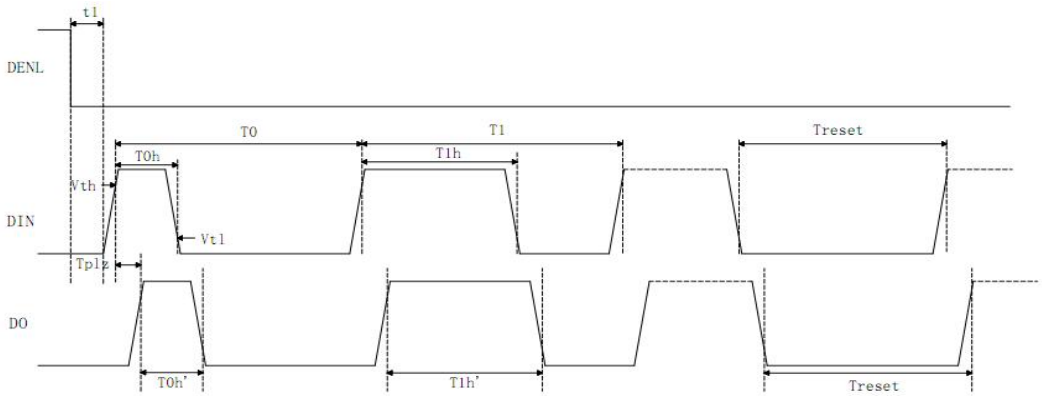
Symbol	Parameter	Range	Min	Typ	Max	Unit
VDD	voltage		4	5	5.5	V
Vin	DIN, FDIN port voltage	VDD=5V, DIN, FDIN series 1kΩ resistor			VDD+0.4	V
Vdo	D01, DO2 port voltage	VDD=5V, D01、D02 series 1kΩ resistor			VDD+0.4	V
Vout	OUT port voltage	OUT=OFF			5	V

Electrical specification (VDD=5V , Ta=25℃)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Voh	High level output voltage	Ioh=6mA	VDD-0.5	-	-	V
Vol	Low level output voltage	Iol=10mA	-	-	0.3	V
Vih	High level input voltage	VDD=5.0V	3.5	-	VDD	V
Vil	Low level input voltage	VDD=5.0V	0	-	1	V
Ioh	High level output current	VDD=5.0V,Vdo=4.9V	-	1.4	-	mA
Iol	Low level output current	VDD=5.0V,Vdo=0.4V	-	12	-	mA
Iin	Input Current	DIN, FDIN connected to VDD	-	500	-	μA
IDD	Quiescent Current	VDD=4.0V, GND=OV, other ports are left floating	-	0.8	-	mA
Iout	OUT output current	R,G,B=ON,Vout=3.0V	2	-	25	mA
Iolkg	OUT output leakage current	R,G,B=OFF,Vout=5.0V		-	0.3	μA
ΔIolc0	Constant current error between channels	R,G,B=ON,Vout=3.0V		-	±3	%
ΔIolc1	Constant current error between chips	R,G,B=ON,Vout=3.0V	-	-	±5	%

Dynamic parameter (VDD=5V , Ta=25℃)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Fin	Data rate			1.2		MHz
Fout	OUT PWM output	R,G,B		2		KHz
Tpz1	Transmission delay time	DIN→D01、D02 FDIN→D01、D02		150		ns
Ci	Input capacitance				15	pF



Name	Describe	Min	Typ	Max	Allowable error	Unit
T0h	Enter 0 code, high time	200	240	280	VDD=5.0V GND=0V	ns
T1h	Input 1 code, high time	400	480	560		ns
T0h'	Output 0 code, high time	200	240	280		ns
T1h'	Output 1 code, high time	400	480	560		ns
T0/T1	0 code or 1 code cycle		830			ns
Treset	Reset code, low time	80	-	-		μs

(1) 0 code or 1 code period in the range of 830ns (frequency 1.2MHz) to 2.5us (frequency 400KHz), the chip can work normally, but 0 code and 1 code high time must meet the corresponding value range in the above table ;

(2) When no reset is required, the low time between bytes should not exceed 25us, otherwise the chip may be reset, and the data will be re-received after reset, and the data cannot be transmitted correctly.

Function description

Mode setting

This chip is a single - line and double - channel communication, using zero - code way to send signals.

Before receiving and displaying data, the chip needs to configure the correct working mode and select the way of receiving and displaying data. The first 24bit is the command code, and the last 24bit is the check code. The chip reset begins to accept data. There are four commands for mode setting:

(1) 0XFFFFFF_000000 command: the chip is configured to work normally.

For the first time in this mode, the default DIN receive display data, chip to detect the port has signal input, has maintained the port to receive, if more than 160 ms did not receive the data, then switch to FDIN receives the data, the chip to detect the port has signal input, has maintained the port to receive, if received more than 160 ms are not data, are now switch to the DIN receive display data. DIN and FDIN rotate in turn to receive display data.

(2) 0XFFFFFA_000005 command:

the chip is configured to DIN working mode, in this mode, the chip only receives display data input by DIN side, FDIN side data is invalid.

(3) 0XFFFFF5_00000A command:

The chip is configured to work in FDIN mode. In this mode, the chip only receives display data input from the FDIN side, and the DIN side data is invalid.

(4) 0XFFFFF0_00000F command:

The chip is configured for test mode

Display the data

After the chip is powered on and reset and receives the mode setting command, it begins to receive the constant current value setting command, and then receives the display data. After receiving the 24bit, DO1 and DO2 ports start to forward the data from DIN or FDIN terminal to provide display data for the next cascade chip. Ports DO1 and DO2 remain low until data is forwarded. If DIN or FDIN end Reset

The chip adopts automatic shaping and forwarding technology, so the signal will not be distorted and attenuated. For all chips that are cascaded together, the cycles of data transmission are consistent.

A full frame data structure

C1	C2	C3	D1	D2	D3	D4	…	Dn	Reset	C1	C2	C3	D1	D2	D3	D4	…	Dn	Reset

C1 and C2 mode setting commands, each contains 24 bit data bits, each chip receives and forwarding C1 and C2, which is suitable for normal working mode 0 xffffff_000000 command, 0 xfffffa_000005 command for DIN work mode, 0 xfffff5_00000a work for FDIN mode command, 0 xfffff0_00000f command for the chip test mode, C3 is constant current value set command, every chip receives and forwarding C1, C2 and C3.

D1, D2, D3, D4... Dn is the PWM setting command for each chip.

Reset represents the Reset signal, and the low level is valid.

C3 data format

R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0

The C3 command contains 8×3bit data bits, the high order starts, and R7, G7, and B7 are fixed at 0.

R[6:0]: Used to set R output constant current value. All 0 code is 2mA, all 1 code is 25mA, 128 class adjustable.

G[6:0]: Used to set G output constant current value. All 0 code is 2mA, all 1 code is 25mA, 128 class adjustable.

B[6:0]: Used to set B output constant current value. All 0 code is 2mA, all 1 code is 25mA, 128 class adjustable.

The data format of Dn

R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0

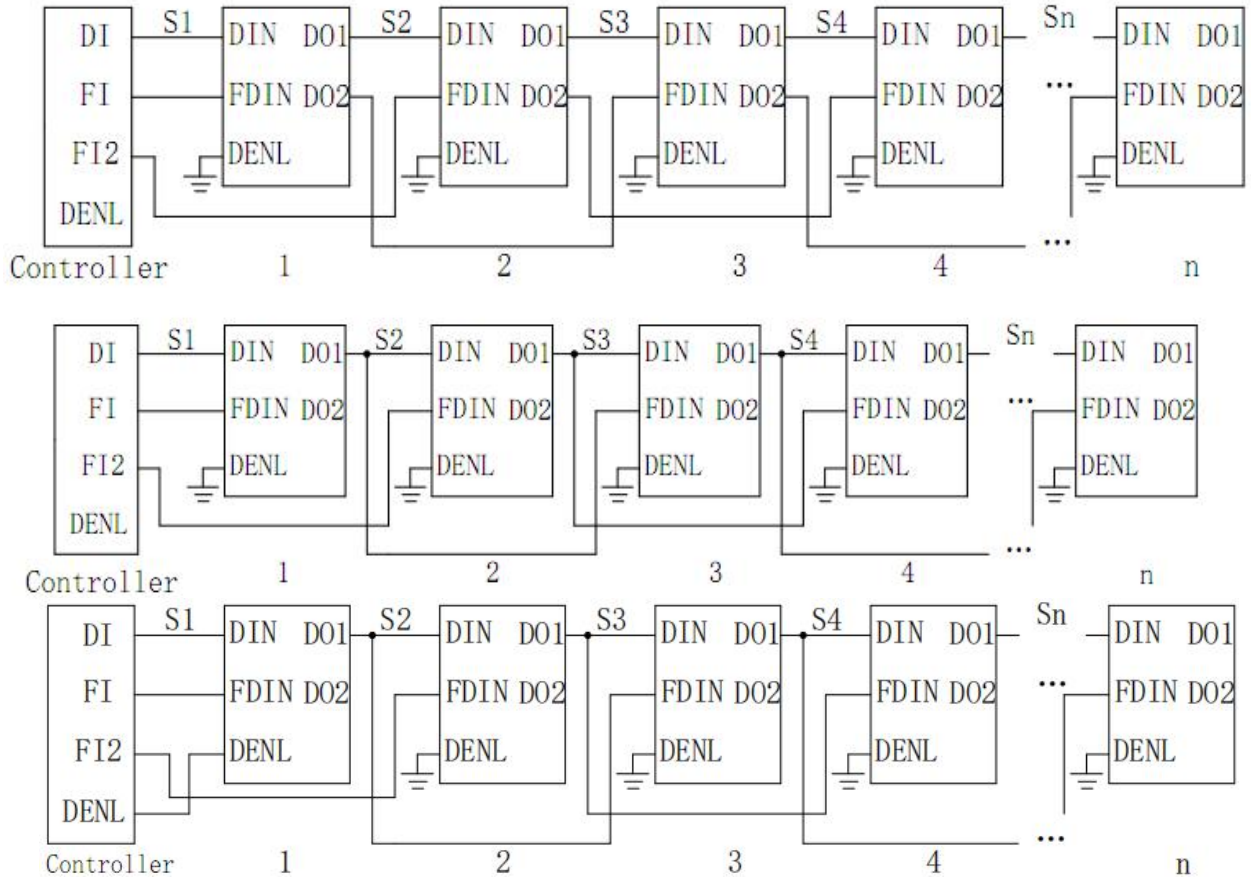
Each PWM setting command contains 8×3 bits of data, with the top starting

R[7:0]: Used to set the PWM duty ratio of R output. All 0 code is off, all 1 code is duty cycle maximum, 256 level adjustable

G[7:0]: Used to set the PWM duty ratio of G output. All 0 code is off, all 1 code is duty cycle maximum, 256 level adjustable

B[7:0]: Used to set the PWM duty ratio of B output. All 0 code is off, all 1 code is duty cycle maximum, 256 level adjustable.

data receiving and forwarding

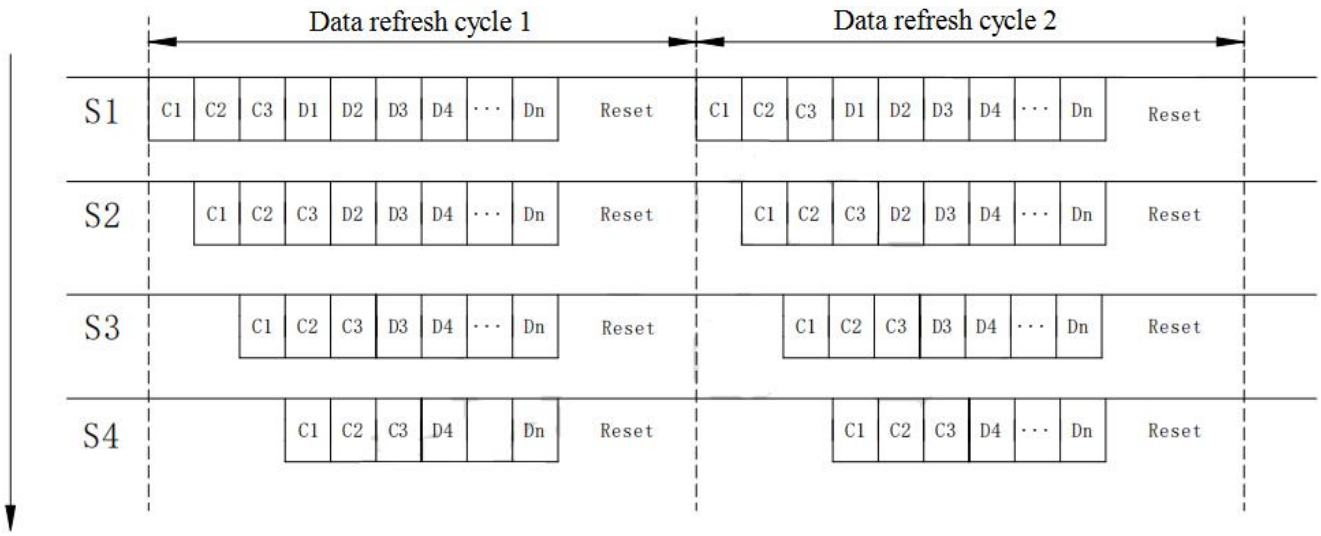


Where S1 is the data sent by controller Di port, S2, S3, S4 and Sn are the data forwarded by cascading TM1908.

Controller Di and Fi2 port data structure: C1C2C3D1D2D3D4... Dn.

Controller Fi port data structure: C1C2C3DxD1D2D3..... Dn.

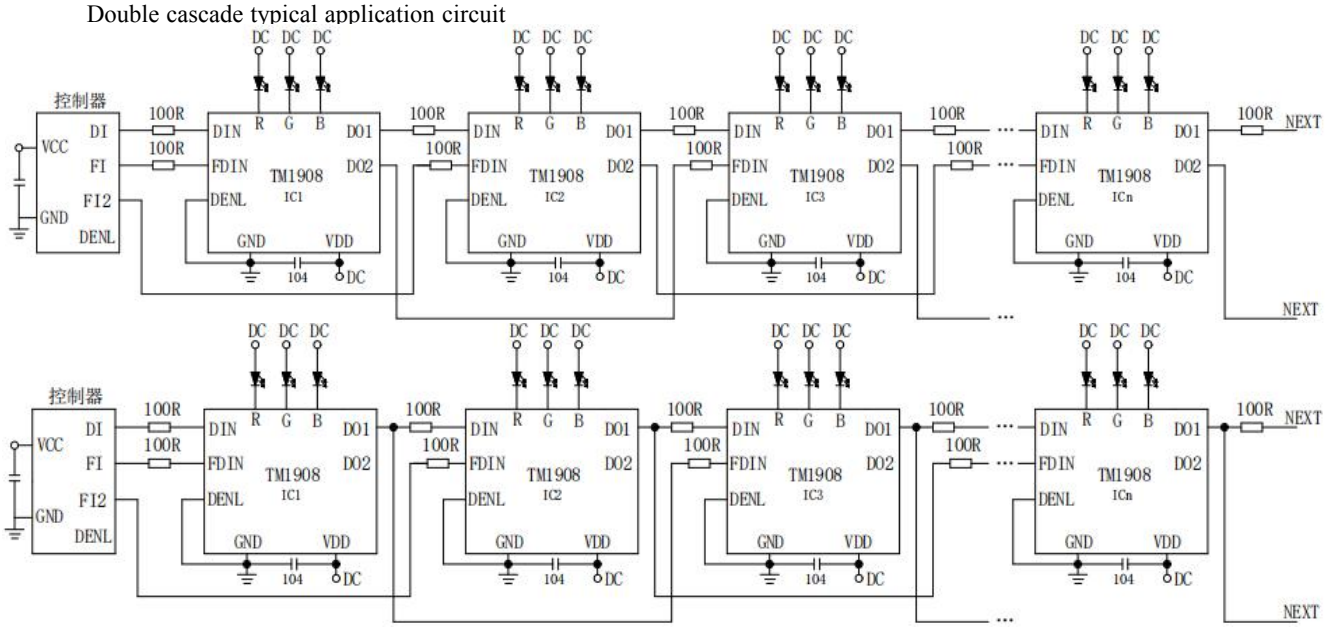
Where, Dx is any 24bit data bit.



The process of chip cascade and data transmission and forwarding is as follows: Controller sends data S1, chip 1 receives C1,C2 and C3 for verification. If the command is correct, it forwards C1,C2 and C3 and absorbs D1. If there is no Reset signal at this time, chip 1 will always forward the data sent by controller. Chip 2 also receives C1, C2 and C3 for verification. If the command is correct, it forwards C1, C2 and C3 and absorbs D2. If there is no Reset signal at this time, chip 2 will always forward the data sent by chip 1. And so on, until the controller sends a Reset signal, completes a data refresh cycle, and the chip is ready to receive again. Effective when Reset to low level. Maintain low level for longer than 80 s. Chip Reset.

Application information

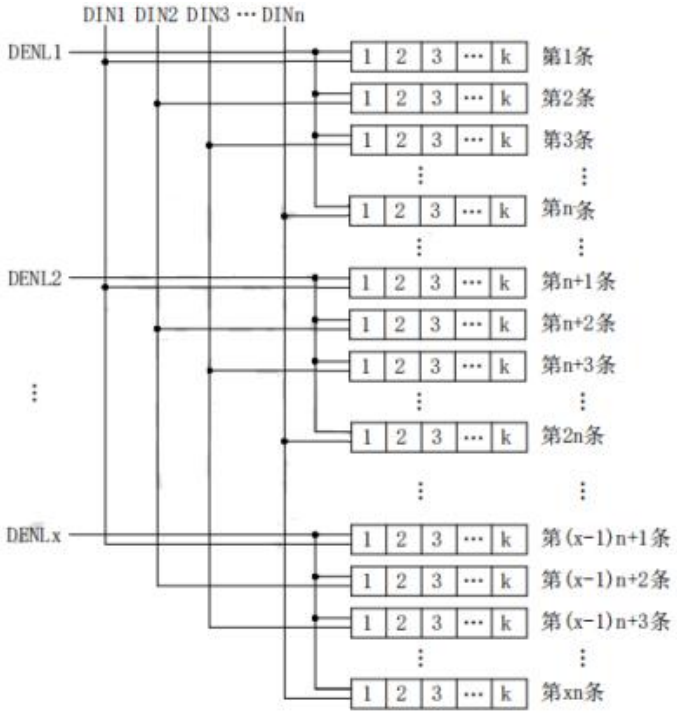
Double cascade typical application circuit



To prevent products charged plug during testing of instantaneous high pressure in chip signal input and output pins damaged, should be in the concatenated signal input and output foot 100 Ω protection resistance. In addition, the 104 decoupling capacitors of each chip in the figure are indispensable, and the VDD and GND pins that lead to the chip should be as short as possible to achieve the best decoupling effect and stabilize the chip operation.

Application circuit diagrams that control communications through DENL ports

Through DENL port and DIN port, matrix wiring can be formed to significantly reduce wiring channels, and time-sharing control of multiple lamp belts can be realized. The DENL of the first chip of each lamp belt is controlled by MCU, and the DENL of the later chip is connected to GND. Wiring of each lamp belt is shown in Figure 7.



Circuit diagram details:

Coefficient X represents the number of lamp bands, coefficient N represents the number of roots in each group, and coefficient K represents the number of chips per root.

For example, if x=5, n=10, k=15, it means there are 5 groups of light bands, each group has 10, each has 15 chips.

Control process is as follows:

1. DEN1L pull down, delay T1, and the DIN1~DINn data line of the controller write data to the first ~ NTH lamp band controlled by DENL1 respectively. Completion of writing, delay t2.

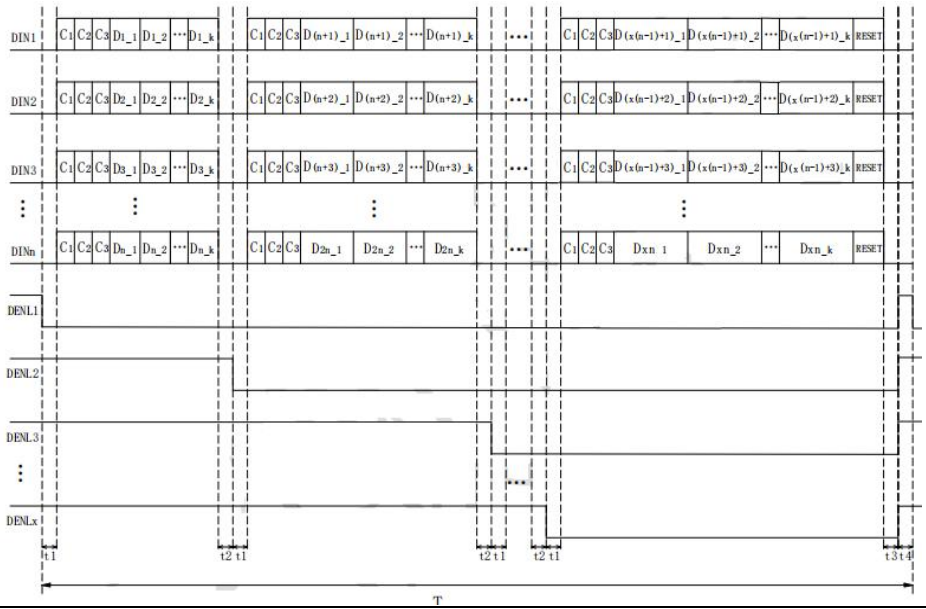
2. DENL2 pull down, delay T1. The DIN1~DINn data line of the controller writes data to the first ~ NTH lamp band controlled by DENL2 respectively. Completion of writing, delay t2.

3. DENL3 pull down, delay T1, DIN1~DINn data line of controller write data to the first ~ NTH lamp strip controlled by DENL3 respectively. Completion of writing, delay t2.

By successively pulling down DENL, after all lamp tape write data is completed, reset code is sent to update data output, and delay T3. Pull up all DENL and wait for the next cycle after T4.

Note: After each DENL is pulled down to enable, DIN1~DINn data is sent. Even if an equal lamp strip does not need to update data, it must send the same data as the currently held data.

The sequence diagram of write data is as follows:



Selection Guide

Part No.	Chip Materials	Lens Type	Luminous intensity(mcd) @ 5mA			Viewing Angle
			Min	Typ	Max	2θ1/2
YL5050/1R2G3B/XXX/P2/D25I-C	Red (AlGaInP)	Water Clear	150	- -	350	120
	Green (InGaN)		450	- -	900	
	Blue (InGaN)		70	- -	250	

Note:

1.1/2 is the angle from optical centerline where the luminous intensity is 1/2 the optical centerline value.

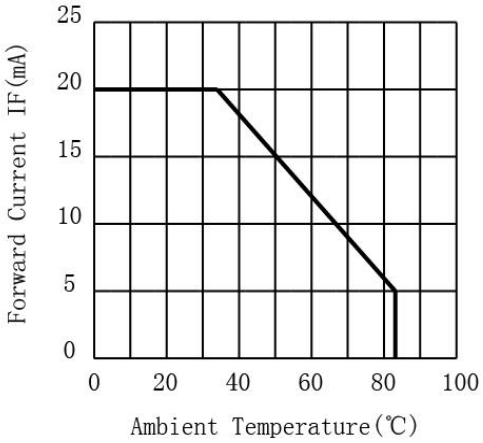
2.the above luminous intensity measurement allowance tolerance ±10%

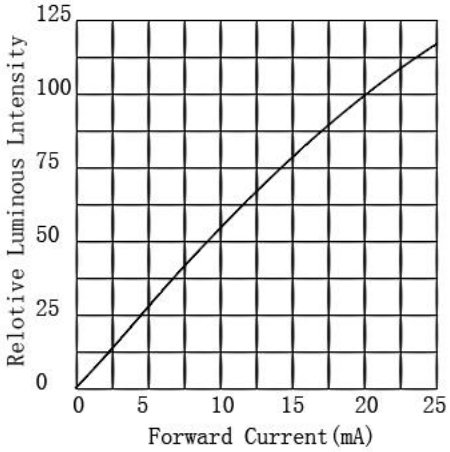
Electrical / Optical Characteristics at Ta=25°C

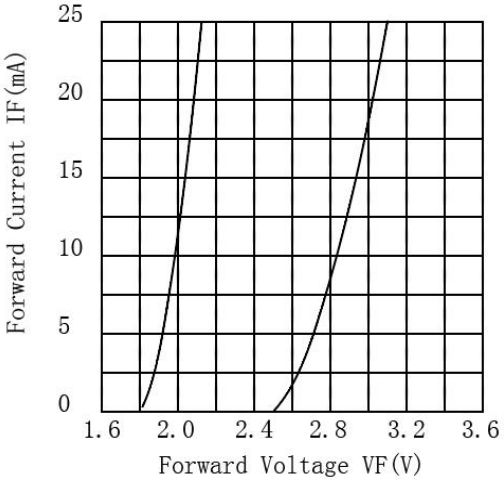
Parameter	Symbol	Min.	Typ.	Max.	Units	test conditions
Forward Voltage	R	1.7	- -	2.1	V	IF=5mA
	G	2.5	- -	2.9		
	B	2.6	- -	3.2		
Reverse Current	IR	- -	- -	10	uA	VR = 5V
Dominate Wavelength	R	615	- -	630	nm	IF=5mA
	G	520	- -	535		
	B	460	- -	475		

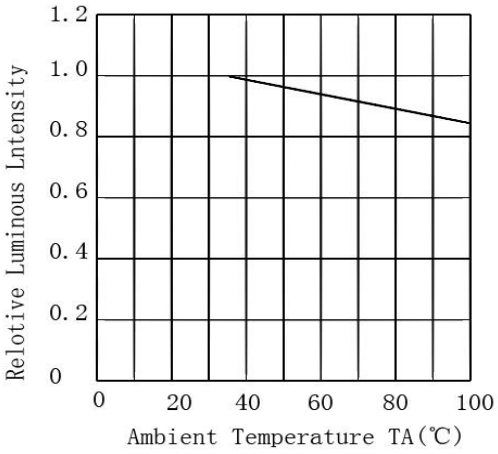
Typical optical characteristics curves

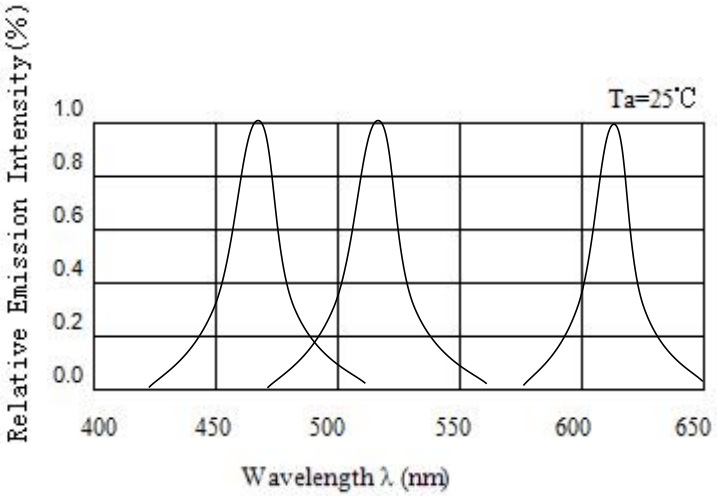
Ambient Temperature VS. Forward Current

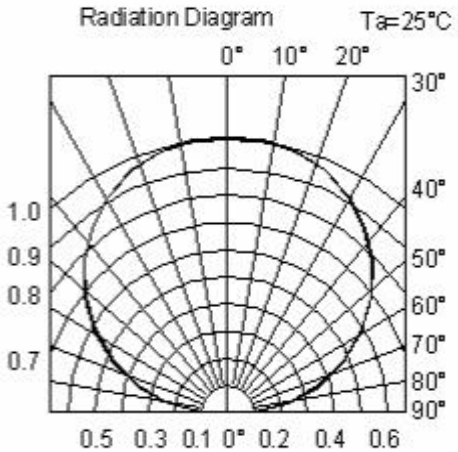












Reliability Test Items And Conditions

Test Items	Ref.Standard	Test conditions	Time	Quantity	Ac/Re
Reflow Soldering	JESD22-B106	Temp.:260℃±5℃ Min.5sec.	3 times.	22Pcs.	0/1
Temperature Cycle	JESD22-A104	100℃±5℃ 30 min. ↑↓5 min -40℃±5℃ 30 min.	100 Cycles	22Pcs.	0/1
High Temperature Storage	JESD22-A103	Temp:100℃±5℃	1000Hrs	22Pcs.	0/1
Low Temperature Storage	JESD22-A119	Temp:-40℃±5℃	1000Hrs	22Pcs.	0/1
Life Test	JESD22-A108	Ta=25℃±5℃ IF=5mA	1000Hrs	22Pcs.	0/1
High temperature and high humidity storage experiment	JESD22-A101	85℃±5℃/ 85%RH	1000Hrs	22Pcs.	0/1

Criteria For Judging Damage

Test Items	Symbol	Test conditions	Criteria For Judgement	
			Min.	Max.
Forward Voltage	VF	IF=5mA		U.S.L*)x1.1
Reverse Current	IR	VR = 5V		U.S.L*)x2.0
Luminous intensity	IV	IF=5mA	L.S.L*)x0.7	

U.S.L: Upper standard level L.S.L: Lower standard level

The technical information shown in the data sheets are limited to the typical characteristics and circuit examples of the referenced products.It does not constitute the warranting of industrial property nor the granting of any license.

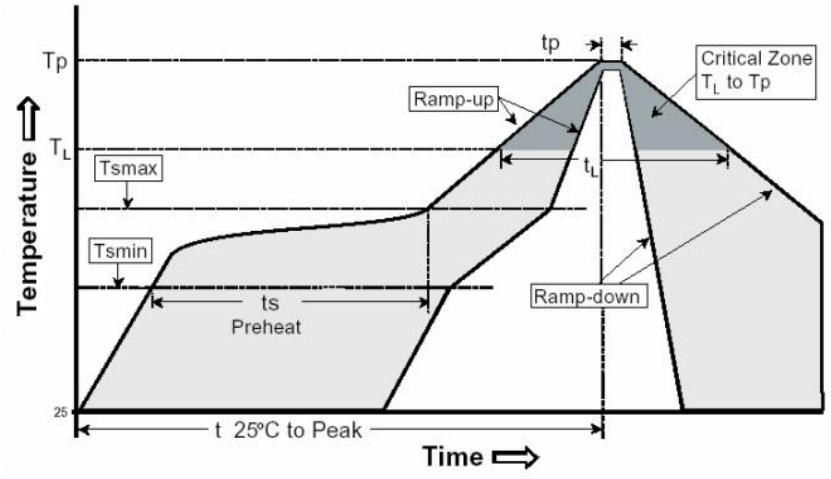
SMT Reflow Soldering Instructions

1. The number of reflow soldering shall not exceed two times,and the time from the second processing to the first completion shall not exceed 24H

2. When soldering , do not put stress on the LEDs during heating .

3.Reflow temperature distribution (Acc.to J-STD-020D)

Profile Feature	Sn-Pb Eutectic Assembly		Pb-Free Assembly	
	Large Body	Small Body	Large Body	Small Body
Average ramp-up rate (TL to Tp)	3℃/second max.		3℃/second max.	
Preheat -Temperature Min(TSmin) -Temperature Max(TSmax) -Time(min to max)(ts)	100℃ 150℃ 60-120 seconds		150℃ 200℃ 60-180 seconds	
Tsmax to TL -Ramp-up Rate			3℃/second max.	
Time maintained above: -Temperature(TL) -Time(tL)	183℃ 60-150 seconds		217℃ 60-150 seconds	
Peak Temperature(Tp)	225+0/-5℃	240+0/-5℃	245+0/-5℃	260+0/-5℃
Time within 5℃ of actual Peak Temperature(tp)	10-30 seconds	10-30 seconds	10-30 seconds	20-40 seconds
Ramp-down Rate	6℃/second max.		6℃/second max.	
Time 25℃ to Peak Temperatur	6 minutes max.		8 minutes max.	



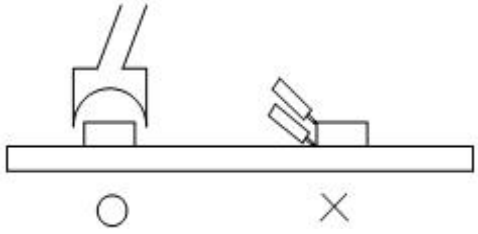
Soldering iron

1.When hand soldering, the temperature of the iron must less than 350℃ for 3 seconds

2.The hand solder should be done only one times

Repairing

Repair should not be done after the LEDs have been soldered. When repairing is unavoidable, a double-head soldering iron should be used(as below figure). It should be confirmed in advance whether the characteristics of LEDs will or will not be damaged by repairing.



Storage

This product uses sealing anti-moisture antistatic packaging, and with desiccant, humidity card.

Before packaging is opened:

1. The storage environment is: the ambient temperature should be maintained between 5 ° C and 30 ° C, and the relative humidity should be kept within 60% RH. (The storage period is 2 months. If more than two months, please return the product to our company to help dehumidify)

2. Please check the package for leaks before opening. If there is a leak, return to the factory for dehumidification.

After opening the package:

1. After opening the package, check whether the humidity card has a discoloration phenomenon. Please remove the material from the bag and use it after dehumidifying 24H at 65 °C.

2. Environmental conditions: The ambient temperature should be kept between ≤ 30 ° C and relative humidity The lower 60 % RH should be maintained.

3. if the material is not produced after exposure in the workshop for more than 24 hours, the product must be put back in the oven, dehumidified with 65 °C 24H, and then can be used again. If the material is not produced after 48 hours of exposure in the workshop, return the material to the SMD plant for high temperature dehumidification.

4. When the material is dehumidified, please do not open the oven in the middle, so that the oven temperature will not drop to the dehumidification effect.

Please refer to the following operating methods when the material needs to be dehumidified

Correct way: material desiccant need to remove the bag, use the way of hanging baked
正确的方法：材料需要去掉袋子，使用挂烤的方式烘烤。

Wrong way: the material is dehumidified without removing the bag, in a stacking manner
错误的做法是：以堆叠方式或材料不取出袋子烘烤。

ESD

Static Electrisity will damage the LED.

The following steps can reduce the likelihood of ESD causing product damage

1. All productive machinery and test instruments must be electrically grounded.

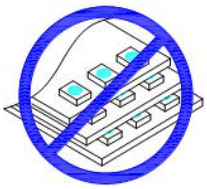
2. Use a condustive wrist band or anti-electostatic glove when handling these LEDs.

3. Manintain a humidity level of 50%RHor higher in production areas.

4. Use anti-static packaging for transport and storage.

Handling Precautions

1. Do not stack the assembled PCB together. This may scratch the surface of the product or damage the circuit.

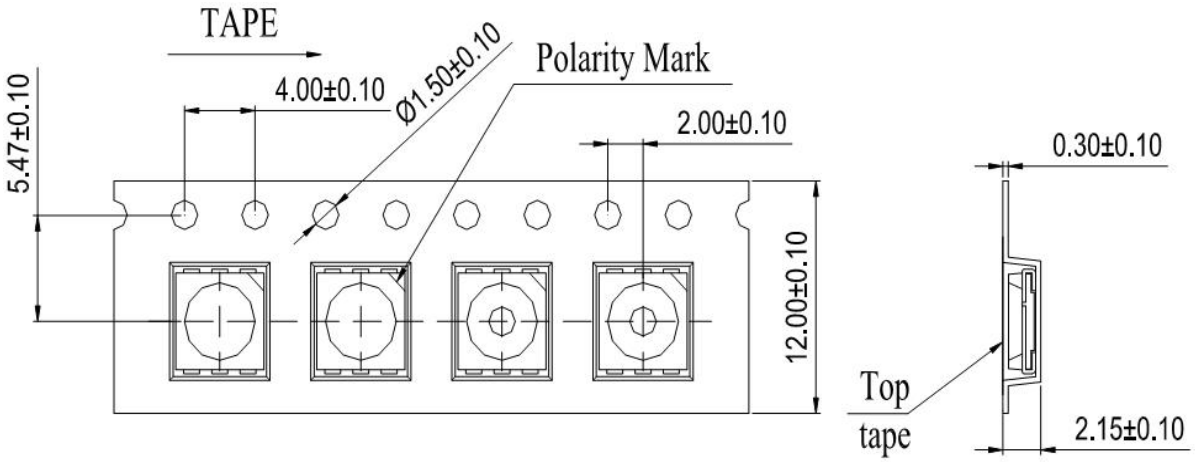


2. Not available in the situation of acidity for PH.

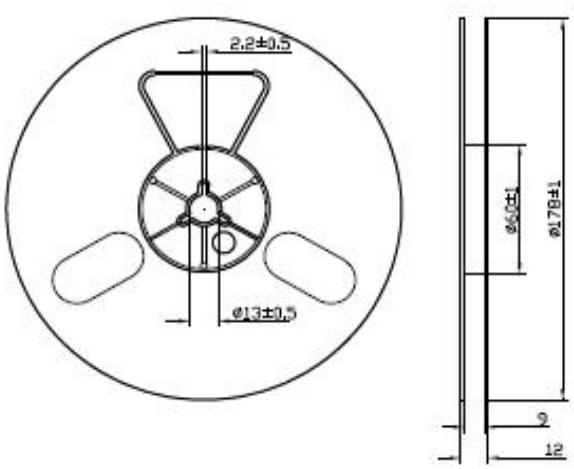
3. Electrostatic sensitive device

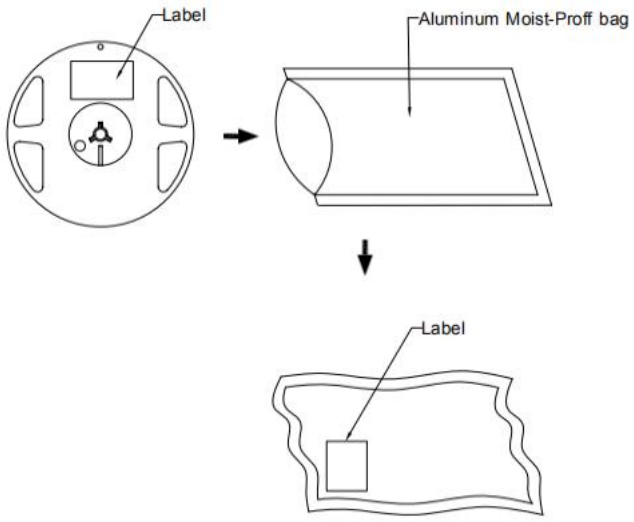
YL5050/1R2G3B/XXX/P2/D25I-C

Package：1000pcs/reel



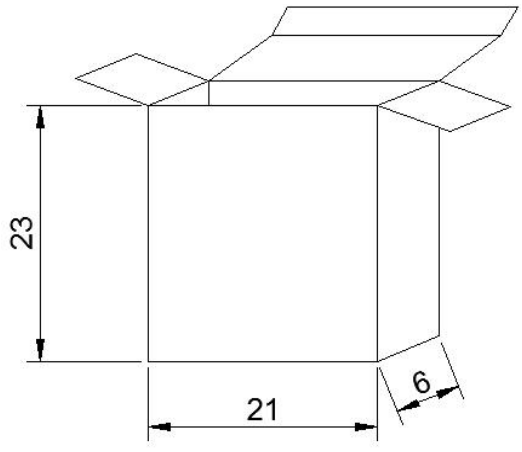
Moisture Resistant Packaging





Cardboard Box

Maximum packing quantity (5 packs of material)



Maximum packing quantity (27 bags of material or 5 small boxes)