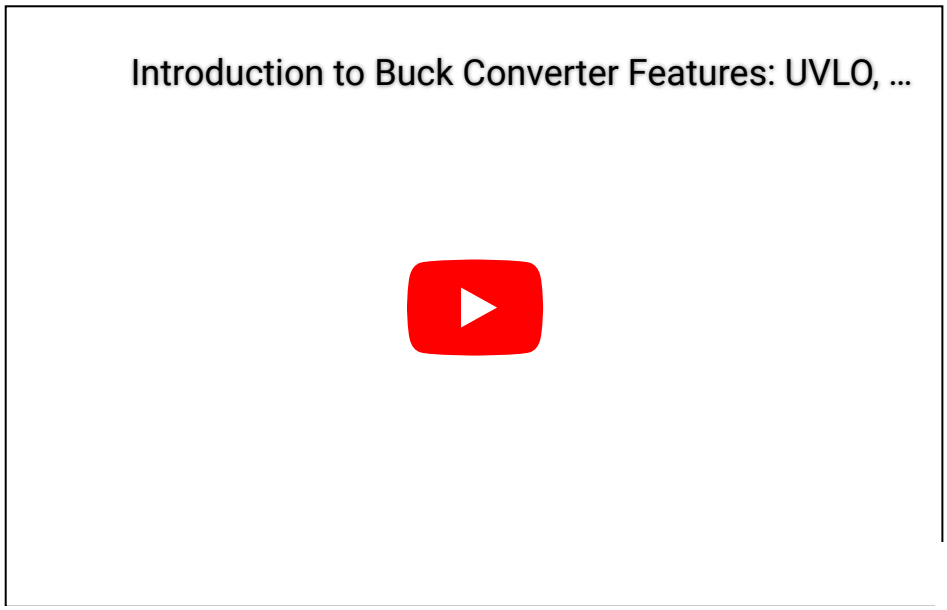
**RIP-Felix**
Senior Member

| | |
|---|---|
| Joined: | Oct 4, 2020 |
| Messages: | 1,837 |
| Likes Received: | 1,924 |
| Trophy Points: | 297 |
| Gender: | Male |

> *When I met @marciolsf whe started do capture some signals. I captured signal of pins:*
>
> *Click to expand...*
>
> - *19 (Gate 3)*

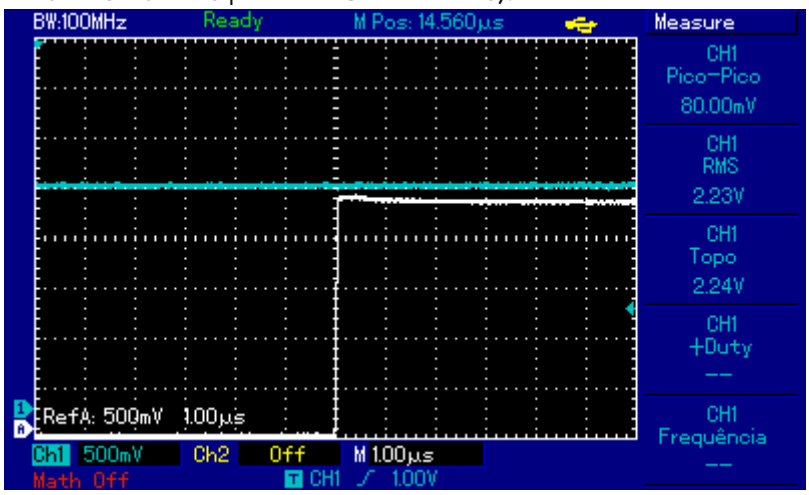
Can I just say, this post completely flew past me when I first read it! After countless hours of watching videos and reading the datasheets of the PWM controller and DC/DC converter this is finally beginning to make sense. The 1002 error was correctly characterized way before I did it, and more completely. Props to you guys!

I think I have an explanation for why SONY has 1002 labeled "RSX VRAM Power Fail." I think they meant to type "RSX VRM Power Fail." I mean, that makes A LOT more sense! VRM is more encompassing than "no drive signal," which is a symptom not the cause. So it would cover a broader spectrum of potential causes. And they have this section on the service manual labeled "VRM for RSX (2Phases)." I'm pretty sure that's just a typo.




**Under Voltage Lockout (UVLO) circuit:**
Consists of the Enable and V input to the controller. Enable is controlled by the SYSCON directly. The controller will refuse to work if it's input voltage is not sufficient. Now these controllers are powered directly off 12v_Main which is supplied by the PSU. There isn't much conditioning before it gets there. So a bad PSU could trigger an UVLO. I suspect this is the cause of some 1001 errors.

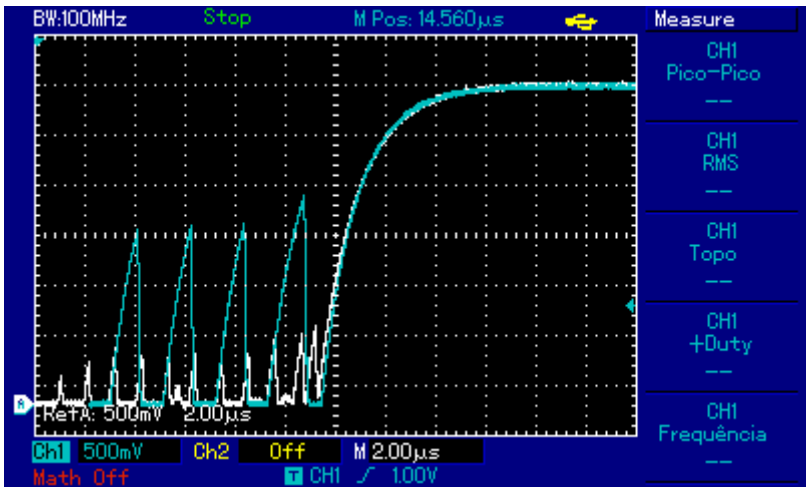
First thing I notice is that the Drive pin is low when it should be high (blue = Bad RSX tokins | WHT = Good Tokins):




The controller's drive signal tells the buck converters to switch on and power the processor. It does so through an AND Gate, but only when both PWRGD and Drive signals are present!

This gives us a new thing to test. If Drive and PWRGD are high on the input side of that AND gate (IC6107/IC6204 for CPU/RSX VRM respectively), then output should be high! Check it has all the correct voltages. Replace if not.

PWRGD is also interesting (Blue = Bad Tokins | WHT = Good Tokins)...




PWRGD (AKA reset) notifies the system when voltage falls out of regulation. It has protection built in that prevents false triggering due to voltage spikes/noise from transient loads. So PWRGD "shouldn't" go low without cause.

From watching this video...

Spoiler: Testing PG Signalon ATX PSU

the Power Control line is enabled. When the SYSCON enables the Power Control Line, enable signals travel across the board to many subsystem controllers, initializing main system voltages, VRM, etc. There is a proper amount of time that needs to elapse before the SYSCON begins to worry. If the time between the Power control line enable signal and Power Good signals coming back to the SYSCON from across the board are too short or long, it get's mad, takes control of the situation, and waits ominously for your to figure out how to resolve the issue.

By way of analogy:


- Jeff Goldbloom = Enable Signal
- Infant = Hardware issue
- The Trailer = A busy Controller trying to resolve the issue...
- Mommy = SYSCON

I think the time delay is needed to account for Softstart (SS = Pin6), which limits inrush currents. It's set using C6208 (0.1uF) according to the equations presented in the Introduction to Buck Converter Features video. Also, it just takes a certain amount of time for a chip to power up and report power good. That's the rise time you see in the power good signal.

Without a proper delay the SYSCON assumes something is wrong, triggers an error code, and shuts off the console. @DeadEnd found that out when he injected 3.3V into PWRGD (power good) of IC6103 (CPU Buck controller). It generated error 20 1001 and 20 3010. So, I think we can now conclude definitively 1001 is related to the CPU VRM, and that 3010 can be interpreted as "PWRGD signal time too short," since it would have been a 0ms delay if powered externally.

Spoiler: Side note

(bigger/wider peaks) in the console with bad tokins. I wonder if that is used to gauge the extent of the ripple. Say it's higher than half the final 3.3v PWRGD signal, maybe that over the threshold for triggering a 1002. Say it's more than 75%, then maybe it's over the threshold for triggering 3004. Of course it could be 25% and 50% respectively, IDK. It's just a hypothesis, but it makes sense there would be some mechanism for generating a standard voltage ripple/noise pulse during the check. I'm wondering if that's what those spikes are before PWRGD goes high.

That's enough to digest for now.

## To be continued...

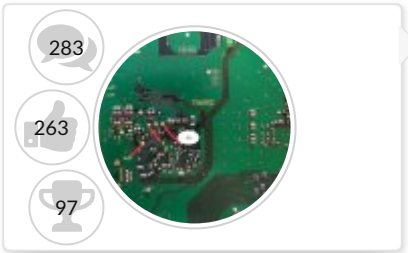
READ THIS - Links to super useful information (Schematics, pinouts, SYSCON and Frankenstein Tutorials, Tantalizer, Statistical Analysis of what really cause the YLOD, etc.)

RIP-Felix, Dec 6, 2021 Report #2020 Like + Quote Reply

sandungas likes this.

< Prev 1 ← 99 100 101 102 103 → 165 Next >

1,272 more messages...




Write your reply...

Post Reply Upload a File More Options...

Tags: ps3 syscon uart E ···