Gaohong Liu

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SUMMARY OF QUALIFICATION

- Proficient in Computer Architecture, Embedded Computing and VLSI System design: Digital IC design, simulate and layout, CPU and GPU architecture, Computation/Algorithm Accelerator Design. Embedded System Software design, development, and test. ASIC and FPGA. Data Structure and Algorithm.
- Programming Language: SystemVerilog, C/C++, Java, Python.
- Computer Engineering background in Computer Architecture. Experience with developing Low Power multicore CPU such as Risc-V and High Performance SoC design such as Deep Convolution Neural Networking Accelerator.
- Physics Research background in Quantum Information. Understand Quantum Algorithm such as Deutsch algorithm, Grover Search algorithm. EM Waves grating coupler design for long range fiber communication.
- Strong design and testing skill with demonstrated experience and background using Software such Quartus, Cadence Virtuoso, Synopsis Compiler and Library, Spice, Matlab, Mathematica and Hardware such as Xilinx FPGA and Arduino Board.
- Effective Project Management, Group Communication, Teaching and Leadership as demonstrated through project, assignment, teaching assistant and other teamwork Experience.

EDUCATION

University of Washington, Seattle, WA Cumulative GPA: 3.62 Expected Graduation Date: June 2019

Bachelor of Science in Electrical and Computer Engineering (ECE)

Bachelor of Science in Physics, Comprehensive Track (PHYS)

Emphasis: Computer Architecture, Digital VLSI Design, Embedded Computing, Quantum Information.

RELEVANT EXPERIENCE

Research Assistant, Bespoke Silicon Group, University of Washington, Seattle WA March 2018 – present

- Beginning with RISC-V ISA, fully understood Architecture and Micro-architecture of Ariane version of RISC-V and ran several bench marks such as Dhrystone and Rsort, etc. Successfully figured out the reasons which could influence the performance.
- Currently work on improving Ariane version of RISC-V from in-order issue to superscalar, four threads SMT and two cores which are both performance and energy proper for Internet of Things.

Research Assistant, Optical Spintronics and Sensing Lab, University of Washington, Seattle WA January 2018 – present

- Successfully designed multi-wavelength Grating Coupler for Difference-Frequency Generation(DFG) and Single-Harmonic Generation(SHG) which can be used for Photon Frequency Conversion. The power efficiency can reach 20% total. By using one Grating Coupler rather than traditional multiple Grating Couplers, it extremely decreases the total chip area.

Member, Computation Accelerator ASIC Design Team, University of Washington, Seattle WA January 2018 – March 2018

- Implemented Streaming Convolutional Neural Networking Accelerator on ASIC with completed I/O pads which can be used for image recognition in lower cost and smaller core area using SAED90nm Technology.
- Used Bespoke Silicon Group (Led by Prof. Michael Taylor) open sources Hardware IP Cores and passed completely formal verification including Formality, GDS Merging, DRC, LVS, STA and SI Testing.

Member, CPU Design Team, University of Washington, Seattle, WA September 2017 – December 2017

- Implemented 64-bit 5-stage ARM pipeline CPU using System Verilog and ran on FPGA.
- Designed 16-bit SAPR Register File and Brent-Kung Tree ALU layout manually using TSMC65nm technology so that critical path, efficiency, space utility and power consumption get optimized.

Member, Course Project, University of Washington, Seattle, WA March 2017 - June 2017

- Successfully implemented highly-fidelity serial to parallel and parallel to serial communication channel using FPGA as IO to communicate with Microcontroller and Laptop.
- Additionally, served as team coordinator, successfully managed project organization and schedule, member working schedule, and member relation and communication.

OTHER EXPERIENCE

Teaching Assistant, University of Washington, Seattle, WA January 2017 – January 2018

- Administrated and instructed UW PHYS12x tutorial section with totally approximately 160 students.
- Strong communication, organizing and teaching ability with professors, TAs, and Students.