Gaohong Liu

206.954.6826 | gaohol@uw.edu

SUMMARY OF QUALIFICATION

- Proficient in Computer Architecture, Embedded Computing and VLSI System design: Digital IC design, simulate and layout, CPU and GPU architecture, Computation/Algorithm Accelerator Design. Embedded System Software design, development, and test. ASIC and FPGA, Networking Architecture, TCP/IP. Data Structure and Algorithm.
- Programming Language: SystemVerilog, C/C++, Java, Python, Chisel, Scala, ML.
- Computer Engineering Research background in Computer Architecture. Experience with developing Low Power multicore CPU such as RISC-V and High Performance SoC design such as Deep Convolution Neural Networking Accelerator.
- Physics Research background in Quantum Information. Understand Quantum Algorithm such as Deutsch algorithm, Grover Search algorithm. EM Waves grating coupler design for long range fiber communication.
- Strong design and testing skill with demonstrated experience and background using Software such Quartus, Code Compose Studio, Cadence Virtuoso, Synopsis Compiler and Library, Spice, MATLAB, Mathematica and Hardware such as Xilinx and Intel FPGA, Arduino Development Board and Raspberry Pi Development Platform.
- Effective Project Management, Group Communication, Teaching and Leadership as demonstrated through project, assignment, teaching assistant and other teamwork Experience.

EDUCATION

University of Washington, Seattle, WA Cumulative GPA: 3.65 Expected Graduation Date: June 2019

Bachelor of Science in Electrical and Computer Engineering (ECE)

Bachelor of Science in Physics, Comprehensive Track (PHYS)

Emphasis: Computer Architecture, Digital VLSI Design, Embedded Computing, Quantum Information.

RELEVANT EXPERIENCE

Firmware Engineer, Sensor Systems Lab & WiBotic, University of Washington, Seattle WA June 2018 – August 2018

- Maintained firmware of Battery-Free Phone including updating firmware code to adapt new IDE and compiler and making Battery-Free Phone accept signal from USRP. (C)
- Modified and improved communication model and microwave transmission architecture which used on USRP to send signal such as message and audio file to Battery-Free Phone. (Python)

Research Assistant, Bespoke Silicon Group, University of Washington, Seattle WA March 2018 – August 2018

- Beginning with RISC-V ISA, fully investigated Architecture and Micro-architecture of Ariane version, Rocket Core, SiFive E54 and U51 of RISC-V and ran several bench marks such as Dhrystone and Rsort, etc. Successfully figured out the reasons which could influence the performance. (Chisel and SystemVerilog)
- Implemented a 4-Issue 7-Stage Out-Of-Order Superscalar RISC-V Microprocessor using customized Tomasulo Algorithm which is both performance and energy proper for Internet of Things. Currently working on testing to support Linux System.

Individual Project, System Programming Course, University of Washington, Seattle WA June 2018 – August 2018

- Successfully implemented a file search engine using self-implemented and optimized doubly linkedlist and hashtable and web search engine using Dijkstra algorithm. (C/C++)
- To speed up the file search engine, wrote code that takes an in-memory inverted index produced by file search engine and wrote it out to disk in an architecture-neutral format. (C/C++)
- Implemented a multithreaded Web Server speed which allows user following TCP/IP to use this search engine and fix security issue such as Cross-Site Scripting flaw and Directory Traversal Attack. (C++ and HTTP)

Member, Embedded System Development, University of Washington, Seattle WA March 2018 – June 2018

- Successfully developed a remote Human Body Physiological Indexes Measurement Equipment using Arduino ATMega2560 and Uno as developing platform. Wrote a ROTS Kernel on Arduino ATMega2560 to schedule and issue commands, manage memory, and handle communication. Used Arduino Uno as Peripheral System to measure temperature, diastolic pressure, systolic pressure, pulse rate, respiration rate and EKG. (C++)
- Implemented high fidelity communication between ATMega2560 and Uno, remote interaction using PUTTY and local user interaction using touch screen.

Member, Computation Accelerator ASIC Design Team, University of Washington, Seattle WA January 2018 – June 2018

- Implemented Streaming Convolutional Neural Networking Accelerator on ASIC with completed I/O pads which can be used for image recognition in lower cost and smaller core area using SAED90nm Technology. (SystemVerilog)
- Used Bespoke Silicon Group open sources Hardware IP Cores and passed completely formal verification and source code can be loaded on Intel Altera FPGA to recognize streaming image at 60FPS.

Research Assistant, Optical Spintronics and Sensing Lab, University of Washington, Seattle WA January 2018 – present

- Successfully designed multi-wavelength Grating Coupler for Difference-Frequency Generation(DFG) and Single-Harmonic Generation(SHG) which can be used for Photon Frequency Conversion. The power efficiency can reach 20% total. By using one Grating Coupler rather than traditional multiple Grating Couplers, it extremely decreases the total chip area. (FDTD Solutions and MATLAB)

Member, CPU Design Team, University of Washington, Seattle, WA September 2017 – December 2017

- Implemented 64-bit 5-stage ARM pipeline CPU using System Verilog and ran on FPGA. (SystemVerilog)
- Designed 16-bit SAPR Register File and Brent-Kung Tree ALU layout manually using TSMC65nm technology so that critical path, efficiency, space utility and power consumption get optimized. (Verilog designed and Manually drew the layout)

Member, Digital System Design Course, University of Washington, Seattle, WA March 2017 - June 2017

- Successfully implemented highly-fidelity serial to parallel and parallel to serial communication channel using FPGA as IO to communicate with Microcontroller and Laptop. (Verilog)
- Additionally, served as team coordinator, successfully managed project organization and schedule, member working schedule, and member relation and communication.

OTHER EXPERIENCE

Teaching Assistant, University of Washington, Seattle, WA January 2017 – January 2018

- Administrated and instructed UW PHYS12x tutorial section with totally approximately 160 students.
- Strong communication, organizing and teaching ability with professors, TAs, and Students.