Gaohong Liu

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SUMMARY OF QUALIFICATION

- Proficient in Computer Architecture and VLSI System design, Operating System, Networking System, Embedded Computing, Data Structure and Algorithms: CPU and GPU Architecture, Computation/Algorithm Accelerator Design, Digital IC design. Basic Implementation of Unix-like Operating system, TCP/IP, Embedded System Software Design, Development, and Testing,
- Physics Background in Quantum Mechanics and basic Quantum Information, Electrodynamics, Semiconductor Physics and Integrated Photonics Design and Simulation.
- Programming Language: System Verilog, C/C++, Java, Python, Chisel, Scala, ML.
- Strong design and testing skill with demonstrated experience and background using Software: Unix-like Operating System, Docker, Quartus, Code Compose Studio, GNU Radio, Cadence Virtuoso, Synopsis Compiler and Library, Spice, MATLAB, FDTD Solution, Mathematica and Hardware: Xilinx and Intel FPGA, Arduino Development Board and Raspberry Pi Development Platform.

EDUCATION

University of Washington, Seattle, WA Cumulative GPA: 3.65 Expected Graduation Date: June 2019

Department of Electrical and Computer Engineering (ECE)

Department of Physics, Comprehensive Track (PHYS)

Emphasis: Computer Architecture, Digital VLSI Design, Operating and Networking System, Embedded Computing, Integrated Photonics Design.

RELEVANT EXPERIENCE

Firmware Engineer, Sensor Systems Lab & WiBotic, Inc, **Battery-free Phone Project**

University of Washington, Seattle WA, June 2018 – Present

- Maintained firmware of Battery-Free Phone including updating firmware code to adapt new IDE and compiler and making Battery-Free Phone receive and transmit signal from and to USRP. (C)
- Modified and improved communication model and microwave transmission architecture which used on USRP to send signal such as message and audio file to Battery-Free Phone. (Python)

Research Assistant, Bespoke Silicon Group, **4-Issue 7-Stage Out-Of-Order Superscalar RISC-V CPU Design**

University of Washington, Seattle WA, March 2018 – August 2018

- Beginning with RISC-V ISA, fully investigated Architecture and Micro-architecture of Ariane version, Rocket Core, SiFive E54 and U51 of RISC-V and ran several bench marks such as Dhrystone and Rsort, etc. Successfully figured out the reasons which could influence the performance. (Chisel and System Verilog)
- Implemented a 4-Issue 7-Stage Out-Of-Order Superscalar RISC-V Microprocessor using customized Tomasulo Algorithm (Presented in 2017 UW EE Capstone Fair) which is both performance and energy proper for Internet of Things. Currently working on testing to support Linux System.

Member, ASIC Design Team, **Convolutional Neural Networking Accelerator ASIC and Image Recognition System**

University of Washington, Seattle WA, January 2018 – June 2018

- Implemented Streaming Convolutional Neural Networking Accelerator ASIC with completed I/O pads which can be used for image recognition in lower cost and smaller core area using SAED90nm Technology. (System Verilog)
- Successful Implemented and demonstrated Image Recognition System which loaded on Intel Altera FPGA to recognize streaming image edge at 60FPS with any camera and pretrained data set.

Course Project, Operating System Course, **JOS Operating System**

University of Washington, Seattle WA, September 2018 – Present

- Successfully implemented JOS, an operating system which has Unix-likes functions but implemented in an exokernel style including Virtual Memory, User Environment, Preemptive Multitasking, File System and Shell, NIC Driver. (C, X86 Assembly)
- Now working on transplant and simulate JOS on Ariane, a RISC-V CPU.

Research Assistant, Optical Spintronics and Sensing Lab, **Multiwavelength Grating Coupler Optimization**

University of Washington, Seattle WA, January 2018 – August 2018

- Successfully designed multi-wavelength Grating Coupler for Difference-Frequency Generation(DFG) and Single-Harmonic Generation(SHG) which can be used for Photon Frequency Conversion. The power efficiency can reach 20% total. By using one Grating Coupler rather than traditional multiple Grating Couplers, it extremely decreases the total chip area. (FDTD Solutions and MATLAB)

Course Project, System Course, **Web-search Engine, File-search Engine and Multithreaded Web Server**

University of Washington, Seattle WA, March 2018 – August 2018

- Successfully implemented a file search engine and web search engine using self-implemented, optimized doubly linked list, Hash Map, hash table, AVL Tree, and Binary Heap and Dijkstra Algorithm. (C/C++, JAVA)
- To speed up the file search engine, wrote code that takes an in-memory inverted index produced by file search engine and wrote it out to disk in an architecture-neutral format. (C/C++)
- Implemented a multithreaded web server which allows user following TCP/IP to use this search engine and fix security issue such as Cross-Site Scripting flaw and Directory Traversal Attack. (C++ and HTTP)

Member, Embedded System Development, **E-Doctor Project**

University of Washington, Seattle WA, March 2018 – June 2018

- Successfully developed a remote Human Body Physiological Indexes Measurement Equipment using Arduino ATMega2560 and Uno as developing platform. Wrote a ROTS Kernel on Arduino ATMega2560 to schedule and issue commands, manage memory, and handle communication. Used Arduino Uno as Peripheral System to measure temperature, diastolic pressure, systolic pressure, pulse rate, respiration rate and EKG. (C++)
- Implemented high fidelity communication between ATMega2560 and Uno allowing remote interaction using PUTTY.

Member, CPU Design Team, **5-stage ARM CPU with Manually Layout Register File and Brent-Kung Tree ALU**

University of Washington, Seattle, WA, September 2017 – December 2017

- Implemented 64-bit 5-stage ARM pipeline CPU using System Verilog and ran on FPGA. (System Verilog)
- Designed 16-bit SAPR Register File and Brent-Kung Tree ALU layout manually using TSMC65nm technology so that critical path, efficiency, space utility and power consumption get optimized. (Most Compact Layout Design of the Class)

Member, CPU Design Team, **Parallel to Serial Communication Channel on FPGA**

University of Washington, Seattle, WA, March 2017 - June 2017

- Successfully implemented highly-fidelity serial to parallel and parallel to serial communication channel using FPGA. (Verilog)
- Successfully sent messages between cell phone and computer using Bluetooth as interface to connect between FPGA and cell phone.

OTHER EXPERIENCE

Teaching Assistant, Department of Physics

University of Washington, Seattle, WA, January 2017 – January 2018

- Administrated and instructed UW PHYS12x tutorial section with totally approximately 160 students.
- Strong communication, organizing and teaching ability with professors, TAs, and Students.