CAD ASSIGNMENT 4

EE476 DIGITAL INTEGRATED CIRCUIT DESIGN

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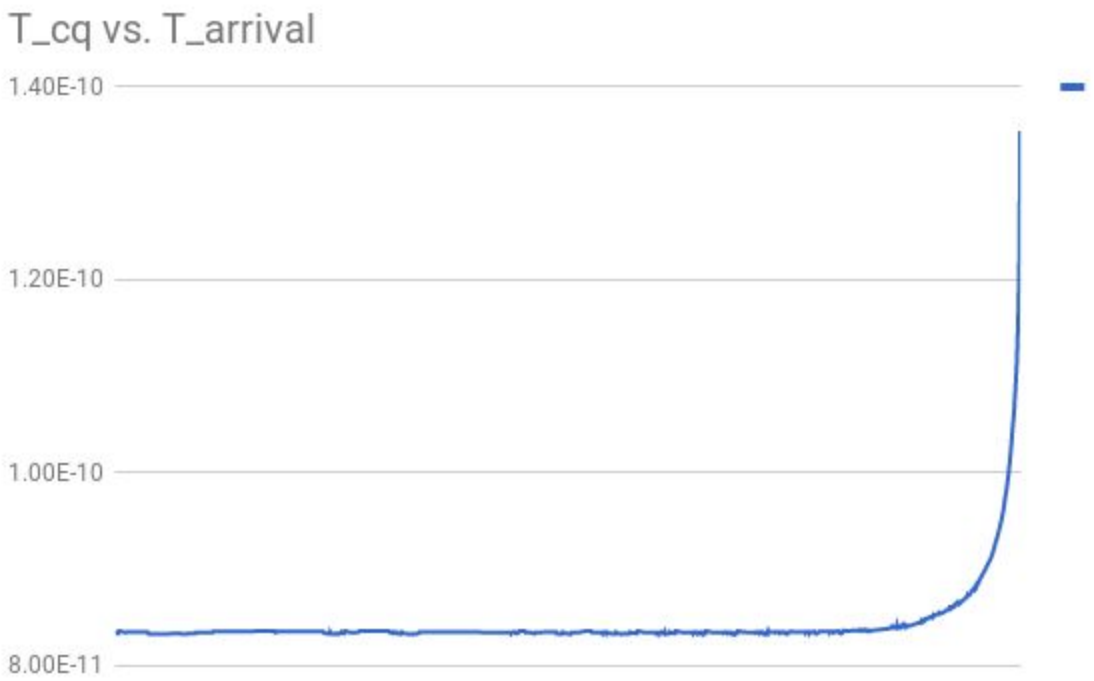
Part 6: Additional Question

a)



b) 1.2v. Because comparing with 0.8v, 1.2v setting has smaller Tcq, which means lower delay, and smaller Tsetup and Thold, which means data can be stable within shorter time.

c)R+C+CC, because it has larger powerconsumption.

d)R+C+CC has larger resistance, larger rise time but smaller fall time. Circuit with or without load can have huge difference.