EE 476 Final Project: Brent-Kung Adder ALU

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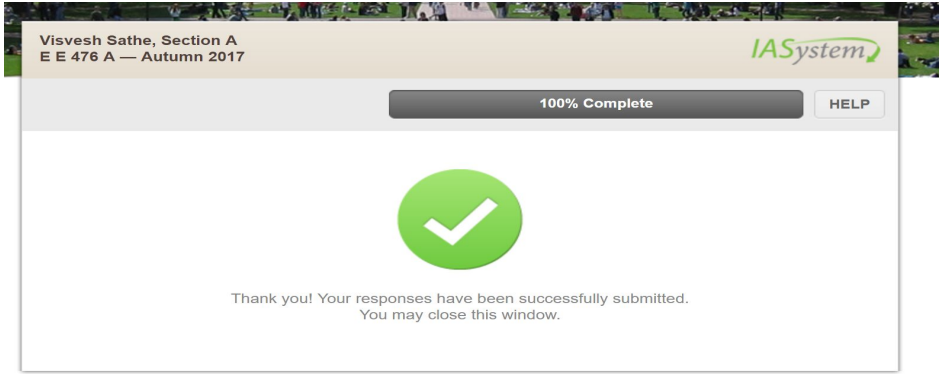
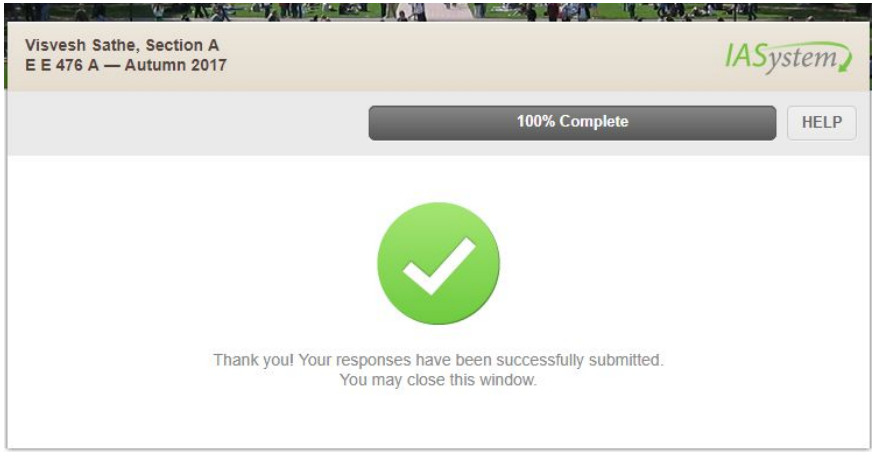
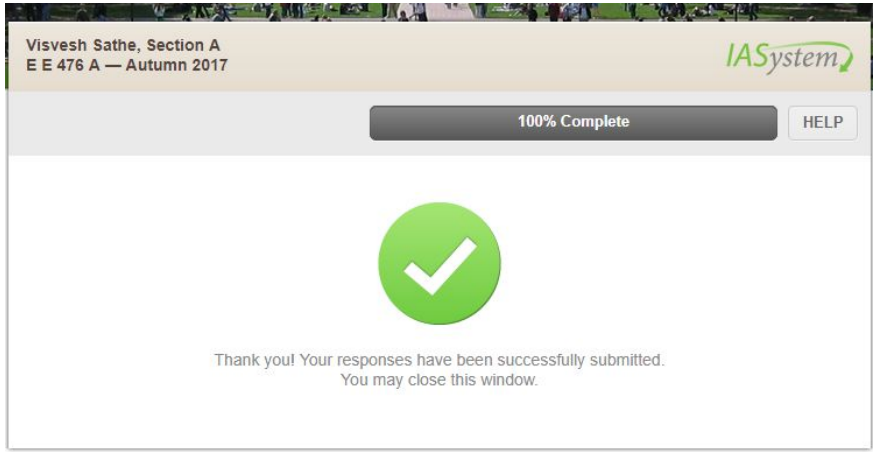
Proof of Review



Joshua Shackelford



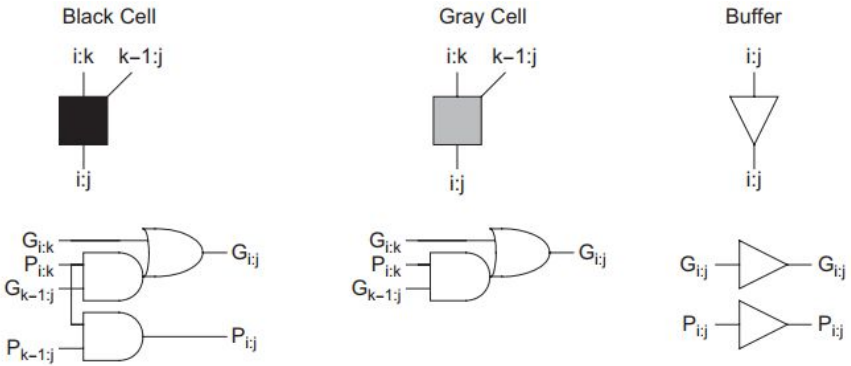
Gaohong Liu



Jiachen Zou

Basic Adder Logical blocks

- Conventional tree cells setup



Source:W&H

- Exploiting logic: Using or gate for propagate block

For Carry-Look Ahead Adder(tree adder),
AB+(A+B)Cin = AB+(A^B)Cin
Case covered by sequential AOI gate

Brent-Kung Carry Tree

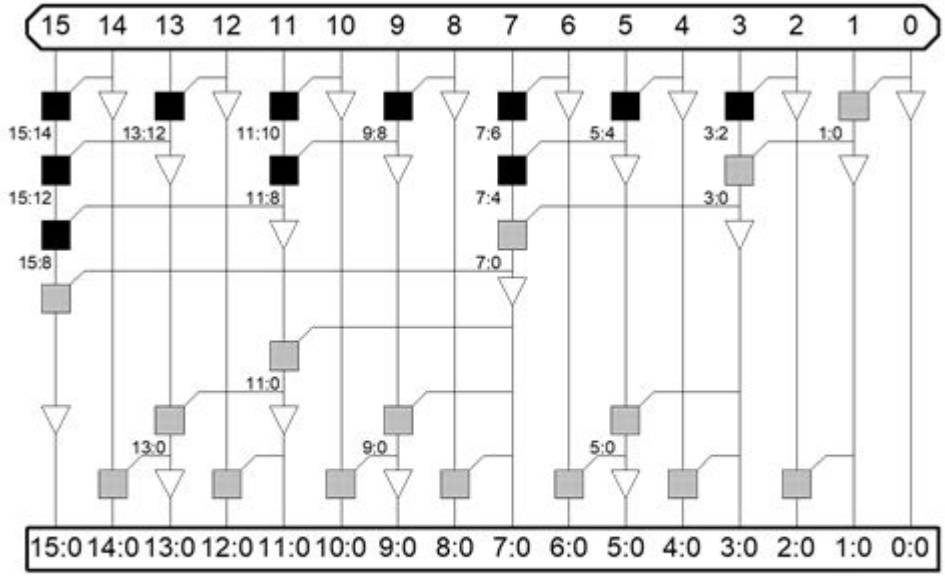
Basic Carry Tree

Cons:

- Needs to traverse the tree twice
- Can be slower for lower N (e.g. 16)

Pros:

- Handles Fan-out well
- Layout Compact(relatively lower power)



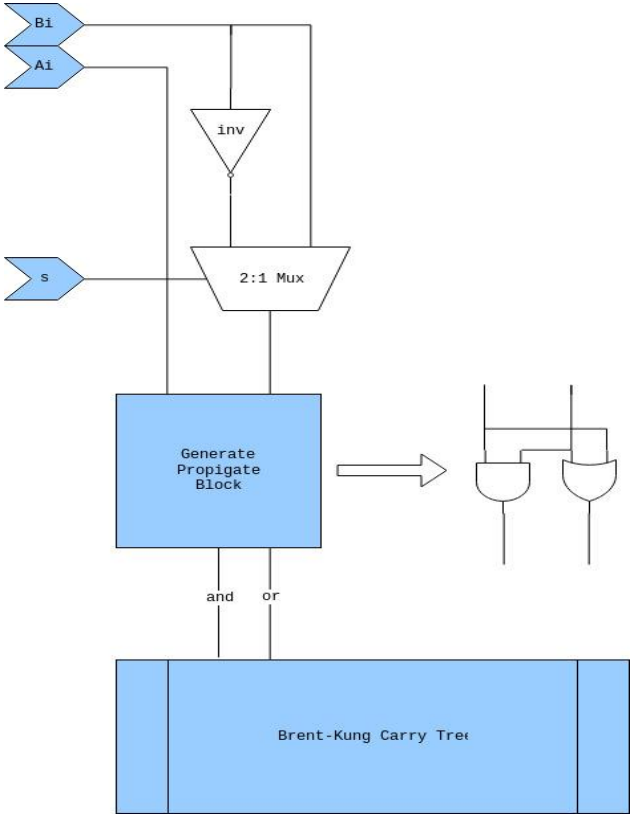
Source: W&H

Subtraction modification(need for c_in port):

1. Bit 0: Gray cell added to the top
2. Bit 1: Black cell added to the top

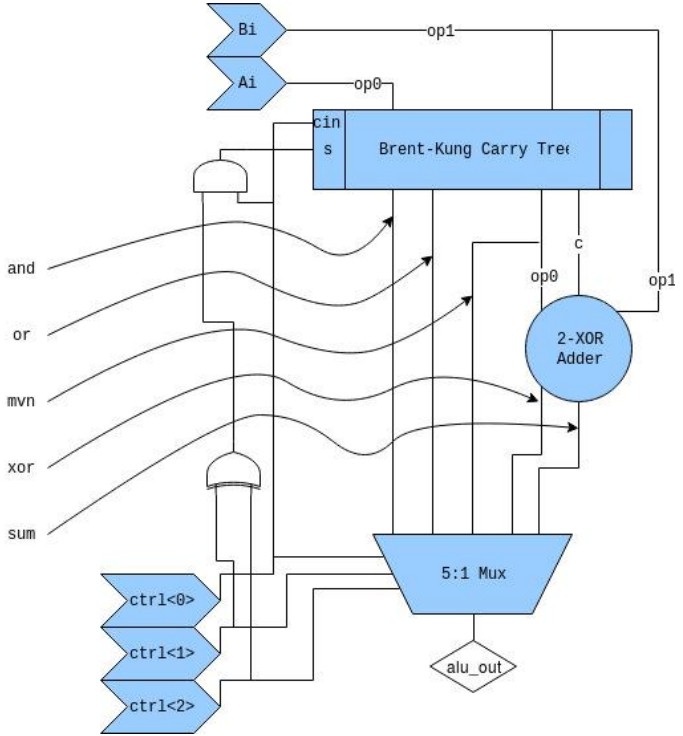
Modifications for Subtraction

In order to efficiently handle the subtract and mvn commands of our ALU, we added inverters and mux selection into the top of our BK Tree.



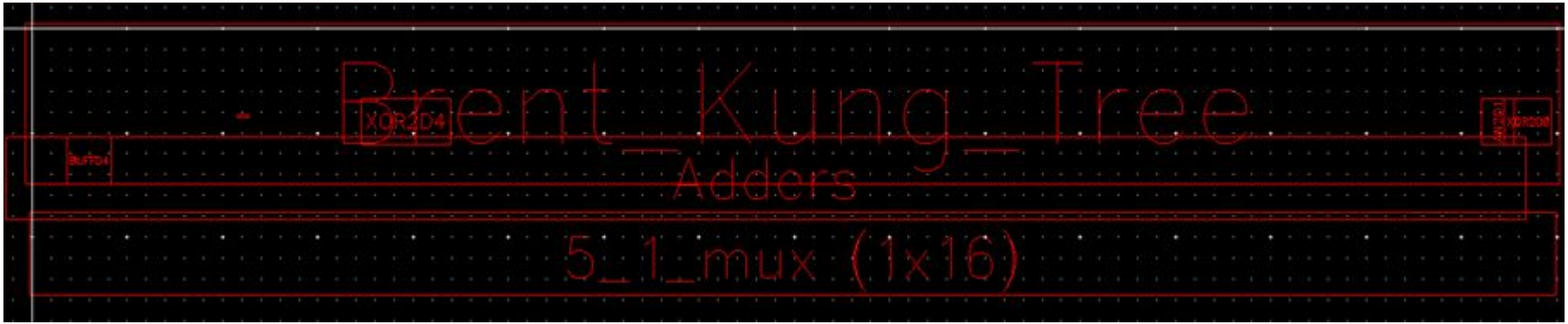
Architectural Block Diagram

Flags:
Carry Out Flag: Set as the final carry-out of the Carry Tree
Overflow Flag: Set as the XOR between the carry out of bit 14 and 15
Negative Flag: Set as the value of alu_out<15>



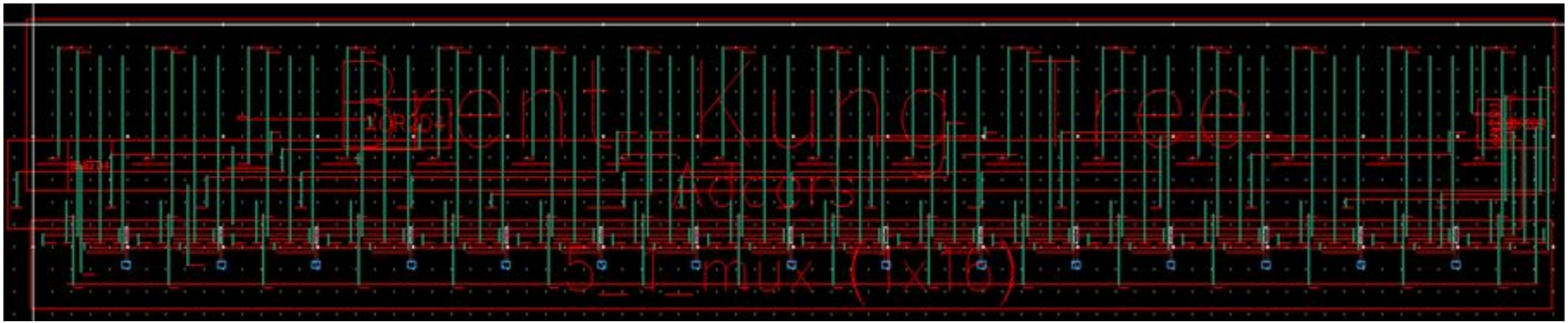
- CMOS logical blocks from input to output: increase in size and strength
- Embedded parallel computation of multiple operations in the tree adder
- Modified Brent-Kung Tree for subtraction feature
- 5 to 1 mux, determine add/sub by input inverter control logic

Layout Topology: Basic Design



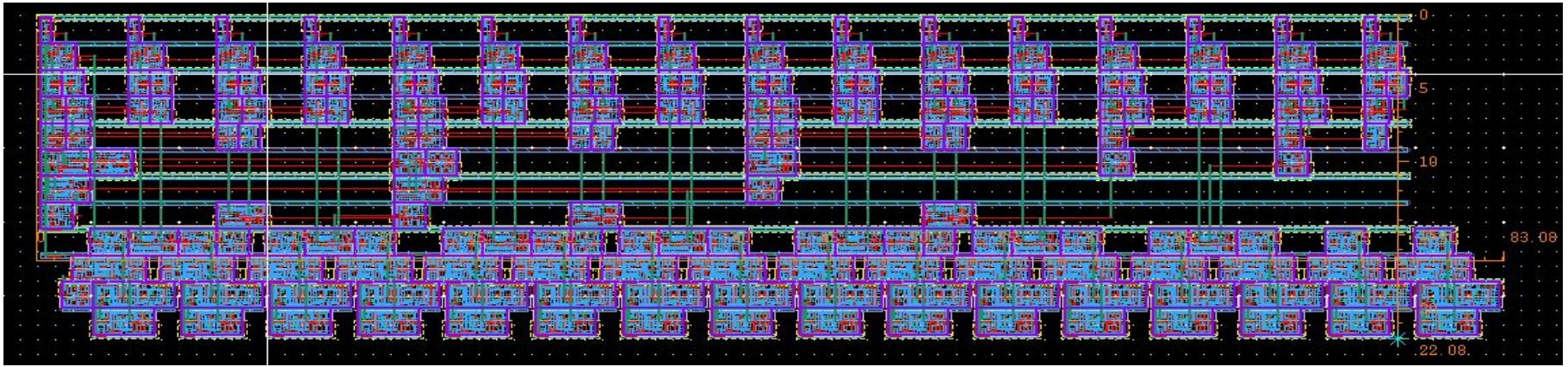
Brent-Kung Carry Tree,
Adders,
5-to-1 Output Mux Selectors,
Flag & control logic

Layout Topology: Data Pathing



M3 Vertical Data Lines primary for top-level connection between blocks(eg. Tree, adders,5 to 1 mux)
M2 Horizontal Data Lines primary for interconnection of gates

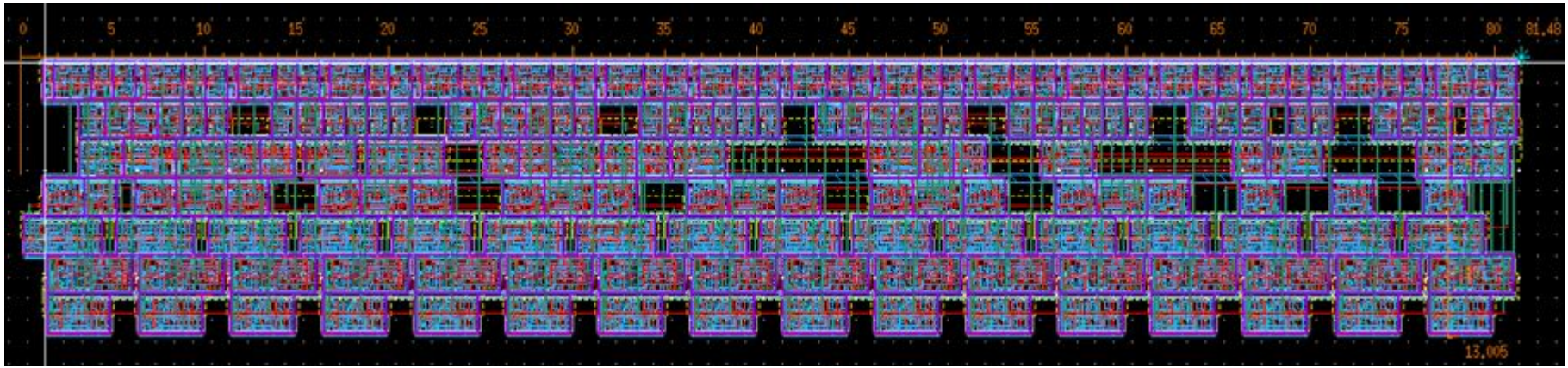
Initial Layout Topology: ALU



Length: 83.08 um
Width: 22.08 um
Area: 1834.41 um2

- Easy routing, but extremely large area.
- 5um I/O bit slice spacing
- Terrible space utilization and alignment

Layout Topology: Final ALU



Length: 81.48 um
Width: 13.005 um
Area: 1059.65 um2

- Multi-stage blocks merging for compact structure
- 5um I/O bit slice spacing
- Maximized space utilization and alignment

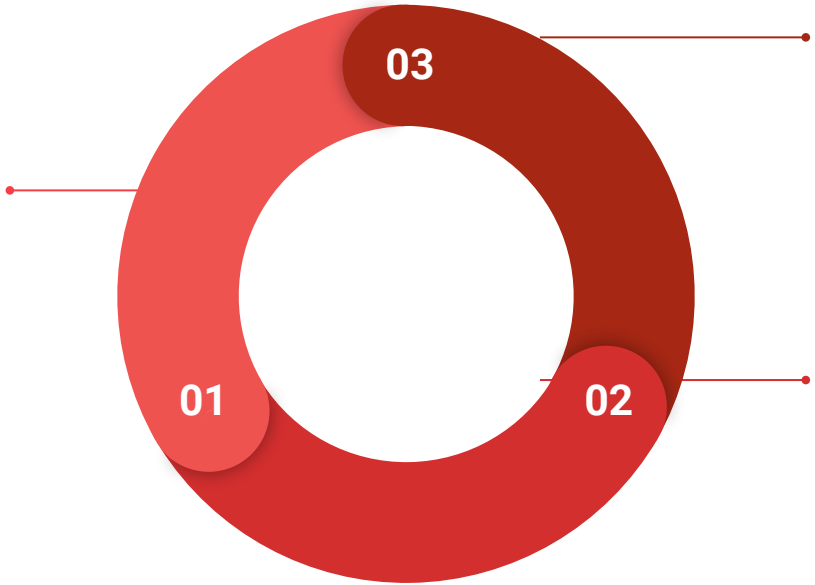
Verification Methodology

Corner Case Testing for critical path

Manually create corner case test and simulate to get critical path. If the result is not satisfying, modify the critical path sizing minorly and start over.

Script-generated random test vectors

Using valid random tests with varying cycle time to figure out the rough range of critical path case characteristics



Hspice Testing and waveform tracking

In the roughly critical path test waveform, look for slowest output port. Locating the nets causing the critical path error in the waveform.

Performance Evaluation

	Schematic	Layout
Critical Path(min cycle time)	0.44ns	0.85ns
Max Operating frequency	2.27GHz	1.176GHz

- Specific corner case test for critical path: (0x7fff | 0xffff) switch to (0x0000-0x8000)
- Critical path output port: N_flag

Power & Energy Evaluation

Energy (joule/cycle)	5 to 1 Mux	Brent-Kung tree	Adder	Overall
Schematic	6.2e-13	8.15e-13	8.18e-13	2.3e-12
Layout	7e-13	1.35e-12	9.5e-13	3e-12

Average Power (mW)	5 to 1 mux	Brent-Kung tree	Adder	Overall
Schematic	0.2485	0.3268	0.3278	0.9217
Layout	0.3799	0.8683	0.4693	1.809

- 100 cycles random test cases simulation

Thank you!