CAD ASSIGNMENT 1

EE476 DIGITAL INTEGRATED CIRCUIT DESIGN

Contributor: Gaohong Liu

Instructor: Visvesh Sathe, Naveen John

University of Washington

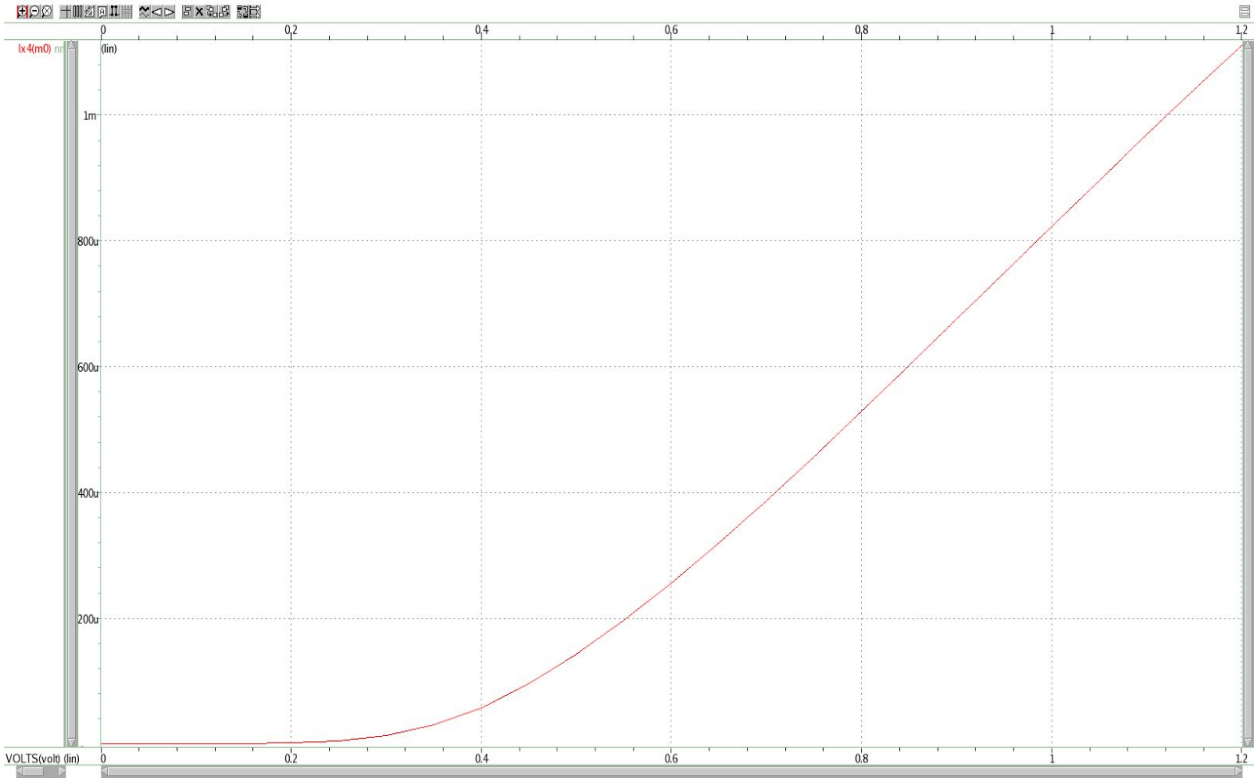
Department of Electrical Engineering

Table of Content

Procedure 1: IV Characteristics

Part a

In part a, we are required find the iv characteristics of nmos with w = 1μm, and l = 60nm. In cadence, I just build circuit as required and I set one voltage source as 1.2 volts to Vdd and one voltage source as 1.2volts to Vg for my declaration. In order to get the plot of Ids versus Vgs, I set up an DC analysis that Vgs can change from 0 volts to 1.2 volts, then I get plot of Ids versus Vgs as below. It makes sense because when Vgs is larger than 0.2 which is approximately the threshold voltage, the nmos will turn on with below characteristics.

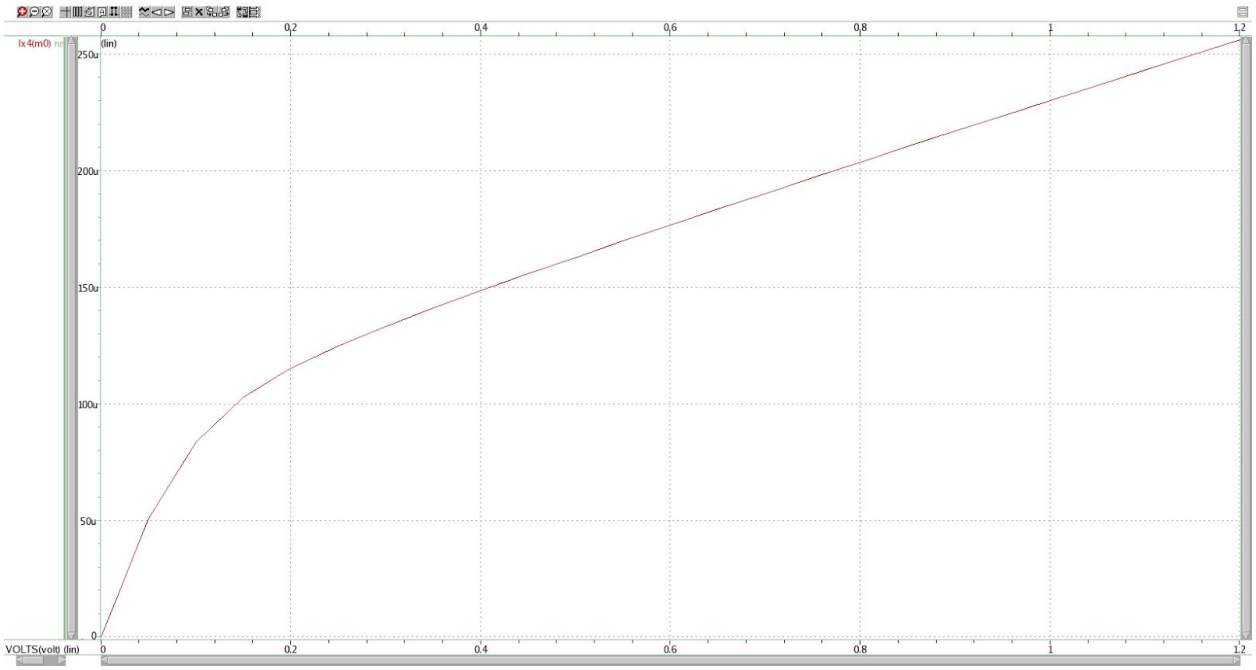


Part b

In part b, we are required the iv characteristics of nmos with two sets of Vgate, one is 0.6 volts and one is 1.2 volts. Because we want to plot of Ids versus Vds to get behavior of nmos within different operation region, we need execute a DC analysis that can change voltage across nmos. To achieve this, in my control file, I set up an voltage source as 1.2 to Vdd, and I connect

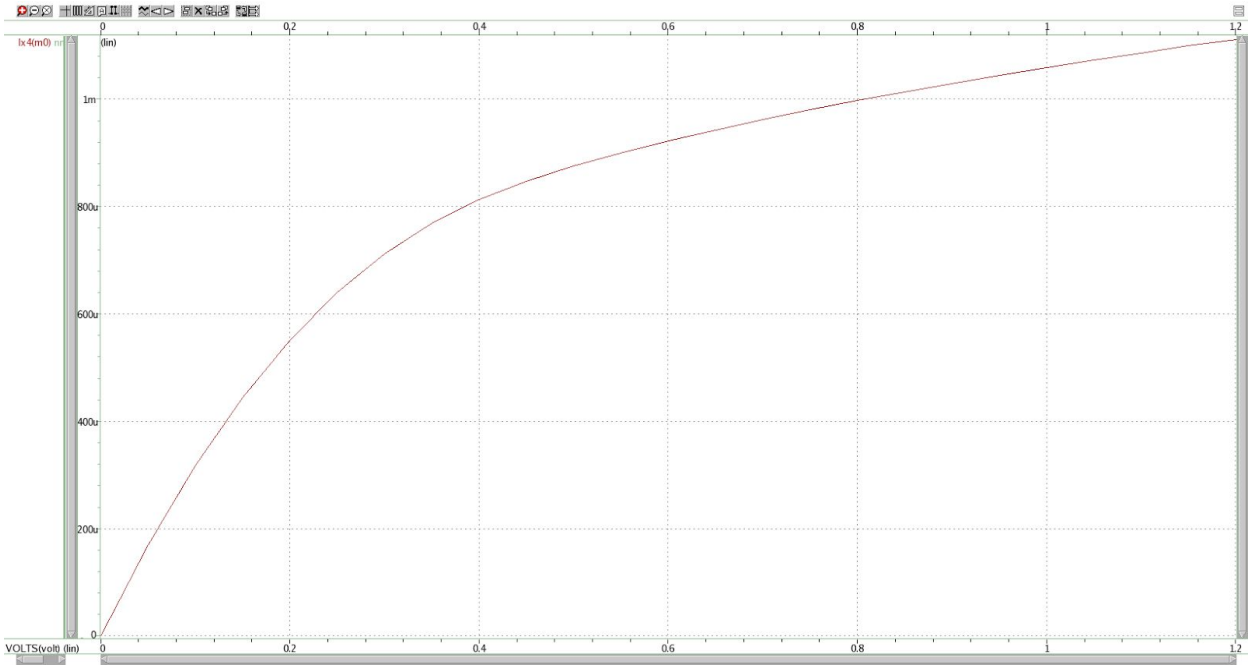
Vg to ground and gives it voltage as required, which is 0.6volts and 1.2volts separately. The waveforms below are my results.

For Vg = 0.6v



Under this situation, at the very beginning, the nmos is under cut off region, and then it enters triode region, and finally it stays in saturation region. When it enters saturation region, the Vds is approximately equal to 0.4volts. It makes sense because Vgs equal to 0.6volts and Vth is approximately equal to 0.2volts.

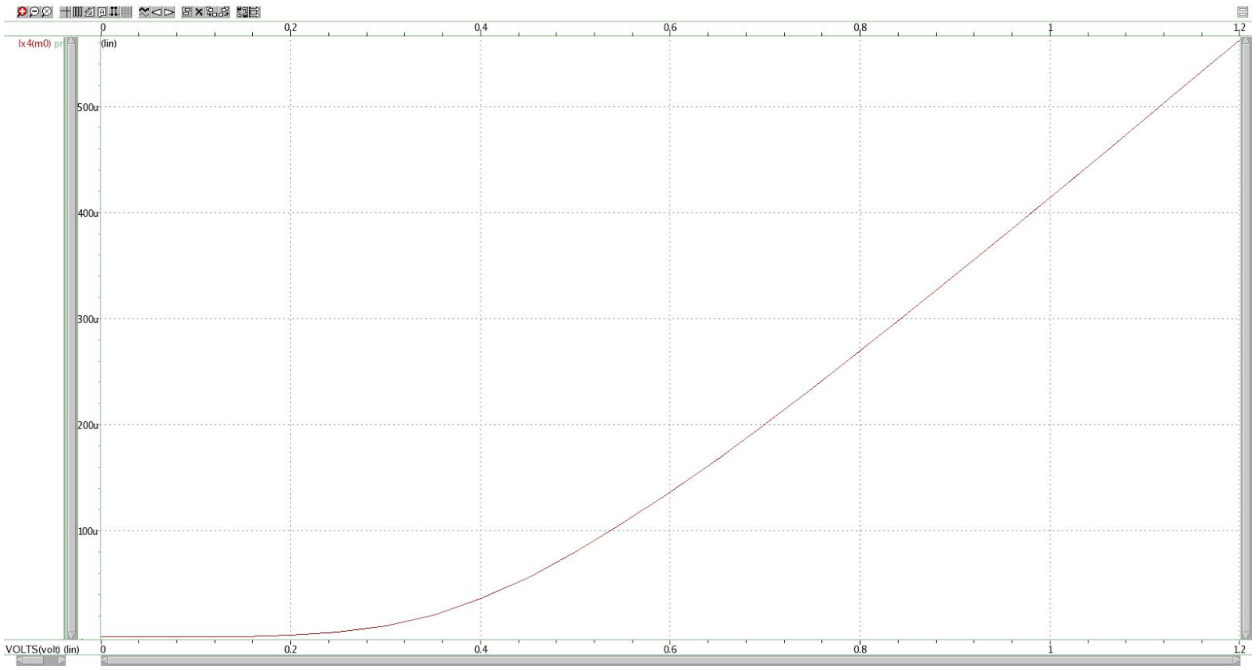
For Vg = 1.2v



Under this situation, at the very beginning, the nmos is under cut off region, and then it enters triode region, and finally it stays in saturation region. When it enters saturation region, the Vds is approximately equal to 1volts. It makes sense because Vgs equal to 1.2volts and Vth is approximately equal to 0.2volts.

Part c

In part C, we are required do the same thing to pmos as we did to nmos. The pmos we choose has w = 1μm, and l = 60nm characteristics. I build the circuits as shown in specification. Because we need to find the iv characteristics that Isd versus Vsg, so in my control file, I set voltage source Vdd as 1.2 and set up a DC analysis that I connect Vdd! with Vg and the voltage between them can sweep from 0volt to 1.2volts. Then I got my result as below. This waveform is totally correct because when we increase Vsg, pmos then can turn on and then go to triode region until it becomes saturated.

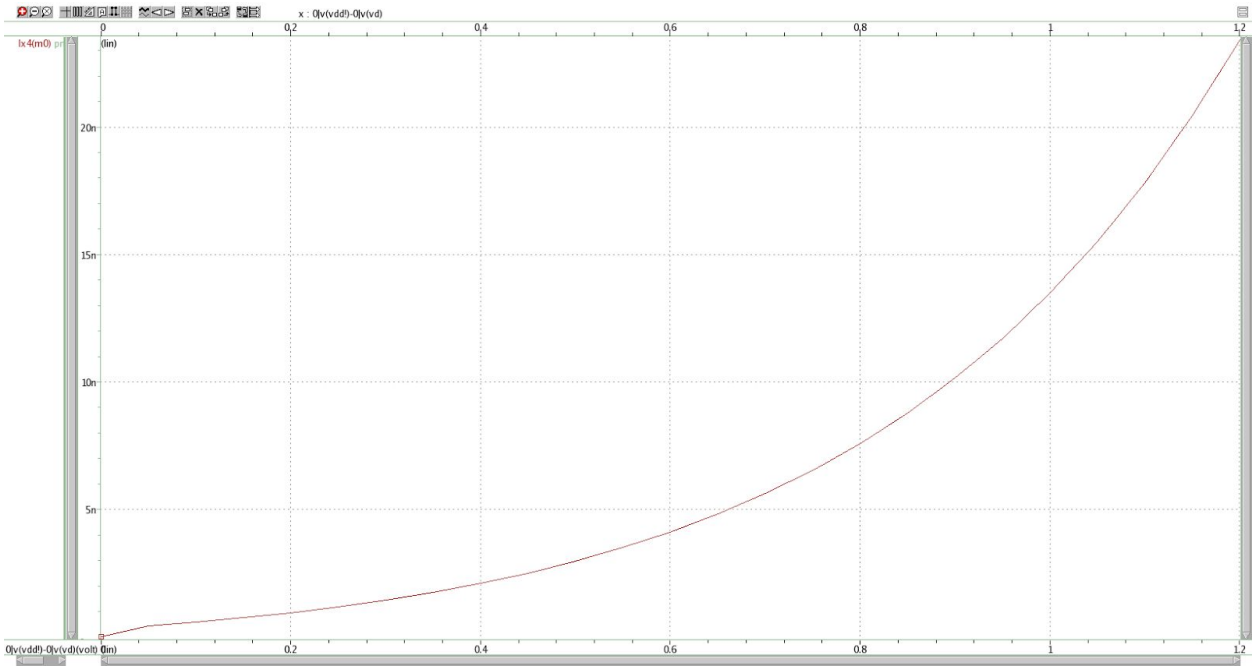


Part d

In part d, we did the same thing to pmos as we did in part b. In order to see the behavior of pmos when it enters different operation regions, we need to find the waveform Isd versus Vsd. Then we create two sets of Vg that 1.2volts and 0.6volts. In my control file, I set up two three voltage sources that one is Vg for gate voltage, one is Vdd which is 1.2volts and one is voltage supply that connects between pmos and ground which is used for make Vgs stable, and not change which Vds. Then I set up a DC analysis that change voltage supply change from 1.2volts to 0volt because then we can have Vsd change from 0volt to 1.2 volts. Additionally, because set a DC analysis about Vsupply, but we want waveform that about Vsd, I change my

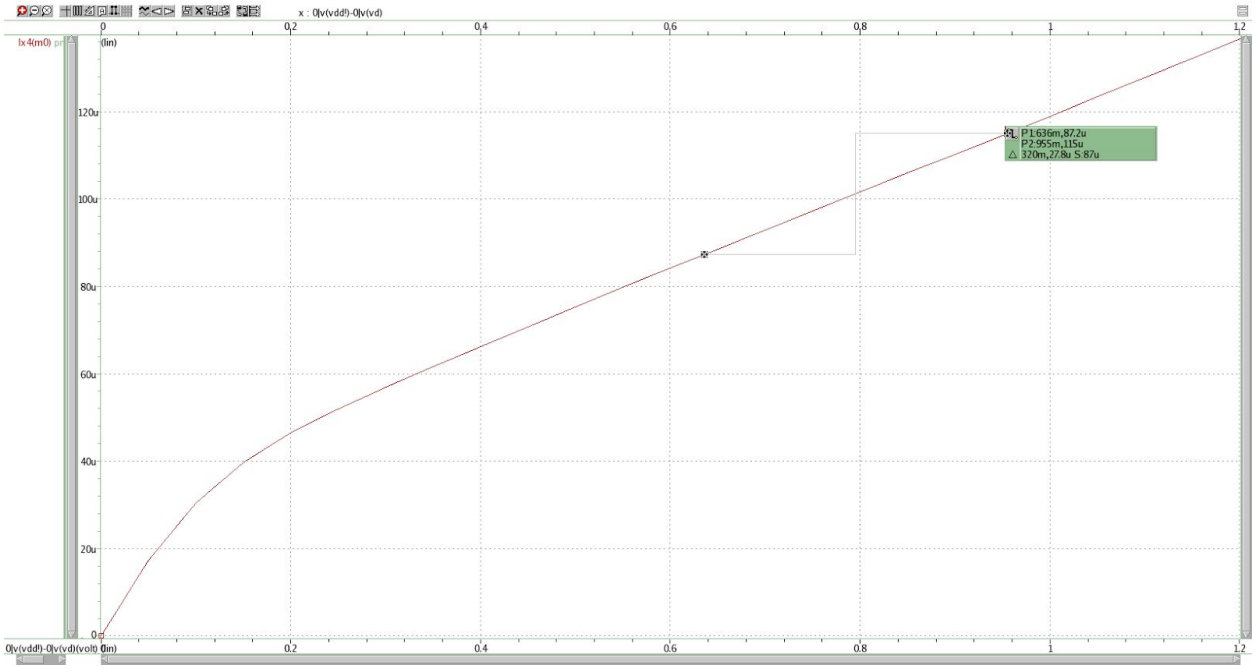
waveform axis using built-in function that change my x axis to Vsd not Vsupply, then I got my results as below.

For Vg = 1.2v



As shown in data, this pmos is alway in cutoff region.

For Vg = 0.6v

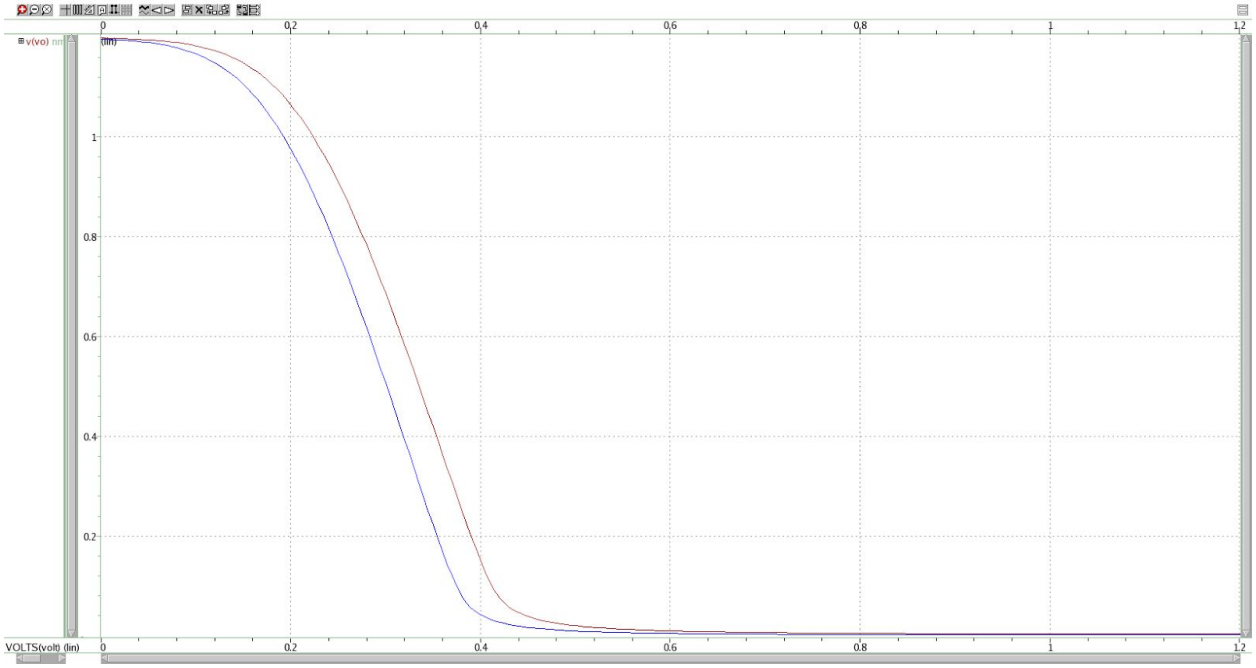


As shown in waveform, the pmos is initially at cutoff region, and then it goes to triode region and finally it goes to saturation region. When it enters saturation, the Vds approximately equals to 0.8

Procedure 2: FET's with Resistances

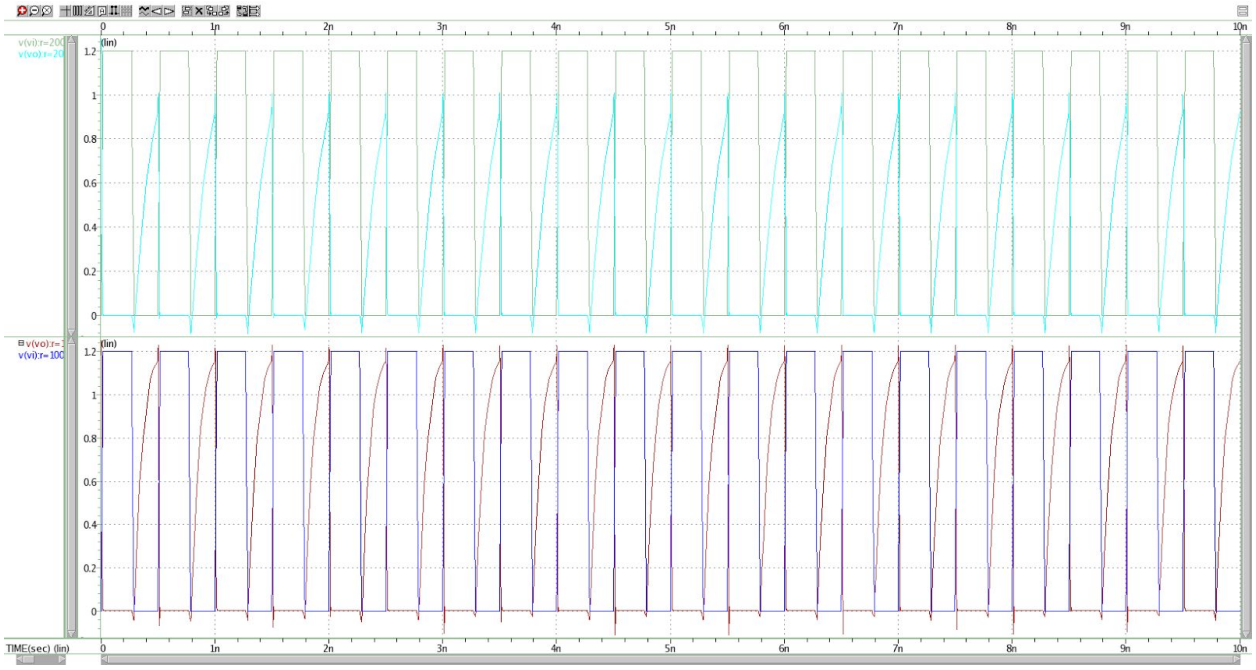
Part a

In part a, we are required find drain voltage of nmos with different resistor while changing the gate voltage from 0volt to 1.2volts. In my cadence set up, I build circuit required in specification without resistor connection. I did not connect resistor with Vdd and nmos transistor, and inversely, I leave them in schematic level without connect. However, in my control file I put resistor into DC analysis where resistor can change from 100k to 200k in one step, so I get two different resistor setting at one time. Additionally I put Vgate into DC analysis to change Vgate from 0volt to 1.2volts, and I set a voltage source at Vdd as 1.2volts. Then I got results as below.



Part b

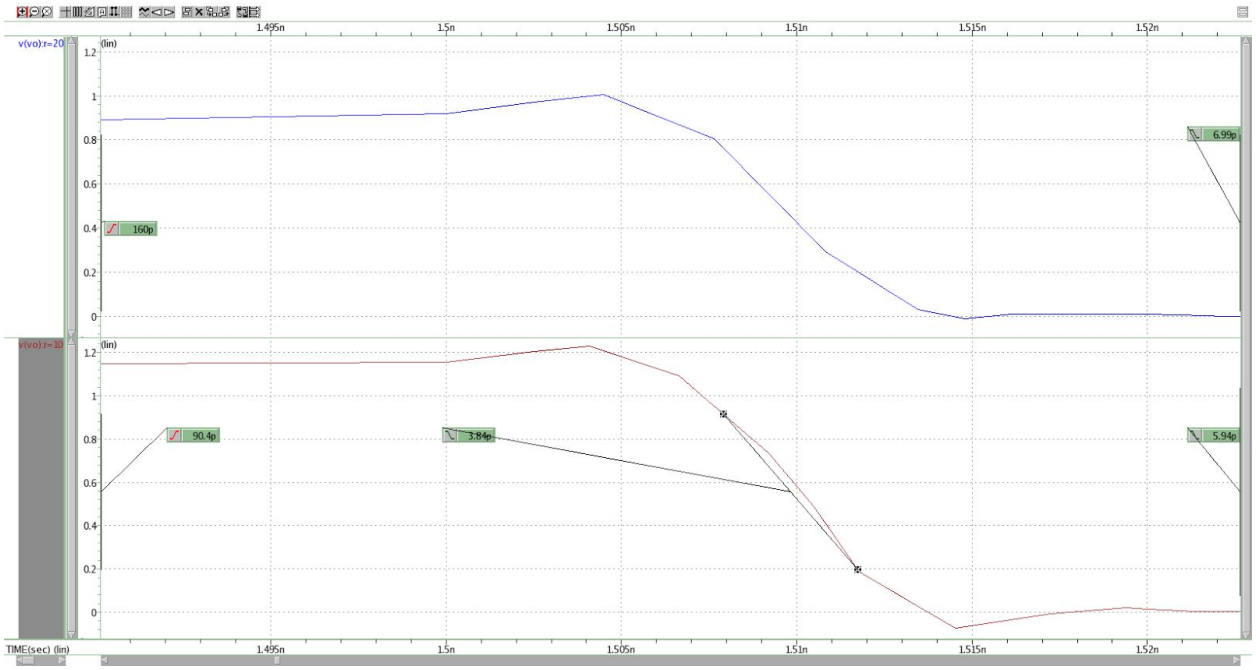
The basic setting is as same as part b. However, we need to change Vgate into a square wave voltage source where T=500ps, Trise=20ps, and Tfall=20ps. Then I got below results.



Part c

In part c, we need to find the rise time and fall time of Vo with r=100kΩ in '.MEAS' and Measurement Tool ways. In .MEAS way, I just put .MEAS with rise time and fall time command. In .mt0 file where it contains my measurement results I got **rise_time=8.931e-11s and fall_time=3.973e-11s**. Using Measurement Tool, I choose fall time and rise time function, and enlarge the signal segment I want which are fall time part and rise time part. Then I result as following, where my measurement tool result is approximately equal to my .MEAS method

result, which means my results are reliable.



Procedure 3: FET's as Resistances

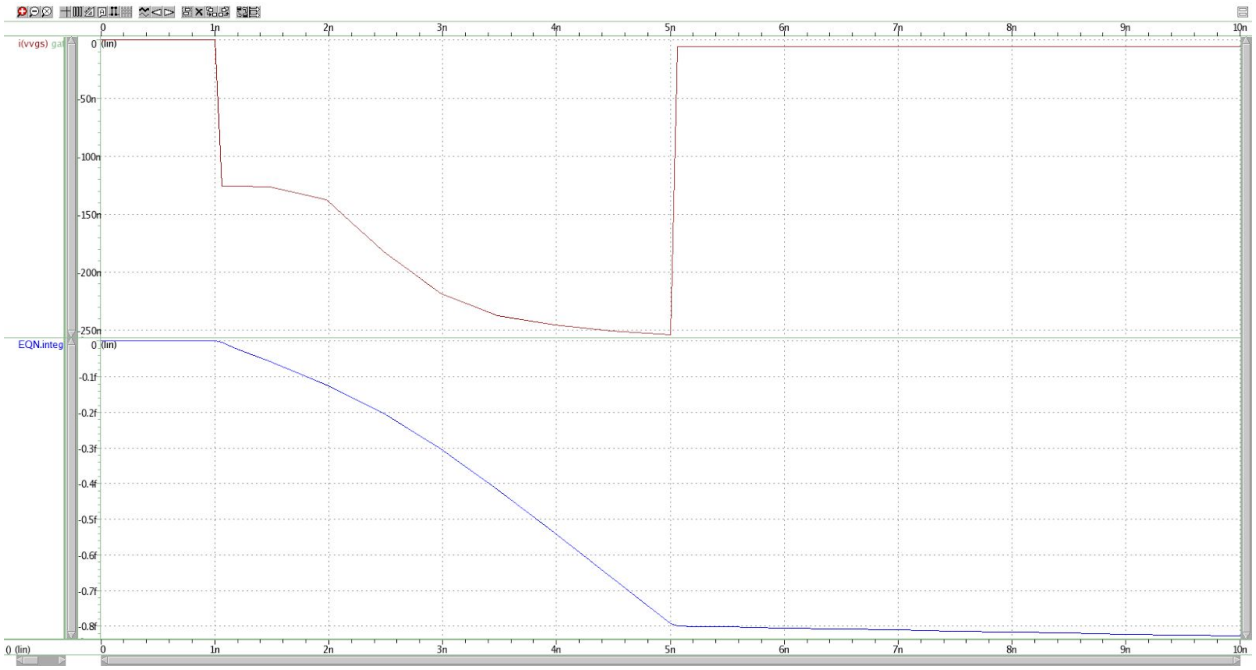
In procedure 3, we need to find resistance of nmos transistor. The basic idea is that I measure the current through the transistor and then use Vds to divide by it and then I will get the corresponding resistance. So in my control file, I set a DC analysis of Vdd where it can jump from 25mv to 250mv at one time so I can get both resistance with different Vds at same time. Then I set Vgate=1.2volts as required. As for .MEAS command, I first ask it to FIND the current through transistor, and then I use .MEAS to use Vds/Ids, and so on the result stored in .ms0 file is the resistance as required.

In my .ms0, I get my results that when **Vds=25mv, R=2.845e02Ω**, and when **Vds=250mv, R=3.090e02Ω**.

Procedure 4: Gate Capacitance

In procedure 4, we need to find capacitance of gate. The basic idea is, we generate a pulse voltage, and then use .MEAS command to find the current through gate. After measurement, using waveform of current through gate and Function inside silicon explore to calculate charge through gate over time because $Q = \int idt$. So I build circuit as described in specification, and use

PWL command to generate a pulse that in 1ps that the voltage across gate can increase from 0volt to 1volts and then use.MEAS command to calculate Q. In my .mt0 file I get Q=-8.053e-16c and because C=Q/V, c=8.053c/v. To verify I get a reliable data, I use Measurement Tool's function to generate integral waveform and I got below result.



The total charge across gate is approximately equal to 0.8c so I get a reliable data in .mt0 file.

Procedure 5: Additional Question

Part a

In part a, I try to find Vth first. I locate saturation region in my waveform, and then I find the derivation line across that point. By finding the point that derivation line across x-axis, I got **Vth=0.38volts**. Then I locate two random points at saturation region. One is V1=1.19volts, I=1.1mA, and one is V2=1.18volts, I=1.08mA. I plug these data and Vth into function $I = \frac{1}{2}\beta(Vgs - Vth)^n$, then I got a pair of equations. By dividing them, we can cancel β and get an equation about n. Solving it we get **n=1.8**. Finally plug back we get **β=0.002241**

Part b

Same procedure with part a, we get **Vth=0.39volts**, **n=2.1375**, and **β=0.001142.** (Point1:V1=1.18volts, I2=551uA; Point2:V2=1.19volts, I2=559uA)

Part c

$\frac{\beta_{nmos}}{\beta_{pmos}}$ = 1.9657

Part d

λ is the slope of the saturation region, so I simply use Measurement Tool in Silicon Explorer, the difference function to get slope. Then I get **λ=271u A/V**

Part e

Same procedure in part d, I get **λ=87u A/V**