CAD ASSIGNMENT 6

EE476 DIGITAL INTEGRATED CIRCUIT DESIGN

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Additional Questions:

a. After test, the critical path for our schematic design is 0.44ns. The test case we used is 0x0000-0x8000 while previous operands were 0x7fff || 0xffff. The test case means to test the subtraction, which is the longest datapath in the ALU. The reason I choose 0x0000-0x8000 is to get a negative number with longest propagation. In this case, the highest bit for op0 is 1. After inverter, the op1+(~op0) will produce propagation for all bits except the highest bit. Because of the highest bit is kill, we will produce an overflow and negative flag. During the random test we did before this, we found hitting at critical path always result in unclear n_flag. And the critical path error control input is always 101(sub) with previous control 010(or). Consequently, this test case gave us the critical path. We do expect the layout-level critical path to be exercised by the same input transition and path. One reason is that our layout is fairly compact. There won't be too many resistive and capacitive difference in long wires. Since we did similar mechanic for layout, start from random test, find similarity between different test error trials, to find the critical path test case; and we get the same test case being the critical path. We eventually get critical path of 0.85ns for layout.

According to our previous measurement, our energy-delay product is around 3e-12 * 0.85e-9 = 2.55e-21