JASON HO

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EDUCATION

University of Texas, Austin *Aug 2022 - Current*
Ph.D. Electrical and Computer Engineering, ACSES Computer Architecture

Brown University *Sept 2018 - May 2022*
Sc.B. Computer Engineering with Honors GPA: 3.94
Thesis: Tools for Understanding the Computational Behaviors of Biofilms
Relevant Coursework: VLSI Design, Computer Architecture, Digital Signal Processing, Topics in Bioelectronics, Operating Systems, Semiconductor Physics

RESEARCH EXPERIENCE

Graduate Researcher, SLAM Lab, UT Austin *Jan 2021 - Present*
Advisor: Professor Andreas Gerstlauer
- Researching machine learning models to simulate analog neuron models for neuromorphic computing architecture simulators

Undergraduate Researcher, SCALE Lab, Brown University *Jan 2021 - Jun 2022*
Advisor: Professor Sherief Reda
- Modelled biofilm coupling interactions using SciPy, NumPy, Pandas, and MatPlotLib between three or more biofilms in two dimensional arrays as Kuramoto oscillators for non-conventional oscillatory computing systems
- Performed architecture state space search of the computational ability in biofilms with varying phenotype expression using coupled biofilm interaction models
- Developed super-resolution techniques for impedance imaging for use in deep learning GANs pipeline

PUBLICATIONS

K. Hu, **J. Ho** and J. K. Rosenstein, "Super-Resolution Electrochemical Impedance Imaging with a 512×256 CMOS Sensor Array," in IEEE Transactions on Biomedical Circuits and Systems, 2022, doi: 10.1109/TBCAS.2022.3183856.

TEACHING AND MENTORING EXPERIENCE

Head Teaching Assistant, ENGN 1640: Design of Computing Systems *Jan 2022 - May 2022*
- Ran office hours twice a week in computing lab to help students build RISC-V processors on Altera FPGA boards. - Held conceptual hours for students and helped guide students toward designs optimized that minimized logic, or speed

Teaching Assistant, ENGN 1580: Communication Systems *Jan 2022 - May 2022*
- Designed final project for students to emulate communication across a physical channel in the midst of noise and crosstalk on the channel.

Head Teaching Assistant, CSCI 1600: Real-Time and Embedded Software *Sept 2021 - Dec 2021*
- Lead two lab sessions a week teaching students Arduino and breadboarding on topics such as timers, interrupts, real-time operating systems, and sensors
- Held conceptual hours once a week for any students to come to as well - Guided and provided advice to students for their final design projects

Mentor, MAPS (Matched Advising Program for Sophomores) *Jan 2021 - May 2022*
- Advised mentees interested in concentrating in Computer Engineering, Computer Science, or related

fields on classes, research, and internship opportunities

Mentor, School of Engineering *Jan 2021 - May 2022*
- Helped mentees to devise plans on completing concentration requirements as well as providing advice on classes, research, internship opportunities and approach to learning

Teaching Assistant, ENGN 0500: Digital Computing Systems *Jan 2021 - May 2021*
- Held weekly office hours to provide conceptual understanding of digital design,computer architecture, and programming assignments
- Helped teach students in class with interactive digital design demonstrations and embedded systems coding

ADDITIONAL ENGINEERING EXPERIENCE

VLSI Read Channel Design and Verification Intern, Seagate Technology *Jun 2022 - Aug 2022*
- Researched verification environment transactions with DUT to enforce object-oriented data structures in transition to UVM.
- Developed firmware initialization and configuration code for read channel UVM environment.

VLSI Design and Verification Engineering Intern, Seagate Technology *May 2021 - Aug 2021*
- Designed and verified new RTL block responsible for optimizing throughput of ECC correction on hard drive reads set to tape-out in early 2022
- Designed testing infrastructure and deployed tests for the new RTL block in VMM for the new RTL features

FPGA Engineering Intern, Nabsys *Jun 2020 - Sept 2020*
- Developed parallel signal processing algorithms and state machines on Xilinx FPGAs for analysis of tagged DNA for whole genome sequencing
- Optimized FPGA design to significantly reduce slices used by 2x, allowing for increased parallelization of algorithms for greater throughput
- Verified FPGA design with a combination of C++ and Python scripting

Security Engineering Intern, Brown OIT *Apr 2019 - Sept 2019*
- Designed Copyright infringement scripts in Python that parsed DMCA emails, searched firewall logs and verified infringement on University firewall traffic, saving non-technical staff over 3 hours of time per case
- Queried SQL databases to aggregate Crowdstrike data with firewall permit-deny traffic on real-time dashboards to display malicious traffic by optimizing firewall parsing by 20 times using Regex

RELEVANT PROJECTS

Convolution ASIC Tapeout, Brown Chip Design *Jan 2021 - Present*
- Designing architecture and implementing RTL for ASIC tapeout in Efabless shuttle for real-time 2D image convolution using Yosys, Magic, and OpenLane
- Working to create a club in the engineering school to continue iterating on the initial design and get underclassmen interested in computer architecture

RISC-V Processor on FPGA *Apr 2021 - May 2021*
- Implemented front end RTL on abbreviated RISC-V instruction set with branch prediction and five stage pipeline on Intel FPGA board
- Verified all design blocks in ModelSim and ran RTL through Intel Quartus

VOLUNTEER WORK

Project Manager and Developer, Develop for Good *Sept 2020 - Jan 2021*
- Developed and deployed Django website for CARE International on analysis and visualization of USAID Hamzari data in an internal website
- Supervised a team of 6 Frontend, Backend, UI/UX developers, and Data Scientists

AWARDS

Cockrell School of Engineering Fellow, UT Austin *2022-Current*
UT Austin Graduate Excellence Fellow, UT Austin *2022-Current*
Sigma Xi Research Honor Society, Brown University *May 2022*
NSF GRFP Honorable Mention, NSF *Apr 2022*
Tau Beta Pi Engineering Honor Society, Brown University *Dec 2021*
Grimshaw-Gudewicz Annual Scholar *2020-2022*
Best Use of Google Cloud, Hack @ Brown *Jan 2020*
Valedictorian, Seekonk High School *May 2018*

PROFESSIONAL MEMBERSHIPS

Student Member, IEEE *2021 - Present*
Student Member, ACM *2021 - Present*

SKILLS

Programming Languages
Verilog, SystemVerilog, C, C++, RISC-V ASM, Python

Applications
Innovus, Genus, DC Compiler, Verdi, ModelSim, LTSpice, Electric, Matlab

Languages
English (Fluent), Cantonese (Fluent)