Jason Ho

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EDUCATION

University of Texas at Austin — **Austin, TX**
Ph.D. in Electrical and Computer Engineering (*Computer Architecture*), ***GPA: 3.96*** — *August 2022 - Current*

- Researching mixed-signal neuromorphic architectures for ML inference acceleration under Dr. Andreas Gerstlauer

University of Texas at Austin — **Austin, TX**
M.S.E. in Electrical and Computer Engineering, ***GPA: 3.96*** — *August 2022 - December 2024*

- *Relevant Coursework*: Accelerator Design, Low-Power Design, Parallel Computer Architecture, ML for Systems

Brown University — **Providence, RI**
Sc.B. with Honors in Computer Engineering, ***GPA: 3.96*** — *September 2018 - May 2022*

- **Thesis:** *Tools for Understanding Computational Behaviors of Bacterial Biofilms*, supervised by Dr. Sherief Reda
- *Relevant Coursework*: VLSI Design, Digital Signal Processing, Operating Systems

EXPERIENCE

University of Texas at Austin — **Austin, TX**
Graduate Researcher — *August 2022 - Current*

- Investigating ML-based power and performance surrogate models of analog compute blocks in large-scale mixed-signal simulators which achieves 12x speedup over state-of-the-art simulation methodologies
- Researching co-design strategies for hybrid analog-digital neuromorphic computing systems to combine analog energy efficiency with digital scalability
- Authored paper: **J. Ho**, J. Boyle, A. Gerstlauer, "LASANA: Large-scale Surrogate Modeling for Analog Neuromorphic Architecture Exploration", 2025. (under review)
- Authored paper: J. Boyle, **J. Ho**, M. Plagge, S. Cardwell, F. Chance, A. Gerstlauer, "Exploring Dendrites in Large-Scale Neuromorphic Architectures", 2025. (under review)

AMD — **Austin, TX**
Power and Performance Lead/Architect Intern — *May 2023 - August 2023*

- Characterized power and performance for future APU with discrete GPU platforms, focusing on optimal power allocation algorithms for GPU-bound benchmarks
- Developed and deployed an internal data analysis tool for multi-phasic statistical analysis of benchmarks which achieved more than 100x speedup over prior methods

Seagate Technology — **Longmont, CO**
VLSI Read Channel Design Engineering Intern — *May 2021 - Aug 2021 | May 2022 - August 2022*

- Designed and verified new RTL block which increased ECC correction throughput in hard drive read pipelines
- Spearheaded migration of existing VMM verification infrastructure for the ECC correction IP block to UVM

PROJECTS

CNN FPGA Hardware Accelerator — *September 2022 - December 2022*

- Designed and deployed a CNN accelerator with two team members on AWS FPGA using blocking systolic matrix multipliers with Xilinx Vitis HLS tools
- Reduced parameter size by 75% using custom fixed-point 8-bit values with minimal impact on test accuracy

Super-Resolution Impedance Imaging — *September 2021 - June 2022*

- Developed super-resolution techniques for impedance tomography on a custom mixed-signal imaging and stimulation platform designed for oscillatory computing system exploration
- Authored paper: K. Hu, **J. Ho** and J. K. Rosenstein, "Super-Resolution Electrochemical Impedance Imaging with a 512 × 256 CMOS Sensor Array," in IEEE Transactions on Biomedical Circuits and Systems, 2022.

SKILLS

- **Programming**: Verilog, SystemVerilog, C, C++, Python, PyTorch
- **Tools**: Matlab, Innovus, ModelSim, HSPICE, Gem5, Virtuoso