

# JASON HO

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## EDUCATION

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### **Brown University**

*Sept 2018 - Jun 2022*

Sc.B. Computer Engineering

GPA: 3.94

*Current Coursework:* Topics in Bioelectronics, Digital Signal Processing, Materials Science, Computational Probability and Statistics

*Relevant Coursework:* VLSI Design, Digital Electronics Design, Design of Computing Systems, Communication Systems, Linear System Analysis

## RESEARCH EXPERIENCE

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### **Undergraduate Researcher**, SCALE Lab, Brown University

*Jan 2021 - Present*

*Advisor:* Sherief Reda

- Modelling biofilm coupling interactions using SciPy, NumPy, Pandas, and Matplotlib between three or more biofilms in two dimensional arrays as Kuramoto oscillators for non-conventional oscillatory computing systems
- Exploring the state space of computational ability in biofilms with varying phenotype expression, leading to changes in communication strength and coupling strength
- Debugging and developing source code of previous tape-out that failed due to floating wires for new micro-controller connected to CMOS biofilm sensing array

## TEACHING AND MENTORING EXPERIENCE

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### **Mentor**, MAPS (Matched Advising Program for Sophomores)

*Jan 2021 - Present*

- Advised mentees interested in concentrating in Computer Engineering, Computer Science, or related fields on classes, research, and internship opportunities

### **Mentor**, School of Engineering

*Jan 2021 - Present*

- Planned with mentees to devise plans on completing concentration requirements as well as providing advice on classes, research, internship opportunities and approach to learning

### **Teaching Assistant**, ENGN 0500: Digital Computing Systems

*Jan 2021 - May 2021*

- Held weekly office hours to provide conceptual understanding of digital design, computer architecture, and programming assignments
- Helped teach students in class with interactive digital design demonstrations and embedded systems coding

## ADDITIONAL ENGINEERING EXPERIENCE

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### **VLSI Design and Verification Engineering Intern**, Seagate Technology

*May 2021 - Aug 2021*

- Designed and verified new RTL block responsible for optimizing throughput of ECC correction on hard drive reads set to tape-out in early 2022
- Designed and developed verification environment in VMM and UVM in SystemVerilog for new RTL features

### **FPGA Engineering Intern**, Nabsys

*Jun 2020 - Sept 2020*

- Developed signal processing algorithms and state machines in Vivado on Xilinx FPGA for analysis of tagged DNA for whole genome sequencing; able to perform real time data processing of hundreds of detectors.

- Optimized FPGA design to significantly reduce slices used, allowing for increased parallelization of algorithms on FPGA, significantly increasing throughput.
- Verified design of FPGA with C++ scripts and Python scripting.

#### **Security Engineering Intern, Brown CIS**

*Apr 2019 - Sept 2019*

- Designed Copyright Infringement Script in Python that parsed DMCA emails, searched firewall logs and verified infringement on University traffic, saving non-technical staff over 3 hours of time per case.
- Queried SQL databases to correlate CrowdStrike data with firewall permit-deny traffic in real-time dashboards to display current state of malicious traffic by optimizing firewall parsing by 20 times using Regex.

### **RELEVANT PROJECTS**

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#### **Convolution ASIC Tapeout, Brown Chip Design**

*Jan 2021 - Present*

- Designing architecture and implementing RTL for ASIC tapeout in Efabless shuttle for real-time 2D image convolution using Yosys, Magic, and OpenLane
- Working to create a club in the engineering school to continue iterating on the initial design and get underclassmen interested in computer architecture

#### **RISC-V Processor on FPGA**

*Apr 2021 - May 2021*

- Implemented front end RTL on abbreviated RISC-V instruction set with branch prediction and five stage pipeline on Intel FPGA board - Verified all design blocks in ModelSim and ran RTL through Intel Quartus

### **VOLUNTEER WORK**

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#### **Project Manager and Developer, Develop for Good**

*Sept 2020 - Jan 2021*

- Developed Django website for CARE International on analysis and visualization of USAID Hamzari data in an internal website
- Supervised a team of 6 Frontend, Backend, UI/UX developers, and Data Scientists

### **AWARDS**

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**Best Use of Google Cloud, Hack @ Brown**

*2020*

**Valedictorian, Seekonk High School**

*2018*

### **PROFESSIONAL MEMBERSHIPS**

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**Student Member, IEEE**

*2021 - Present*

**Student Member, ACM**

*2021 - Present*

### **SKILLS**

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#### **Programming Languages**

Verilog, SystemVerilog, C, C++, x86 ASM, RISC-V ASM, Python, Java

#### **Applications**

Innovus, Genus, DC Compiler, Verdi, ModelSim, LTSpice, Electric, Vivado HLS, Matlab

#### **Languages**

English (Fluent), Cantonese (Fluent)