Jason Ho

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EDUCATION

University of Texas at Austin — **Austin, TX**
Ph.D. in Computer Architecture, ***GPA: 4.0*** — *Aug 2022 - Current*

- Researching applications of analog neuromorphic architectures and developing simulators for them
- *Relevant Coursework*: Cross-Layer ML HW/SW Design, Computer Architecture, Unconventional Computation

Brown University — **Providence, RI**
Sc.B. with honors in Computer Engineering, ***GPA: 3.96*** — *Sept 2018 - May 2022*

- **Thesis:** *Tools for Understanding Computational Behaviors of Bacterial Biofilms*
- *Relevant Coursework*: VLSI Design, Digital Signal Processing, Computer Architecture

EXPERIENCE

Seagate Technology — **Longmont, CO**
VLSI Read Channel Design and Verification Intern — *May 2022 - Aug 2022*

- Researched verification environment transactions with DUT to enforce object-oriented structures in transition to UVM
- Developed firmware initialization and configuration code for read channel UVM environment

Seagate Technology — **Longmont, CO**
VLSI Design and Verification Engineering Intern — *May 2021 - Aug 2021*

- Designed and verified new RTL block responsible for optimizing throughput of ECC correction on hard drive reads
- Developed verification environment in VMM and UVM in SystemVerilog for new RTL features

Nabsys — **Providence, RI**
FPGA Engineering Intern — *June 2020 - September 2020*

- Fabricated signal processing algorithms and state machines for analysis of tagged DNA for genome sequencing
- Optimized FPGA design to significantly reduce slices used, allowing for 16x throughput to process real time streaming of 128 sensors

PROJECTS

CNN FPGA Hardware Accelerator — *Sept 2022 - Dec 2022*

- Designed and deployed CNN accelerator on AWS FPGAs using blocking systolic matrix multipliers on FashionMNIST dataset with Xilinx Vitis HLS tools
- Reduced trained parameter sizes by 75% using custom fixed-point 8 bit value representations with no loss to test accuracy

RISC-V Processor on FPGA — *Apr 2021 - May 2021*

- Implemented front end RTL on abbreviated RISC-V instruction set with branch prediction and five stage pipeline on Intel FPGA board
- Verified all design blocks in ModelSim and ran RTL through Intel Quartus

AWARDS

Cockrell School of Engineering Fellow, UT Austin — 2022-Current
UT Austin Graduate Excellence Fellow, UT Austin — 2022-Current
Sigma Xi Research Honor Society, Brown University — May 2022
NSF GRFP Honorable Mention, NSF — Apr 2022
Tau Beta Pi Engineering Honor Society, Brown University — Dec 2021

SKILLS

- **Programming**: Verilog, SystemVerilog, C, C++, Python, Pytorch
- **Tools**: Innovus, Genus, DC Compiler, Verdi, ModelSim, LTSpice, Electric, Matlab