Jason Ho

chekfung.github.io/portfolio | jasonchekfungho@gmail.com | chekfung | 401-965-7728

EDUCATION

University of Texas at Austin — **Austin, TX**
*Ph.D. in Electrical and Computer Enginering (Computer Architecture), **GPA: 4.0*** — *August 2022 - Current*

- Researching analog neuromorphic architectures with Dr. Andreas Gerstlauer
- *Relevant Coursework*: Accelerator Design, Prediction Mechanisms, Parallel Computer Architecture

Brown University — **Providence, RI**
*Sc.B. with Honors in Computer Engineering, **GPA: 3.96*** — *September 2018 - May 2022*

- **Thesis:** *Tools for Understanding Computational Behaviors of Bacterial Biofilms* under Dr. Sherief Reda
- *Relevant Coursework*: VLSI Design, Digital Signal Processing, Computer Architecture, Operating Systems

EXPERIENCE

AMD — **Austin, TX**
Power and Performance Lead/Architect Intern — *May 2023 - Aug 2023*

- Characterized power and performance on future APU plus discrete GPU platforms focused on power allocation algorithms between the APU and GPU on GPU-bound benchmarks
- Owned and deployed an internal data analysis tool that linked Power BI and internal databases to automate multi-phasic statistical analysis of benchmark logs, providing an **average 100x speedup** from previous methods
- Maintained, built and ran benchmarks on 8 separate systems for power and performance characterization

Seagate Technology — **Longmont, CO**
VLSI Read Channel Verification Engineering Intern — *May 2022 - Aug 2022*

- Lead verification transition for the team from VMM to UVM environment while reusing as much code as possible
- Developed firmware initialization and configuration code for read channel UVM environment with functionality for large-scale read channel testbenches

Seagate Technology — **Longmont, CO**
VLSI Read Channel Design Engineering Intern — *May 2021 - Aug 2021*

- Designed and optimized RTL block to increase ECC correction throughput in the hard drive read pipeline
- Developed VMM infrastructure with one other engineer to verify the new RTL block robustly

Nabsys — **Providence, RI**
FPGA Engineering Intern — *June 2020 - September 2020*

- Fabricated two signal processing algorithms for the analysis of tagged DNA data for genome sequencing
- Optimized FPGA design to reduce size by 2x while increasing throughput by 16x to process streaming of 128 sensors

PROJECTS

CNN FPGA Hardware Accelerator — *September 2022 - December 2022*

- Designed and deployed CNN accelerator with two other team members on AWS FPGAs using blocking systolic matrix multipliers with Xilinx Vitis HLS tools
- Reduced trained parameter size by 75% using custom fixed-point 8 bit values with almost no loss to test accuracy

AWARDS

Cockrell School of Engineering Fellow, UT Austin — 2022 - Current
UT Austin Graduate Excellence Fellow, UT Austin — 2022 - Current
NSF GRFP Honorable Mention, NSF — April 2022
Tau Beta Pi Engineering Honor Society, Brown University — December 2021

SKILLS

- **Programming**: Verilog, SystemVerilog, C, C++, Python, Pytorch, SQL
- **Tools**: Innovus, DC Compiler, ModelSim, SPICE, Matlab, Gem5, ChampSim, PowerBI