School of Electrical, Electronic and Computer Engineering

Automation of strained-Si device characterisation

Literature Review

Author: Antonios Dragoneas (079116617)

Supervisor: Dr. Sarah Olsen

Module Code: EEE-8094

Date: December 13, 2007

Table of Contents

Automation of strained-Si device characterisation Literature Review 1
Abstract 3
Introduction 4
Strained-Si concept 5
Strained-Si Integrated Circuit Manufacture and Quality 7
Device Characterisation and Automation 8
Conclusion 9
References 10

Abstract

This literature review illustrates the significance and potential contribution of strained-Si to the evolution of integrated circuit performance in the coming years. Firstly, the reasons which spur the pursuit of new techniques and materials for integrated circuit production, as well as a review of the strained material concept from a physics perspective are given. Secondly, a focus on the device manufacturing issues and the additional constraints that the application of strain implies follows. Thirdly, a reference to the importance of electrical measurements on these devices and the contribution of automation to their characterisation is given. Finally, the aim of this dissertation and its significance are presented as a conclusion.

Introduction

The very early predictions of Gordon Moore in 1965 and the resulting Moore's Law regarding the evolution of the complexity and thus the performance of integrated circuits by a factor of two every one to two years [1], has constituted a roadmap for the semiconductor industry over the course of the last four decades.

The intended reduction of the gate length has been unavoidably followed by the scaling of many other critical dimensions of the devices [2]. The consequent short channel effects need special techniques in order to be tackled and for this reason, junction depths had to be decreased, substrate doping increased and gate oxide thickness to be reduced [3]. The reduction of the gate oxide thickness offers a higher gate capacitance but induces an increase in the oxide interface roughness [4]. This side effect along with the high vertical electric fields that the inversion layer carriers develop, due to the higher substrate doping mentioned above, results in an increase of carrier scattering [3]. Consequently, the carrier mobility in the channel declines, having a great impact on device performance, which follows the same trend.

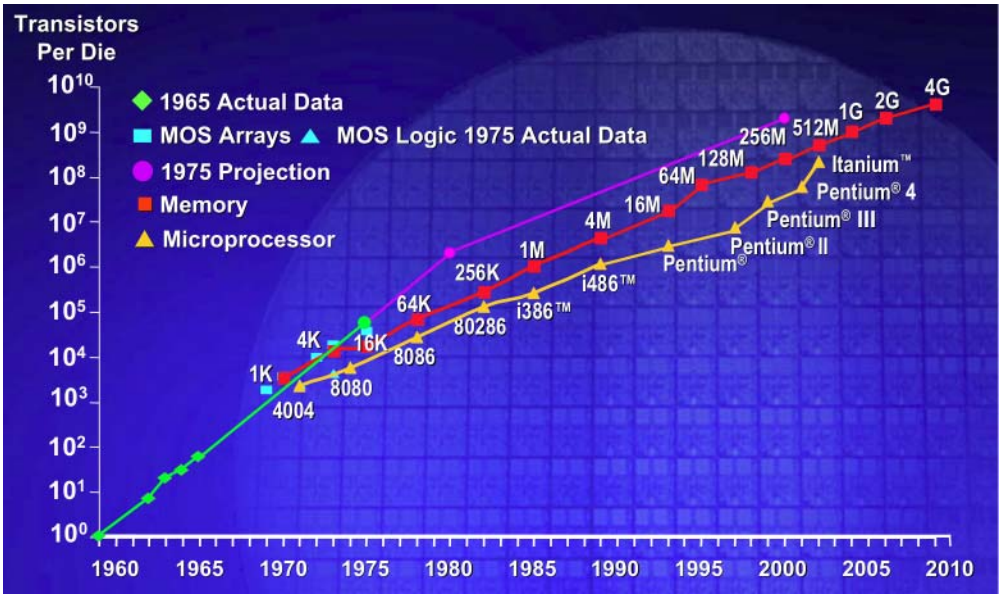

Fig.1: Intergrated Circuit Complexity from 1960 to 2010 **[i]**

As traditional materials and scaling methods seem to be unable to carry out the extension of Moore's Law in the future, new challenges for the industry emerge. Several approaches and feasible solutions to the mobility problem have been proposed as many research groups, both academic and industrial ones, have focused on this significant issue. However, considering the huge investments that have been made in silicon technology and the existing infrastructure, only new techniques that can be easily adopted by the industry without radical changes are more

likely to be nominated as the solution for the future. One of the approaches that fulfil this industrial demand is the use of strained silicon (strained-Si). Studies on the impact of strained-Si on metal-oxide-semiconductor field-effect transistors (MOSFET's), which constitute the workhorse of the integrated circuit industry, have shown that the application of strain offers higher current driving capability by altering the band structure of the channel [5].
Theoretically, strained-Si can induce further performance improvements for the very large scale integrated (VLSI) circuits without being constrained by the magnitude of their geometrical scaling [6], [7].

Strained-Si concept

As carrier mobility enhancement is the terminus, the physical definition of mobility can determine what the key parameters that need to be changed are. Carrier mobility is given by:

$$\mu = \frac{q\tau}{m^*}$$

where m^* is the conductivity effective mass and $1/\tau$ the scattering rate. Thus, the obvious inference is that a reduction of the effective mass and/or a reduction of the scattering rate can result in an increase in carrier mobility.

Studies on the effects of strain on carriers have shown a different behaviour of electrons and holes. For electrons, changes in both effective mass and scattering rate play a significant role in mobility enhancement [8], whereas for holes, only effective mass change caused by the energy band warping and repopulation [9] can be regarded as an important parameter. However, the complexity of the valence band structure of Si compared to the one of its conduction band, along with the valence band warping under strain induces a larger enhancement of hole rather than electron mobility [10].

For the application of strain in the nanoscale level, the atomic spacing difference of 4.2% between Si and Ge has been mainly employed. The growth of Si_xGe_{1-x} alloy layers or areas within traditional devices can selectively strain the Si areas. Regarding MOSFETs, strain targets the channel as higher carrier mobility in the channel enhances the performance of the device.

A key starting point for the evolution of strained semiconductor structures has been the use of the predominant silicon substrates as the base which new devices could be built on. Research on this orientation was commenced in the 1980's and early observations of the special behaviour of strained-Si silicon-germanium (strained SiGe) films grown on this kind of substrate were published by Manasevit *et al.* in 1982 [11] and People *et al.* in 1984 [12].

Today, there are two prevalent approaches for the strain implementation in MOSFETs. The global approach, where strain is applied to the entire substrate, and the local approach where different techniques such as the epitaxial growth of alloys on the substrate or the use of capping materials are employed to yield strain at well defined regions [10]. Nominally, the aforementioned approaches induce either biaxial or universal stress, respectively. Although the early work on strained devices employed the biaxial global approach, universal process-induced stress has been preferred for the first two generations of MOSFETs [13]-[15], as it offers greater hole mobility enhancement at lower strain while it doesn't exhibit high stress-induced n-channel threshold voltage shift [16].

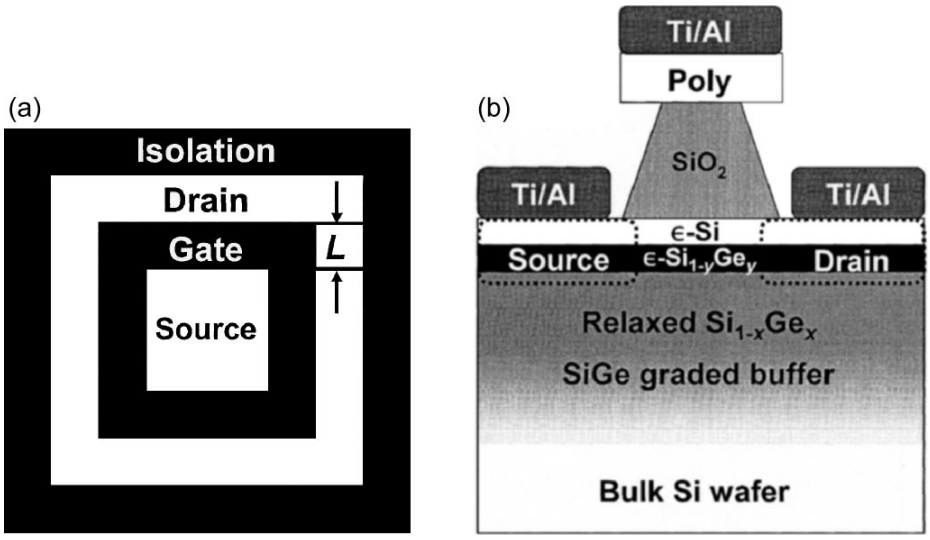

Fig.2: **(a)** Planar view schematic diagram of ring-shaped, single-mask MOSFETs used to quickly measure mobility in SiGe heterostructures. Typical values of *L* are 50–250 mm. **(b)** Cross-sectional diagram of completed single-mask MOSFET **[ii]**

Strain induces different effects on n-MOSFETs and p-MOSFETs. Several parameters such as the Ge content in the $Si_{1-x}Ge_x$ alloy, the thickness of the strained-Si layer and the gate overdrive play an important role for both devices but yield different results in each of them [5],[16]. Computer simulations have outlined the differences between the behaviour of MOSFET n-channels and p-channels [17]. Transconductance (g_m) plots show that ideal n-MOSFETs have higher performance for surface channel devices whereas p-MOSFETs perform better when the channel is buried 2nm below the gate oxide interface; additionally, these results are independent from the carrier mobility [17]. As most of the modern digital electronics are built on complementary metal-oxide-semiconductor (CMOS) logic where both n-MOS and p-MOS devices are integrated close to each other, a solution that can serve as the golden mean for both devices is of vital importance.

Strained-Si Integrated Circuit Manufacture and Quality

The manufacture of strained semiconductor MOSFETs is far more demanding than the traditional procedure followed for bulk silicon device manufacture. Several technical and quality issues detain the transition from research to commercial massive production. The need of quality that is stability and repeatability is imperative and thus forces the industry to pursuit new or more accurate techniques for the production of these elaborate new integrated circuits.

The first challenge were the high defect densities on the SiGe virtual substrate, which turned out to be the major mobility limiting factor for the pioneering Si/SiGE MOSFETs in the mid-1980's [18],[19]. A feasible solution to this problem was given by the employment of epitaxial growth of a $Si_{1-x}Ge_x$ buffer on the Si wafers which allows the $Si_{1-x}Ge_x$ alloy to relax creating a virtual substrate (VS) for the device [20].

Another important parameter is the thickness of the strained-Si layer grown on SiGe virtual substrate; potential instability and strain relaxation has been observed for strained layers that exceed a critical thickness (h_c) threshold [21]. Moreover, considering that a minimum thickness of 5nm is needed for acceptable carrier conduction [16],[22] and that both chemical-mechanical polishing (CMP) procedure and gate oxidation consume part of the layer [23], the optimization of the strained-Si thickness is a must. Furthermore, an annealing process with high thermal budgets can constitute another factor of strain relaxation. [23].

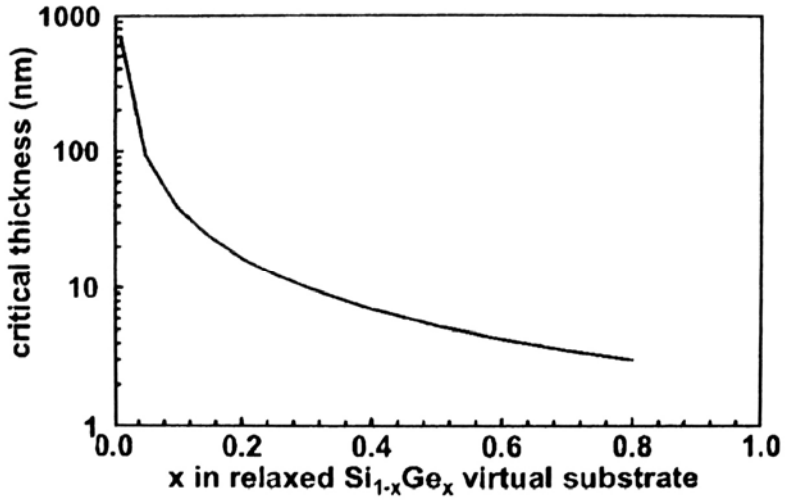

Fig.3: Theoritical curve for strained Si critical thickness as a function of Ge content in the virtual substrate **[iii]**

Moreover, the Ge content in the SiGe alloy is a critical factor for the device performance and stability. Studies have shown that electron mobility saturates for $Si_{1-x}Ge_x$ substrates with x~0.2-0.25 [16],[24]. However, hole mobility enhancement reaches a peak under higher strain that is higher Ge content in the SiGe alloy [25],[26]. Considering CMOS technology and the technical

issues mentioned above, the realization of CMOS structures on a Si/SiGe substrate implies compromises in either n-MOS or p-MOS performance as enhancement of the former's performance can counteract the expected gain on the latter and vice versa . In addition to this complexity, a high Ge content in the substrate reduces the critical thickness [27] due to Ge diffusion into the overlying strained-Si layer; this phenomenon can also trigger additional mobility degrading mechanisms [23]. Apart from Ge, diffusion of dopants such as As and P can play its part in the degradation of the device performance [5].

Lastly, studies have shown that the quality of all surface channel MOS devices depends on the quality of Si/SiO_2 interface [28]-[30]. Also, the optimum conditions for the device growth procedure, especially the thermal budget applied, remain controversial [3]. What is more, as attempts are made for strained-Si technology to be combined with other innovative high mobility technologies, such as high-κ gate dielectrics and insulating substrates (strained-Si on insulator, SSOI), new compatibility and quality issues arise.

Device Characterisation and Automation

The existence of all the aforementioned constraints induces uniformity issues across the wafer; theoretically identical devices grown on the same wafer can exhibit varying behaviour due to local strain relaxation or other factors given above. As the limitation of this variance is paramount for the commercial success of an integrated circuit design, device characterisation plays a key role for quality assurance.

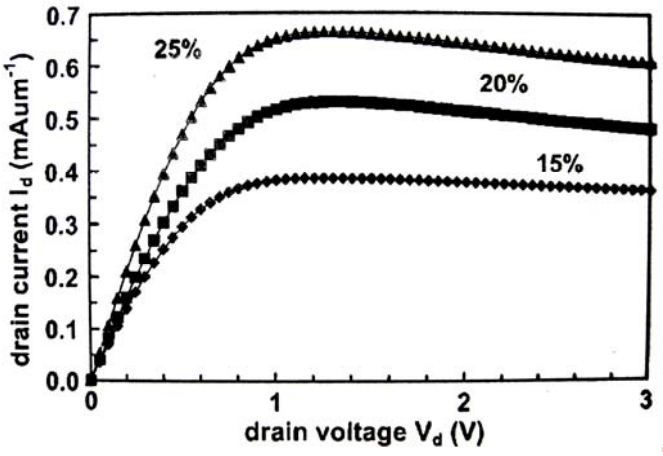

Fig.4: Drain current (I_d) vs drain voltage (V_d) characteristics measured at a gate overdrive voltage ($V_g - V_t$)=2.0V devices with gate lengths (L) of 0.3μm and gate widths (W) of 5μm. **[iv]**

Electrical measurements remain the main reference for device characterisation. Conductance, transconductance and capacitance measurements under specific conditions provide the most important information for the determination of the characteristics of a device. Further process of

the results and comparison of the tested devices can map out the device behaviour as a function of their coordinates on the wafer. Furthermore, comparison of the electrical measurements with observations made through microscopes can provide a correlation of the electrical characteristics of the device with the material quality [31].

As the amount of devices on a single wafer can be rather large, the manual conduct of measurements can be very time consuming. Semi-automatic probe stations are capable of significantly facilitating and accelerating the characterisation procedure provided that identical or similar devices are tested. In this case, the probe station can be programmed to move the wafer following a pre-defined pattern while the position of its probes remains intact. The device that needs to be tested is positioned under the probes and the wafer is raised in order for the probes to touch the device contacts. The design of an accurate pattern that is a wafer-map, and the development of an advanced data-acquisition mechanism can boost characterisation speed and efficiency.

Conclusion

Considering the distinctiveness of strained-Si wafers and the fact that these devices are under research and development, their characterisation exhibits a special interest. Thorough measurements are needed for the study of strain distribution across a wafer and its effects on the devices. The aim of this dissertation is the characterisation of multiple strained-Si devices grown on a single wafer. Automation of this procedure will be attempted by the use of the Cascade Summit 12101B semi-automatic probe station which Newcastle University possesses. For this reason, special software parameterization of the probe station and LabVIEW programming for the data-acquisition part will be employed.

References

[1] G. E. Moore, Electronics, **38** (1965)

[2] J. R. Brews, W. Fichtner, E. H. Nicollian, and S. M. Sze, IEEE Electron Device Letters, **1**, 2 (1980)

[3] S. H. Olsen, A. G. O'Neill, S. Chattopadhyay, K. S. K. Kwa, L. S. Driscoll, J. Zhang, D. J. Robbins, V. Higgs, Journal of Applied Physics, **94**, 10 (2003)

[4] S. J. Fang, W. Chen, R. Yamanaka, and C. R. Helms, Journ. Electrochem. Soc. **144**, 2886 (1997)

[5] M. L. Lee, E. A. Fitzgerald, M. T. Bulsara, M. T. Currie, and A. Lochtefeld, J. Applied Physics, **97**, 011101 (2005)

[6] D. A. Antoniadis, Symposium on VLSI Technology Digest of Technical Papers (Honolulu, HI, 2002), pp. 2-5

[7] J. L. Hoyt, H. M. Nayfeh, S. Eguchi, I. Aberg, G. Xia, T. Drake, E. A. Fitzgerald, and D. A. Antoniadis, Technical Digest-International Electron Devices Meeting (San Francisco, CA, 2002), pp. 23-26

[8] C. Zhi-Yuan, M. T. Currie, C. W. Leitz, G. Taraschi, E. A. Fitzgerald, J. L. Hoyt, and D. A. Antoniadis, "Electron-mobility enhancement in strained-Si n-MOSFETs fabricated on SiGe-on-insulator (SGOI) substrates", IEEE Electron Device Letters, **22**, pp. 321-323, (2001)

[9] S. E. Thompson, G. Sun, K.Wu, J. Lim, and T. Nishida, "Key differences for process-induced uniaxial vs. substrate-nduced biaxial stressed Si and Ge channel MOSFETs", Tech. Digest IEEE Int. Electron Device Meeting, pp 221-224 (2004)

[10] N. Mohta, and S. E. Thompson, IEEE Circuits and Devices Magazine, Sep-Oct 2005, pp.19-22

[11] H. M. Manasevit, I. S. Gergis, and A. B. Jones, Applied Physics Letters, **41**, 464 (1982)

[12] R. People, J. C. Bean, D. V. Lang, A. M. Sergent, H. L. Stormer, K. W. Wecht, R. T. Lynch, and K. Baldwin, Applied Physics Letters, **45**, 1231 (1984)

[13] S. E. Thompson, M. Armstrong, C. Auth, S. Cea, R. Chau, G. Glass, T. Hoffman, J. Klaus, Ma Zhiyong, B. Mcintyre, A. Murthy, B. Obradovic, L. Shifren, S. Sivakumar, S. Tyagi, T. Ghani, K. Mistry, M. Bohr, and Y. Elmansy, "A logic nanotechnology featuring strained silicon", IEEE Electron Device Letters, **25**, pp 191-193, (2004)

[14] T. Ghani, M. Armstrong, C. Auth, M. Bost, R. Charvat, G. Glass, T. Hoffmann, K. Johnson, C. Kenyon, J. Klaus, B. McIntyre, K. Mistry, A. Murthy, J. Sandford, M. Silberstein, S. Sivakumar, P. Smith, K. Zawadski, S. Thompson, and M. Bohr, "A 90nm high volume manufacturing technology featuring novel 45nm gate length strained silicon CMOS transistors", Tech. Dig. IEEE Int. Electron Devices Meeting, pp.11.6.1-11.6.3 (2003)

[15] M. D. Giles, M. Armstrong, C. Auth, S. M. Cea, T. Ghani, T. Hoffmann, R. Kotlyar, P. Matagne, K. Mistry, R. Nagisetty, B. Obradovic, R. Shasheed, L. Shifren, M. Stettler, S. Tyagi, X. Wang, C. Weber, and K. Zawadzki, "Understanding stress enhanced performance in Intel 90nm technology", Proc. Symp. VLSI Technology, p. 118 (2004)

[16] M. T. Currie, C. W. Leitz, T. A. Langdo, G. Taraschi, and E. A. Fitzgerald, Journ. Vac. Sci. Technol., **B 19**, 2268 (2001)

[17] S. G. Badcock, A. G. O'Neill, E. G. Chester, "Device and circuit performance on SiGe/Si MOSFETs", Solid State Electron, **46**, pp.1925-1932 (2002)

[18] H. Daembkes, H. Herzog, H. Jorke, H. Kibbel, and E. Kaspar, IEEE Trans. Electron Devices, **33**, 633 (1986)

[19] G. Arbstreiter, H. Brugger, T. Wolf, H. Jorke, and H. J. Herzog, Phys. Rev. Letters, **54**, 2441 (1985)

[20] E. A. Fitzgerald, Y. H. Xie, M. L. Green, D. Brasen, A. R. Kortan, J. Michel, Y. J. Mii, and B. E. Weir, Appl. Phys. Letters, **59**, 811 (1991)
[21] J. W. Matthews, and A. E. Blakeslee, "Defects in epitaxial multilayers", J. Cryst. Growth, **27**, pp. 118-125 (1974)
[22] A.G. O'Neill, unpublished
[23] S. H. Olsen, K. S. K. Kwa, L. S. Driscoll, S. Chattopadhyay, and A. G. O'Neill, IEE Proc.-Circuits Devices Syst., **151**, 5, pp. 431-437 (2004)
[24] J. Welser, J. L. Hoyt, S. Tagaki, and J. F. Gibbons, Tech. Dig. – Int. Electr. Devices Meeting, 373 (1994)
[25] M. V. Fischetti, and S. E. Laux, J. Appl. Phys., **80**, 2234 (1996)
[26] K. Rim *et al.*, Symposium on VLSI Technology, Honolulu, Hawaii (2002), (IEEE, Piscataway, NJ, 2002), p. 98
[27] S. H. Olsen, A. G. O'Neill, P. Dobrosz, S. J. Bull, L. S. Driscoll, S. Chattopadyay, and K. S. K. Kwa, Journ. Appl. Physics, **97**, 114504 (2005)
[28] A. G. Sabnis, J. T. Clemens, IEDM Tech. Dig., **18** (1979)
[29] T. Ohmi, K. Kotani, A. Teramoto, and M. Miyashita, IEEE Electron Dev. Let.,**12**, 652 (1994)
[30] J. Koga, S. Takagi, A. Toriumi, IEDM Tech Dig., 475 (1994)
[31] S. H. Olsen, A. G. O'Neill, D. J. Norris, A. G. Cullis, N. J. Woods, J. Zhang, K. Fobelets, and H. A. Kemhadjian, Semic. Sci. Techn., **17**, pp. 655-661 (2002)

Figures

[i] URL: http://www.cmg.org/measureit/issues/mit41/m_41_2/plot.png
[ii] M. L. Lee, E. A. Fitzgerald, M. T. Bulsara, M. T. Currie, and A. Lochtefeld, J. Applied Physics, **97**, 011101, fig. 7 (2005)
[iii]S. H. Olsen, A. G. O'Neill, P. Dobrosz, S. J. Bull, L. S. Driscoll, S. Chattopadyay, and K. S. K. Kwa, Journ. Appl. Physics, **97**, 114504, fig.1 (2005)
[iv]S. H. Olsen, A. G. O'Neill, P. Dobrosz, S. J. Bull, L. S. Driscoll, S. Chattopadyay, and K. S. K. Kwa, Journ. Appl. Physics, **97**, 114504, fig.6 (2005)