Low-Power Contest: Slack-Driven Dual Vth Assignement

Synthesis and Optimization A.Y. of Digital Systems 2015/2016

Authors: *Luca Mocerino s229006 Lorenzo Chelini s229230*

For this contest we developed an algorithm, that starting from a circuit synthesized LVT performs a reduction in the leakage power consumption under some user constraints: arrival time, slack window and number of paths in the slack window. The algorithm works in three main phases:

Phase 1 : *From LVT to HVT*

In the first phase, we swap all LVT cells for HVT cells

Phase 2 : *Match user arrival time*

In the second phase at each iteration we select the cells from the worst critical path and we swap them in HVT until the arrival time of the circuit is less than or equal to the arrival time provided by the user, we exit if the condition cannot be match. Moreover in this phase (and also in the last one) we elaborated a mechanism to step out from a local minimum. The local minimum happened when we still have some HVT cells, so basically we still have some margin to lowering down the arrival time, but the critical path is composed by all LVT cells and that path still remain critical on the next iteration, so actually the arrival time remain stack.

Phase 3 : *Match number of paths in the slack window*

In the third phase we adjust the number of path in the slack window computed as follow:
$slack\_window = [RT-ATu,(RT-ATu) + SWin]$
where:
RT is the required time of the circuit synthesized LVT
ATu is the arrival time requested by the user
Swin is the size of the window imposed by the user

In this step we bring in the slack window a total number of paths less than or equal to the number imposed by the user, swapping the cells to LVT and hence shifting the arrival time of path. We exit if the condition cannot be match.